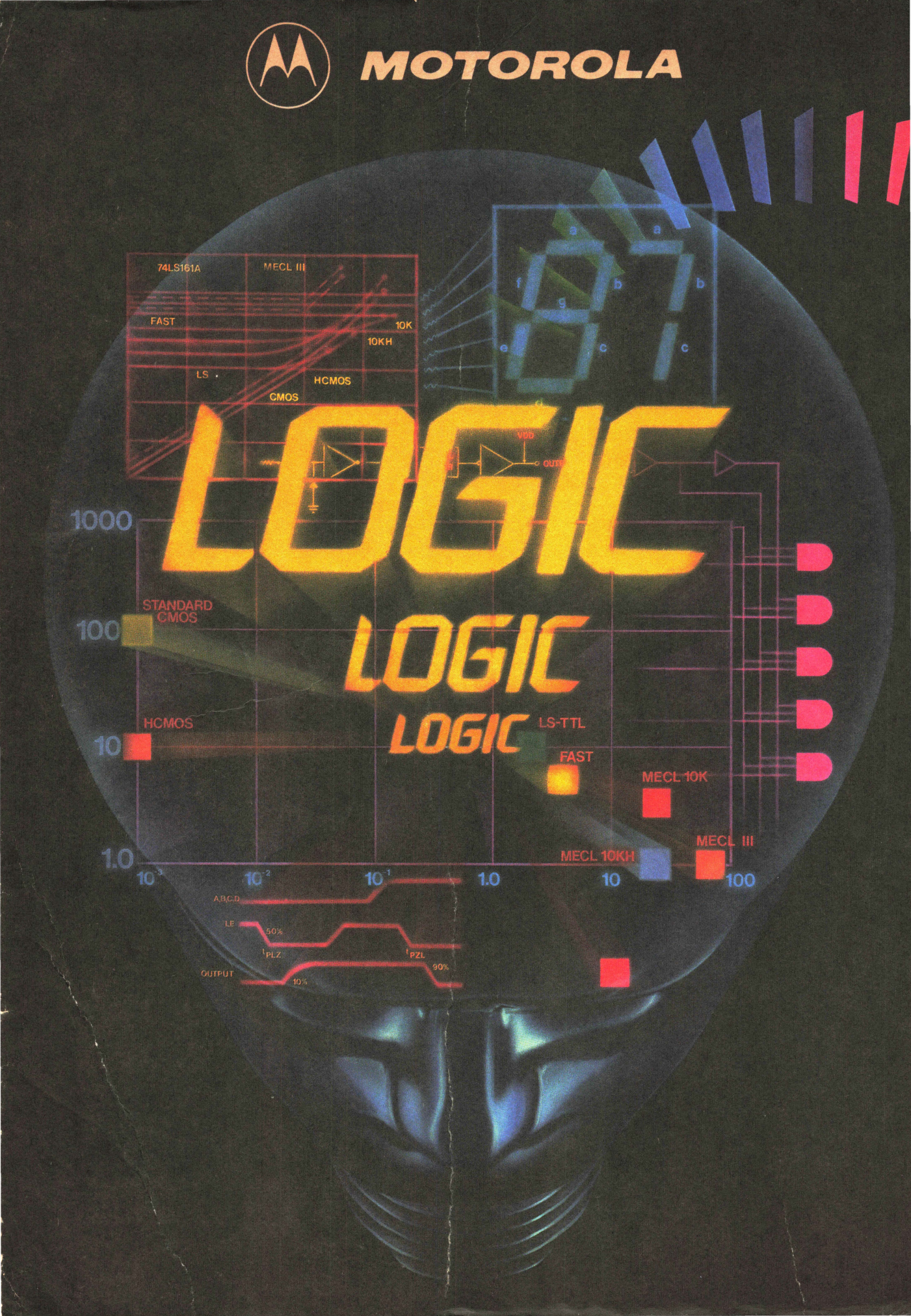
1988
IC MASTER
2
Integrated Circuit
Manufacturers
Technical Data

MOTOROLA


74LS161A
MECL III
FAST
10K
10KH
LS
HCMOS
CMOS
LOGIC
LOGIC
LOGIC
1000
100
10
1.0
STANDARD CMOS
HCMOS
LS-TTL
FAST
MECL 10K
MECL III
MECL 10KH
$10^{-3}$
$10^{-2}$
$10^{-1}$
1.0
10
100
A,B,C,D
LE
50%
$t_{PLZ}$
$t_{PZL}$
OUTPUT
10%
90%

1988

# IC MASTER

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## HOW TO USE THE IC MASTER

The 1988 edition of the IC MASTER is arranged in three volumes. Each volume serves a specific purpose to help you find the integrated circuit or related product you need. The table of contents on page 1 describes what is in each volume. The table also includes the starting page number for each advertiser.

The IC MASTER is a functional work. You know what you need. The MASTER helps you find it.

Here are typical problems.

**Q. What kinds of functions does the MASTER cover?**

A. Turn to page 8 in **Volume One.** Here is a complete list of the devices covered. The page and line numbers refer you to the beginning of the Section in which a particular function appears.

**Q. Who makes a 16384 x 1 static RAM with an access time of 70ns or faster? What are my technology choices?**

A. Pick up Volume 1. Turn to the MEMORY section. The first page of the section tells you where the listings of your device begin. See this under:

RAMs
Bubble
Dynamic
**Static**

Turn to the first page of static RAMs. In the first column you see the **Organization.** Browse through the pages until you reach the **16384 x 1** listings. Now look through the listings until you find the access time and characteristics you need. Device numbers are shown by manufacturer. The device numbers of advertisers in the 1988 IC MASTER appear in **bold face.** The page number following the device number is where additional information may be found in **Volume Two.** At the extreme right you will see line numbers. These are the specific lines where a device appears.

**Q. Which microprocessors are listed in the MASTER? How do I find the microprocessor I need?**

A. All commercially available microprocessors are listed in the MASTER. Start with the **microprocessor** listing in the **Master Selection Guide Index** (starts on page 8). Here you will find the various kinds of products you will need listed according to function and bit size. Turn to the various pages shown and then to the advertiser's page where more detail may be available.

**Q. Who makes a Dual, Low Offset Voltage OpAmp?**

A. This is a **LINEAR** device. Turn to the LINEAR section in Volume One. The first page of the section shows the starting page for each type of device. Turn to the page where **Dual Units** appear. Look down the list for the device you need. Advertisers' devices are listed in **bold face.** Turn to the page in Volume Two where more information may be available.

**Q. I need an IC with Music capability. Which Master Selection Guide should I use?**

A. Turn to the **Master Selection Guide Index** starting on page 8. Look through the list until you find **Music.** The page numbers for each kind of device are shown.

**Q. I plan to use a digital gate array or some other semicustom ASIC in my next project. Where do I find it in the MASTER? Who makes these things?**

A. Turn to Volume Three. Turn to the first page of **ASICs/Custom.** Find Gate Arrays and all of the other devices listed here. Now you can find the device you need. After you find the type of device you need, turn to the proper page and find the manufacturer. Advertisers' pages follow the selection guides in Volume Three.

**Q. I know the digital IC I need is available. Is it available in a surface mount package?**

A. There are two ways to solve this problem. If you know the manufacturer's device number, turn to the Part Number Index in Volume One. Find the basic number and the page number and line where that device is listed in the MASTER. Turn to that page. If the device is available for surface mounting, an open diamond symbol will appear. You can also turn directly to the DIGITAL section and turn to the function of the device you want. The symbol will indicate an SMD is available.

**Q. I am looking for an application note on a specific device. Where can I find out if one is currently available?**

A. Pick up Volume One. Turn to the Application Note Directory. Here you will find app notes arranged by **function.** Find the function involved and turn to the page where the app note is listed.

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**Q. We need a device that meets MIL standards. Where do I look in the Master?**

A. Turn to the MILITARY Section in Volume One. The Military Device Testing table shows which manufacturers do what kinds of MIL work. Read the instructions on the first page. The cross reference on the following pages tells you which commercial parts have MIL equivalents. This is followed by the MIL to commercial listing. This is followed by a cross reference of DESC drawing numbers to QPL-38510 parts. The next list is a QPL listing based on the latest Defense Electronics Supply Center (DESC) Qualified Product Listing. Additional information is often supplied by the advertisers' pages in Volume Two.

**Q. I know the basic part number is 2502 and that's all I know. Where do I look?**

A. That's easy in the MASTER. Turn to the Part Number Index. All prefixes and suffixes have been stripped away. Turn to the page where 2502 appears. All manufacturers with that kind of number appear in order along with the page and line number where the device is described.

**Q. How many manufacturers claim to make a pin-for-pin and function-for-function equivalent to Motorola MC68000?**

A. Turn to the Alternate Source Directory in the back of Volume One. Turn to Motorola. Those manufacturers who claim to be equivalent are listed in order. If you have an MS-DOS computer with a hard drive, you can get the 1988 IC MASTER Alternate Source Directory on a disk. The disk is Clipper compiled from dBaseIII + and is delivered compressed by PKARC. This is the complete list of alternate sources and allows you to add notes such as your own part numbers, prices, sources and the like. Call Hearst (516) 227-1300 and ask for Book Sales for further information.

**Q. I looked in the Alternate Source Directory. The part I want an alternate source for isn't listed. Why not?**

A. Are you sure you looked through the entire listing for the original manufacturer? Some devices may be listed in odd ways depending on how the MASTER's editors receive the information. Then there is the probability that no other manufacturer makes an exact replacement for your part. It is important for you to understand how the Alternate Source Directory is compiled. Manufacturers supply the information that **their** part is an exact replacement for **another** part. The original manufacturer does **not** tell us his part can be replaced by those listed.

**Q. I need an 8/16-bit microcomputer board with an 8MHz clock frequency and a multibus support system. Can I find this in the MASTER?**

A. Yes! Pick up Volume Three. Turn to the MICROCOMPUTER BOARD Section. Continue to turn pages until the 8/16 appears in the first column. Then look at all of the available boards to find the boards you can use.


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**Q. I have Valid Logic's "Summary" workstation. Which front end tools are compatible? Can I get one with circuit simulation? What capabilities does it have? Who makes it?**

A. Pick up Volume Three. Turn to the Design Automation Section. Check the first page. You will see what is available in the Section. Under Design Tools you will find Front End Tools and Circuit Simulators. Read down for your parameters and across for the vendor.

**Q. What do the manufacturers' part numbers mean? I have a Signetics N8X02N. What do all the letters and numbers mean?**

A. Look in Volume One for the Part Number Guide. Turn to the Signetics portion. Now you know the **N** prefix means, zero to plus seventy degrees Centigrade. The **N** suffix indicates the package style. The numbers and letters in the middle are the device type. Each manufacturer has a different code system. Understanding the system is a great help in comparing devices.

**Q. I found the device I want in the MASTER. What are the pinouts? Where can I get more details? Where can I get a price? What is the delivery time?**

A. You have just defined exactly what the IC MASTER does. The MASTER is a guide to tell you which devices are available on a commercial basis. After you know this, the next step is to contact the manufacturer, a local sales office or a distributor.

**Q. Where can I find the addresses and telephone numbers of manufacturers, local sales offices and distributors?**

A. Pick up Volume Two. Turn to the Manufacturers and Distributors Directory. Read the first page. The information on this page will help you understand why the information in the Directory is so important. It will save time and aggravation.

**Q. I just saw a new device advertised in Electronic Products magazine. It isn't listed in the MASTER. Why not? When will it be listed?**

A. Preparing the information for the annual IC MASTER is a tremendous undertaking. It requires the cooperation of every single manufacturer. All of the material must be organized, cross referenced and placed in the data base. This data base must be closed off in November in order to meet the publishing date of late January. That is why some devices are not listed. They came on the market too late for the deadline. There are two updates to the annual MASTER. They are called the **IC MASTER UPDATE.** One is issued in the late Spring and the other in early Fall. Be sure to sign up for copies when you get your new IC MASTER. If you are not sure whether or not you have requested the updates, please write to the Circulation Department at the address shown on page 2 of this MASTER. Be sure to indicate which edition of the MASTER you are using.

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# ABBREVIATIONS OF COMPANY NAMES

| | |
|---|---|
| **AB Assoc** | AB Associates |
| **Abionics** | Abionics |
| **ACASI** | American Computer Automated Systems |
| **ACE** | Action Computer Enterprise |
| **Acotech** | Acotech |
| **AD** | Analog Devices |
| **AdvControl** | Advanced Control Systems Corp. |
| **AdvDigital** | Advanced Digital Corp. |
| **AdvEngSol** | Advanced Engineering Solutions |
| **AdvLinear** | Advanced Linear Devices |
| **AdvMicroSys** | Advanced Micro Systems |
| **AIArchitects** | A. I. Architects Inc. |
| **Aida** | Aida |
| **AjidaTech** | Ajida Technologies |
| **Alcyon** | Alcyon Corp. |
| **Aldec** | Aldec |
| **AllenSys** | Allen Systems |
| **Alloy** | Alloy Computer Products |
| **Alphatron** | Alphatron |
| **Altera** | Altera |
| **AMA** | American Automation |
| **AMCC** | Applied Micro Circuits |
| **AMD** | Advanced Micro Devices |
| **Amperex** | Amperex Electronic Corp. |
| **Ampro** | Ampro Computers Inc. |
| **Amtelco** | Amtelco |
| **Anadigics** | Anadigics |
| **AnalDesTools** | Analog Design Tools |
| **AnalogSys** | Analog Systems |
| **Analogic** | Analogic |
| **ANALOGY** | Analogy |
| **Anasco** | Anasco Corp. |
| **Antona** | Antona Corp. |
| **Apex** | Apex Microtechnology |
| **Applicon** | Applicon |
| **AppBusComp** | Applied Business Computer |
| **AppMicroSys** | Applied Microsystems Corp. |
| **ApplSys** | Applied Systems Corp. |
| **Aptek** | Aptek Microsystems |
| **Aptos** | Aptos Systems |
| **Argus** | Argus Software |
| **ArrayTech** | Array Technology |
| **ASEA-HAFO** | ASEA-HAFO |
| **Astro** | Astrosystems Inc. |
| **Atec** | Atec |
| **ATITech** | ATI Technologies Inc. |
| **Atlanta** | Atlanta Signal Processors |
| **Atmel** | Atmel Corp. |
| **AT&T** | AT&T |
| **Augat** | Augat, Inc. Systems Div. |
| **AutoDesk** | AutoDesk |
| **AutoSys** | Automated Systems Inc. |
| **Babcock** | Babcock Material Handling Group |
| **Barvon** | Barvon BiCMOS Technolgy Inc. |
| **Basicon** | Basicon Inc. |
| **B&C Micro** | B&C Microsystems |
| **Bedford** | Bedford Control Systems Inc. |
| **Berne** | Berne Electronics |
| **Bicc-Vero** | Bicc-Vero Electronics |
| **BinaryTech** | Binary Technology |
| **Bipolar** | Bipolar Integrated Tech |
| **Bishop** | Bishop Graphics |
| **Bit3Comp** | Bit 3 Computer Corp |
| **Brainpower** | Brainpower |
| **Brooktree** | Brooktree |
| **Buckminster** | Buckminster Corp |
| **Bummer** | Bummer Electronics |
| **Burr-Brown** | Burr-Brown Corporation |
| **Cadam** | Cadam |
| **CAD Group** | CAD Group |
| **Cadic** | Cadic, Inc. |
| **Cadnetix** | Cadnetix |
| **CAECO** | CAECO |
| **Caedent** | Caedent |
| **Calay** | Calay Systems |
| **CalDevices** | California Devices |
| **Calma** | Calma |
| **Calmos** | Calmos Systems |
| **Calos** | Calos |
| **Cambridge** | Cambridge Digital Systems |
| **CAN-TRON** | CAN-TRON |
| **CaseTech** | Case Technology |
| **Catalyst** | Catalyst, Semiconductors |
| **CentData** | Central Data Corp. |
| **Cermetek** | Cermetek |
| **CharlesRiver** | Charles River Data |
| **Cherry** | Cherry Semiconductor |
| **Chips&Tech** | Chips & Technology |
| **Chrislin** | Chrislin Industries |
| **CIC** | Custom Integrated Circuits |
| **Cirrus** | Cirrus |
| **Clarity** | Clarity Systems |
| **Clearpoint** | Clearpoint Inc. |
| **CMA** | Custom MOS Arrays |
| **CMCIntl** | CMC International |
| **CMD ASIC** | CMD ASIC Division |
| **CMD Micro** | CMD Microcircuits Division |
| **Codar** | Codar Technology Inc. |
| **Comark** | Comark Corp. |
| **Comlinear** | Comlinear Corporation |
| **Commodore** | Commodore Semiconductor Group |
| **Compact** | Compact Software |
| **CompAuto** | Computer Automation |
| **CompDyn** | Computer Dynamics |
| **CompModules** | Computer Modules Inc. |
| **Computrol** | Computrol Inc. |
| **CompVision** | Computervision |
| **ConnMicro** | Connecticut MicroComputer |
| **Contemporary** | Contemporary Control Systems |
| **Context** | Context Corp. |
| **ControlData** | Control Data |
| **Controlex** | Controlex Corp. |
| **Conway** | Conway |
| **CreMicro** | Creative Micro Systems |
| **Crystal** | Crystal Semiconductor |
| **CTI** | Circuit Technology Inc. |
| **Cubit** | Cubit Inc. |
| **CustomArrays** | Custom Arrays Corp. |
| **Cyberchron** | Cyberchron Corp. |
| **Cybernetic** | Cybernetic Micro Systems |
| **Cypress** | Cypress Semiconductor |
| **Daisy** | Daisy Systems |
| **Dallas** | Dallas Semiconductor |
| **Dasoft** | Dasoft Design Systems |
| **DataGen** | Data General |
| **Datal/O** | Data I/O |
| **DASystems** | Data Systems |
| **dataCon** | dataCon Inc. |
| **Datacube** | Datacube Inc. |
| **Dataram** | Dataram Corporation |
| **DataTrans** | Data Translation |
| **Datel** | Datel |
| **Datricon** | Datricon Corporation |
| **Davidge** | Davidge Corp. |
| **DEC** | Digital Equipment Corp. |
| **Den/Pas** | Densan/Pascot |
| **Dense-Pac** | Dense-Pac |
| **Devtek** | Devtek Systems |
| **Dexter** | Dexter Research Center |
| **Digital RF** | Digital RF Solutions Corp. |
| **Digitronics** | Digitronics Sixnet |
| **Dionics** | Dionics Inc. |
| **DistComp** | Distributed Computer Systems |
| **DiversTech** | Diversified Technology |
| **DraftingDyn** | Drafting Dynamics |
| **DSB Systems** | DSB Systems |
| **DSP-Systems** | DSP-Systems Corp. |
| **DUAL** | Dual Systems Corp. |
| **ECAD** | ECAD |
| **ECISemi** | ECI Semiconductor |
| **EDI** | Electronic Designs Inc. |
| **EdsunLabs** | Edsun Laboratories, Inc. |
| **EES** | Electrical Engineering Software |
| **EEsof** | EEsof Inc. |
| **EG&G-Reticon** | EG&G-Reticon |
| **Elantec** | Elantec |
| **Electrologic** | Electrologic Inc. |
| **ElecConServ** | Electronics Consulting Service |
| **Elfab** | Elfab Test Systems |
| **Elxsi** | Elxsi |
| **Emulogic** | Emulogic |
| **ENDOT** | ENDOT Inc. |
| **Enterprise** | Enterprise Systems |
| **ESP** | Electronic Software Products |
| **European** | European Silicon Structures |
| **Exar** | Exar Corporation |
| **EXEL** | EXEL Microelectronics |
| **Excelan** | Excelan Inc. |
| **Factron** | Factron-EDA |
| **Fairchild** | Fairchild |
| **Faraday** | Faraday |
| **Ferranti** | Ferranti Electric |
| **Force** | Force Computers |
| **Ford** | Ford Microelectronics |
| **FujitsuA** | Fujitsu America |
| **Fujitsu** | Fujitsu Microelectronics, Inc. |
| **FutureNet** | FutureNet |


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| | |
|---|---|
| **GainElec** | Gain Electronics |
| **Galil** | Galil Motion Control |
| **Gateway** | Gateway Design Automation |
| **GE/Intersil** | GE/Intersil |
| **GE/RCA** | GE/RCA Solid State |
| **GE Semi** | GE Semiconductor |
| **GenMicro** | General Microsystems |
| **Gennum** | Gennum Corporation |
| **GenRad** | GenRad |
| **GENROCO** | GENROCO |
| **Gerber** | Gerber Scientific Instrument |
| **GigaBit** | GigaBit Logic |
| **GIM** | General Instrument Microelectronics |
| **GoldStar** | GoldStar Semiconductor |
| **Golden** | Golden Electronics |
| **Gordos** | Gordos Arkansas |
| **Gould** | Gould Inc. |
| **GTSys** | GT Systems |
| **GW-Three** | GW Three Inc. |

| | |
|---|---|
| **Harris** | Harris Semiconductor |
| **HEI** | HEI Corporation |
| **Hercules** | Hercules Computer Technology |
| **Heurikon** | Heurikon Corp. |
| **HHB-Sys** | HHB Systems |
| **HiLevel** | Hi-Level Technology |
| **Hitachi** | Hitachi America, Ltd. |
| **HiTech** | HiTech Equipment Corporation |
| **Holt** | Holt Inc. |
| **Honeywell** | Honeywell |
| **HoneywellSPT** | Honeywell Signal Processing Technologies |
| **HP** | Hewlett-Packard |
| **Hughes** | Hughes Aircraft, Solid State Products |
| **HybridSys** | Hybrid Systems |
| **HyComp** | HyComp |
| **Hytek** | Hytek Microsystems |
| **Hyundai** | Hyundai Electronics America |

| | |
|---|---|
| **IBM** | IBM |
| **ICC** | International Cybernetics |
| **ICDC** | Integrated Circuit Design Centre |
| **ICI** | Integrated Circuits Inc. |
| **IC Options** | IC Options, Inc. |
| **ICSensors** | IC Sensors, Inc. |
| **ICT** | International CMOS Technology |
| **ICT Comp** | ICT Computer Drafting |
| **IDT** | Integrated Device Technology |
| **IKON** | Ikon Corp. |
| **IKOS** | IKOS Systems |
| **ILC-DDC** | ILC Data Device Corporation |
| **iLSi** | Integrated Logic Systems |
| **IMI** | International Microcircuits, Inc. |
| **IMP** | International Microelectronic Products |
| **Imaging** | Imaging Technology Inc. |
| **IndComp** | Industrial Computer Designs |
| **IndTech** | IndTech Inc. |
| **Inmos** | Inmos Corporation |
| **InnovRes** | Innovative Research |
| **Inova** | Inova Microelectronics |
| **InrVision** | Inner Vision |

| | |
|---|---|
| **IntCirSys** | Integrated Circuit Systems |
| **IntMeasSys** | Integrated Measurement Systems |
| **IntSolutions** | Integrated Solutions |
| **IntTech** | Integrated Technology |
| **Intech** | Intech Advanced Analog |
| **Intel** | Intel |
| **Intelicom** | Intelicom Systems Ltd. |
| **IntelComp** | Intelligent Computer Integration |
| **Interactive** | Interactive Circuits and Systems, Ltd. |
| **Interconics** | Interconics |
| **InterconMicro** | Intercontinental Micro Systems |
| **Interdesign** | Interdesign/Ferranti |
| **Intergraph** | Intergraph |
| **Interphase** | Interphase Corp. |
| **Intronics** | Intronics |
| **Intusoft** | Intusoft |
| **Inventive** | Inventive Systems Inc. |
| **Ioinc** | Io Incorporated |
| **IPS** | Integrated Power Semiconductors |
| **Ironics** | Ironics Inc. |
| **Isocom** | Isocom, Inc. |
| **ITT** | ITT Semiconductors |
| **IXYS** | IXYS Corp. |

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|---|---|
| **KSystems** | K-Systems Inc. |
| **Kern** | Kern Systems |
| **Kontron** | Kontron Electronics |

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|---|---|
| **Lambda** | Lambda Semiconductors |
| **Laserpath** | Laserpath |
| **Lattice** | Lattice Semiconductor |
| **LitMach** | Little Machines, Inc. |
| **LinearTech** | Linear Technology Corp. |
| **LMS** | LMS Electronics |
| **LogicAuto** | Logic Automation |
| **LogicDev** | Logic Devices Inc. |
| **LogicalDes** | Logical Design Group |
| **Logicraft** | Logicraft Inc. |
| **Lomas** | Lomas Data Products, Inc. |
| **LPKF-Pacific** | LPKF-Pacific |
| **LSIComp** | LSI Computer Systems |
| **LSI Logic** | LSI Logic |
| **LupiData** | Lupi Data, Inc. |

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|---|---|
| **M2M** | M2M Robotics |
| **Magnum** | Magnum Opus |
| **Marconi** | Marconi Electronic Devices Inc. |
| **Marinco** | Marinco Computer Products |
| **MasterLogic** | Master Logic Corporation |
| **Matra** | Matra Design Systems |
| **Matra-Harris** | Matra-Harris Semiconductors |
| **Matrix** | Matrix Corp. |
| **Matrox** | Matrox Electronics Systems |
| **Maxim** | Maxim Integrated Products |
| **MCE** | MCE Semiconductor |
| **Mentor** | Mentor Graphics |
| **MTC** | Mesa Technology Corp. |
| **MetaSoft** | Meta Software |
| **Metatek** | Metatek Inc. |
| **Micom Int** | Micom-Interlan |
| **Micra** | Micra Corp. |

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|---|---|
| **Micrel** | Micrel |
| **MicroAide** | Micro Aide Corp. |
| **Microbar** | Microbar Systems, Inc. |
| **MicroCompSys** | Microcomputer Systems |
| **Microcosm** | Microcosm |
| **MicroDesigns** | Microdesigns |
| **MicroInds** | Micro Industries Corp. |
| **MicroLinear** | Micro Linear |
| **MicroNet** | Micro Networks |
| **MicronTech** | Micron Technology |
| **Micropac** | Micropac Industries |
| **MicroPwr** | Micro Power Systems |
| **Micro-Link** | Micro-Link Corporation |
| **Micro-Rel** | Micro-Rel |
| **Microsim** | Microsim |
| **MicroSys** | Micro/sys |
| **Microvoice** | Microvoice |
| **Mikros** | Mikros Systems Corp. |
| **MilerTron** | MilerTronics |
| **Miller** | Miller Technology |
| **Mimic** | Mimic, Inc. |
| **MiniCompTech** | Mini Computer Technology |
| **Minntronics** | Minntronics Corp. |
| **Mitchell** | Mitchell Electronics |
| **Mitel** | Mitel Semiconductor |
| **Mitsubishi** | Mitsubishi Electronics America, Inc. |
| **MMI** | Monolithic Memories, Inc. |
| **Modula** | Modula |
| **MonSys** | Monolithic Systems Corp. |
| **Morrow** | Morrow Technologies |
| **Mosaid** | Mosaid |
| **Motorola** | Motorola Semiconductor Products |
| **Multiwire** | Multiwire, Div. Kollmorgen |
| **Mylex** | Mylex Corp. |

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|---|---|
| **NationalInst** | National Instruments |
| **National** | National Semiconductor |
| **NCAI** | North Coast Automation, Inc. |
| **NCM** | NCM Corporation |
| **NCR** | NCR Microelectronics |
| **NEC** | NEC Electronics |
| **NMB** | NMB Semiconductor Corporation |
| **Northern** | Northern Precision Labs |
| **Novix** | Novix |
| **NthGraphics** | Nth Graphics |
| **NTI Group** | NTI Group |

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|---|---|
| **Octagon** | Octagon Systems Corp. |
| **Octal** | Octal |
| **OEI** | Optical Electronics Inc. |
| **OKI** | OKI Semiconductor |
| **Omation** | Omation |
| **Omnibyte** | Omnibyte Corp. |
| **Omnicad** | OMNICAD |
| **Onset** | Onset Computer Corp. |
| **Optima** | Optima Technology |
| **Origin** | Origin, Inc. |
| **Orion** | Orion Instruments |
| **OwlComp** | Owl Computers |

# CONT.

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|---|---|
| **PacificM** | Pacific Microcomputers, Inc. |
| **Pacific** | Pacific Microcircuits |
| **Panasonic** | Panasonic |
| **Panatech** | Panatech Semiconductor |
| **PC-Office** | PC-Office |
| **PCAD** | PCAD |
| **PEP-Modular** | PEP Modular Computers |
| **Performance** | Performance Semiconductor Corp. |
| **PlesseyMicro** | Plessey Microsystems |
| **Plessey** | Plessey Semiconductors |
| **PLXTechnology** | PLX Technology |
| **PMI** | Precision Monolithics Inc. |
| **Polycore** | Polycore Electronics |
| **Praxis** | Praxis Systems |
| **Pro-Log** | Pro-Log Corp. |
| **Proximity** | Proximity |
| **Quadtree** | Quadtree |
| **Qualogy** | Qualogy Corporation |
| **Quantic** | Quantic Laboratories, Inc. |
| **RACAL** | RACAL-REDAC |
| **RanchoTech** | Rancho Technology |
| **RapidSys** | Rapid Systems, Inc. |
| **Raytheon** | Raytheon Semiconductor |
| **RCIData** | RCI Data |
| **Recognition** | Recognition Technology |
| **RELMS** | Relational Memory Systems |
| **Renaissance** | Renaissance GRX |
| **Ricoh** | Ricoh Company Ltd. |
| **RIFA** | RIFA |
| **RLCEnterprise** | R.L.C.Enterprises |
| **Robotrol** | Robotrol Corp. |
| **Rockwell** | Rockwell Semiconductor Products |
| **RTC** | Riehl Time Corporation |
| **S-MOS** | S MOS Systems |
| **Samsung** | Samsung Semiconductor |
| **Sanyo** | Sanyo Semiconductor |
| **SBE** | SBE, Inc. |
| **SDA-Systems** | SDA Systems |
| **SciCalc** | Scientific Calculations |
| **SDA-Systems** | SDA Systems |
| **SeattleSi** | Seattle Silicon Tech. |
| **SEEQ** | SEEQ Technology, Inc. |
| **Semicon** | Semicon, Inc. |
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| **Sertek** | Sertek Inc. |
| **SGS** | SGS Semiconductor |
| **SharedRes** | Shared Resources |
| **Sharp** | Sharp |
| **Siemens** | Siemens |
| **Sierra** | Sierra Semiconductor |
| **Sigma Info** | Sigma Information Systems |
| **Signetics** | Signetics |
| **SiCompilers** | Silicon Compilers |
| **SilControls** | Silicon Controls |
| **SiliconG** | Silicon General |
| **SiliconSys** | Silicon Systems Inc. |
| **Siliconix** | Siliconix |
| **Siltronics** | Siltronics |
| **Silvaco** | Silvaco Data Systems |
| **SilvarLisco** | Silvar Lisco |
| **Simucad** | Simucad |
| **Simulog** | Simulog |
| **SingleBoard** | Single Board Solutions |
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| **SMC** | Standard Microsystems Corporation |
| **SMS** | Scientific Microsystems |
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| **Solarise** | Solarise Enterprises Inc. |
| **Solitron** | Solitron Devices |
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| **Sophia** | Sophia Computer Systems |
| **SpaceResearch** | Space Research Technology, Inc. |
| **Spectrum** | Spectrum Software |
| **Sprague** | Sprague Electric Company |
| **SSM** | Solid State Micro Technology for Music |
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| **STD** | STD Microsystems |
| **STI** | Stanford Telecommunications |
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| **Systek** | Systek |
| **SysCalc** | Systems Calculations |
| **SysDatar** | Systems Datar |
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| **Technitrol** | Technitrol |
| **Techno** | Techno Inc. |
| **Tech80** | Technology 80 |
| **TechModl** | Technology Modeling |
| **Tektronix** | Tektronix |
| **Tek/CAE** | Tektronix/CAE Systems |
| **Tek/ICO** | Tektronix/Integrated Circuit Operations |
| **TeledyneC** | Teledyne Crystalonics |
| **TeledyneP** | Teledyne Philbrick |
| **TeledyneS** | Teledyne Semiconductor |
| **Telefunken** | Telefunken |
| **Teletek** | Teletek Enterprises |
| **Teltone** | Teltone Corporation |
| **Teradyne** | Teradyne |
| **TI** | Texas Instruments |
| **Destek** | The Destek Group |
| **ThirdDomain** | Third Domain |
| **Thomson** | Thomson Components-Mostek |
| **Titan/SESCO** | Titan/SESCO |
| **Toko** | Toko America |
| **TopazSemi** | Topaz Semiconductor |
| **Toshiba** | Toshiba America |
| **Transmag** | Transmagnetics Inc. |
| **TriQuint** | TriQuint |
| **Trimarchi** | Trimarchi and Associates |
| **Trimeter** | Trimeter Technologies |
| **UMC** | United Microelectronics (UMC) |
| **Unicorn** | Unicorn Microelectronics |
| **Unitrode** | Unitrode |
| **Universal** | Universal Semiconductor, Inc. |
| **United** | United Silicon Structures |
| **USDesign** | US Design Corp. |
| **UTMC** | United Technologies Microelectronics Center |
| **Valid** | Valid Systems |
| **Validyne** | Validyne Engineering |
| **VAMP** | VAMP |
| **VDA** | VLSI Design Associates |
| **Vectron** | Vectron Graphics Systems |
| **VersaLogic** | Versalogic Corp. |
| **Vesta** | Vesta Technology |
| **VIA-Systems** | VIA Systems |
| **ViewLogic** | View Logic Systems |
| **Visionics** | Visionics |
| **VisionsUnlim** | Visions Un-limited |
| **Vitelic** | Vitelic Corp. |
| **Vitesse** | Vitesse Electronics |
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| **VME-Microsys** | VME Microsystems Int'l Corp. |
| **VMI** | VLSI Microsystems, Inc. |
| **Votrax** | Votrax |
| **VTC** | VTC |
| **Vutek** | Vutek Systems, Inc. |
| **Waferscale** | Waferscale Integration Inc. |
| **WDC** | Western Design Center |
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| **Western** | Western Digital |
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| **Xerox** | Xerox |
| **Xicor** | Xicor |
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| **Zilog** | Zilog |
| **Ziltek** | Ziltek Corp. |
| **Zitel** | Zitel |
| **Microcosm** | Zuckerboard |
| **Zuken** | Zuken America |
| **ZyMOS** | ZyMOS |


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# MANUFACTURERS AND DISTRIBUTORS/ REPRESENTATIVES DIRECTORY

The Manufacturers and Distributors/Representatives Directory is a comprehensive telephone directory of the entire IC industry. It places at your fingertips the names and phone numbers you need to know. For manufacturers with data pages, it includes domestic and international sales offices, representatives and distributors; it also tells you where and whom to call to obtain technical and ordering information.

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813-932-9853
FAX: 813-977-4111

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Pasadena, California 91107
818-351-5451
TELEX: 279865 ACEI UR

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Pembroke, Massachusetts 02359
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714-891-4004

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Boulder, Colorado 80303
303-499-2910

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**Sunnyvale, California 94088**
**408-732-2400**
**TELEX: 34-6306**

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603-882-1447

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408-980-5200, 800-777-AIDA

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FAX: 805-498-7945

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614-488-7122

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Santa Clara, California 95051
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**FAX: 714-731-6344**

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San Jose, California 95160
408-997-3333

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**Norwood, Massachusetts 02062-9106**
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Texas, Jack Coe, ..... 214-231-5094
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Analog Devices, TEL: 30/31 64 41

**Intl** **West Germany, Buchholz**
Analog Devices GmbH, TEL: 4181-8051

**Intl** **West Germany, Karlsruhe**
Analog Devices GmbH, TEL: 721/61 60 75

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**Intl** **West Germany, Muenchen**
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EIM International Ltd., TEL: 9233257

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**Intl** **Toronto**
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**Intl** **United Kingdom, Middlesex**
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, 404-447-6495

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Sunnyvale, California 94086
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FAX: 408-730-5521

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313-755-7500
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1992 Tarob Court
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408-262-8368

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## Bedford Control Systems

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## Bummer

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**Tucson, Arizona 85734**
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## Cadic

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Milpitas, California 95035-7489
408-434-4000
FAX: 3720067;FAX: 408-434-4372

## Calmos Systems

**Calmos Systems Inc.**
**20 Edgewater St.**
**Kanata, Ontario, Canada K2L 1V8**
**613-836-1014**
**TELEX: 053-4501**

## Calos

Calos, Inc.
3419 Edison Way
Fremont, California 94538
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## Cambridge Digital Systems

Cambridge Digital Systems
65 Bent Street, POB 568
Cambridge, Massachusetts 02139
617-491-2700

## Can-Tron

Can-Tron
PO Box 51515
Pacific Grove, California 93950
408-649-8041

## Case Technology

Case Technology
2141 Landings Dr.
Mt. View, California 94043
415-962-1440

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NY(516) 226-6000
NJ(201) 882-8300
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4051 Burton Drive
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## Central Data Corp.

Central Data Corporation
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217-359-8010;800-482-0315
TWX: 910-245-0787
FAX: 217-359-6904

## Cermetek Microelectronics

Cermetek Microelectronics, Inc.
1308 Borregas Avenue, P.O. Box 3565
Sunnyvale, California 94088-3565
408-752-5000
TWX: 910-379-6931

## Charles River Data Systems

Charles River Data Systems
983 Concord Street
Framingham, Massachusetts 01701

## Cherry Semiconductor

Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818
401-885-3600
TELEX: WUI-6817157
FAX: 401-885-5786;Easylink 535609

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Chips and Technologies, Incorporated
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408-434-0600
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Chrislin Industries, Inc.
Computer Products Division
31332 Via Colinas, No. 106
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**Farmingdale, New York 11735**
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## Clearpoint

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617-435-5395, 617-435-2301
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201-881-1200

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## Custom Arrays

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## Custom MOS Arrays

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Tech Sales, Inc., 602-246-1614

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**CA** **Mt. View**
Intectra, 415-967-8818

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Datel, 408-286-1872

**CA** **San Jose**
Datel, 408-286-1872

**CA** **Santa Ana**
Datel, 714-835-2751

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Datel, 714-835-2751

**CO** **Denver**
Elcom, Inc., 303-337-2300

**CO** **Denver**
Elcom Inc., 303-337-2300

**FL** **Coral Springs**
H.A. Incorporated, 305-752-7520

**FL** **Coral Springs**
H. A. Inc., 305-752-7520

**GA** **Roswell**
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**GA** **Roswell**
EMA, Inc., 800-647-3773

**HI** **Honolulu**
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Adtech, Inc., 808-941-0708

**IL** **Hoffman Estates**
Carvel Engineering & Sales, Inc., 312-885-8800

**IA** **Marion**
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**KS** **Wichita**
ENSCO-REP, Inc., 316-683-1070

**KS** **Wichita**
Ensco-Rep, Inc., 316-683-1070

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Datel, 617-339-3000

**MA** **Mansfield**
A. Risley (GE Datel), 617-339-3000

**MI** **Auburn**
Infinity, Inc., 313-853-9880

**MN** **Edina**
Carvel Engineering & Sales, Inc., 612-835-7929

**MO** **Maryland Heights**
ENSCO-REP, Inc., 314-423-3935

**MO** **Maryland Heights**
Ensco-Rep, Inc., 314-423-3935

**MO** **Maryland Hts**
Ensco-Rep, Inc., 314-423-3935

**NJ** **Wayne**
Astrorep, Inc., 201-696-8200

**NJ** **Wayne**
ASTROREP, Inc., 201-696-8200

**NM** **Albuquerque**
Cleveland Enterprises, Inc., 505-265-7893

**NM** **Albuquerque**
Cleveland Entprs., Inc., 505-265-7893

**NY** **Babylon**
Astrorep, Inc., 516-422-2500

**NY** **Babylon**
Astrorep, Inc., 516-422-2500

**NY** **Clark Mills**
KLM-Garner, 315-853-6126

**NY** **New York**
C.A. Int'l. Export & Import Co. (China), 212-925-2553, 966-0061

**NY** **Rochester**
KLM-Garner, 716-381-8350

**NC** **Charlotte**
Electronic Manufacturers Agents, 704-365-0547

**NC** **Raleigh**
Electronic Manufacturers Agents, 919-846-6888

**NC** **Raleigh**
EMA Inc. No. Carolina, 919-846-6888

**OH** **Cleveland**
Authur Baier Co., 216-461-6161

**OH** **Dayton**
Arthur Baier Co., 513-276-4128

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Wyncote Instrumentation Company, 215-572-6500

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Wyncote Instrmn. Co., 215-572-6500

**PA** **Pittsburgh**
, 412-823-7005

**PA** **Pittsburgh**
Arthur Baier Co., 412-367-7799

**SC** **Charlotte**
EMA Inc. So. Carolina, 704-365-0547

**TX** **Austin**
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**TX** **Austin**
Technical Mktg., Inc., 512-835-0064

**TX** **Carrollton**
Technical Marketing, Inc., 214-387-3601

**TX** **Carrollton**
Technical Mktg., Inc., 214-387-3601

**TX** **Houston**
Technical Marketing, Inc., 713-783-4497

**TX** **Houston**
Technical Mktg., Inc., 713-783-4497

**UT** **Salt Lake City**
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Elcom Inc., 801-485-7415

**VA** **Arlington**
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**Can** **Lachine, Quebec**
Vitel Elctrns., 514-636-5951

**Can** **Mississauga, Ontario**
Vitel Electronic

**Intl** **Australia, Adelaide**
Elmeasco Instruments Pty. Ltd., TEL: (08) 271-1830

**Intl** **Australia, Brisbane**
Elmeasco Instruments Pty. Ltd., TEL: (07) 369-8688

**Intl** **Australia, Concord N.S.W.**
Elmeasco Instrs. Pty. Ltd., TEL: 02-7362888

**Intl** **Australia, Gosnells**
Elmeasco Instruments Pty. Ltd., TEL: (09) 398-3362

**Intl** **Austria, Landstrasse**
Othmar Lackner, TEL: 43-222-752618

**Intl** **Belgium, Brussels**
Master Chips, TEL: 32-2-219-5862/1484

**Intl** **Denmark, Kokkedal**
C-88 APS, TEL: 45-2-244888

**Intl** **Finland, Espoo**
Kauko Markkinat, TEL: 35-8-05211

**Intl** **France, Saint Cloud**
Datel, TEL: 33-1-4602-5711

**Intl** **Germany, Muenchen**
Datel, TEL: 49-89-530741

**Intl** **Greece, Piraeus**
General Electronics, Ltd., TEL: 30-1-491-3591

**Intl** **Hong Kong, Hong Kong**
Schmidt & Co., TEL: 852-5-8330222

**Intl** **Hong Kong, Kowloon**
Electronic Components, TEL: 416-479-1443

**Intl** **Hong Kong, Kowloon**
Tektron Electronic, TEL: 852-3-880629

**Intl** **Iceland, Grettisgata**
Sameind HF, TEL: 354-191-21366

**Intl** **India, Secunderabad**
Kaytronics Electronics Eng., TEL: 77924

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STG Intl. Ltd., TEL: 972-3-03/248231

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Datek KK, TEL: 81-3-779-1031

**Intl** **Korea, Seoul**
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**Intl** **Kuwait, Safat**
Al-Khaldiya Trading & Contracting, TEL: 414910;411726

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David Reid Ltd., TEL: 64-9-488-049

**Intl** **Norway, Oslo**
Hightech A.S., TEL: 42-2-02-749330

**Intl** **Singapore**
Francotone Elctrns. Ltd., TEL: 65-283-0888/289-1618

**Intl** **South Africa, Transvaal**
Electronic Building Elements, TEL: 27-12-46-922123456789

**Intl** **Spain, Madrid**
Amitron, S.A., TEL: 341-1-247-9313/248-5863

**Intl** **Sweden, Hagersten**
Martinsson Elektronik AB, TEL: 46-8-744-0300

**Intl** **Switzerland, Dietikon**
Ineltro AG, TEL: 41-1-7414121

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Sertek International, TEL: 886-2-5010055

**Intl** **Thailand, Bangkok**
Measuretronix, TEL: 66-2-3742516

**Intl** **The Netherlands**
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**Intl** **United Kingdom, England, Hampshire**
Datel, TEL: 44-256-469085

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Elmeasco Instruments Pty. Ltd., TEL: 61-2-7362888

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B.T. Hightech A.S., TEL: 42-2-02-749330

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Sertek International, TEL: 886-2-5010055

**Intl** **Thailand, Bangkok**
Measuretronix, Ltd., TEL: 66-2-3742516

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Simac Electronics B.V., TEL: 31-40-582911

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415-493-7841, 800-843-4222

## Davidge Corporation

Davidge Corporation
94-E Commerce Dr., P. O. Box 1869
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805-688-9598
TELEX: 910-250-0233

## Densan/Pascot

Densan/Pascot
17981 Skypark Circle, Ste. B
Irvine, California 92714
714-261-5220

## Dense-Pac

**Dense-Pac Microsystems, Inc.**
**7321 Lincoln Way**
**Garden Grove, California 92641**
**714-898-0007**
**TWX: 510-601-1045**
**FAX: 714-897-1772**

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**FL** **Largo**
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**UT** **North Salt Lake**
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**Can** **Kanata, Ontario**
Vitel Electronics, 613-592-0090
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EMM - Dense-Pac Ltd., TEL: 0628 72135
**Intl** **Denmark**
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**Intl** **Edinburgh**
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**Intl** **France**
Esprit, TEL: 0703 229695
**Intl** **France**
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**Intl** **Germany**
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Kontron, TEL: 14354425

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A.J. Distributors Pty. Ltd., TEL: 08-269-1244
**Intl** **South Melbourne**
A.J. Distributors Pty. Ltd., TEL: 03-699-8365

## Devtek Systems

Devtek Systems
P.O. Box 5224
Lancaster, Pennsylvania 17601
717-560-0652

## Dexter Research Center

Dexter Research Center, Inc.
7300 Huron River Drive
Dexter, Michigan 48103
313-426-3921

## Digital Equipment

Digital Equipment Corporation
77 Reed Road
Hudson, Massachusetts 01749
617-568-4000

## Digital RF Solutions

**Digital RF Solutions Corp.**
**3080 Olcott, Ste. 200-D**
**Santa Clara, California 95054**

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**FL** **Longwood**
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**ID** **Santa Clara**
Digital RF, 800-782-6266
**IL** **Arlington Hts.**
Dytec-Central, 312-394-3380
**IL** **Springfield**
Dytec-South, 417-883-3592
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**KS** **Lenexa**
Dytec-South, 913-888-0215
**KS** **Wichita**
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Beacon-North, 703-478-2480
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Dytec-South, 402-334-1222
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**NM** **Albuquerque**
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USTM, 516-724-4250
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Robtron, 315-685-5731
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**OR** **Bellevue**
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**PA** **Marlton**
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**WI** **Brookfield**
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Digital RF, TEL: 408-727-5995, 800-782-6266
**PR** **San Turce**
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## Digitronics Sixnet

Digitronics Sixnet
P.O. Box 767
Clifton Park, New York 12065
518-877-5173

## Dionics

Dionics Inc.
65 Rushmore Street
Westbury, New York 11590
516-997-7474
TWX: 510-222-0974

## Distributed Computer Systems

Distributed Computer Systems
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Waltham, Massachusetts 02154
617-890-8200



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P.O. Box 465, 112 East State Street
Ridgeland, Mississippi 39157
601-856-4121

## Drafting Dynamics

Drafting Dynamics
4615 Industrial St., Ste. 1H
Simi Valley, California 93063
818-348-2532

## DSB Systems

DSB Systems
94-E Commerce Drive, P.O. Box 1869
Buellton, California 93427
805-688-9598

## DSP Systems

DSP Systems Corporation
1081 North Shepard St. Unit H
Anaheim, California 92806
714-630-1330

## Dual Systems

Dual Systems Corporation
2530 San Pablo Avenue
Berkeley, California 94702
415-549-3854

## ECAD

ECAD, Inc.
2455 Augustine Dr.
Santa Clara, California 95054
408-727-0264

## ECI Semiconductor

ECI Semiconductor
975 Comstock Street
Santa Clara, California 95054
408-727-6562

## Edsun Laboratories

Edsun Laboratories, Inc.
7 Sears Road
Wayland, Massachusetts 01778
617-358-5667
TELEX: 853664

## EEsof Inc.

EEsof Inc.
5795 Lindero Canyon Rd.
Westlake Village, California 91362
818-991-7530

## EG&G Reticon

**EG&G Reticon Corporation**
**345 Potrero Avenue**
**Sunnyvale, California 94086-4197**
**408-738-4266**
**TWX: 910-339-9343**

**Specific Product Information:**
Camera Product Marketing: EG&G Reticon
Analog Product Marketing: EG&G Reticon
Image Sensor Product Marketing: EG&G Reticon

**Literature:**
Sales Service Dept.

**Price and Delivery:**
Sales Service Dept.

**Follow up on Order:**
Sales Service Dept.

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**CA** **Glendale**
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**CA** **Tustin**
Orion Sales, 714-832-9687

**CT** **Stratford**
Gerald Rosen Co., Inc., 203-375-5456

**FL** **Brandon**
R.C. Simon & Co., Inc., 813-689-6524

**FL** **Lighthouse Point**
R.C. Simon & Co., Inc., 305-941-2757

**GA** **Roswell**
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**MA** **Salem**
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**KS** **Wichita Falls**
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Total Electronics, TEL: (03) 288-4044

**Intl** **Austria, Wien**
Othmar Lackner, TEL: (0222) 752618

**Intl** **Belgium SA/NV, Bruxelles**
Inelco, TEL: (02) 216 01 60

**Intl** **Denmark, DK-2200 Copenhagen, N.**
Scansupply, TEL: (01) 83 50 90

**Intl** **Eastern Europe, D-8028 Taufkirchen**
Opteltec, Div. Neumuller GmbH, TEL: (089) 6118-0

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**Intl** **France, Verf St.-Denis**
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Telsys Ltd., TEL: 494891-5

**Intl** **Japan, Tokyo**
Tokyo Electron Ltd., TEL: 03-343-4411

**Intl** **Netherlands, Postbus 125, 2600 AC Delft**
Koning En Hartman, TEL: 015-609906

**Intl** **New Zealand, Auckland 9**
Professional Electronics Ltd., TEL: 493-029

**Intl** **Norway, N-1364 Hvalstad**
Nordisk Elektronik (Norge) A/S, TEL: (02) 84 62 10

**Intl** **South Africa, Pretoria 0001**
Electronic Bldg. Elements Pty. Ltd., TEL: (012) 46-9221/7

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J-Tek, TEL: 782-8039/49

**Intl** **Spain, 28008 Madrid**
Amitron, TEL: (91) 248 79 59

**Intl** **Sweden, Huvudstagatan**
Ingenjorsfirman Nordisk, TEL: 4687349770

**Intl** **Switzerland, 8304 Wallisellen/Zurich**
Industrade AG, TEL: (01) 830 50 40

**Intl** **Taiwan, Taipei**
Mitac Corp., TEL: 02-501-8231

**Intl** **West Germany, 8000, Munich 80**
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**TWX: 910-997-0649**
**FAX: 408-945-9305**

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Central, Ray Runquist ..... 214-664-1168
West, Bruce Elliott ..... 408-945-1323 (outside CA, 1-800-821-7429)

**Applications Engineering:**
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Central, Jon Dutra ..... 1-800-821-7429
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**CA** **Mountain View**
Brooks Technical Group, 415-960-3880

**CA** **San Diego**
Bestronics, Inc., 619-693-1111

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**FL** **Casselberry**
Lawrence Associates, 305-339-3885
**FL** **Palm Harbor**
Lawrence Associates, 813-737-2773
**GA** **Norcross**
Electronic Sales, Inc., 404-448-6554
**IL** **Wheaton**
Splon Associates, 312-665-5993
**IN** **Indianapolis**
STB & Associates, 317-844-9227
**IA** **Hiawatha**
Gassner & Clark, 319-393-5763
**MD** **Columbia**
Delta III, 301-730-4700
**MA** **No. Reading**
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**MA** **Wellesley**
Elantec, Inc., 617-239-8182
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High Technology Sales, 612-944-7274
**MO** **Florissant**
Hitec Central Inc., 314-831-9377
**MO** **Independence**
Hitec Central Inc., 816-796-6684
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**NM** **Albuquerque**
Reptronix Limited, 505-292-1718
**NY** **E. Syracuse**
Ossman Associates, 315-437-7052
**NY** **Henrietta**
Ossman Associates, 716-359-1200
**NY** **Lake Ronkonkoma**
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**NY** **Richmond Hills**
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**NC** **Cary**
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**TX** **Houston**
O M Associates, 713-789-4426
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O M Associates, 214-690-6746
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**Can** **Ottawa**
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**Can** **Pointe Claire**
Har-Tech Electronics, Inc., 514-694-6110
**Can** **Toronto**
Har-Tech Electronics, Inc., 416-665-7290
**Can** **Vancouver, B.C.**
Davetek Marketing, 604-430-3680
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Insight Electronics, Inc., 818-707-2100
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**CA** **Calabasas**
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Insight Electronics, Inc., 714-556-6890
**CA** **Irvine**
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**CA** **Irvine**
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**MD** **Columbia**
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**Intl** **Denmark**
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**Intl** **England**
Die Technology Ltd., TEL: 44-6162-63827
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**Intl** **France**
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**Intl** **Holland**
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Lagercrantz Electronik AB, TEL: 4676086120
**Intl** **Switzerland**
Datacomp
**Intl** **Taiwan**
Galaxy Far East, TEL: 886-2-7057266
**Intl** **United Kingdom**
Microelectronics Tech. Ltd., TEL: 44-844-68781
**Intl** **W. Germany**
Scantec GMBH, TEL: 49-8985-98021
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## Electrical Engineering Software

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4675 Stevens Creek Blvd., No. 101
Santa Clara, California 95051
408-296-8151

## Electrologic

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Signal Hill, California 90806
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Irvine, California 92714
714-261-1777

## Electronics Consulting

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Reading, Pennsylvania 19608
215-777-7357

## Elfab

Elfab Test System Division
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214-221-8776

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## Emulogic

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Norwood, Massachusetts 02062
617-769-2980

## Endot

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216-229-8900
FAX: 216-229-2307

## Enterprise Systems

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603-742-7363

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EXAR EXEL

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**TWX: 910-339-9233**

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Candal Inc., 303-233-0155

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**MO** **Maryland Heights**
Design Solutions, 314-961-7170

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Quality Comps., 315-682-8885

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Tech. Mktg., 512-244-2291

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**WA** **Spokane**
Components West, 509-922-2412

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**Can** **Nepean, Ontario**
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**Intl** **Bangalore, India**
Testech Elec, TEL: 611201

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ROHM Elctrna. Ltda., TEL: 421-4577

**Intl** **Denmark, Horsholm**
Mer-el A/S, TEL: 571000

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**Intl** **Japan, Tokyo**
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Silcom Elec, TEL: 49/2161 60752

**Intl** **Netherlands, Amsterdam**
Nijkerk Elek., TEL: 20-5495969

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Professional Elctrns. Ltd., TEL: 493-0480

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**Intl** **Singapore, Singapore**
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**CA** **Thousand Oaks**
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Reptron, 612-938-0000

**MN** **Plymouth**
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GCI, 609-768-6767

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**NJ** **Fairfield**
Marshall Elctrns., 201-882-0320

**NJ** **Mt. Laurel**
Marshall Elctrns., 609-234-9100

**NJ** **Mt. Laurel**
Future Electronics, 609-778-7600

**NJ** **Totowa**
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Betatron, 505-344-2318

**NM** **Albuquerque**
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**NY** **Hauppauge**
JACO, 516-273-5500

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Future Elec., 315-451-2371

**NY** **N. Amityville**
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Marshall Elctrns., 716-235-7620

**NY** **Rochester**
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**NC** **Raleigh**
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**OH** **Dayton**
Bell Industries, 513-434-8231

**OH** **Dayton**
Bell Industries, 513-435-8660

**OH** **Solon**
Marshall Elctrns., 216-248-1788

**OH** **Westerville**
Marshall, 614-891-7580

**OH** **Worthington**
Reptron Elctrns., 614-436-6675

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**OK** **Tulsa**
Radio, Inc., 918-587-9123

**OR** **Beaverton**
Western Microtechnology, 503-641-9312

**OR** **Beaverton**
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**OR** **Lake Oswego**
Bell Inds., 503-241-4115

**OR** **Portland**
Radar Elec. Co., Inc., 503-232-3404

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**PA** **Pittsburgh**
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**Can** **Burnaby, B.C.**
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**Can** **Winnipeg, Manitoba**
Future Electronics, 204-339-0554

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## Excelan

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## EXEL Microelectronics

**EXEL Microelectronics, Inc.**
**A Subsidiary of EXAR Corp.**
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**San Jose, California 95131**
**408-942-0500**
**TELEX: 171339**
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**FAX: 408-434-6444**

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**TX** **Dallas**
TL Marketing, 214-484-6800

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**WA** **Spokane**
Components West, 509-922-2412

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Janus, Inc., 414-542-7575

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**Intl** **Italy, Rome**
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Microtronics Assoc. PTD, Ltd., TEL: 748-1835

**Intl** **Solna**
AB Betoma, TEL: (08) 820280

**Intl** **Spain, Madrid**
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**Intl** **Switzerland, Baden-Daettwill**
Primotec AG, TEL: 056-840171

**Intl** **Tokyo, Japan**
Systems Mktg, TEL: 254-2751

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South Continental Devices, TEL: 789-2400

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**MA** **Woburn**
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Bell Industries, 513-435-8660

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## Factron

Factron EDA
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NJ(201) 882-8300
MA(617) 777-8800

FAIRCHILD

## Fairchild

Fairchild Semiconductor Corporation
10400 Ridgeview Court, P.O. Box 1500
Cupertino, California 95014
408-255-3700
TELEX: CORPHQ.MVAC

## Faraday

Faraday Electronics
743 Pastoria Ave.
Sunnyvale, California 94086
408-749-1900
TELEX: 706738

## Ferranti

Ferranti Electric, Inc.
87 Modular Avenue
Commack, New York 11725
516-543-0200
TWX: 510-226-1490

## Force Computers

Force Computers, Inc.
3165 Winchester Blvd.
Campbell, California 95008
408-370-6300

## Ford Microelectronics

Ford Microelectronics, Inc.
10340 State Highway 83 North
Colorado Springs, Colorado 80908-3698
800-824-0812, 303-528-7600

## Fujitsu America

Fujitsu America
910 Sherwood, Suite 23
Lake Bluff, Illinois 60044
312-295-2610

## Fujitsu

**Fujitsu Microelectronics, Inc.**
**3320 Scott Blvd.**
**Santa Clara, California 95054-3197**
**408-562-1000**
**TWX: 910-338-0190**

**Specific Product Information:**
Jim Wilcox, Director of Standard Product Mktg.

**Applications Engineering:**
Gary Hess, Director of Custom Product Mktg.

**Literature:**
Technical publications

**Price and Delivery:**
Respective sales office



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**Follow up on Order:**
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**All Other Information:**
Jim Wilcox (LD) 408-562-1000

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**IL** **Glendale Heights**
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**NY** **Hauppauge**
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**OH** **Richfield**
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**CT** **Wallingford**
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Milgray Florida, 305-647-5747

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Milgray Atlanta, 404-393-9666

**GA** **Norcross**
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Classic Comp. Supply, 312-272-9650

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Time Electronics, 312-350-0610

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**MI** **Livonia**
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**818-700-0691**

## Gain Electronics

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Somerville, New Jersey 08876
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## Galil Motion Control

Galil Motion Control
1928A Old Middlefield Rd.
Mountain View, California 94043
415-964-6494
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## Gateway Design

Gateway Design Automation Corp.
Six Lyberty Way, P.O. Box 573
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## GE Semiconductor

GE Semiconductor
See GE Solid State for sales offices
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## GE/Intersil

**GE/Intersil, Inc.**
**See GE Solid State for sales offices**
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**Cupertino, California 95014**
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## GE Solid State

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## ILC Data Device

ILC Data Device Corp.
105 Wilbur Place
Bohemia, New York 11716
516-567-5600
TWX: 510-228-7324

## Imaging Technology

Imaging Technology, Inc.
600 West Cummings Park
Woburn, Massachusetts 01801
617-938-8444
TELEX: 948263
FAX: 617-938-1757

## IndTech

IndeTech, Inc
1275 Hammerwood Avenue
Sunnyvale, California 94089
408-743-4300

## Industrial Computer Designs

Industrial Computer Designs
31264 La Baya Drive
Westlake Village, California 91362
818-889-3179

## Inmos

**Inmos**
**P.O. Box 16000**
**Colorado Springs, Colorado 80935**
**303-630-4000**
**FAX: Easylink; 62944936**

**Specific Product Information:**
Field Sales Offices

**Applications Engineering:**
Applications ..... 303-630-4493

**Literature:**
Field Sales Offices

**Place an Order:**
Field Sales Offices/Distributors

**All Other Information:**
Marketing ..... 303-630-4361

### Sales Office & Representatives

**AL** **Huntsville**
Macro-Marketing Assoc., 205-883-9630

**AZ** **Phoenix**
Compass Mktg. & Sales, 602-996-0635

**AZ** **Tucson**
Compass Mktg., 602-293-1220

**CA** **San Diego**
Hadden Assoc., 619-565-9444

**CA** **Santa Ana**
Inmos Sales, 714-957-6018

**CA** **Santa Clara**
Inmos Sales, 408-727-7771

**CA** **Santa Clara**
Criterion Sales, 408-988-6300

**CO** **Denver**
Inmos Sales, 303-252-4100

**CO** **Wheatridge**
Waugaman Associates, 303-423-1020

**CT** **Brookfield**
M & M Associates, Inc., 203-775-6888

**FL** **Coral Springs**
Graham Associates, 305-755-6733

**FL** **Indiatlantic**
Graham Associates, 305-773-6631

**FL** **Palm Beach**
Graham Associates, 305-622-4049

**FL** **Winter Garden**
Graham Associates, 305-656-9369

**GA** **Norcross**
Inmos Sales, 404-242-7444

**GA** **Norcross**
Macro-Marketing Assoc., 404-662-5580

**IL** **Schaumburg**
Micro-Tex, 312-382-3001

**KS** **Kansas City**
B.C. Electronic Sales, 913-342-1211

**KS** **Wichita**
B.C. Electronic Sales, 316-722-0104

**MD** **Columbia**
Inmos Sales, 301-995-6952

**MD** **Severna Park**
New Era Sales, 301-544-4100

**MA** **Needham Heights**
Kanan Assoc., 617-449-7400

**MA** **Westborough**
Inmos Sales, 617-366-4020



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## Inmos (Cont'd)

**MN** **Edina**
Mel Foster Tech Sales, 612-941-9790

**MN** **Minnetonka**
Inmos Sales, 612-932-7121

**MO** **St. Louis**
B.C. Electronic Sales, 314-521-6683

**NJ** **Teaneck**
Technical Marketing Group, 201-692-0200

**NM** **Albuquerque**
Compass Mktg. & Sales, 505-888-0800

**NY** **E. Rochester**
Tri-Tech Electronics, Inc., 716-385-6500

**NY** **Endwell**
Tri-Tech Electronics, Inc., 607-754-1094

**NY** **Fayetteville**
Tri-Tech Electronics, Inc., 315-446-2881

**NY** **Fishkill**
Tri-Tech Electronics, Inc., 914-897-5611

**NY** **Melville**
Technical Marketing Group, 516-351-8833

**NC** **Myrtle Beach**
J & B Sales, Inc., 803-272-3475

**NC** **Raleigh**
J&B Sales, Inc., 919-783-9440

**OH** **Beachwood**
E.S.I., 216-831-9555

**OK** **Tulsa**
B.P. Sales, 918-744-9964

**OR** **Portland**
W3C Technology, 503-629-9871

**PA** **Feasterville**
Knowles Assoc., 215-322-7100

**TX** **Dallas**
Inmos Sales, 214-490-9522

**TX** **Houston**
B.P. Sales, 713-782-4144

**TX** **Richardson**
B.P. Sales, 214-234-8438

**UT** **Salt Lake City**
Waugaman Associates, 801-261-0802

**WA** **Seattle**
W3C Technology, 206-285-0201

**WI** **Waukesha**
Micro-Tex, 414-542-5352

**Can** **Downsview, Ontario**
Har-Tech Electronics, 416-665-7773

**Can** **Ottawa, Ontario**
Har Tech Elctrns., 613-726-9410

**Can** **Pointe Claire, Quebec**
Har-Tech Electronics, 514-694-6110

**Intl** **France, Paris**
Inmos SARL, TEL: 1-4687-22-01

**Intl** **Hong Kong, Hong Kong**
PALIMAX, TEL: 5-468161 ext 555

**Intl** **Italy, Milan**
Cefra SRL, TEL: 02-65-68-68

**Intl** **Japan**
Inmos Japan K.K., TEL: 035-052-840

**Intl** **Japan, Tokyo**
Matsushita Electric, TEL: 03-435-4501

**Intl** **Korea**
Tess-KO Enterprises, TEL: 82-2-552-9483

**Intl** **Singapore**
CALTRON, TEL: 4567222

**Intl** **Taiwan**
Helm Engineering, TEL: 02-7091888

**Intl** **United Kingdom, Bristol**
Inmos Sales, TEL: 454-616616

**Intl** **United Kingdom, Cheshire**
TC Electronics, TEL: 061-427-2020

**Intl** **United Kingdom, Herts**
Dexter Electronics, TEL: 0438-36

**Intl** **United Kingdom, Lanarkshire**
Stuart Electronics, TEL: 0555-892-393

**Intl** **United Kingdom, West Sussex**
Hartech Ltd., TEL: 0243-773511

**Intl** **West Germany**
Inmos Sales, TEL: 089-319-1028

## Distributors

**AL** **Huntsville**
Arrow Elctrns., 205-837-6955

**AL** **Huntsville**
Pioneer-Standard, 205-837-9300

**AZ** **Phoenix**
Wyle, 602-866-2888

**AZ** **Tempe**
Arrow Elctrns., 602-968-4800

**AZ** **Tempe**
Anthem Elctrns., 602-966-6600

**CA** **Calabasas**
Wyle, 818-880-9001

**CA** **Chatsworth**
Arrow Electronics, 818-701-7500

**CA** **Chatsworth**
Anthem Elctrns., 818-700-1000

**CA** **El Segundo**
Wyle, 213-322-8100

**CA** **Garden Grove**
Wyle, 714-891-1717

**CA** **Hayward**
Arrow Elctrns., 415-487-4300

**CA** **Irvine**
Wyle, 714-863-9953

**CA** **Irvine**
Wyle (Military), 714-851-9953

**CA** **Irvine**
Anthem Electronics, 714-768-4444

**CA** **Rancho Cordova**
Wyle, 916-638-5282

**CA** **Sacramento**
Anthem Electronics, 916-922-6800

**CA** **San Diego**
Wyle, 619-565-9171

**CA** **San Diego**
Anthem Elctrns., 619-453-4871

**CA** **San Diego**
Arrow Elctrns., 619-565-4800

**CA** **San Jose**
Anthem Elctrns., 408-295-4200

**CA** **Santa Clara**
Wyle, 408-727-2500

**CA** **Sunnyvale**
Arrow Elctrns., 408-745-6600

**CA** **Tustin**
Arrow Elctrns., 714-838-5422

**CO** **Denver**
Arrow Elctrns., 303-696-1111

**CO** **Englewood**
Anthem Electrns., 303-790-4500

**CO** **Thornton**
Wyle, 303-457-9953

**CT** **Meriden**
Lionex, 203-237-2282

**CT** **Milford**
Falcon Elctrns., 203-878-5272

**CT** **Wallingford**
Arrow Elctrns., 203-265-7741

**FL** **Deerfield Beach**
Arrow Electronics, 305-429-8200

**FL** **Ft. Lauderdale**
Pioneer Standard, 305-428-8877

**FL** **Ft. Lauderdale**
Arrow Elctrns., 305-776-7790

**FL** **Orlando**
Pioneer Standard, 305-834-9090

**FL** **Palm Bay**
Arrow Elctrns., 305-725-1480

**GA** **Norcross**
Pioneer Standard, 404-448-1711

**GA** **Norcross**
Arrow Elctrns., 404-449-8252

**IL** **Elk Grove**
Anthem Electronics, 312-640-6066

**IL** **Schaumburg**
Arrow Elctrns., 312-397-3440

**IN** **Indianapolis**
Arrow Elctrns., 317-243-9353

**IA** **Cedar Rapids**
Arrow Elctrns., 319-395-7230

**KS** **Lenexa**
Arrow Electronics, 913-541-9542

**MD** **Columbia**
Lionex Corporation, 301-995-6640

**MD** **Columbia**
Arrow Elctrns., 800-842-7769

**MD** **Gaithersburg**
Pioneer Standard, 301-921-0660

**MA** **Westborough**
Future Electronics, 613-820-8313

**MA** **Wilmington**
Lionex Corp., 617-657-5170

**MA** **Woburn**
Arrow Elctrns., 617-933-8130

**MI** **Ann Arbor**
Arrow Elctrns., 313-971-8220

**MI** **Grand Rapids**
Arrow Electronics, 616-243-0912

**MN** **Eden Praire**
Lionex, 612-944-5454

**MN** **Edina**
Arrow Elctrns., 612-830-1800

**MO** **St. Louis**
Arrow Elctrns., 314-567-6888

**NH** **Manchester**
Arrow Elctrns., 603-668-6968

**NJ** **Fairfield**
Lionex Corp., 201-227-7960

**NJ** **Marlton**
Arrow Electronics, 609-596-8000

**NJ** **Parsippany**
Arrow Electronics, 201-538-0900

**NM** **Albuquerque**
Arrow Elctrns., 505-243-4566

**NY** **Farmingdale**
Arrow Electronics, 516-293-6363

**NY** **Hauppauge**
Arrow Elctrns., 516-231-1000

**NY** **Hauppauge**
Lionex Corp., 516-273-1660

**NY** **Melville**
Arrow Elctrns., 516-694-6800

**NY** **Rochester**
Arrow Elctrns., 716-427-0300

**NC** **Charlotte**
Pioneer Standard, 704-527-8188

**NC** **Raleigh**
Arrow Elctrns., 919-876-3132

**NC** **Winston-Salem**
Arrow Electronics, 919-725-8711

**NC** **Winston-Salem**
Arrow Elctrns., 919-725-8711

**OH** **Centerville**
Arrow Elctrns., 513-435-5563

**OH** **Solon**
Arrow Elctrns., 216-248-3990

**OK** **Tulsa**
Arrow Elctrns., 918-665-7700

**OR** **Beaverton**
Anthem Elctrns., 503-643-1114

## Inmos (Cont'd)

**OR** **Portland**
Wyle, 503-640-6000
**OR** **Tigard**
Arrow Elctrns., 503-684-1690
**PA** **Horsham**
Lionex Corp., 215-443-5150
**PA** **Horsham**
Pioneer, 215-674-4000
**PA** **Monroeville**
Arrow Elctrns., 412-856-7000
**TX** **Austin**
Arrow Electronics, 512-835-4180
**TX** **Austin**
Wyle, 512-834-9957
**TX** **Carrollton**
Arrow Elctrns., 214-380-6464
**TX** **Houston**
Wyle, 713-879-9953
**TX** **Houston**
Arrow Elctrns., 713-530-4700
**TX** **Richardson**
Wyle, 214-235-9953
**UT** **Salt Lake City**
Wyle, 801-974-9953
**UT** **Salt Lake City**
Anthem Elctrns., 801-973-8555
**UT** **Salt Lake City**
Arrow Elctrns., 801-972-0404
**WA** **Bellevue**
Wyle, 206-453-8300
**WA** **Bellevue**
Arrow Elctrns., 206-643-4800
**WA** **Redmond**
Anthem Elctrns., 206-881-0850
**WI** **Brookfield**
Arrow Elctrns., 414-792-0150
**Can** **Baxter Ctr., Ontario**
Future Elctrns., 613-820-8313, All Literature to: Westborough, MA 613-820-8313
**Can** **Calgary, Alberta**
Future Elctrns., 403-235-5325
**Can** **Downsview, Ontario**
Future Elctrns., 416-638-4771
**Can** **Pointe Claire, Quebec**
Future Elctrns., 514-694-7710
**Can** **Vancouver, British Columbia**
Future Elctrns., 604-438-3321
**Intl** **Australia, Sydney**
Hawk Electronics, TEL: 023-255-30
**Intl** **Austria, Vienna**
Othmar Lackner, TEL: 43-0222-75-26-18
**Intl** **Belgium, Brussels**
Diode, TEL: 02-216-21-00
**Intl** **Denmark, Silkeborg**
Peter Peterson A/S, TEL: 45-6-83-62-11
**Intl** **Finland, Helsinki**
Field Oy, TEL: 0-692-25-77
**Intl** **France**
Scaib SA, TEL: 14-687-23-13
**Intl** **France, Paeig**
Tekelec Airtronic, TEL: 45-34-75-35
**Intl** **Ireland, Dublin**
Micro Marketing Ltd., TEL: 0001-856288
**Intl** **Israel, Tel Aviv**
R.D.T. Elctrns. Ltd., TEL: 03-483211
**Intl** **Italy, Milan**
Celdis Italiana S.p.A., TEL: 61-21-651
**Intl** **Netherlands, Haaften**
Techmation Elctrns. BV, TEL: 041-89-22-22
**Intl** **Norway, Oslo**
Ola Tandberg Elektro A/S, TEL: 02-26-99-55
**Intl** **Portugal, Lisbon**
Teleprinta, TEL: 1-54-84-23
**Intl** **South Africa, Pretoria**
Electronic Building Elements, TEL: 27-12-469-221
**Intl** **Spain, Madrid**
Diode Espana, TEL: 01-455-36-86
**Intl** **Sweden, Stockholm**
AB Gosta Backstrom, TEL: 08-54-10-80
**Intl** **Switzerland, Zurich-Schlieren**
Datacomp A.G., TEL: 01-740-51-40
**Intl** **United Kingdom, High Wycombe**
Rapid Silicon Ltd., TEL: 0494-26271
**Intl** **United Kingdom, Sunbury on Thames, ddlesex**
Hawke Elctrns., TEL: 01-979-7799
**Intl** **West Germany, Munich**
E2000 A.G., TEL: 089-42-00-10
**Intl** **West Germany, Quickborn**
Astek Elctrns., TEL: 41-91-87-11

## Innervision Computers

Innervision Computers
1634 Roll Street
Santa Clara, California 95050
408-244-8474

## Innovative Research

Innovative Research, Inc.
17071 Kampen Lane
Huntington Beach, California 92647
714-842-0492

## Inova Microelectronics

**Inova Microelectronics Corp.**
**2220 Martin Avenue**
**Santa Clara, California 95050**
**408-980-0730**
**TELEX: 510-601-8887**
**FAX: 408-980-1805**

## Intech

**Intech Advanced Analog**
**2270 Martin Avenue**
**Santa Clara, California 95050**
**408-988-4930**
**TWX: 910-338-2213**
**FAX: 408-988-2702**

### Sales Office & Representatives

**AZ** **Scottsdale**
Tusar, 602-998-3688
**CA** **Mtn. View**
Marcon, 415-964-8046
**CA** **Orange**
XBX, 714-998-8200
**CA** **San Diego**
Bestronics, 619-693-1111
**CA** **San Diego**
Bestronics, 619-693-1111
**CA** **Santa Clara**
Reptech, 408-749-9494
**CO** **Englewood**
Taylor Mktng., 303-850-0207
**CT** **North Haven**
Kitchen & Kutchin, 203-239-0212
**FL** **Coral Springs**
CBC, 305-755-1111
**FL** **Longwood**
, 305-831-5380
**GA** **Norcross**
, 404-447-6478
**ID** **Boise**
N.R. Schultz, 208-377-8686
**IL** **Berkeley**
ESA Assoc., 312-544-0120
**IN** **Indianapolis**
CC Electro, 317-255-1508
**MD** **Towson**
Arbotek, 301-825-0775
**MA** **Burlington**
Kitchen & Kutchin, 617-229-2660
**MI** **Madison Heights**
Pine Sales, 313-589-0350
**MN** **Eden Prairie**
High Technology, 612-944-7274
**MO** **Hazelwood**
Acorn, 314-731-2002
**NY** **Huntington**
Compar, New York, 516-423-5660
**NY** **Syracuse**
, 315-437-2845
**NC** **Raleigh**
, 919-851-8165
**OH** **Cincinnati**
Makin, 513-871-2424
**OR** **Beaverton**
N.R. Schultz, 503-643-1644
**TX** **Dallas**
MGR, 214-238-5246
**UT** **Ogden**
Taylor Mktng., 801-546-9570
**WA** **Bellevue**
N.R. Schultz, 206-454-0300
**Can** **Ontario, Concord**
Kaytronics, 416-669-2262
**Can** **Quebec, Ville St. Pierre**
Kaytronics, 514-367-0101
**Can** **Vancouver**
Kaytronics, 604-581-5005

## Integrated Circuit Design Centre

Integrated Circuit Design Centre (PTY) Ltd.
CEFIM Building, University of Pretoria, P.O. Box 11393
Brooklyn 0011, Republic of South Africa
27 12 420-2952 (International), (012) 420-2952 (National)
TELEX: 321648
FAX: 342 1209

## Integrated Circuit Systems

**Integrated Circuit Systems, Inc.**
**2626 Van Buren Ave., P.O. Box 968**
**Valley Forge, Pennsylvania 19482-0968**
**215-666-1900**
**FAX: 215-666-1099**

**Specific Product Information:**
VP Sales/Marketing ..... Dr. Jere Hohmann

### Sales Office & Representatives

**MA** **Columbia**
Robert Electronics, 301-995-1900
**OH** **Aurora**
EMA, 216-562-6104
**OH** **Centerville**
EMA, 513-433-2800
**PA** **Huntingdon Valley**
Omega, 215-947-4135

## Integrated Circuits Inc.

Integrated Circuits Inc.
10301 Willow Rd. N.E.
Redmond, Washington 98052
206-882-3100


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## Integrated Device Technology

**Integrated Device Technology, Inc.**
**3236 Scott Boulevard**
**Santa Clara, California 95054**
**408-727-6116**
**TWX: 910-338-2070**

### Sales Office & Representatives

**AL** **Huntsville**
Montgomery Marketing, 205-830-0498

**AL** **Huntsville**
Hamilton/Avnet, 205-837-7210

**AL** **Huntsville**
Hall-Mark Electronics, 205-837-8700

**AZ** **Phoenix**
Hall-Mark Electronics, 602-437-1200

**AZ** **Scottsdale**
Western High Tech. Mktg., 602-860-2702

**AZ** **Tempe**
Insight Electronics, 602-829-1800

**AZ** **Tempe**
Hamilton/Avnet, 602-231-5100

**CA** **Agoura**
Insight Electronics, 818-707-2100

**CA** **Canoga Park**
Hall-Mark Electronics, 818-716-7300

**CA** **Chatsworth**
Hamilton/Avnet, 818-700-6500

**CA** **Chatsworth**
Hamilton/Avnet, 818-700-2600

**CA** **Citrus Heights**
Hall-Mark Electronics, 916-722-8600

**CA** **Costa Mesa**
Hamilton/Avnet, 714-641-4100

**CA** **Costa Mesa**
Hamilton/Avnet, 714-754-6111

**CA** **Costa Mesa**
Insight Electronics, 714-556-6890

**CA** **Culver City**
Hamilton/Avnet

**CA** **Gardena**
Hamilton/Avnet, 213-217-6700

**CA** **Ontario**
Hamilton/Avnet, 714-989-4602

**CA** **Sacramento**
Hamilton/Avnet, 916-925-2216

**CA** **San Diego**
Quest-Rep, 619-565-8797

**CA** **San Diego**
Hall-Mark Electronics, 619-268-1202

**CA** **San Diego**
Hamilton/Avnet, 619-571-7510

**CA** **San Diego**
Insight Electronics, 619-587-0471

**CA** **San Jose**
Hall-Mark Electronics, 408-946-0900

**CA** **Santa Ana**
IDT—Southwestern Area, 714-641-0601

**CA** **Santa Clara**
IDT Sales Office—Northwestern Area, 408-727-6116

**CA** **Sunnyvale**
Hamilton/Avnet, 408-743-3355

**CA** **Torrance**
Hall-Mark Electronics, 213-217-8400

**CA** **Tustin**
Hall-Mark Electronics, 714-669-4700

**CA** **Woodland Hills**
IDT, 818-347-4530

**CO** **Denver**
IDT, 303-628-5494

**CO** **Englewood**
Hall-Mark Electronics, 303-790-1662

**CO** **Englewood**
Hamilton/Avnet, 303-740-1000

**CO** **Englewood**
Thorson Rocky Mountain, 303-799-3435

**CT** **Danbury**
Hamilton/Avnet, 203-797-2800

**CT** **Southbury**
Lindco Assoc., 203-266-0728

**CT** **Wallingford**
Hall-Mark Electronics, 203-269-0100

**FL** **Clearwater**
Hall-Mark Electronics, 813-530-4543

**FL** **Clearwater**
Delmac Sales IInc., 813-447-5192

**FL** **Deerfield Beach**
Delmac Sales Inc., 305-447-7788

**FL** **Ft. Lauderdale**
Hamilton/Avnet, 305-971-2900

**FL** **Longwood**
Delmac Sales Inc., 305-831-0040

**FL** **Melbourne**
I.D.T. Sales Offices, 305-242-1821

**FL** **Orlando**
Hall-Mark Electronics, 305-855-4020

**FL** **Pompano Beach**
Hall-Mark Electronics

**FL** **St. Petersburg**
Hamilton/Avnet, 813-576-3930

**FL** **Winter Park**
Hamilton/Avnet, 305-628-3888

**GA** **Norcross**
Hall-Mark Electronics, 404-447-8000

**GA** **Norcross**
Hamilton/Avnet, 404-447-7507

**GA** **Norcross**
Montgomery Marketing, 404-447-6124

**IL** **Bensenville**
Hamilton/Avnet, 312-860-7700

**IL** **Park Ridge**
Synmark Sales/Inc., 312-390-9696

**IL** **Schaumberg**
IDT Sales Offices, 312-843-1262

**IL** **Wooddale**
Hall-Mark Electronics, 312-860-3800

**IN** **Carmel**
Hamilton/Avnet, 317-844-9333

**IN** **Ft. Wayne**
Arete Sales, 219-423-1478

**IN** **Greenwood**
Arete Sales, 317-882-4407

**IN** **Indianapolis**
Hall-Mark Electronics, 317-872-8875

**IA** **Cedar Rapids**
Hamilton/Avnet, 319-362-4757

**IA** **Cedar Rapids**
REP Assoc., 319-373-0152

**KS** **Lenexa**
Hall-Mark Electronics, 913-888-4747

**KS** **Overland Park**
Hamilton/Avnet, 913-888-8900

**KS** **Shawnee Mission**
Design Solutions, 913-677-4747

**KY** **Lexington**
Hamilton/Avnet, 606-259-1475

**MD** **Annapolis**
IDT, 301-858-5423

**MD** **Baltimore**
Micro Comp, 301-644-5700

**MD** **Columbia**
Hall-Mark Electronics, 301-988-9800

**MD** **Columbia**
Hamilton/Avnet, 301-995-3500

**MD** **Columbia**
Vantage Components, 301-720-5100

**MA** **Billerica**
Hall-Mark Electronics, 617-935-9777

**MA** **Framingham**
IDT Sales Office—Eastern Area, 617-872-4900

**MA** **Peabody**
Hamilton/Avnet, 617-531-3701

**MI** **Grand Rapids**
Hamilton/Avnet, 616-243-8805

**MI** **Livonia**
Hamilton/Avnet, 313-522-4700

**MI** **Southfield**
Rathsburg Assocs., 313-559-9700

**MN** **Eden Prairie**
Hall-Mark Electronics, 612-854-3223

**MN** **Eden Prairie**
Comprehensive Tech. Sales, 612-941-7181

**MN** **Minneapolis**
IDT, 612-831-5422

**MN** **Minnetonka**
Hamilton/Avnet, 612-932-0600

**MO** **Earth City**
Hamilton/Avnet, 314-344-1220

**MO** **Earth City**
Hall-Mark Electronics, 314-291-5350

**MO** **Maryland Heights**
Design Solutions, 314-739-3630

**NH** **Manchester**
Hamilton/Avnet, 603-624-9400

**NJ** **Cherry Hill**
Hamilton/Avnet, 609-424-0100

**NJ** **Clifton**
Vantage Components, 201-777-4100

**NJ** **Fairfield**
Hall-Mark Electronics, 201-575-4415

**NJ** **Fairfield**
Hamilton/Avnet, 201-575-3390

**NJ** **Mt. Laurel**
SJ Associates, 609-866-1234

**NJ** **Mt. Loral**
Hall-Mark Electronics, 609-424-7300

**NJ** **Pinebrook**
Hall-Mark Electronics, 201-882-9773

**NM** **Albuquerque**
Western High Tech Marketing, 505-884-2256

**NM** **Albuquerque**
Hamilton/Avnet, 505-765-1500

**NY** **Buffalo**
Quality Components, 716-837-5430

**NY** **Commack**
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**Specific Product Information:**
Ronald Colino

**Applications Engineering:**
Ronald Colino

**Literature:**
Nancy Leidig

**Price and Delivery:**
Nancy Leidig

**Follow up on Order:**
Nancy Leidig

**All Other Information:**
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**VA** **Sterling**
Beacon North, 703-478-2480

## MICRO/SYS

MICRO/SYS
1011 Grand Central Avenue
Glendale, California 91201-3010
818-244-4600

## Microbar Systems

Microbar Systems Inc.
785 Lucerne Drive
Sunnyvale, California 94086
408-720-9300
FAX: ;910-373-2047

## Microcomputer Systems

Microcomputer Systems Inc.
1814 Ryder Drive
Baton Rouge, Louisiana 70808
504-769-2154

## Microcosm

Microcosm
15275-E S.W. Koll Parkway
Beaverton, Oregon 97006
503-626-6100
TELEX: 759527

## Microdesigns

Microdesigns, Inc.
1874 Forge Street
Tucker, Georgia 30084
404-493-6318

## Micron Technology

Micron Technology
2805 E. Columbia Road
Boise, Idaho 83706
208-383-4000
TWX: 910-970-5973

## Micropac

Micropac Industries, Inc.
905 East Walnut Street
Garland, Texas 75040
214-272-3571
TWX: 910-860-5186

## Microsim

Microsim
23175 La Cadena Dr.
Laguna Hills, California 92653
714-770-3022

## Microvoice

Microvoice Corp.
5 Vanderbilt
Irvine, California 92718
714-859-1091

## Mikros Systems Corp.

Mikros Systems Corp.
3828 Quakerbridge Road
Mercerville, New Jersey 08619

## MilerTronics

MilerTronics
Division of George Miler, Inc.
303 Airport Road
Greenville, South Carolina 29607
803-242-9232

## Miller Technology

Miller Technology Inc.
647 North Santa Cruz Avenue
Los Gatos, California 95030
408-395-2032

## Mimic

Mimic, Inc.
P.O. Box 705
Islington, Massachusetts 02090
617-329-9593

## Mini Computer Technology

Mini Computer Technology
696 E. Trimble Road
San Jose, California 95131
408-435-1616
TWX: 910 338-2281
FAX: 408 435-2709

## Minntronics

Minntronics Corporation
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St. Paul, Minnesota 55109
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## Mitchell Electronics

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614-594-8532


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## Mitsubishi Electronics

**Mitsubishi Electronics America, Inc.**
**Semiconductor Division**
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**Sunnyvale, California 94086**
**408-730-5900**
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**TWX: 910-339-9549**

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**KS** **Wichita**
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**MA** **Woburn**
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**Can** **Neapean, Ontario**
Tech Rep Electronics Ltd., 613-225-9186

**Can** **St. Laurent, Quebec**
Tech Rep Electronics Ltd., 514-337-6046

**PR** **San Turce**
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**CA** **Chatsworth**
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**CA** **Costa Mesa**
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**UT** **Salt Lake City**
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**Can** **Toronto, Ontario**
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**Can** **Vancouver, British Columbia**
Space Elec Sales, Corp., 604-437-3611

## Modula

Modula Corp
1121 South Orem Blvd.
Orem, Utah 84058
801-375-7400

## Monolithic Memories

Monolithic Memories, Inc.
2175 Mission College Blvd.
Santa Clara, California 95054
408-970-9700

## Monolithic Systems

Monolithic Systems Corporation
84 Inverness Circle East
Englewood, Colorado 80112
303-790-7400

## Morrow Technologies

Morrow Technologies Corp.
3026 Owen Drive
Antioch, Tennessee 37013
615-793-3555

## Mosaid

Mosaid Inc.
P.O. Box 13579
Kanata, Ontario, Canada K2K 1X6
613-836-3134

## Motorola

**Motorola Semiconductor Products**
**5005 East McDowell Road**
**Phoenix, Arizona 85008**

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**Literature:**
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Motorola, 305-628-2636
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**WA** **Bellevue**
Thorson Co. Northwest, 206-455-9180

**WI** **Milwaukee/Wauwatosa**
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**Can** **Burnaby, B.C.**
Motorola, 604-434-9134

**Can** **Montreal, Quebec**
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**Can** **North York, Ontario**
Motorola, 416-497-8181

**Can** **Ottawa, Ontario**
Motorola, 613-226-3491

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**Intl** **Australia, Sydney**
Motorola, TEL: (02) 438-1955, 439-2242

**Intl** **Austria, Vienna**
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**Intl** **Brazil, Sao Paulo**
Motorola, TEL: (011) 572 3553

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Galena Technology Group, TEL: 702-786-5030

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**Intl** **Switzerland, Geneva**
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**Intl** **Switzerland, Zurich**
Motorola, TEL: (01) 730 40 74

**Intl** **United Kingdom, Aylesbury**
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**AZ** **Phoenix**
Schweber Elect., 602-997-4874

**AZ** **Tempe**
Bell Elect., 602-966-7800

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Time Electronics, 714-937-0911

**CA** **Anaheim**
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**CA** **Canoga Park**
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**CA** **Canoga Park**
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Hamilton Elect., 818-700-6500

**CA** **Chatsworth**
Hamilton Electro Sls, 818-700-6500

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Time Electronics, 818-998-7200

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**CA** **Costa Mesa**
Hamilton Electro Sales, 714-641-4100

**CA** **Culver City**
Hamilton/Avnet Corporate, 213-558-2501

**CA** **Culver City**
Hamilton Electro Sales/L.A., 213-558-2501

**CA** **Gardena**
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Schweber Elctrns., 213-537-4321, 714-863-0200

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Bell Industries, 916-969-3100

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**CO** **Denver**
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**CO** **Englewood**
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Allied Electronics, 312-697-8200

**IL** **Chicago**
Bell Industries, 312-640-1910

**IL** **Fort Wayne**
Bell Industries, 219-423-3422

**IL** **Urbana**
Bell Industries, 217-328-1077

**IL** **Woodale**
Hall-Mark Elctrns., 312-860-3800

**IN** **Indianapolis**
Hall-Mark Electronics, 317-872-8875

**IN** **Indianapolis**
Pioneer Elctrns, 317-849-7300

**IN** **Indianapolis**
Bell Industries, 317-299-5487

**IN** **Indianapolis**
Bell Industries, 317-875-8200

**IA** **Cedar Rapids**
Bell Industries, 319-395-0730

**KS** **Lenexa**
Hall-Mark Elctrns., 913-888-4747

**MD** **Baltimore**
Hall-Mark Elctrns., 301-988-9800

**MD** **Baltimore**
Allied Electronics, 301-381-1560

**MD** **Baltimore**
Allied Electronics, 301-423-0161

**MD** **Gaitherberg**
Hall-Mark Elctrns., 301-921-0660

**MA** **Billerica**
Hall-Mark Electronics, 617-935-9777



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Allied Electronics, 617-942-0150

**MA** **Boston**
Semi Dice, Inc., 617-238-8344

**MA** **Lexington**
Pioneer, 617-861-9200

**MA** **Norwood**
Gerber Elctrns., 617-769-6000

**MA** **Westborough**
Future Elctrns., 617-366-2400

**MI** **Ann Arbor**
Bell Industries, 313-971-9093

**MI** **Grand Rapids**
Pioneer, 616-698-1800

**MI** **Livonia**
Pioneer Elctrns., 313-525-1800

**MN** **Bloomington**
Hall-Mark Elctrns., 612-941-2600

**MN** **Minnetonka**
Pioneer Elctrns., 612-935-5444

**MO** **Earth City**
Hall-Mark Elctrns., 314-291-5350

**NJ** **Fairfield**
Hall-Mark Elctrns., 201-575-4415

**NJ** **Fairfield**
Nu-Horizons Electronics, 201-882-8300

**NJ** **Mt. laurel**
Allied Electronics, 609-234-7769

**NJ** **Mt. laurel**
Hall-Mark Electronics, 609-235-1900

**NJ** **Mt. Laurel**
Hall-Mark Elctrns., 609-235-1900

**NJ** **Pine Brook**
Pioneer Elctrns., 201-575-3510

**NM** **Albquerque**
Hall-Mark Electronics, 505-344-2454

**NM** **Albuquerque**
Bell Inds., 505-292-2700

**NY** **Binghampton**
Pioneer Elctrns., 607-722-9300

**NY** **Buffalo**
Sumit Distributors, Inc., 716-887-2800

**NY** **Fairport**
Pioneer Elctrns., 716-381-7070

**NY** **Long Island**
Hall-Mark Elctrns., 516-737-0600

**NY** **Long Island**
Allied Electronics, 516-248-2360

**NY** **No. Amityville**
Nu-Horizons Electronics, 516-226-6000, 800-645-9222

**NY** **Rochester**
Allied Electronics, 716-244-9449

**NY** **Woodbury**
Pioneer, 516-921-8700

**NC** **Charlotte**
Pioneer Elctrns., 704-527-8188

**NC** **Raleigh**
Hall-Mark Elctrns., 919-872-0712

**NC** **Raleigh**
Allied Electronics, 919-876-5845

**OH** **Cleveland**
Pioneer Elctrns, 216-587-3600

**OH** **Dayton**
Pioneer Elctrns, 513-236-9900

**OH** **Dayton (Industrial)**
Bell Industries, 513-435-8660

**OH** **Dayton (Military)**
Bell Industries, 513-434-8231

**OH** **Solon**
Hall-Mark Elctrns., 216-349-4632

**OH** **Worthington**
Hall-Mark Elctrns., 614-888-3313

**OK** **Tulsa**
Hall-Mark Elctrns., 918-251-1663

**OR** **Portland**
Bell Industries, 503-241-4115

**OR** **Portland**
Anthem Electronics, Inc., 503-643-1114

**PA** **Horsham**
Pioneer Elctrns, 215-674-4000

**PA** **Pittsburgh**
Pioneer Elctrns, 412-782-2300

**PA** **Pittsburgh**
Allied Electronics, 412-367-4124

**TN** **Nashville**
Bell Industries, 615-367-4400

**TX** **Austin**
Pioneer, 512-835-4000

**TX** **Austin**
Hall-Mark Elctrns., 512-258-8848

**TX** **Dallas**
Pioneer, 2214-386-7300

**TX** **Dallas**
Hall-Mark Elctrns., 214-341-1147

**TX** **Dallas**
Hall-Mark Electronics, 214-533-4300

**TX** **Dallas**
Bell Industries, 214-690-0466

**TX** **Dallas**
Allied Electronics, 214-553-4370

**TX** **Dallas**
Pioneer, 214-386-7300

**TX** **Ft. Worth**
Allied Electronics, 817-336-5401

**TX** **Houston**
Pioneer, 713-988-5555

**TX** **Houston**
Hall-Mark Elctrns., 713-781-6100

**UT** **Salt Lake City**
Anthem Elctrns., 801-973-8555

**UT** **Salt Lake City**
Bell Inds., 801-972-6969

**WA** **Redmond**
Anthem Elctrns., 206-881-0850

**WA** **Seattle**
Bell Inds., 206-747-1515

**WA** **Seattle**
Allied Electronics, 206-547-2827

**WI** **Milwaukee**
Bell Industries, 414-547-8879

**WI** **New Berlin**
Hall-Mark Elctrns., 414-797-7844, 800-242-5252

**Can** **British Columbia, Vancouver**
Intek Elctrns. Ltd., 604-294-8100

**Can** **Calgary, Alberta**
Future Elctrns., 403-259-6408

**Can** **Downsview, Ontario**
Future Elctrns. Corp., 416-638-4771

**Can** **Ottawa, Ontario**
Future Elctrns. Corp., 613-820-8313

**Can** **Pointe Claire, Quebec**
Future Elctrns., Inc., 514-694-7710

**Can** **Vancouver, B.C.**
Future Elctrns., 604-294-1166

**Intl** **Bancouver, British Columbia**
Saynor Varah, TEL: 604-461-2222

## Pro-Log

Pro-Log Corporation
2560 Garden Road
Monterey, California 93940
408-372-4593
TWX: 910-360-7082

## Proximity

Proximity Technology Inc.
3511 NE 22nd Av.
Ft. Lauderdale, Florida 33308
305-566-3511

## Quadtree

Quadtree
1170 Route 22
Bridgewater, New Jersey 08807
201-725-2272

## Qualogy

Qualogy Corp.
2241 Lundy Avenue
San Jose, California 95131
408-946-5800

## Quantic Laboratories, Inc.

Quantic Laboratories, Inc.
200-281 McDermot Ave.
Winnepeg, Canada R3B059
204-343-2552

## RLC Enterprises

R.L.C. Enterprises
1117 Hillview Drive
Milpitas, California 95035
408-946-7471

## Racal-Redac

Racal-Redac
4 Liberty Way
Westford, Massachusetts 01886
617-692-4900

## Rancho Technology

Rancho Technology Center
8632 Archibald Avenue, Suite 109
Rancho Cucamonga, Calfornia 91730
714-987-3966

## Rapid Systems

Rapid Systems
433 N. 34th Street
Seattle, Washington 98103
206-547-8311
TELEX: 265017UR

## Raytheon Semiconductor

**Raytheon Company**
**Semiconductor Division**
**350 Ellis Street**
**Mountain View, California 94039-7016**
**415-968-9211**
**TWX: 910-379-6481**

**Specific Product Information:**
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Digital ..... G. Jones
Discrete ..... G. Jones
LSI/Memory ..... Jack Von Den Heuvel
Gate Array ..... D. McCoy

**Price and Delivery:**
Local Field Sales Office

**Place an Order:**
Local Field Sales Office

**Follow up on Order:**
Customer Service

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### Sales Office & Representatives

**AL** **Huntsville**
Macro Mktg. Assocs., 205-883-9630

**AZ** **Scottsdale**
Semper Fi Sales Co., 602-991-4601

**CA** **Irvine**
Raytheon Regional Sales Office, 714-833-9042

**CA** **Irvine**
Raytheon Sales Office, 714-833-9042

**CA** **Mtn. View**
Raytheon Regional Sales Office, 415-966-7636

**CA** **San Diego**
Earle Associates, Inc., 619-278-5441

**CO** **Littleton**
Simpson Assoc., 303-794-8381

**CO** **Littleton**
Simpson Assocs., Inc., 303-794-8381

**CT** **Guilford**
Data Mark, Inc., 203-454-0575

**FL** **Alamonte Springs**
Raytheon Regional Sales Office, 305-339-4820

**FL** **Coral Springs**
Raytheon District Office, 305-752-2797

**FL** **Oviedo**
Conley Associates, 305-365-3283

**GA** **Norcross**
Macro Marketing, 404-662-5580

**GA** **Norcross**
Raytheon District Office, 404-449-4092

**IL** **Des Plaines**
Raytheon Regional Sales Office, 312-297-5540

**IL** **Elk Grove Village**
Carlson Elctrn. Sales Co., 312-956-8240

**IN** **Indianapolis**
J & W Sales, 317-842-3740

**IA** **Cedar Rapids**
Carlson Elctrn. Sales, 319-377-6341

**MD** **Towson**
Arbotec Assoc. Inc., 301-825-0775

**MA** **Lexington**
Raytheon Regional Sales Office, 617-861-1830

**MA** **Waltham**
Dynasel Assoc., 617-890-6777

**MN** **Eden Prairie**
Aldridge Assoc. Inc., 612-944-8433

**MN** **Minneapolis**
Raytheon Regional Sales Office, 612-920-7935

**MO** **St. Louis**
John G. Macke Co., 314-432-2830

**NM** **Albuquerque**
Rep NEW Tec, 505-293-2582

**NY** **Commack**
ERA, Inc., 516-543-0510

**NY** **Hauppauge**
Raytheon Regional Sales Office, 516-582-3646

**NY** **Syracuse**
Pi'Tronics, Inc., 315-455-7346

**OH** **Beachwood**
Thompson & Assocs., Inc., 216-831-6277

**OH** **Dayton**
Raytheon District Office, 513-293-1888

**OH** **Dayton**
Thompson & Assocs., Inc., 515-435-7733

**OH** **Orient**
Thompson & Associates, 614-877-4304

**OK** **Tulsa**
Logic I, 214-234-0765

**PA** **Erdenheim**
OMNI Sales, 215-233-4600

**PA** **King of Prussia**
Raytheon Regional Sales Office, 215-687-8300

**TX** **Austin**
Logic I, 512-459-1297

**TX** **Farmers Branch**
Raytheon District Office, 214-484-5882

**TX** **Ft. Worth**
Logic I, 817-336-2192

**TX** **Houston**
Logic I, 713-981-0233

**TX** **Richardson**
Logic 1, 214-234-0765

**UT** **Midvale**
Simpson Assoc., 801-566-3691

**WA** **Bellevue**
Raytheon District Office, 206-883-7547

**Can** **Brampton, Ontario**
Cantec Reps. Inc., 416-791-5922

**Can** **Dollard des Ormeaux, Quebec**
Cantec Reps. Inc., 514-683-6131

**Can** **Ottawa, Ontario**
Cantec Reps. Inc., 613-725-3704

**Intl** **France, Le Plessis Robinson**
Raytheon Semiconductor France, TEL: 01 631 06 76

**Intl** **Germany, Munchen**
Raytheon HALBLEITER GmbH, TEL: 089/539693

**Intl** **Germany, Radolfzell**
Raytheon Halbleiter GmbH, TEL: 07732-56691/92

**Intl** **Germany, Uetersen**
Raytheon Halbleiter GmbH, TEL: 04122-44950

**Intl** **Japan, Tokyo**
New Japan Radio Co., Ltd., TEL: (502) 2331

**Intl** **United Kingdom, Bucks**
Raytheon Semiconductor, TEL: (0494) 450327

### Distributors

**AL** **Huntsville**
Kierulff Electronics, 205-833-6070

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Kierulff Electronics, 205-833-6070

**AZ** **Phoenix**
Arizona Comps. Co., 602-269-5655

**AZ** **Phoenix**
Kierulff Elctrns., 602-437-0750

**AZ** **Tempe**
Arrow Electronics, 602-968-4800

**CA** **Burbank**
Elmo Semiconductor, 818-768-7400

**CA** **Chatsworth**
Arrow Electronics, 213-701-7500

**CA** **Commerce**
Kierulff Elctrns., 213-725-0325

**CA** **Cypress**
Kierulff Electronics, 714-220-6300

**CA** **San Diego**
Arrow Elctrns., 619-565-4800

**CA** **San Diego**
Kierulff Elctrns., 619-278-2122

**CA** **San Jose**
Kierulff Electronics, 408-971-2600

**CA** **Sunnyvale**
Arrow Elctrns., 408-745-6600

**CA** **Sunnyvale**
Bell Inds., 408-734-8570

**CA** **Tustin**
Arrow Electronics, 714-838-5422

**CA** **Tustin**
Kierulff Elctrns., 714-731-5711

**CA** **Walnut**
ACI, 714-594-1731

**CA** **Yorba Linda**
Zeus Comps., Inc., 714-921-9000, 714-632-6880

**CO** **Aurora**
Arrow Elctrns., 303-932-2999

**CO** **Englewood**
Kierulff Electronics, 303-790-4444

**CO** **Wheatridge**
Bell Inds., 303-424-1985

**CT** **Wallingford**
Kierulff Electronics, 203-265-1115

**CT** **Wallingford**
Arrow Elctrns., 203-265-7741

**FL** **Deerfield Beach**
Arrow Electronics, 305-429-8200

**FL** **Ft. Lauderdale**
Kierulff Electronics, 305-486-4004

**FL** **Orlando**
Chip Supply, 305-275-3810

**FL** **Oviedo**
Zeus Components, 305-365-3000

**FL** **Palm Bay**
Arrow Elctrns., 305-725-1480

**FL** **St. Petersburg**
Kierulff Elctrns., 813-576-1966

**GA** **Norcross**
Kierulff Electronics, 404-447-5252

**GA** **Norcross**
Arrow Elctrns., 404-449-8252

**IL** **Itasca**
Kierulff Electronics, 312-250-0500

**IL** **Rosemont**
Advent Elctrns., 312-298-4210

**IL** **Schaumburg**
Arrow Electronics, 312-397-3440

**IN** **Indianapolis**
Arrow Elctrns., 317-243-9353

**IA** **Cedar Rapids**
Advent Elctrns., 319-363-0221

**IA** **Cedar Rapids**
IA, 319-395-7230

**KS** **Lenexa**
Arrow Electronics, 913-541-9542

**MD** **Columbia**
Zeus Components, 301-997-1118

**MD** **Columbia**
Arrow Elctrns., 301-995-0003

**MD** **Timonium**
Zebra Elctrns., 301-252-6576, 800-638-1103

**MA** **Billerica**
Kierulff Elctrns., 617-667-8331

**MA** **Lexington**
Zeus Components, 617-863-8800

**MA** **Newton**
The Greene-Shaw Co., Inc., 617-969-8900, 800-225-8804

**MA** **Peabody**
MCI, 617-535-7270

**MA** **Woburn**
Arrow Elctrns., 617-933-8130

**MI** **Ann Arbor**
Arrow Elctrns., 313-971-8220

**MI** **Grand Rapids**
Arrow Electronics, 616-243-0912

**MN** **Edina**
Arrow Elctrns., 612-830-1800

**MN** **Edina**
Kierulff Elctrns., 612-941-7500

**MO** **Maryland Heights**
Kierulff Electronics, 314-739-0855

**MO** **St. Louis**
Arrow Electronics, 314-567-6888

**NH** **Manchester**
Arrow Electronics, 602-668-6968

**NJ** **Clifton**
Vantage, 201-777-4100

**NJ** **Marlton**
Arrow Elctrns., 609-596-8000



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Kierulff Electronics, 609-235-1444

**NJ** **Parsippany**
Arrow Elctrns., 201-538-0900

**NM** **Albuquerque**
Alliance Electronics, 505-292-3360

**NM** **Albuquerque**
Arrow Elctrns., Inc./Elctrns. Distribution Div., 505-243-4566

**NY** **Hauppauge**
Arrow Electronics, 516-231-1000

**NY** **Liverpool**
Arrow Elctrns., 315-652-1000

**NY** **Melville**
SAI, 516-293-2710

**NY** **Melville**
Arrow Elctrns., 516-694-6800

**NY** **Patterson**
Intercept Electronics Corp., 914-878-3355

**NY** **Plainview**
ACI Elctrns. Corp., 516-293-6630

**NY** **Port Chester**
Zeus Comps., Inc., 914-937-7400

**NY** **Rochester**
Arrow Elctrns., 716-427-0300

**NY** **Woodbury**
Pioneer/Harvey, 516-921-8700

**NC** **Raleigh**
Arrow Electronics, 919-876-3132

**NC** **Winston-Salem**
Arrow Elctrns., 919-725-8711

**OH** **Beechwood**
Kierulff Electronics, 216-831-5222

**OH** **Centerville**
Kierulff Electronics, 513-439-0045

**OH** **Centerville**
Arrow Elctrns., 513-435-5563

**OH** **Solon**
Arrow Elctrns., 216-248-3990

**OK** **Tulsa**
Kierulff Electronics, 918-252-7537

**OR** **Tigard**
Arrow Electronics, 503-684-1690

**PA** **Monroeville**
Arrow Elctrns., 412-856-7000

**TX** **Austin**
MINCO Technology Labs, 512-834-2022

**TX** **Austin**
Arrow Electronics, 512-835-4180

**TX** **Austin**
Kierulff Electronics, 512-835-2090

**TX** **Carrollton**
Arrow Elctrns., 214-380-6464

**TX** **Garland**
Kierulff Electronics, 214-840-0110

**TX** **Houston**
Arrow Electronics, 713-530-4700

**TX** **Houston**
Kierulff Electronics, 713-530-7030

**TX** **Richardson**
Zeus Components, 214-783-7010

**UT** **Salt Lake City**
Arrow Electronics, 801-972-0404

**UT** **Salt Lake City**
Kierulff Electronics, 801-973-6913

**UT** **Salt Lake City**
Bell Inds., 801-972-6969

**WA** **Bellevue**
Arrow Elctrns., 206-643-4800

**WA** **Kent**
Kierulff Elctrns., 206-575-4420

**WI** **Brookfield**
Arrow Elctrns., 414-792-0150

**WI** **Waukesha**
Kierulff Electronics, 414-784-8160

**Can** **Downsview, Ontario**
Future Elctrns., 416-663-5563

**Can** **Ontario, Nepean**
Arrow, 613-226-6903

**Can** **Ontario, Toronto**
Arrow, 416-661-0220

**Can** **Pointe Claire, Quebec**
Future Elctrns., 514-694-7710

**Can** **Quebec**
Arrow, 418-687-4231

**Can** **Quebec, Montreal**
Arrow, 514-735-5511

## RCI/Data

RCI/Data
P.O. Box 4570
Toms River, New Jersey 08754-4570
201-341-5592

## Recognition Technology

Recognition Technology, Inc.
160 E. Main Street
Westborough, Massachusetts 01581
617-429-7804

## Relational Memory System

Relational Memory Systems (RELMS)
1650-B Berryessa Road
San Jose, California 95131
408-729-3011
TWX: 910-379-0014

## Renaissance GRX

Renaissance GRX, Inc.
2265 116th Avenue N.E.
Bellevue, Washington 98004
206-454-8086

## Ricoh

Ricoh Corp.
Electronic Devices
3001 Orchard Park Way
San Jose, California 95134
408-942-8100

## Riehl Time

Riehl Time Corporation
53 South Jefferson Road
Whippany, New Jersey 07981
201-887-4506

## RIFA

RIFA AB
Kista
Stockholm, Sweden S-16381
8-757-5000

## Robotrol

Robotrol Corporation
16100 Caputo Drive
Morgan Hill, California 95037
408-778-0400

## Rockwell International

**Rockwell International**
**Semiconductor Products Division**
**4311 Jamboree Rd., P.O. Box C**
**Newport Beach, California 92658-8902**
**714-833-4700**
**TWX: 910-591-1654**

## S-MOS Systems

**S-MOS Systems, Inc.**
**2460 N. 1st Street**
**San Jose, California 95131**
**408-992-0200**

### Sales Office & Representatives

**AL** **Huntsville**
Electronic Sales, Inc., 205-533-1735

**AZ** **Scottsdale**
AMI Inc., 602-948-2778

**CA** **Irvine**
Mission Ridge Marketing, 714-253-4626

**CA** **Manhattan Beach**
Mission Ridge Marketing, 213-545-3128

**CA** **Placerville**
Pro Associates, 916-621-1460

**CA** **San Diego**
Miner and Associates, 619-566-9891

**CA** **San Jose**
Pro Associates, 408-248-5300

**CO** **Wheatridge**
Wescom Marketing, 303-422-8957

**FL** **Casselberry**
Dyne-A-Mark, 305-831-2822

**FL** **Clearwater**
Dyne-A-Mark, 813-441-4702

**FL** **Ft. Lauderdale**
Dyne-A-Mark, 305-771-6501

**GA** **Norcross**
Electronic Sales, Inc., 404-448-6554

**IL** **Skokie**
Industrial Reps. Inc., 312-967-8430

**IN** **Indianapolis**
J and W Sales, 317-842-3740

**KS** **Olathe**
Crimson Technologies, 913-764-1079

**KY** **Louisville**
J and W Sales, 502-897-0989

**MD** **Pasadena**
Logical Technology, 301-437-7400

**MA** **Burlington**
Eastern Area Sales Office, 617-272-3174

**MA** **Wilmington**
Anacon Sales Associates, 617-270-3712

**MI** **Jenison**
R.C. Nordstrom, 616-457-5762

**MI** **Southfield**
R.C. Nordstrom & Co., 313-559-7373

**MN** **Hamel**
James R. Johnson & Assoc., 612-478-9442

**NY** **Bronx**
Pen/Man Technical Sales, 212-798-5456

**NY** **Rochester**
Bristol Associates, 716-442-8414

**NC** **Cary**
Electronic Sales, Inc., 919-467-8486

**NC** **Charlotte**
Electronic Sales, Inc., 704-522-8428

**OH** **Dayton**
Lyons Corp., 513-278-0714

**OH** **Richfield**
Lyons Corp., 216-659-9224

**OH** **Westerville**
Lyons Corp., 614-895-1447

## S-MOS Systems (Cont'd)

**OR** **Tigard**
Electronic Component Sales, 503-245-2342

**PA** **Huntingdon Valley**
Omega Electronics Sales, 215-947-4135

**UT** **Salt Lake City**
Wescom Marketing, 801-269-0419

**WA** **Mercer Island**
Electronic Component Sales, 206-232-9301

**WI** **Milwaukee**
Industrial Reps. Inc., 414-259-0966

**Can** **Etobicoke, Ontario**
Dynasty Components, Inc., 416-674-8060

**Can** **Ormeaux, Quebec**
Dynasty Components, Inc., 514-620-7734

**Can** **Ottawa, Ontario**
Dynasty Components, Inc., 613-738-1200

**Can** **Vancouver, B.C.**
Dynasty Components, Inc., 604-688-2010

### Distributors

**AL** **Huntsville**
Hammond Electronics, 205-830-4764

**AZ** **Phoenix**
Cetec-Future, 602-968-7140

**AZ** **Tempe**
Time Electronics, 602-946-9977

**CA** **Agoura**
Image, 818-707-0911

**CA** **Agoura Hills**
Time Electronics, 818-707-2890

**CA** **Anaheim**
Time Electronics, 714-937-0911

**CA** **Chatsworth**
Time Electronics, 818-998-7200

**CA** **Glendale**
Diplomat Electronics, 818-841-4573

**CA** **Irvine**
Cetec-Future, 714-250-4141

**CA** **Orange**
Ryno Electronics, 714-637-0200

**CA** **San Diego**
Time Electronics, 619-586-1331

**CA** **San Diego**
AVED, Inc., 619-278-1990

**CA** **San Diego**
Ryno Electronics, 619-453-8430

**CA** **San Jose**
Diplomat Electronics, 408-434-6475

**CA** **San Jose**
Cetec-Future, 408-434-1114

**CA** **Santa Clara**
Cypress Electronics, 408-980-2500

**CA** **Saratoga**
Western Microtechnology

**CA** **Sunnyvale**
Time Electronics, 408-734-9888

**CA** **Torrance**
Time Electronics, 213-320-0880

**CA** **Tustin**
AVED, Inc., 714-259-8258

**CA** **Tustin**
Image, 714-259-0900

**CO** **Engelwood**
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312-634-9313

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Hallmark Elctrns., 201-575-4415

**NJ** **Mount Laurel**
Hallmark Elctrns., 609-235-1900

**NY** **Ronkonkoma**
Hallmark Elctrns., 516-737-0600

**NC** **Raleigh**
Hallmark Elctrns., 919-872-0712

**OH** **Solon**
Hallmark Elctrns., 216-349-4632



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**TX** **Austin**
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Hallmark Elctrns., 214-553-4300
**TX** **Houston**
Hallmark Elctrns., 713-781-6100
**UT** **West Valley City**
Hallmark Elctrns., 801-972-1008
**WI** **New Berlin**
Hallmark Elctrns., 414-797-7844
**Intl** **Argentina, Buenos Aires**
YEL S.R.L., TEL: 46-2211
**Intl** **Australia, Victoria**
R&D Electronics, TEL: 3-288-8911
**Intl** **Brazil**
Hitech, TEL: 11-533-9566
**Intl** **Denmark**
C-88, TEL: 02 24 48 88
**Intl** **England, Essex**
Pronto Electronic Systems Ltd., TEL: 01 554 6222
**Intl** **Finland, ESP0021**
Komdel Oy, TEL: 0-885011
**Intl** **France**
Datadis, TEL: 1-605-6000
**Intl** **Germany, Munich**
Atlantik Elektronik GmbH, TEL: (0 89) 8 57 20 86-89
**Intl** **Greece, Athens**
Peter Caritato & Assoc. Ltd., TEL: 01/3619379, 01/3623614
**Intl** **Hong Kong, Hong Kong**
CET LTD, TEL: 5-200922
**Intl** **India**
Gaekwar Enterprise, TEL: 011-91-22-494-2583
**Intl** **Israel, Tel Aviv**
RAPAC, TEL: 03 47 71 15
**Intl** **Italy**
Cefra S.R.L., TEL: (02) 23.52.64, (02) 23.60.154
**Intl** **Japan, Tokyo**
Internix, TEL: 03 (369) 1101
**Intl** **Mexico**
Panamtek, TEL: 91 36 303029
**Intl** **Mexico**
Panamtek, TEL: 905-754-0426
**Intl** **Norway, Nesbru**
Hans Schive, TEL: 2-845160
**Intl** **Seoul, Korea**
Hanaro Corporation, TEL: (02) 784-1144
**Intl** **Singapore**
Dynamar International, TEL: 7476188
**Intl** **South Africa, Randburg**
South Continental Devices, TEL: (011) 789-2400
**Intl** **Sweden, Taby**
Bexab Ele., TEL: 08-7680560
**Intl** **Taiwan, Taipei**
Dynamar International, TEL: 5418251
**Intl** **Zurich**
Eleyptic, TEL: 1-493-1000

## Siliconix

Siliconix Inc.
2201 Laurelwood Road
Santa Clara, California 95054
800-554-5565
TWX: 910-338-0227

## Siltronics

Siltronics Ltd.
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Kanata, Ontario K2L 1T9
613-836-5003

## Silvaco Data Systems

Silvaco Data Systems
2328 Walsh Avenue
Santa Clara, California 95051
408-988-2862

## Silvar-Lisco

Silvar-Lisco
1080 Marsh Rd.
Menlo Park, California 94025
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TWX: 910-373-2056

## SimuCad

SimuCad
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## Simulog

Simulog
3211 Scott Blvd., Suite 104
Santa Clara, California 95051
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FAX: 408-727-8534

## Single Board Solutions

Single Board Solutions, Inc.
20045 Stevens Creek Blvd.
Cupertino, California 95014
408-253-0250

## Slicer Computers

Slicer Computers Inc.
3450 Snelling Ave. So.
Minneapolis, Minnesota 55406
612-724-2710

## Great Softwestern

The Great SoftWestern Company
207 W. Hickory St., Suite 309
Denton, Texas 76201
817-383-4434, 800-231-6880

## Solarcom Technology

Solarcom Technology, Inc.
P. O. Box 4715
Hayward, California 94544
415-489-3141

## Solarise Enterprises

Solarise Enterprises Inc.
19220 Stevens Creek Blvd.
Cupertino, California 95014
408-446-9343

## Solid State Micro Technology

Solid State Micro Technology for Music, Inc.
2076B Walsh Avenue
Santa Clara, California 95050
408-727-0917
TELEX: 171189
FAX: 408-727-5418

## Solitron Devices

Solitron Devices, Inc.
Semiconductor Division
8808 Balboa Avenue
San Diego, California 92123
619-278-8780

## Sony

Sony Corporation of America
10833 Valley View Street
Cypress, California 90630
714-220-9100

## Sophia Computer Systems, Inc.

**Sophia Computer Systems, Inc.**
**3337 Kifer Road**
**Santa Clara, California 95051**
**408-733-1571, 800-824-9294, 800-824-6706(in CA)**
**TELEX: 853394**
**FAX: 408-749-8172**

### Sales Office & Representatives

**AL** **Huntsville**
Advanced Components Marketing, 205-881-5493
**AZ** **Phoenix**
Zeus Electronics Inc., 602-263-6022
**CA** **Burlingame**
CMS, 415-347-0614
**CA** **Santa Clara**
Sophia Computer Systems, Inc., 408-733-1571
**CA** **West Lake Village**
Advanced Products Sales, 818-706-8351
**CO** **Denver**
Zeus Electronics, Inc., 303-321-4246
**FL** **Plantation**
EMS, Inc., 305-587-7146
**GA**
H & A Technical Sales, 919-846-0082
**IL** **Arlington Heights**
Phoenix Electronic Sales, Inc., 312-394-4422
**MA** **Chelmsford**
ICS Associates, Inc., 617-256-3350
**MI** **Pontiac**
EQS, 313-338-2280
**MN** **Golden Valley**
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Scientific Associates, Inc., 609-662-5222
**NM** **Albuquerque**
Zeus Electronics, Sales, 505-842-6633
**NY** **Ronkonkoma**
Electronic Research Group, 516-585-2344
**NC** **Raleigh**
H & A Technical Sales, 919-846-0082
**OH** **Chesterland**
EQS, 216-729-2222
**OH** **Huber Heights**
EQS, 513-236-7676
**PA** **Bethel Park**
EQS, 412-833-8083
**UT** **Salt Lake City**
Zeus Electronic, Inc., 801-534-0500
**WA** **Bellevue**
Systems Technical Sales, 206-462-8088
**Intl** **Boksburg**
Altech Electronic Systems, TEL: 011-788-1700
**Intl** **Fern Tree Gully, Victoria**
Alfatron, TEL: 03-758-9000

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Ellettronucleonica, TEL: 024982451

**Intl** **Telaviv**
Madel Tech., TEL: 03-494179

## Space Research

Space Research Technology, Inc.
1120 Capital of Texas Hwy. S.
Austin, Texas 78746
512-329-1055

## Spectrum Software

Spectrum Software
1021 S. Wolfe Rd.
Sunnyvale, California 94086
408-738-4387

## Sprague Electric

**Sprague Electric Company**
**Semiconductor Group**
**115 Northeast Cutoff**
**Worcester, Massachusetts 01606**
**617-853-5000**
**TWX: 710-340-6304**

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Linear-Radio, Audio ..... H. LeDuc, Jr.
Telecommunications ..... S. Dumery
Military CMOS ..... L. Delony

**Applications Engineering:**
T. Wood

**Literature:**
Literature:
41 Hampden Rd., Mansfield, MA 02048
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**Place an Order:**
J Genest

**Follow up on Order:**
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**AL** **Huntsville**
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**AZ** **Tempe**
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William J. Purdy Co., 415-347-7701

**CA** **Campbell**
Sprague Electric Company, 408-374-1017

**CA** **Costa Mesa**
Sprague Elec. Co., 714-549-9913

**CA** **Inglewood**
Sprague Elec. Co., 213-649-2600

**CA** **San Diego**
R. David Miner Inc., 619-566-9891

**CA** **San Diego**
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**CA** **Santa Clara**
Criterion Sales, 408-988-6300

**CA** **Van Nuys**
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William J. Purdy Co., 303-777-1411

**CO** **Denver**
Wm. J. Purdy Company, 303-753-6800

**CO** **Longmont**
Todd & Fry Associates, 303-776-7331

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Ray Perron & Co., 203-354-2569

**CT** **Southbury**
Sprague Electric Company, 203-264-9595

**CT** **Trumbull**
Sprague Elec. Co., 203-261-2551

**CT** **Wallingford**
New England Technical Sales, 203-284-8300

**DC** **Washington**
Sprague Elec. Co. (Gov't sales only), 202-337-7820

**FL** **Altamonte Springs**
Sprague Elec. Co., 305-831-3636

**FL** **Altamonte Springs**
Sprague Electric Company, 305-831-3636

**FL** **Ft. Lauderdale**
Sprague Elec. Co., 305-491-7411

**FL** **Ft. Lauderdale**
Sprague Electric Company, 305-491-7411

**FL** **St. Petersburg**
Electramark Florida, Inc., 813-894-2299

**FL** **Tampa**
Sprague Electric Company, 813-962-1882

**GA** **Atlanta**
Elctrn. Mktg. Assocs., 404-448-1215

**GA** **Norcross**
Sprague Electric Company, 404-263-3715

**GA** **Norcross**
Montgomery Marketing, Inc., 404-447-6124

**IL** **Park Ridge**
Sprague Elec. Co., 312-296-6620

**IL** **Rolling Meadows**
Sumer, Inc., 312-991-8500

**IN** **Indianapolis**
Sprague Elec. Co., 317-253-4247

**IN** **Indianapolis**
SAI Marketing Corporation, 317-545-1010

**IN** **Indianapolis**
Sprague Electric Company, 317-253-4247

**IA** **Cedar Rapids**
J.R. Sales Engineering, 319-393-2232

**KS** **Overland Park**
EPI Inc., 913-648-4154

**KS** **Overland Park**
EPI Inc., 913-641-9118

**KY** **Lexington**
Sprague Electric Company, 606-224-4230

**MD** **Laurel**
Sprague Electric Company, 301-792-4890

**MA** **Burlington**
New England Technical Sales, 617-272-0434

**MA** **Framingham**
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**MA** **Needham**
Ray Perron & Co., 617-449-6162

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**MI** **Fenton**
SAI Marketing Corporation, 313-750-1922

**MI** **Jackson**
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HMR, Inc., 612-888-2122

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HMR Inc., 612-888-2122

**MS** **Jackson**
EPI Southwest, 601-856-6251

**MO** **St. Louis**
EPI Inc., 314-962-1411

**MO** **St. Louis**
EPI Inc., 314-962-1411

**NH** **Dover**
Ray Perron & Co., 603-742-2321

**NJ** **Cherry Hill**
Trinkle Sales Inc., 609-795-4200

**NJ** **Cherry Hill**
Trinkle Sales Inc., 609-795-4200

**NJ** **Wayne**
Sprague Elec. Co., 201-696-8200

**NJ** **Wayne**
Astrorep, Inc., 201-696-8200

**NM** **Albuquerque**
William J. Purdy Co., 505-266-7959

**NY** **Babylon**
Astrorep, Inc., 516-422-2500

**NY** **Central Islip**
Sprague Elec. Co., 516-234-8700

**NY** **Central Islip**
Sprague Electric Company, 516-234-8700

**NY** **E. Syracuse**
Ossmann Associates, Inc., 315-437-7052

**NY** **Henrietta**
Ossmann Associates, Inc., 716-359-1200

**NY** **Larchmont**
Sprague Elec. Co., 914-834-4439

**NY** **Larchmont**
William Rutt, Inc., 914-834-8555

**NY** **Syracuse**
Paston-Hunter Co., 315-437-2843

**NY** **Syracuse**
Sprague Elec. Co., 315-437-7311

**NC** **Charlotte**
Sprague Elec. Co., 704-527-1306

**NC** **Charlotte**
Sprague Electric Company, 704-527-1306

**NC** **Raleigh**
Elctrn. Mktg. Assoc., 919-847-8800

**NC** **Raleigh**
Montgomery Marketing, Inc., 919-851-0010

**OH** **Beachwood**
Elctrn. Salesmasters, Inc., 800-362-2616

**OH** **Columbus**
SAI Marketing Corporation, 614-451-0778

**OH** **Dayton**
SAI Marketing Corporation, 513-435-3181

**OH** **Shaker Heights**
SAI Marketing Corporation, 216-751-3633

**OH** **Springfield**
Sprague Elec. Co., 513-322-3881

**OR** **Beaverton**
William J. Purdy Co., 503-641-9373

**OR** **Portland**
Sprague Electric Company, 503-225-0493

**PA** **Philadelphia**
Trinkle Sales Inc., 215-922-2080

**SC** **Greenville**
Elctrn. Mktg. Assocs., 803-233-4637

**TX** **Austin**
Sprague Elec. Co., 512-458-2514

**TX** **Austin**
Sprague Electric Company, 512-458-2514

**TX** **Dallas**
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**VA** **Lexington**
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**WA** **Redmond**
William J. Purdy Co., 206-882-3144

**WA** **Seattle**
Sprague Elec. Co., 206-632-7761

**WA** **Vancouver**
Sprague Elec. Co., 206-892-0361

**WA** **Vancouver**
Sprague Electric Company, 206-892-0361

**WI** **Brookfield**
Sumer, Inc., 414-784-6641

**WI** **Milwaukee**
D. Dolin Sales, 414-482-1111

**Can** **Ottawa, Ontario**
Sprague Elec. of Can., 613-238-2542

**Can** **Surrey, BC**
Lenbrook Elec., 604-585-9599

**Can** **Toronto, Ontario**
Sprague Elec. of Can., 416-766-6123

**Intl** **Belgium, Ronse**
Sprague-Benelux, TEL: 055-21-53-22

**Intl** **England, Salfords, Surrey**
Sprague Elec. (U.K.) Ltd., TEL: 02934-5666

**Intl** **France, Cachan**
Sprague France S.A.R.L., TEL: (1) 547-6600

**Intl** **Germany, Frankfurt**
Sprague Elek. GmbH, TEL: 0611-60551

**Intl** **Germany, Munchen**
Sprague Elek. GmbH, TEL: 089-430-1077

**Intl** **Hong Kong, Hong Kong**
Sprague World Trade Corp., TEL: 3-7440010

**Intl** **Italy, Milano**
Sprague Elec. Co., TEL: 02-498-7891

**Intl** **Japan, Tokyo**
Sprague Japan K.K., TEL: (03) 348-5221

**Intl** **Korea, Seoul**
Tecnomil Ltd., TEL: (2) 783-9784

**Intl** **Singapore, Singapore**
Sprague World Trade Corp., TEL: 475-1826

**Intl** **Sweden, Stocksund**
Sprague Scandinavia A.B., TEL: (04) 08 8502 20

**Intl** **Switzerland, Geneva**
Sprague World Trade Corp., TEL: 98 4021

**Intl** **Taiwan, Taipei**
Sprague Taiwan/Tecnomil, TEL: (2) 771-9582

## Sprague Electric

**Sprague Electric Company**
**Sensor Division**
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**Concord, New Hampshire 03301**
**603-224-1961**
**TWX: 710-361-1495**

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NJ)201) 882-8300
MA(617) 777-8800

STANDARD MICROSYSTEMS CORPORATION

## Standard Microsystems

**Standard Microsystems Corporation**
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**Hauppauge, New York 11787**
**516-273-3100, 275808 SMC UR**
**TELEX: 510-227-8898**

**Specific Product Information:**
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**Applications Engineering:**
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.. Paul Michaelson at Turk Enterprises 714-955-1575
South
..... Mike O'Connell at Standard Microsystems Corp. Lewisville, TX 214-436-4008
Europe
..... William Stypa at European Sales Office 49-89-919594 West Germany, Munich
Far East
... Larry Chen at SMC International Taipei, Taiwan 02 700-5457

**Literature:**
Debra Randall

**Price and Delivery:**
Lynn Thurber

**Follow up on Order:**
Lynn Thurber

**All Other Information:**
Lynn Thurber
International Sales Information ..... Cathy Peragine (Buoniello)
Board Level Products ..... Jay Marcacci

## Stanford Telecommunications

**Stanford Telecommunications Inc.**
**2421 Mission College Blvd.**
**Santa Clara, California 95054**
**408-748-1010**

### Sales Office & Representatives

**CA** **Santa Clara**
Stanford Telecommunications, Inc., 408-980-5684

**Intl** **England**
Chiptech, Ltd., TEL: 0727 40476

**Intl** **Neve-Monosan, Israel**
Regev Aviation, TEL: 03-352359

**Intl** **Suresnes, France**
Rep' France, TEL: (1) 42.04.29.25

**Intl** **Taipei, Taiwan**
Industrial Electronics, TEL: (02) 713-4257

**Intl** **Tokyo, Japan**
Rikei Corporation, TEL: 03 345-1411

## Stantel-STC

Stantel Components Inc.
636 Remington Road
Schaumburg, Illinois 60195
312-490-7150
TWX: 910-291-2180

## STD Microsystems

STD Microsystems
399 Sherman Avenue
Palo Alto, California 94306
415-327-6800

## Stynetic Systems

Stynetic Systems Incorporated
Flowerfield—Building 1
Saint James, New York 11780
516-862-7670

## Sunshine Semiconductor

Sunshine Semiconductor Inc.
2727 Newport Boulevard West, Suite 209
Newport Beach, California 92663
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TWX: 910-595-2809

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NU HORIZONS ELECTRONICS CORP.
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Supertex inc.

## Supertex

Supertex, Inc.
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Sunnyvale, California 94086
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TWX: 910-339-9388

## Synergy Microsystems

Synergy Microsystems Inc.
1820 Cambridge Ave.
Cardiff, California 92007
619-753-2191

## Syscon Corp.

Syscon Corporation
3990 Sherman Street
San Diego, California 92110
619-296-0085

## Systech

Systech Corporation
6465 Nancy Ridge Drive
San Diego, California 92121
619-453-8970

## Systek

Systek
1027 North Kellog Street
Kennewick, Washington 99336
509-735-1200

## SYStems CALCulations

SYStems CALCulations, Inc.
2309 Calle Luminoso
Santa Fe, New Mexico 87505
505-983-3573

## Systems Datar

Systems Datar
2512 Billingsley Road
Columbus, Ohio 43085-1922
614-761-0333

## Tangent Systems

Tangent Systems Corporation
2840 San Tomas Expwy., 101
Santa Clara, California 95051
408-980-0600

## Tatum Labs

Tatum Labs, Inc.
1478 Mark Twain Court
Ann Arbor, Michigan 48103
313-663-8810

## Technitrol

Technitrol, Inc.
1952 East Allegheny Avenue
Philadelphia, Pennsylvania 19134
215-426-9105
TELEX: 83-4245

## Techno Inc.

Techno Inc.
14 Crandall Avenue
Pompton Lakes, New Jersey 07442
201-839-0740

## Technology Modeling

Technology Modeling Associates
300 Hamilton Ave., 3rd Fl.
Palo Alto, California 94301
415-327-6300
FAX: 415-325-2970

## Technology 80

Technology 80 Inc.
658 Mendelssohn Avenue North
Minneapolis, Minnesota 55427
612-542-9545, 800-328-4827

## Tektronix

Tektronix, Inc.
Computer - Aided Software Engineering Division
P.O. Box 14752
Portland, Oregon 97214
800-TEK-WIDE (EXT 861)
TELEX: 910-467-8708
TWX: Telex: 151754

## Tektronix

Tektronix
Tektronix-Microcomputer Development Products Division
P.O. Box 14752
Portland, Oregon 97214
800-342-5548
TELEX: 910-467-8708
TWX: Telex: 151754

## Tektronix-CAE Systems

**Tektronix-CAE Systems**
**P.O. Box 4600**
**Beaverton, Oregon 97076-4600**
**503-645-6464**
**TELEX: 4742 021 TEK WKRD**
**FAX: 503-645-8986**

### Sales Office & Representatives

**Can** **Barrie, Ontario**
Tektronix Canada, 705-737-2700
**Intl** **Netherlands, Amstelveen**
Tektronix Europe B.V., TEL: (20) 471146
Tektronics-Integrated Circuits Operation
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Beaverton, Oregon 97077
503-627-2515
TWX: 910-467-8708

## Tektronix

Tektronix-Software Development Products Div.
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Portland, Oregon 97214
800-342-5548
TELEX: 151754
TWX: 910-467-8700

## Teledyne Crystalonics

Teledyne Crystalonics
147 Sherman Street
Cambridge, Massachusetts 02140
617-491-1670

## Teledyne Philbrick

Teledyne Philbrick
40 Allied Drive
Dedham, Massachusetts 02026-9103
617-329-1600, 326-6313
TELEX: 212-711
TWX: 710-348-6726

## Teledyne Semiconductor

Teledyne Semiconductor
1300 Terra Bella Avenue, P.O. Box 7267
Mountain View, California 94039-7267
415-968-9241
TWX: 910-379-6494

## Telefunken

AEG-Telefunken Corporation
P.O. Box 3800, Route 22 at Orr Drive
Somerville, New Jersey 08876
201-722-9800
TELEX: 833409

## Teletek Enterprises

Teletek Enterprises, Inc.
4600 Pell Drive
Sacramento, California 95838
916-920-4600

## Teltone

Teltone Corporation
10801-120th Avenue NE
Kirkland, Washington 98033
206-827-9626
TWX: 910-449-2862

## Teradyne, Inc.

Teradyne, Inc.
321 Harrison Ave.
Boston, Massachusetts 02118
617-482-2700

## Texas Instruments

**Texas Instruments, Inc.**
**Semiconductor Group**
**P.O. Box 401560**
**Dallas, Texas 75240**
**214-995-2011**
**TWX: 910-867-4702**

### Sales Office & Representatives

**AL** **Huntsville**
Sales Office, 205-837-7530
**AZ** **Phoenix**
Sales Office, 602-995-1007
**AZ** **Tucson**
Sales Office, 602-624-3276
**CA** **Irvine**
TI Technology Centers, 714-660-8140
**CA** **Irvine**
Sales Office, 714-660-8187
**CA** **Sacramento**
Sales Office, 916-929-1521
**CA** **San Diego**
Sales Office, 619-278-9601
**CA** **Santa Clara**
TI Technology Centers, 408-748-8220
**CA** **Santa Clara**
Sales Office, 408-980-9000
**CA** **Torrence**
Sales Office, 213-217-7010
**CA** **Woodland Hills**
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Sales Office, 305-973-8502
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Sales Office, 305-660-4600
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Sales Office, 813-870-6420
**GA** **Norcross**
Sales Office, 404-662-7900
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TI Technology Centers, 404-662-7945
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TI Technology Centers, 312-640-2909
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**714-832-6300**
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**OH** **Chagrin Falls**
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**OH** **Dayton**
Midwest Mkt. Assoc., 513-433-2511
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West Assoc., 918-665-3465
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Northwest Mkt., 503-620-0441
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REP, Inc., 615-475-9012
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Northwest Marketing, 206-455-5846
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**Can** **Ottawa, Ontario**
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W.D.C., TEL: 011-813-791-2001
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W.D.C., TEL: 011-822-554-0508
**Intl** **Taiwan, Taipei**
W.D.C., TEL: 011-8886-2717-4775
**Intl** **United Kingdom, Surrey**
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**AZ** **Phoenix**
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Bell Industries, 602-966-7800
**AZ** **Tempe**
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**CA** **Irvine**
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**CA** **Los Angeles**
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**CA** **Rancho Cordova**
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Wyle EMG, 619-565-9171
**CA** **San Diego**
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**CA** **San Diego**
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Anthem Electronics, 408-946-8000
**CA** **San Jose**
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Kierulff Electronics, 303-790-4444
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Anthem Electronics, 303-790-4500
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**CO** **Wheatridge**
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**FL** **Clearwater**
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**FL** **Ft. Lauderdale**
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**FL** **Ft. Lauderdale**
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**GA** **Norcross**
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Time Electronics, 301-995-1668

MD **Columbia**
Lionex Corporation, 301-964-0040

MD **Gaithersburg**
Pioneer Electronics, 301-921-0660

MD **Linthicum**
Kierulff Electronics, 301-636-5800

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MA **Lexington**
Pioneer Electronics, 617-861-9200

MA **Peabody**
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MA **Wilmington**
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MA **Wilmington**
RC Components, 617-657-4310

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Diplomat Electronics, 617-935-6611

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Pioneer Electronics, 313-525-1800

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MN **Minnotonka**
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MO **St. Louis**
Time Electronics, 314-391-6444

NJ **Fairfield**
Lionex Corporation, 201-277-7960

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Kierulff Electronics, 201-575-6750

NJ **Mt. Laurel**
Kierulff Electronics, 609-235-1444

NJ **Pine Brook**
Pioneer Electronics, 201-227-1262

NJ **Totowa**
Diplomat Electronics, 201-785-1830

NM **Albuquerque**
Alliance Electronics, 505-292-3360

NY **East Syracuse**
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Pioneer Electronics, 716-381-7070

NY **Farmingdale**
S.A.I., 816-293-2710

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Time Electronics, 516-273-0100

NY **Hauppauge**
Lionex Corporation, 516-273-1660

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Diplomat Electronics, 315-652-5000

NY **Melville**
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Pioneer Electronics, 607-748-8211

NY **Woodbury**
Pioneer Electronics, 516-921-8700

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Kierulff Electronics, 216-587-6558

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Pioneer Electronics, 216-587-3600

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Kierulff Electronics, 918-252-7537

OK **Tulsa**
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OR **Lake Oswego**
Anthem Electronics, 503-684-2661

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PA **Horsham**
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PA **King of Prussia**
Time Electronics, 215-337-0900

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Quality Components, 214-733-4300

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Pioneer Electronics, 512-835-4000

TX **Austin**
Diplomat Electronics, 512-452-5254

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UT **Salt Lake City**
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UT **West Valley City**
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Semad Electronics, 514-636-4614

Can **Quebec, St. Laurent**
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Daneva Australia Pty., TEL: 61/03-598-5622

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Indutronic, TEL: 0043-4222-43693

Intl **Austria, Wien**
Hitronik, TEL: 0043-222-824199

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Intl **Denmark, Kokkedal**
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Pronto Elect., Sys., Ltd., TEL: 44/1-5546222

Intl **Finland, Espoo**
Dy Microlog Ltd., TEL: 35/8-08031144

Intl **France, Boulogne**
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Intl **France, Paris**
Edisoft, TEL: 33-01-46-22-71-71

Intl **France, Paris**
Meil, TEL: 33-01-43-42-92-07

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Comprel S.P.A., TEL: 39-02-612-0641

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Sejin Industries, TEL: 82/2-782-8768-9

Intl **Korea, South Korea**
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Sydec Computer Components, TEL: 0031-3463-2344

Intl **Netherlands, Utrecht**
Diode B.V., TEL: 31/030 88 42 14

Intl **Norway, Nesbru**
Hans H. Schive A/S, TEL: 47/2-845160

Intl **Portugal, Queluz**
Topis International, TEL: 351-1-955-452

Intl **Singapore**
Dynamic Systems, TEL: 65/287-6133

Intl **Singapore**
Printed Circuits, TEL: 65/265-8181

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So. Continental Devices, TEL: 27/11-7892400

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Teleimport AB, TEL: 46/8-761-7220

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**Intl** **Switzerland, Echallens/VD**
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**Intl** **Taiwan, Taipei**
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**Intl** **Turkey, Istanbul**
Teleteknik, TEL: 00301-131-1550

**Intl** **West Germany, Hamburg**
ABC Trading, TEL: 040/2277021

**Intl** **West Germany, Muenchen**
Electronic 2000, TEL: 089/42001-0

**Intl** **West Germany, Niedernberg**
M & S Elktronik, TEL: 06028/4040

**Intl** **West Germany, Ratingen**
Raffel Electronics, TEL: 02102/41033-38

**Intl** **West Germany, Stuttgart**
Leoffelhardt, TEL: 0711/5207-0

## WinSystems

WinSystems Inc.
Box 121361
Arlington, Texas 76012
817-274-7553

## Wintek

**Wintek Corporation**
**1801 South Street**
**Lafayette, Indiana 47904-2993**
**317-742-8428, 800-742-6809**
**TELEX: 70-9079**

## XCAT

XCAT, Inc.
1275 Grey Fox Road, Bldg. 700
St. Paul, Minnesota 55112
612-633-8700

## Xerox

Xerox
Engineering Intosuation Systems
2945 Oatemead Village Court
Santa Clara, California 95051
408-982-8187

## Xicor

**Xicor, Inc.**
**851 Buckeye Court**
**Milpitas, California 95035**
**408-432-8888**
**TWX: 910-379-0033**
**FAX: 408-432-0640**

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**CA** **Irvine**
Centaur Corporation, 714-261-2123

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Xicor Southwestern Sales Office, 714-752-8700

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**CT** **Danbury**
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Delmac Sales Inc., 813-447-5192

**FL** **Deerfield**
Delmac Sales Inc., 305-427-7788

**FL** **Longwood**
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**IL** **Schaumburg**
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**IN** **Greenwood**
Arete Sales, Inc., 317-882-4407

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Midwest Tech Sales, 319-365-4011

**IA** **Cedar Rapids**
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Midwest Tech Sales, 316-794-8565

**KS** **Lenexa**
Midwest Tech Sales, 913-888-5100

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**MA** **Westwood**
Comp Rep Associates, 617-329-3454

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The Twist Co., 612-941-2040

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Midwest Tech Sales, 314-441-1012

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**NY** **Syracuse**
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CSR Electronics Inc., 919-878-9200

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**OH** **Dayton**
Omega Sales Corp., 513-274-5035

**OH** **University Hts.**
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**OR** **Tigard**
Vantage Corp., 503-620-3280

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**TX** **Houston**
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**WA** **Spokane**
Vantage Corp., 509-924-4410

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**Can** **Surrey, B.C.**
Kaytronics, 604-581-5005

**Can** **Ville St. Pierre, Quebec**
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R & D Electronics, TEL: 61.3.288.8232

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Othmar Lackner Elektronische, TEL: 222.752618

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C.88 A/S, TEL: 452.244888

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Micro Call Ltd., TEL: 44.84.421.5405

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Power Factor, TEL: 64.9.872.095

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Eltron A/S, TEL: 50.472.0650

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Dynamer International Ltd., TEL: 7476188

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Naxab, TEL: 46.8.98.51.40

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W. Stolz AG, TEL: 411.056.84.01.51

**Intl** **Switzerland, Geneva**
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**Intl** **Taiwan, Taipei**
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**Intl** **Wanchai, Hong Kong**
CET Ltd., TEL: 5.200922

**Intl** **West Germany, Haar Bei Muenchen**
Xicor GmbH, TEL: 011.49.89.463089

**Intl** **West Germany, Korntal**
Memcomp, TEL: 49.711.83.76.36

**Intl** **West Germany, Muenchen**
E2000, TEL: 49.89.42.00.10

**PR** **Caguas**
Delmac Sales Inc., 809-746-1091

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**AL** **Huntsville**
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**AZ** **Phoenix**
Marshall, 602-968-6181

**AZ** **Phoenix**
Wyle Labs, 602-866-2888

**AZ** **Phoenix**
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**CA** **Irvine**
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**CA** **Rancho Cordova**
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**CT** **Wallingford**
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**GA** **Norcross**
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ANALOG DEVICES

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Analog Devices

ANALOG DEVICES

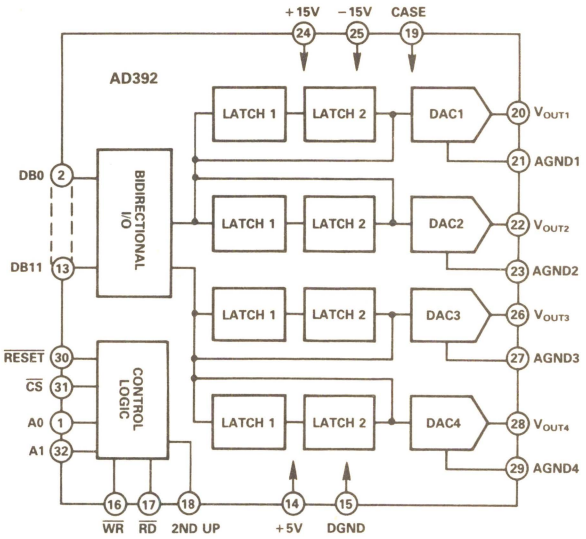
# Complete Quad 12-Bit D/A Converter with Readback

## AD392

**FEATURES**

- **Data Readback Capability**
- **Four Complete, Voltage Output, 12-Bit DACs in One 32-Pin Hermetic Package**
- **Fast Bus Access: 40ns max, $T_{min}$-$T_{max}$**
- **Asynchronous Reset to Zero Volts**
- **Minimum of Two TTL Load Drive (Readback Mode)**
- **Double-Buffered Data Latches**
- **Monotonicity Guaranteed $T_{min}$-$T_{max}$**
- **Linearity Error ±1/2LSB**
- **Low Digital-to-Analog Feedthrough, 2nV sec typ**
- **Factory Trimmed Gain and Offset**
- **Low Cost**

**AD392 FUNCTIONAL BLOCK DIAGRAM**




**PRODUCT DESCRIPTION**

The AD392 is a quad 12-bit, high-speed, voltage output digital-to-analog converter with readback in a 32-pin hermetically sealed package. The design is based on a custom IC interface to complete 12-bit DAC chips which reduces chip count and provides high reliability. The AD392 is ideal for systems requiring digital control of many analog voltages and for the monitoring of these analog voltages especially where board space is a premium. Such applications include ATE, robotics, process controllers and precision filters.

Featuring maximum access time of 40ns, the AD392 is capable of interfacing to the fastest of microprocessors. The readback capability provides a diagnostic check between the data sent from the microprocessor and the actual data received and transferred to the DAC. When $\overline{\text{RESET}}$ is low, all four DACs are simultaneously set to (bipolar) zero providing a known starting point.

The AD392 is laser-trimmed to ±1/2LSB integral linearity and ±1LSB max differential linearity at +25°C. Monotonicity is guaranteed over the full operating temperature range. The high initial accuracy and stability over temperature are made possible by the use of precision thin-film resistors.

The individual DAC registers are accessed by the address lines A0 and A1 and control lines $\overline{\text{CS}}$ and 2ND UP. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be simultaneously updated.

The AD392 outputs are calibrated for a ±10V output range with positive true offset binary input coding.

The AD392 is packaged in a 32-lead ceramic package and is hermetically sealed. The AD392 is specified for operation over the 0 to +70°C temperature range.

**PRODUCT HIGHLIGHTS**

1. The AD392 is packaged in a 32-pin DIP and is a complete solution to space constraint multiple DAC applications.
2. Readback capability provides system monitor of DAC output useful in ATE, robotics or any closed-loop system.
3. Fast bus access time of 40ns maximum allows for fast system updating compatible with high-speed microprocessing.
4. Simultaneous reset to zero volts output is extremely useful for system calibration or simply when all DAC outputs must initially start at zero volts.
5. Readback drive capability of two TTL loads virtually eliminates the need to buffer.
6. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors.
7. Monolithic DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
8. Low digital-to-analog feedthrough (2nV sec typ) is maintained to assure DAC accuracy.
9. New pin stake package provides a low-cost solution to cost constraint applications.

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Analog Devices

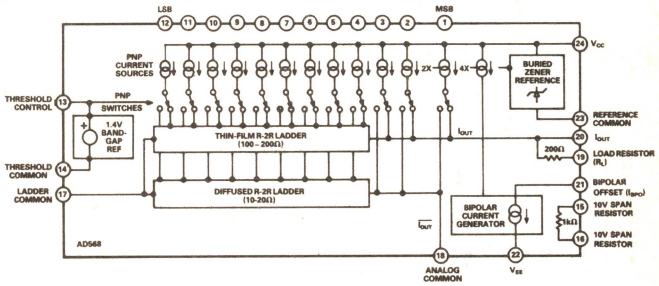
# 12-Bit Ultrahigh-Speed Monolithic D/A Converter

# AD568

## FEATURES

- Ultrahigh Speed: Current Settling to 1LSB in 35ns
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed over Temperature
- 10.24mA Full-Scale Output Suitable for Video Applications
- Integral and Differential Linearity Guaranteed Over Temperature
- 0.3" "Skinny DIP" Packaging
- Variable Threshold Allows TTL and CMOS Interface

## AD568 FUNCTIONAL BLOCK DIAGRAM




## PRODUCT DESCRIPTION

The AD568 is an ultrahigh-speed, 12-bit digital-to-analog converter (DAC) settling to 0.025% in 35ns. The monolithic device is fabricated using Analog Devices' Complementary Bipolar (CB) Process. This is a proprietary process featuring high-speed NPN and PNP devices on the same chip without the use of dielectric isolation or multichip hybrid techniques. The high speed of the AD568 is maintained by keeping impedance levels low enough to minimize the effects of parasitic circuit capacitances.

The DAC consists of 16 current sources configured to deliver a 10.24mA full-scale current. Multiple matched current sources and thin-film ladder techniques are combined to produce bit weighting. The DAC's output is a 10.24mA full scale (FS) for current output applications or a 1.024V FS unbuffered voltage output. Additionally, a 10.24V FS buffered output may be generated using an onboard 1kΩ span resistor with an external op amp. Bipolar ranges are accomplished by pin strapping.

Laser wafer trimming insures full 12-bit linearity. All grades of the AD568 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100Ω ±1.0%. The gain temperature coefficient of the voltage output is 30ppm/°C max (K).

The AD568 is available in three performance grades. The AD568JQ and KQ are available in 24-pin cerdip (0.3") packages and are specified for operation from 0 to +70°C. The AD568SQ features operation from −55°C to +125°C and is also packaged in the hermetic 0.3" cerdip.

## PRODUCT HIGHLIGHTS

1. The ultrafast settling time of the AD568 allows leading edge performance in waveform generation, graphics display and high-speed A/D conversion applications.
2. Pin strapping provides a variety of voltage and current output ranges for application versatility. Tight control of the absolute output current reduces trim requirements in externally-scaled applications.
3. Matched on-chip resistors can be used for precision scaling in high-speed A/D conversion circuits.
4. The digital inputs are compatible with TTL and +5V CMOS logic families.
5. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.

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ANALOG DEVICES

# Monolithic 12-Bit Quad DAC

# AD664



**FEATURES**
- Four Complete Voltage Output DACs
- Data Register Readback Feature
- "Reset to Zero" Override
- Multiplying Operation
- Double-Buffered Latches
- PLCC, LCC and DIP Packages

**APPLICATIONS**
- Automatic Test Equipment
- Robotics
- Process Control
- Disk Drives
- Instrumentation

## PRODUCT DESCRIPTION

The AD664 is four complete 12 bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double buffered input latch structure and a latch data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port.

The I/O port accomodates 4-, 8- and 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response of the outputs to the input data.

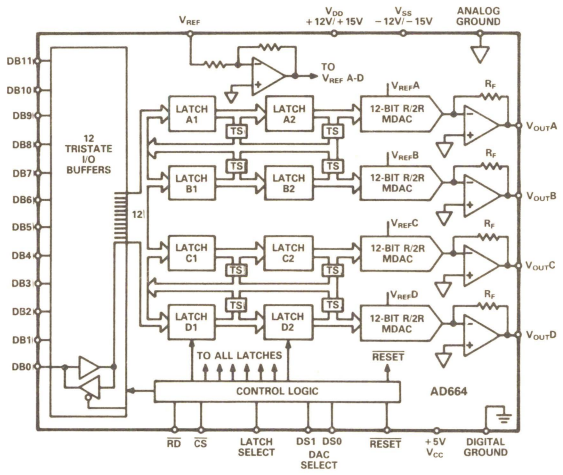
The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, 0 to 10 volts or −10 to +10 volts respectively. All DACs are operated from a single external reference.

The functional completeness of the AD664 results from the combination of Analog Devices' BIMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

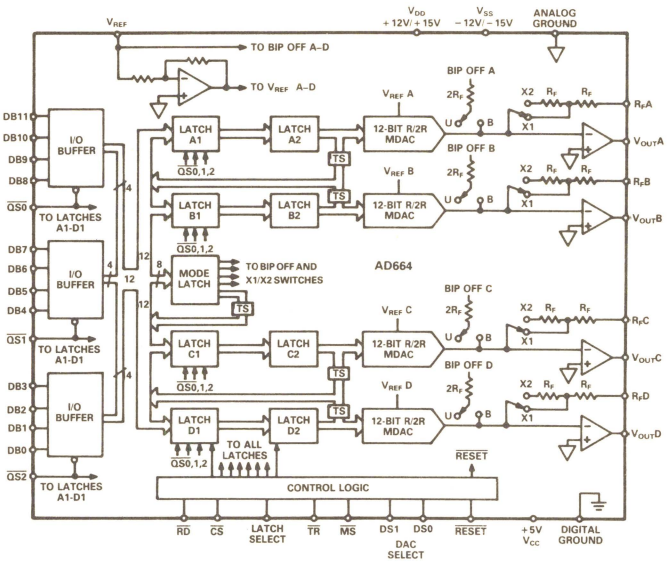
## PRODUCT HIGHLIGHTS

1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit D/A function available.
2. The output range of each DAC is fully and independently programmable.
3. Readback capability allows verification of contents of internal data registers.
4. The asynchronous RESET control returns all D/A outputs to zero volts.

## AD664 FUNCTIONAL BLOCK DIAGRAMS




*28-Pin Block Diagram*




*44-Pin Block Diagram*

5. DAC-to-DAC matching performance is specified and tested.
6. Linearity error is specified to be 1/2LSB at room temperature and 1LSB maximum.
7. DAC performance is guaranteed to be monotonic over the full operating temperature range.
8. Readback outputs have tristate outputs.
9. Multiplying-mode operation allows use with fixed or variable external references.

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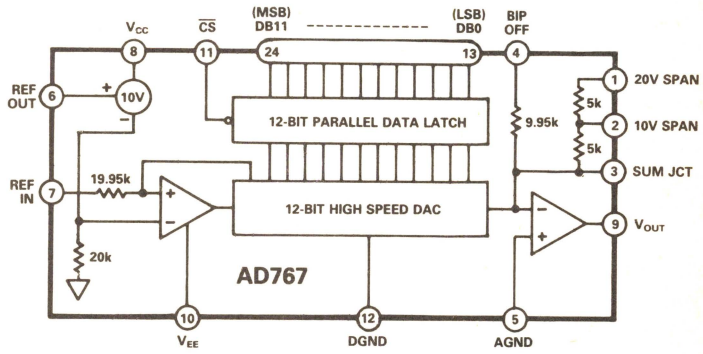
# Microprocessor-Compatible 12-Bit D/A Converter

# AD767*

**FEATURES**

- Complete 12-Bit D/A Function
  - On-Chip Output Amplifier
  - High Stability Buried Zener Reference
- Fast 40ns Write Pulse
- 0.3″ Skinny DIP Package
- Single Chip Construction
- Monotonicity Guaranteed Over Temperature
- Settling Time: 3μs max to 1/2LSB
- Guaranteed for Operation with ±12V or ±15V Supplies
- TTL/5V CMOS Compatible Logic Inputs

**AD767 FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD767 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried zener reference and input latch on a single chip. The converter uses 12 precision high-speed bipolar current steering switches and a laser-trimmed thin-film resistor network to provide high accuracy.

Microprocessor compatibility is achieved by the on-chip latch. The design of the input latch allows direct interface to 12-bit buses. The latch responds to strobe pulses as short as 40ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance of the AD767 result from a combination of advanced switch design, high-speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology.

The subsurface (buried) zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD767 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain T.C. is 5ppm/°C.

*Covered by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.

## PRODUCT HIGHLIGHTS

1. The AD767 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The input latch responds to write pulse widths as short as 40ns assuring direct interface with the industry's fastest microprocessors.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser trimmed for minimum full-scale and bipolar offset errors.
5. The precision high-speed current steering switches and on-board high-speed output amplifier settle within 1/2LSB for a 10V full-scale transition in 3.0μs when properly compensated.



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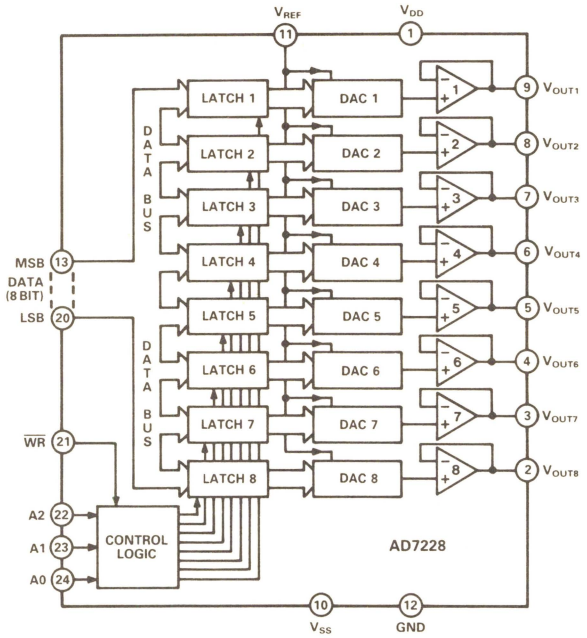
# LC²MOS Octal 8-Bit DAC

# AD7228

**FEATURES**

**Eight 8-Bit DACs with Output Amplifiers**
**Operates with Single or Dual Supplies**
**µP Compatible (95ns $\overline{WR}$ pulse)**
**No User Trims Required**
**0.3" Single Width, 24-Pin DIP**

**AD7228 FUNCTIONAL BLOCK DIAGRAM**




## GENERAL DESCRIPTION

The AD7228 contains eight 8-bit voltage-mode digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the eight D/A converters. Data is transferred into the data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Address inputs A0, A1 and A2 determine which latch is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 to +10V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7228 is fabricated on an all ion-implanted, high-speed, Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuits on the same chip.

## PRODUCT HIGHLIGHTS

1. Eight DACs and Amplifiers in Small Package:
   The single-chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.
2. Single or Dual Supply Operation:
   The voltage-mode configuration of the DACs allows single supply operation of the AD7228. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Microprocessor Compatibility:
   The AD7228 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high-performance 8-bit microprocessors.

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# ANALOG DEVICES

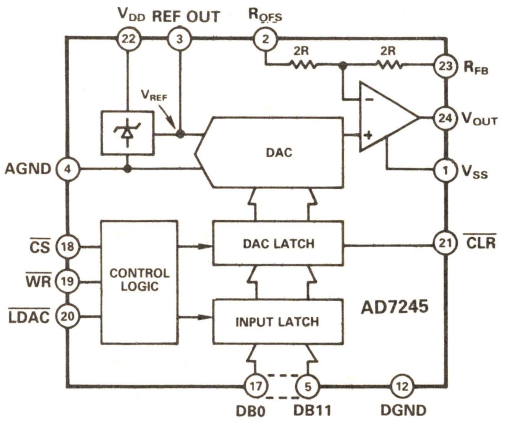
# LC²MOS 12-Bit DACPORT

# AD7245/AD7248

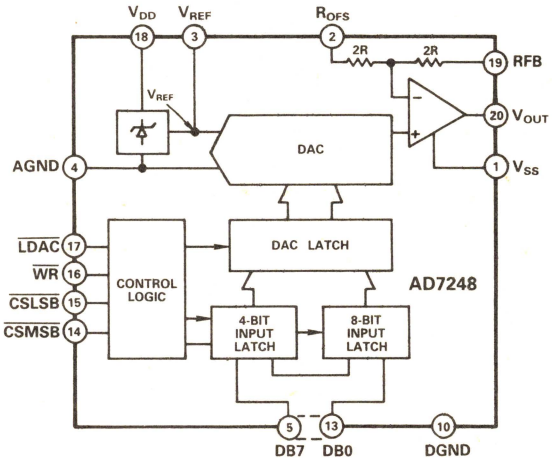
## FEATURES

**12-Bit CMOS DAC with Output Amplifier and Reference**
**Parallel Loading Structure: AD7245**
**(8+4) Loading Structure: AD7248**
**Single or Dual Supply Operation**
**Fast Digital Interface (80ns $\overline{WR}$ Pulse)**
**Low Power (65mW typ)**
**0.3", Skinny, 20- and 24-Pin DIP**
**20- and 28-Terminal Surface Mount Packages**

## AD7245/AD7248 FUNCTIONAL BLOCK DIAGRAMS




*AD7245 Functional Block Diagram*




*AD7248 Functional Block Diagram*

## GENERAL DESCRIPTION

The AD7245/AD7248 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The part features double-buffered interface logic with a 12-bit input latch and 12-bit DAC latch. The data held in the DAC latch determines the analog output of the converter. The AD7245 accepts 12-bit parallel data which is latched into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$. The AD7248 has an 8-bit wide data bus, and data is loaded to the input latch in two write operations, an 8-bit LSB load and a 4-bit MSB load. The input data must be right justified. For both parts, an asynchronous $\overline{LDAC}$ signal transfers data from the input latch to the DAC latch. The AD7245 also has a $\overline{CLR}$ signal on the DAC latch which allow features such as power-on reset to be implemented. All logic inputs are level triggered and are TTL and CMOS (5V) level compatible, while the control logic is speed compatible with most microprocessors.

The on-chip 5V buried zener diode provides a low-noise, temperature compensated reference for the DAC. The gain setting resistors allow a number of ranges at the output: 0 to +5V, 0 to +10V and −5V to +5V, when operated in dual supplies. The part can also be operated in single supply providing unipolar output ranges. The output amplifier is capable of developing +10V across a 2kΩ load.

The AD7245/AD7248 is fabricated in an all ion-implanted high-speed linear compatible CMOS (LC²MOS) process. The AD7245 is packaged in a small, 0.3" wide, 24-pin DIP and 28-terminal surface mount packages. The AD7248 is available in a 0.3" wide, 20-pin DIP and 20-terminal surface mount packages.

## PRODUCT HIGHLIGHTS

1. Complete 12-bit DACPORT™:
   The AD7245/AD7248 is a complete voltage output 12-bit DAC on one chip. This single-chip design of the DAC, reference and output amplifier is inherently more reliable than multichip designs.

2. Microprocessor Compatibility:
   The parallel loading structure of the AD7245 allows connection to microprocessors with a 16-bit wide data bus. The AD7248 is aimed at microprocessors which have an 8-bit wide data bus structure. The high-speed logic of both parts allows direct interfacing to most modern microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7245/AD7248 in multiple DAC systems.

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# LC²MOS µP Compatible 14-Bit DAC

# AD7538

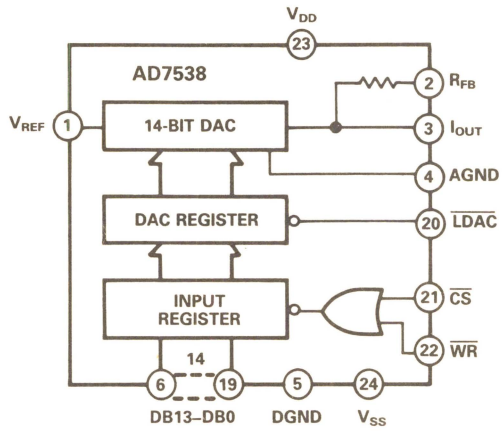
## FEATURES

- All Grades 14-Bit Monotonic over the Full Temperature Range
- Low Cost 14-Bit Upgrade for 12-Bit Systems
- 14-Bit Parallel Load with Double Buffered Inputs
- Small 24-Pin, 0.3″ DIP
- Low Output Leakage (<20nA) over the Full Temperature Range

## APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio
- Precision Servo Control
- Control and Measurement in High Temperature Environments

## AD7538 FUNCTIONAL BLOCK DIAGRAM




## GENERAL DESCRIPTION

The AD7538 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

The DAC is loaded by a single 14-bit wide word using standard Chip Select and Memory Write Logic. Double buffering, which is optional using $\overline{LDAC}$, allows simultaneous update in a system containing multiple AD7538s.

A novel low leakage configuration (U.S. Patent No. 4,590,456) enables the AD7538 to exhibit excellent output leakage current characteristics over the specified temperature range.

The AD7538 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

## PRODUCT HIGHLIGHTS

1. Guaranteed Monotonicity
   The AD7538 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Cost
   The AD7538, with its 14-bit dynamic range, affords a low cost solution for 12-bit system upgrades.
3. Small Package Size
   The AD7538 is packaged in a small 24-pin, 0.3″ DIP.
4. Low Output Leakage
   By tying $V_{SS}$ (Pin 24) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
5. Wide Power Supply Tolerance
   The device operates on a +12 to +15V $V_{DD}$, with a ±5% tolerance on this nominal figure. All specifications are guaranteed over this range.

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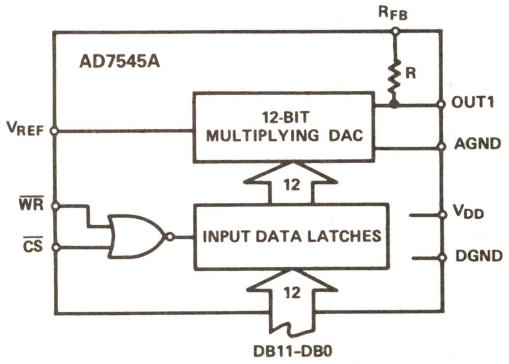
# CMOS 12-Bit Buffered Multiplying DAC

# AD7545A

**FEATURES**
**Improved Version of AD7545**
**Fast Interface Timing**
**All Grades 12-Bit Accurate**
**Small 20-Pin 0.3" DIP**
**Low Cost**

**AD7545A FUNCTIONAL BLOCK DIAGRAM**




## GENERAL DESCRIPTION

The AD7545A, a 12-bit CMOS multiplying DAC with internal data latches, is an improved version of the industry standard AD7545. This new design features a $\overline{WR}$ pulse width of 100ns which allows interfacing to a much wider range of fast 8-bit and 16-bit microprocessors. It is loaded by a single 12-bit wide word under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing unbuffered operation of the DAC.

## ORDERING INFORMATION[1,2]

| Relative Accuracy | Gain Error | Temperature Range and Package | | |
|---|---|---|---|---|
| $T_{min}$-$T_{max}$ | $T_{min}$-$T_{max}$ | 0 to +70°C | −25°C to +85°C | −55°C to +125°C |
| | | **Plastic DIP** | **Cerdip** | **Cerdip** |
| ±1/2 | ±4 | AD7545AKN | AD7545ABQ | AD7545ATQ |
| ±1/2 | ±2 | AD7545ALN | AD7545ACQ | AD7545AUQ |
| | | **PLCC[3]** | **LCCC[4]** | **LCCC[4]** |
| ±1/2 | ±4 | AD7545AKP | AD7545ABE | AD7545ATE |
| ±1/2 | ±2 | AD7545ALP | AD7545ACE | AD7545AUE |

NOTES
[1]To order MIL-STD-883C, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

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# 8-Bit, 250MHz Video D/A Converter

# AD9701

**FEATURES**
**250MHz Update Rate**
**Low Glitch Impulse**
**Complete Composite Functions**
**Internal Voltage Reference**
**Single −5.2V Supply**

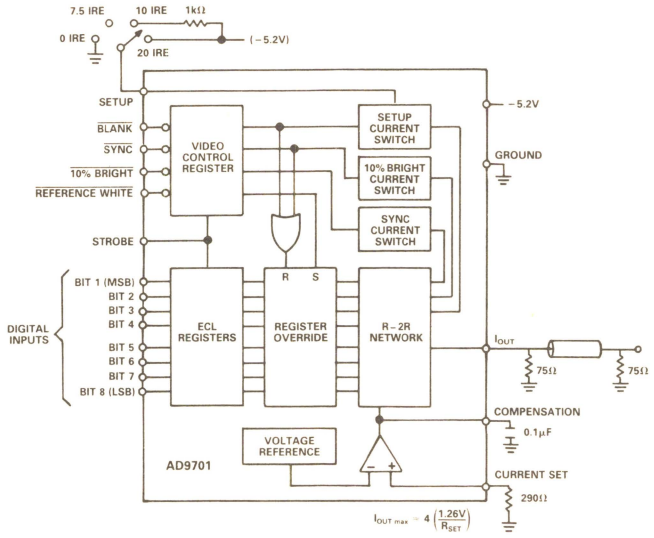
## PRODUCT DESCRIPTION

The AD9701 digital-to-analog converter is a monolithic device capable of accepting eight bits of digital data and fully integrated composite video functions at update rates as high as 250MHz.

System designs using the AD9701 are simplified by the AD9701's blanking, sync, 10% brightness, and reference white control signal inputs. Setup levels are also adjustable from 0 IRE units to 20 IRE units; and an internal voltage reference allows the converter to operate as a stand-alone video reconstruction DAC.

For an industrial temperature range of −25°C to +85°C, the 28-pin ceramic DIP is designated AD9701BQ. For extended temperature ranges of −55°C to +125°C, the AD9701SQ is also in a 28-pin DIP; the AD9701SE is a 28-pin LCC.

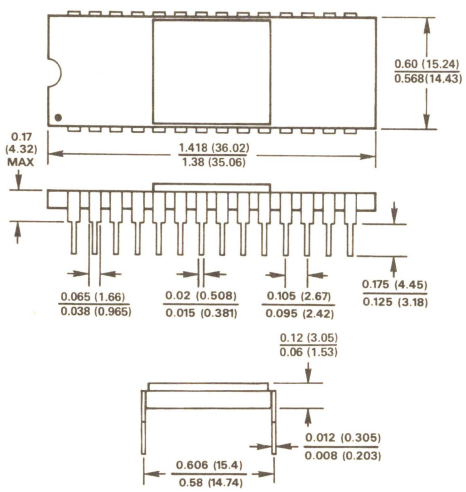
## AD9701 FUNCTIONAL BLOCK DIAGRAM




## OUTLINE DIMENSIONS

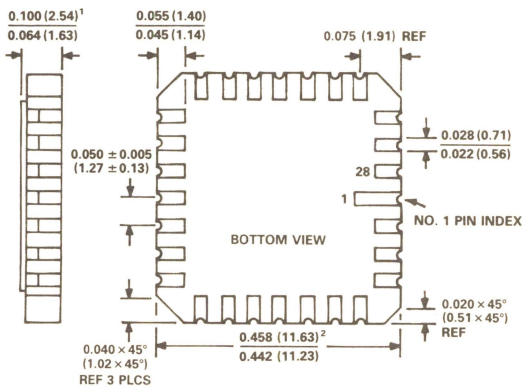
Dimensions shown in inches and (mm).

### 28-Pin Ceramic Package




LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

### 28-Terminal Leadless Chip Carrier




NOTES
[1] THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
[2] APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED.

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# ANALOG DEVICES

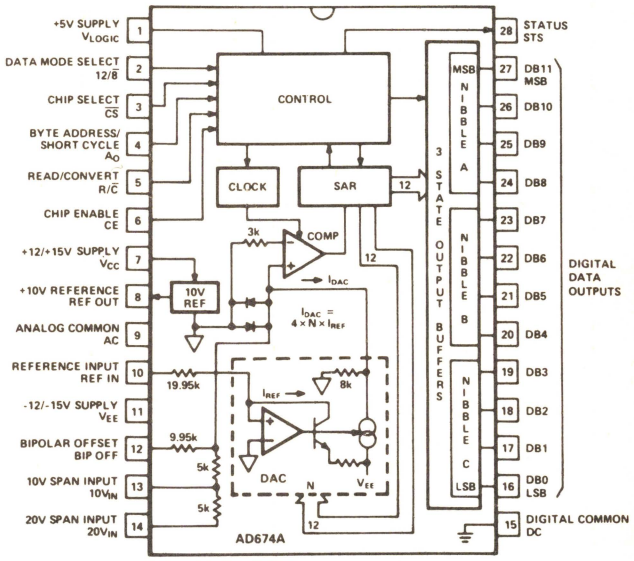
# Complete 12-Bit A/D Converter

# AD674A*

## FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- Faster Version of AD574A
- 8- and 16-Bit Bus Interface
- No Missing Codes Over Temperature
- 15μs max Conversion Time
- ±12V and ±15V Operation
- Unipolar and Bipolar Inputs
- DIP Package

## AD674A FUNCTIONAL BLOCK DIAGRAM




## PRODUCT DESCRIPTION

The AD674A is a complete 12-bit successive-approximation analog-to-digital converter with three-state output buffer circuitry for direct interface to an 8- and 16-bit microprocessor bus. A high-precision voltage reference and clock are included on-chip, and the circuit requires only power supplies and control signals for operation.

The AD674A is pin compatible with the industry-standard AD574A but offers faster conversion time and bus-access speed.

The AD674A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost. The chips are laser trimmed at the wafer stage to obtain full rated performance without external trims.

The AD674A is available in six different grades. The AD674AJ, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD674AS, T, and U are specified for the −55°C to +125°C range. All grades are available in a 28-pin hermetically sealed ceramic DIP.

The S, T, and U grades are also available with optional processing to MIL-STD-883C Class B in 28-pin DIP. The Analog Devices Military Products Databook should be consulted for details on /883B testing of the AD674A.

*Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.

## PRODUCT HIGHLIGHTS

1. The AD674A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 and 0 to +20 volts unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried zener reference is trimmed to 10.00 volts with 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 2.0mA beyond the requirements of the reference and bipolar offset resistors.



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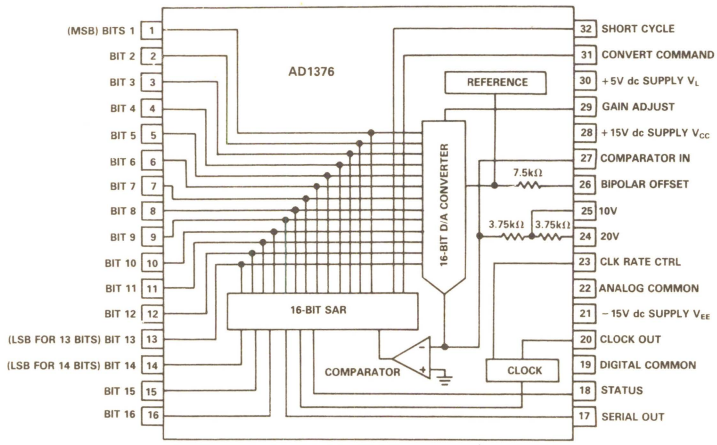
# Complete High-Speed 16-Bit A/D Converter

# AD1376

**FEATURES**

- Complete 16-Bit Converter With Reference and Clock
- ±0.003% Maximum Nonlinearity
- No Missing Codes to 14 Bits Over Temperature
- Fast Conversion – 14μs (14 Bit)
- Short Cycle Capability
- Parallel and Serial Outputs
- Low Power: 645mW Typical
- Industry Standard Pin Out

**AD1376 FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD1376 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin, pin-stake DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR, and maximum 14-bit conversion time of 15μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD1376 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

## APPLICATIONS

The AD1376 is excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

## PRODUCT HIGHLIGHTS

1. The AD1376 provides 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J grade) at 25°C.
2. Conversion time is 14μs typical to 14 bits with short cycle capability, and 16μs to 16 bits.
3. Two binary codes are available on the AD1376 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary twos complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.
5. The AD1376 includes an internal reference and clock, with external clock adjust pin, and a serial output.

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ANALOG DEVICES

# LC²MOS Complete, High-Speed 12-Bit ADC

# AD7572

## FEATURES

- 12-Bit Resolution and Accuracy
- Fast Conversion Time
  - AD7572XX05: 5μs
  - AD7572XX12: 12.5μs
- Complete with On-Chip Reference
- Fast Bus Access Time: 90ns
- Low Power: 135mW
- Small, 0.3", 24-pin Package

## GENERAL DESCRIPTION

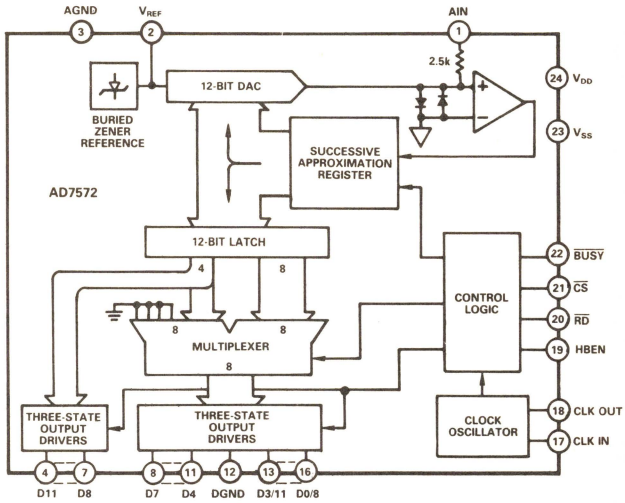
The AD7572 is a complete, 12-bit ADC that offers high-speed performance combined with low, CMOS power levels. The AD7572 uses an accurate, high-speed DAC and comparator in a successive-approximation loop to achieve a fast conversion time. An on-chip, buried zener diode provides a stable reference voltage to give low drift performance over the full temperature range and the specified accuracy is achieved without any user trims. An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation, or the clock input may be driven from an external clock source such as a divided-down microprocessor clock. The only other external components required for basic operation of the AD7572 are decoupling capacitors for the supply voltages and reference output.

The AD7572 has a high-speed digital interface with three-state data outputs and can operate under the control of standard microprocessor Read ($\overline{RD}$) and decoded address ($\overline{CS}$) signals. Interface timing is sufficiently fast to allow the AD7572 to operate with most popular microprocessors, with three-state enable times of only 90ns and bus relinquish times of 75ns.

The AD7572 is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

The AD7572 is packaged in a 0.3", 24-pin DIP and is also available in 28-pin leadless ceramic chip carrier (LCC).

## AD7572 FUNCTIONAL BLOCK DIAGRAM




## PRODUCT HIGHLIGHTS

1. Fast, 5μs and 12.5μs conversion times make the AD7572 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any wideband data acquisition system.
2. On-chip buried-zener reference has temperature coefficient as low as 25ppm/°C, giving low full-scale drift over the operating temperature range.
3. Stable DAC and comparator give excellent linearity and low zero error over the full temperature range.
4. Fast, easy-to-use digital interface has three-state bus access times of 90ns and bus relinquish times of 75ns, allowing the AD7572 to interface to most popular microprocessors.
5. LC²MOS circuitry gives low power drain (135mW) from +5, −15 volt supplies.
6. 24-pin 0.3" package offers space saving over parts in 28-pin 0.6" DIP.

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ANALOG DEVICES

# LC²MOS 10µs µP Compatible 8-Bit ADC

# AD7576

**FEATURES**

- **Single +5V Operation with External Positive Reference**
- **Fast Conversion Time: 10µs**
- **No Missed Codes Over Full Temperature Range**
- **Microprocessor Compatible**
- **Low Cost**
- **Low Power (15mW)**
- **100ns Data Access Time**

## GENERAL DESCRIPTION

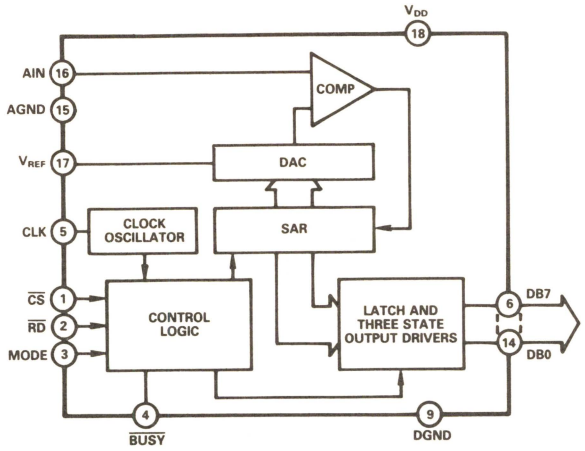
The AD7576 is a low cost, low power, microprocessor compatible 8-bit analog-to-digital converter, which uses the successive approximation technique to achieve a fast conversion time of 10µs. The device is designed to operate with an external reference of +1.23V (standard bandgap reference) and converts input signals from 0V to $2V_{REF}$.

The part is designed for ease of microprocessor interface with three control inputs ($\overline{CS}$, $\overline{RD}$ and MODE) controlling all ADC operations such as starting conversion and reading data. The interface logic allows the part to be easily configured as a memory mapped device. All data outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. The output latches serve to make the conversion process transparent to the microprocessor.

The part is designed for single +5V operation, has on-board comparator, interface logic, and internal/external clock option. This makes the AD7576 ideal for most ADC/µP interface applications.

The AD7576 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process and is packaged in a small, 0.3″ wide, 18-pin DIP.

## AD7576 FUNCTIONAL BLOCK DIAGRAM




## PRODUCT HIGHLIGHTS

1. Single Supply Operation
   Operation from a single +5V supply with a +1.23V reference allows operation of the AD7576 with microprocessor systems without any additional power supplies.
2. Low Power
   CMOS fabrication of the AD7576 results in a very low power dissipation figure of 15mW typical.
3. Versatile Interface Logic
   The AD7576 can be configured to perform continuous conversions or to convert on command. It can be interfaced as SLOW-MEMORY or ROM, allowing versatile interfacing to most microprocessors.
4. Fast Conversion Time
   The fabrication of the AD7576 on Analog Devices' Linear Compatible CMOS (LC²MOS) process enables fast conversion times of 10µs, eliminating the need for expensive Sample-and-Holds in many low frequency applications.

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# ANALOG DEVICES

# LC²MOS 10-Bit Sampling ADC

# AD7579/AD7580

**FEATURES**
- 20μs Conversion Time
- On-Chip Sample-Hold
- 50kHz Sampling Rate
- 25kHz Full-Power Input Bandwidth
- Choice of Data Formats
- Single +5V Supply
- Low Power (50mW)
- Small, 0.3", 24-Pin Package

## GENERAL DESCRIPTION

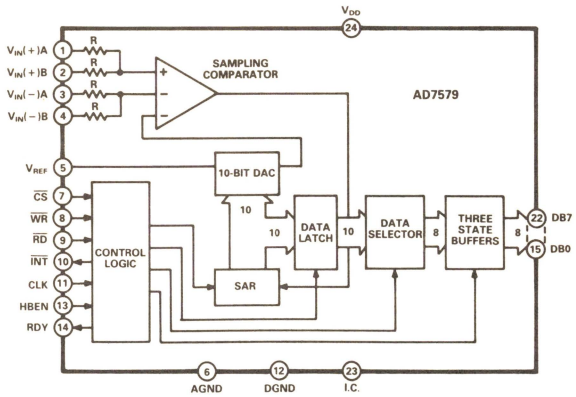
The AD7579 and AD7580 are 10-bit, successive approximation ADCs. They have differential analog inputs that will accept unipolar or bipolar input signals while operating from only a single +5V supply. Input ranges of 0 to +2.5V, 0 to +5V and ±2.5V are possible with no external signal conditioning. Only an external 2.5V reference and clock and control signals are required to make them operate.

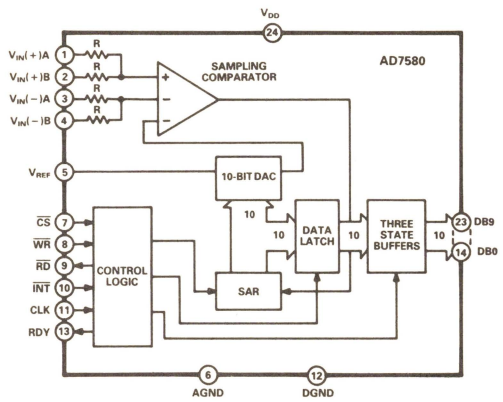
With conversion time of less than 20μs and an on-chip sample-hold amplifier, the devices are ideally suited for digitizing ac signals. The maximum sampling rate is 50kHz, giving an input bandwidth of 25kHz. The parts are specified not only with traditional static specifications such as linearity and offset but also with dynamic specifications (SNR, Harmonic Distortion, IMD).

The AD7579 and AD7580 are microprocessor-compatible with standard microprocessor control inputs ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and data outputs capable of interfacing to high-speed data buses. There is a choice of data formats, with the AD7579 offering an (8+2) read and the AD7580 offering a 10-bit parallel word.

Space saving and low power are also features of these devices. They dissipate less than 50mW from a single +5V supply and are offered in a 0.3", 24-pin package and in plastic/ceramic chip carrier for surface mounting.

## AD7579/AD7580 FUNCTIONAL BLOCK DIAGRAM




## PRODUCT HIGHLIGHTS

1. 20μs conversion time with on-chip sample-hold makes the AD7579 and AD7580 ideal for audio and higher bandwidth signals, e.g., modem applications.
2. Differential analog inputs can accept unipolar or bipolar input signals, but only a single, +5V power supply is needed.
3. Versatile and easy-to-use digital interface has fast bus access/relinquish times, allowing connection to most popular microprocessors.

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ANALOG DEVICES

# LC²MOS High-Speed 12-Bit ADC

# AD7672

**FEATURES**
- 12-Bit Resolution and Accuracy
- Fast Conversion Time
  - AD7672XX03 – 3μs
  - AD7672XX05 – 5μs
  - AD7672XX10 – 10μs
- Unipolar or Bipolar Input Ranges
- Low Power: 110mW
- Fast Bus Access Times: 90ns
- Small, 0.3", 24-Pin Package

## GENERAL DESCRIPTION

The AD7672 is a high-speed 12-bit ADC, fabricated in an advanced, mixed technology, Linear-Compatible CMOS (LC²MOS) process, which combines precision bipolar components with low-power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3μs while dissipating only 110mW of power.

To allow maximum flexibility the AD7672 is designed for use with an external reference voltage. This allows the user to choose a reference whose performance suits the application or to drive many AD7672s from a single system reference, since the reference input of the AD7672 is buffered and draws little current. For digital signal processing applications where absolute accuracy and temperature coefficients may be unimportant, a low-cost reference can be used. For maximum precision, the AD7672 can be used with a high-accuracy reference, such as the AD588, when absolute 12-bit accuracy can be obtained over a wide temperature range.

An on-chip clock-circuit is provided which may be used with a crystal for accurate definition of conversion time. Alternatively, the clock input may be driven from an external source such as a microprocessor clock.

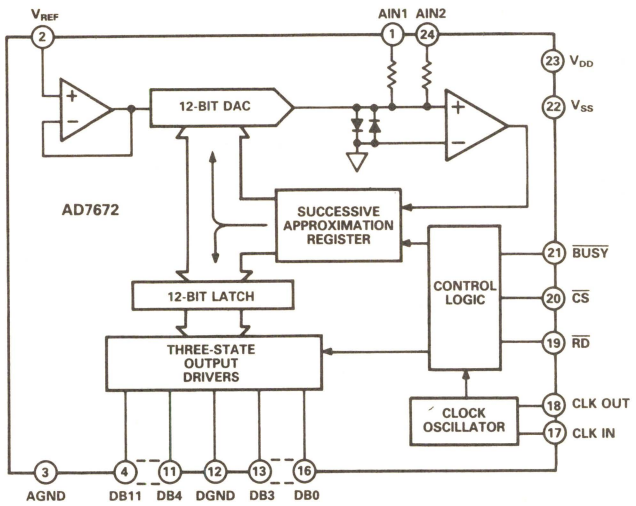
The AD7672 also offers flexibility in its analog input ranges, with a choice of 0 to +5V, 0 to +10V and ±5V.

The AD7672 is also designed to operate from nominal supply voltages of +5V and −12V. This makes it an ideal choice for data acquisition cards in personal computers where the negative supply is generally −12V.

The AD7672 has a high-speed digital interface with three-state data outputs and standard microprocessor control inputs (Chip Select and Read). Bus access time of only 90ns allows the AD7672 to be interfaced to most modern microprocessors.

The AD7672 is available in a variety of space-saving packages; plastic and hermetic 24-pin "skinny" DIP and 28-pin ceramic and plastic chip carrier.

**AD7672 FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT HIGHLIGHTS

1. Fast, 3μs, 5μs and 10μs conversion speeds make the AD7672 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any high-speed data acquisition system.
2. LC²MOS circuitry gives high precision with low power drain (110mW typ).
3. Choice of 0 to +5V, 0 to +10V or ±5V input ranges, accomplished by pin-strapping.
4. Fast, simple, digital interface has a bus access time of 90ns allowing easy connection to most microprocessors.
5. Available in space-saving 24-pin, 0.3" DIP or surface mount package.

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# ANALOG DEVICES

# High-Speed 6-Bit A/D Converter

# AD9000

## FEATURES

**75MHz Minimum Encode Rate**
**Bipolar Input Range**
**Low Error Rate**
**Overflow Bit**

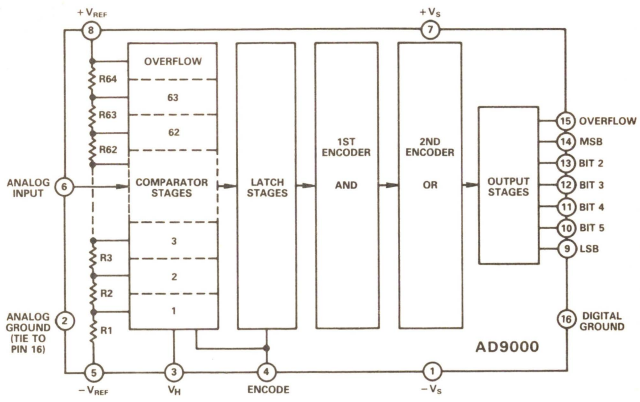
## PRODUCT DESCRIPTION

The AD9000 is a 6-bit, 75MHz analog-to-digital converter in the expanding line of monolithic high-speed data converters available from Analog Devices. It is a "flash" converter which uses 64 parallel comparators to digitize fast-moving analog input signals without the need for external track-and-hold (T/H) circuits.

Careful design techniques assure operation over extended temperature ranges. Its flexibility and usefulness are enhanced by its ability to operate with maximum positive and negative references applied simultaneously. Many other flash converters limit the user to a small range of voltage within the refererence extremes.

The AD9000 is available in commercial and military temperature ranges. Both versions are offered in 16-pin ceramic DIPs; the extended temperature range unit is also available in a 28-pin ceramic LCC package. The extended temperature versions are fully compliant MIL-STD-883, Revision C, devices.

## AD9000 FUNCTIONAL BLOCK DIAGRAM



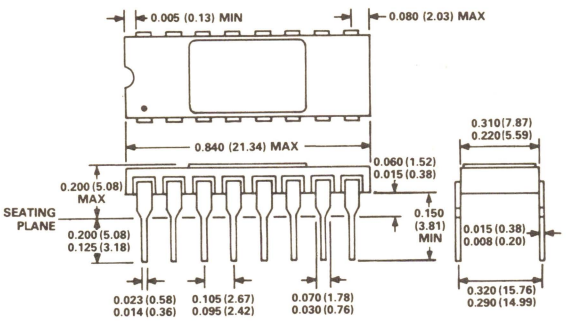

## ORDERING INFORMATION

| Device | Temperature Range | Description |
|---|---|---|
| AD9000JD | 0 to +70°C | 16-Pin DIP, Industrial |
| AD9000SD/883C | −55°C to +125°C | 16-Pin, MIL-STD-883 |
| AD9000SE/883C | −55°C to +125°C | 28-Pin LCC, MIL-STD-883 |

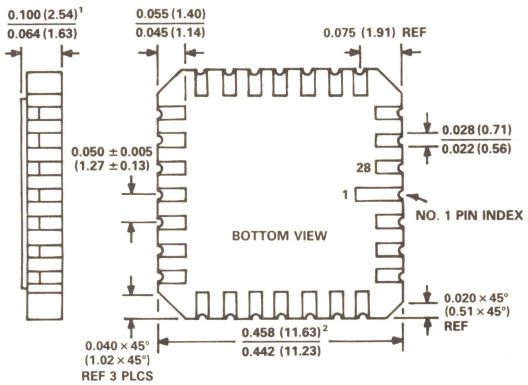
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 16-Pin Ceramic




### 28-Pin LCC




NOTES
[1] THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
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ALL TERMINALS ARE GOLD PLATED.

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Analog Devices

# Ultrahigh-Speed 8-Bit Monolithic ADC

# AD9002

**FEATURES**
**150MHz Encode Rate**
**17pF Input Capacitance**
**Low Power – 750mW**
**−5.2V Single Power Supply**

## PRODUCT DESCRIPTION

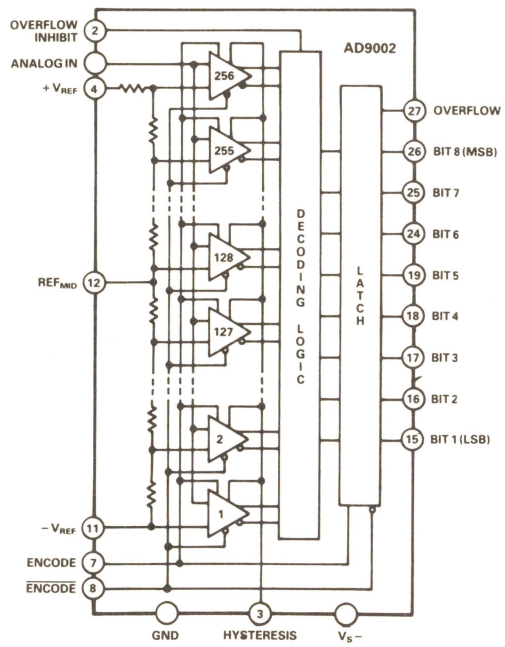
The AD9002 is an 8-bit, ultrahigh-speed, analog-to-digital converter fabricated in an advanced bipolar process which allows operation at sampling rates in excess of 150MHz. Functionally, the AD9002 comprises 256 parallel comparator stages whose outputs are decoded to drive the ECL-compatible output latches.

An innovative comparator design and extremely close attention to device layout details give the AD9002 an exceptional small-signal bandwidth of 115MHz. This wide input bandwidth allows accurate acquisition of high-speed pulse inputs without an external track-and-hold. The decoding scheme used at the output of the comparator minimizes false codes, which is critical for high-speed linearity.

External hysteresis control can optimize comparator sensitivity and improve performance even more. Since it dissipates only 750mW, the AD9002 can be used over the full extended temperature range. An overflow bit signals overrange inputs; this overflow output can be disabled with the overflow inhibit pin.

The AD9002 is available with either 0.5LSB linearity or 0.75LSB linearity; both versions operate over the industrial temperature range of −25°C to +85°C and are packaged in 28-pin DIPs.

## AD9002 FUNCTIONAL BLOCK DIAGRAM

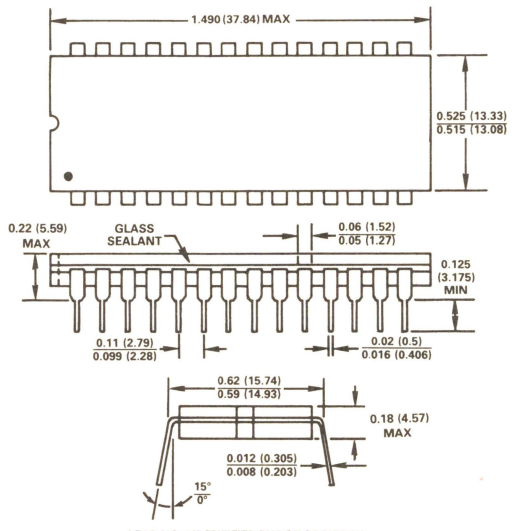



Military temperature range devices for operation over the mil spec temperatures of −55°C to +125°C are in cerdip and LCC packages. Consult the factory for MIL-STD-883 units.

## OUTLINE DIMENSIONS

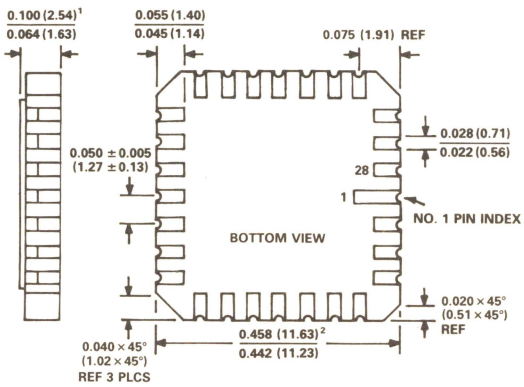
Dimensions shown in inches and (mm).

### 28-Pin Cerdip Package




LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

### 28-Pin Ceramic Leadless Chip Carrier (LCC)




NOTES
[1] THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
[2] APPLIES TO ALL FOUR SIDES.
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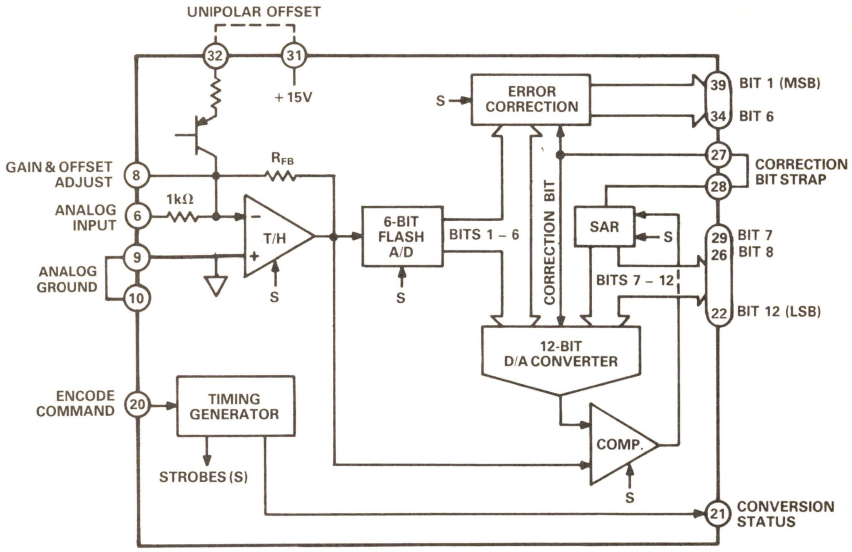
# ANALOG DEVICES

# 12-Bit, 1MHz A/D Converter

# AD9003

**FEATURES**
**12-Bit Resolution**
**1MHz Word Rates**
**T/H and Timing Included**
**Single 40-Pin DIP**

**AD9003 FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD9003 is a complete 12-bit, 1MHz analog-to-digital converter (ADC) which combines low cost and high-performance in a single 40-pin DIP. This unique converter includes track-and-hold (T/H), timing, and encoding functions with a power dissipation of only 2.2 watts.

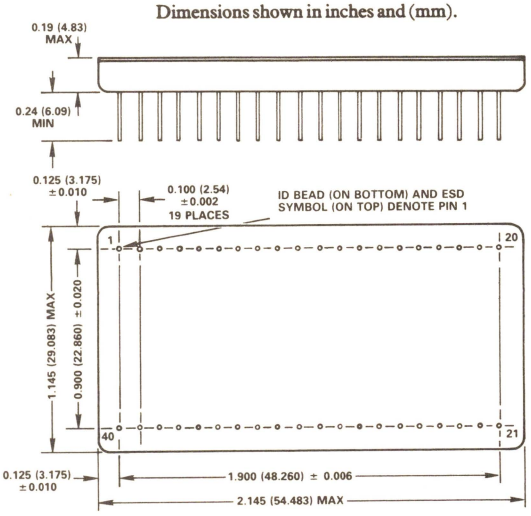
This remarkable unit is capable of converting analog signals to the Nyquist limit at word rates through 1MHz. Its 1μs conversion interval includes acquisition time for the internal T/H, making it a true 1MHz converter.

Proprietary conversion techniques achieve linearity equivalent to the best successive approximation ADC along with subranging conversion speeds. A conversion status signal simplifies transferring output data into system logic. Innovative thick-and thin-film technologies assure excellent performance over temperature without compromising ac characteristics.

The AD9003KM operates at case temperatures from 0 to +70°C; the SM/883B and TM/883B units operate from −25°C to +100°C.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

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# ANALOG DEVICES

# TTL High-Speed 8-Bit Monolithic ADC

# AD9012

**FEATURES**
**Guaranteed 75MHz Encode Rate**
**TTL-Compatible Output**
**17pF Input Capacitance**
**1W Power Dissipation**

## PRODUCT DESCRIPTION

Monolithic construction, TTL-compatiblity, and high word rates are combined in the 8-bit AD9012 A/D converter.

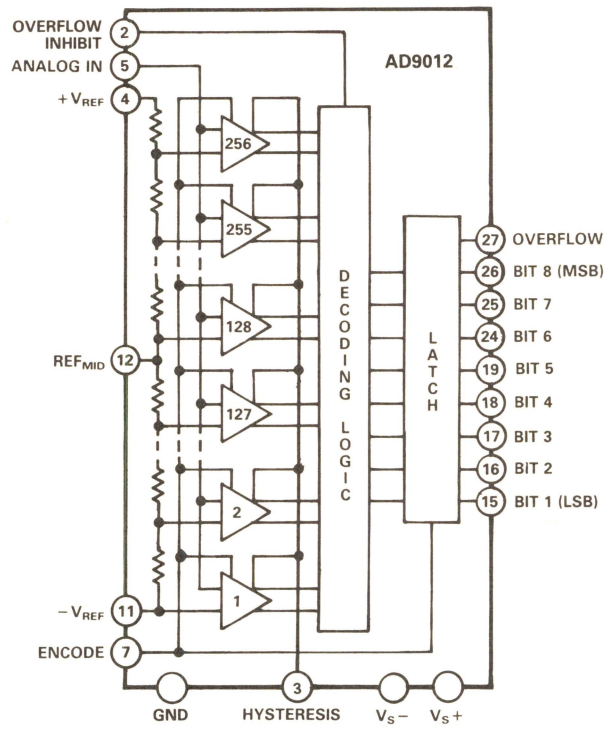
The advanced bipolar process used in the design of the unit guarantees 75MHz word rates; typically, the device is capable of operating at 90MHz. Its low input capacitance of 17pF places fewer demands on the drive amplifier than do many other flash converters.

Functionally, the AD9012 comprises 256-parallel comparator stages whose outputs are decoded to drive TTL-compatible output latches. An innovative comparator design and extremely close attention to device layout give the AD9012 an exceptional small-signal bandwidth of 115MHz. This wide input bandwidth allows accurate acquisition of high-speed pulse inputs without an external track-and-hold.

The decoding scheme used at the output of the comparator minimizes false codes, which is critical for high-speed linearity. An overflow bit signals overrange inputs; this overflow output can be disabled with the overflow inhibit pin.

The AD9012 is available with either 0.5LSB linearity or 0.75LSB linearity; both versions operate over the industrial temperature range of −25°C to +85°C. Military temperature range devices for operation over the mil spec temperatures of −55°C to +125°C are in cerdip and LCC packages.

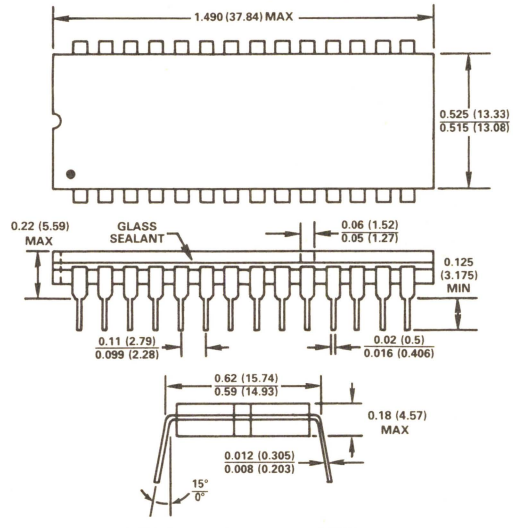
## AD9012 FUNCTIONAL BLOCK DIAGRAM




## OUTLINE DIMENSIONS

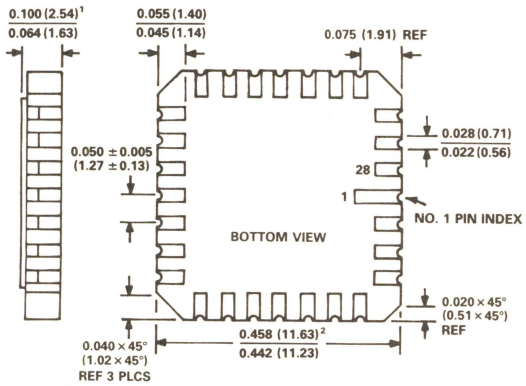
Dimensions shown in inches and (mm).

### 28-Pin Cerdip Package




LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

### 28-Pin Ceramic Leadless Chip Carrier (LCC)




NOTES
1 THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2 APPLIES TO ALL FOUR SIDES.
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# ANALOG DEVICES

# Monolithic 8-Bit Video A/D Converter

# AD9048

**FEATURES**
**8-Bits; 20MSPS Minimum Word Rates**
**420mW Power Dissipation**
**No T/H Required**
**17pF Input Capacitance**
**Industry Standard Pinouts**

## PRODUCT DESCRIPTION

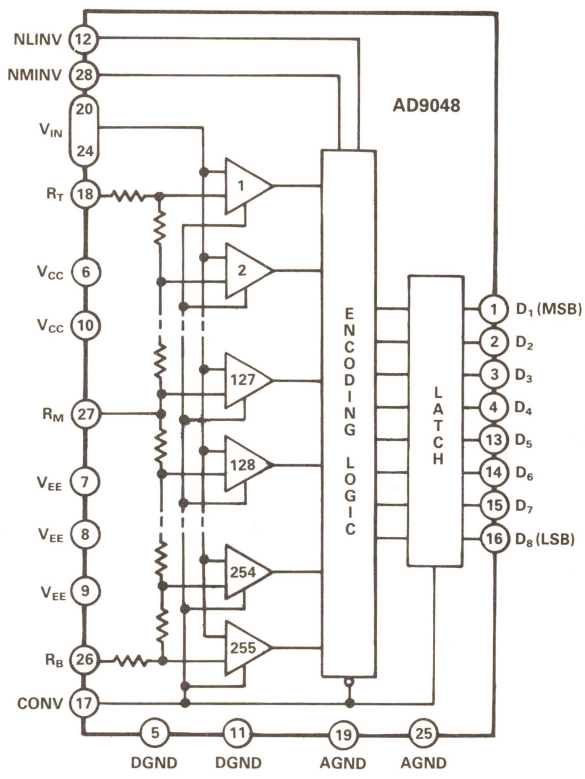
The AD9048 is an 8-bit, 20MSPS flash converter which is pin-for-pin compatible with the TDC1048 unit but offers enhancements over its predecessor. Significantly improved output driver stages and reduced power make the AD9048 attractive for system designs.

Full power bandwidth is 7MHz minimum, making it an ideal choice for doing real-time conversion of video signals, where analog frequency information of interest is seldom higher than 4MHz-5MHz.

Clocked latching comparators, encoding logic, and an output buffer register operating at minimum rates of 20MSPS make it unncecessary to incorporate a sample-and-hold (S/H) or track-and-hold (T/H) into designs using the AD9048. All digital control inputs and outputs are TTL compatible.

Devices which operate over two case temperature ranges and with two grades of linearity are available. Linearities of 0.5LSB or 0.75LSB can be ordered for a commercial range of 0 to +70°C, or extended temperatures of −55°C to +125°C . Units are packaged in 28-pin ceramic DIPs and are also available as LCC packages.

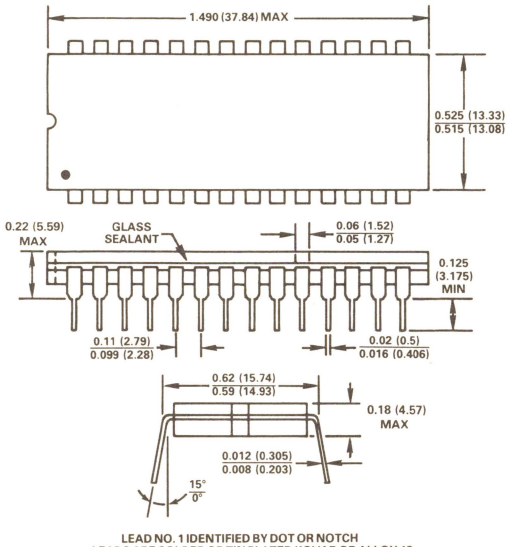
## AD9048 FUNCTIONAL BLOCK DIAGRAM




## OUTLINE DIMENSIONS

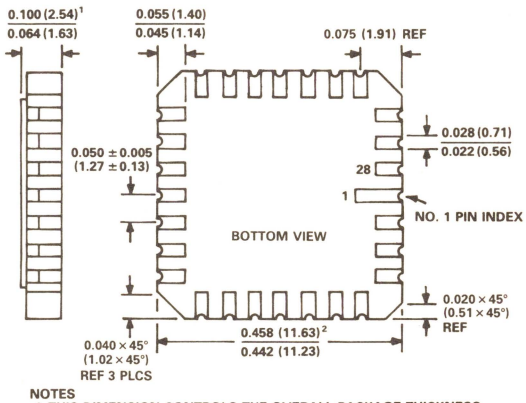
Dimensions shown in inches and (mm).

### 28-Pin Cerdip Package




LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

### 28-Pin Ceramic Leadless Chip Carrier (LCC)




NOTES
[1] THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
[2] APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED.

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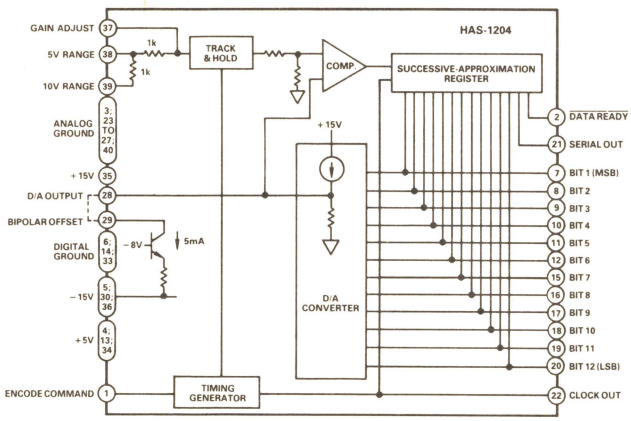
ANALOG DEVICES

# Ultrahigh-Speed 12-Bit A/D Converter

# HAS-1204

**FEATURES**
**12-Bit Resolution**
**500kHz Word Rates**
**Internal Track-and-Hold**
**Single 40-Pin DIP**

## HAS-1204 FUNCTIONAL BLOCK DIAGRAM




## PRODUCT DESCRIPTION

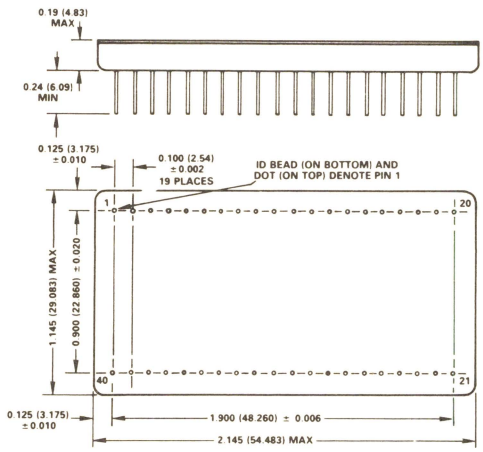
The HAS-1204 is a *complete* 12-bit hybrid A/D converter in a single 40-pin metal DIP. In this context, "complete" means the unit includes a track-and-hold (T/H) amplifier, encoder, and all the necessary timing circuits. It is a complete, self-contained device ready to perform the conversion function without the need for external circuits.

Maximum conversion time of the HAS-1204 is 2.0 microseconds, including the acquisition time of the internal T/H. The large-signal bandwidth of the T/H is 4MHz, and the small-signal bandwidth is 7MHz. This combination of characteristics assures that the HAS-1204 will operate at word rates from dc through 500kHz, digitizing analog signals containing frequency components to 250kHz with minimum attenuation or distortion.

Two versions are available as standard products; both are housed in 40-pin hermetically sealed metal packages. For a temperature range of −25°C to +85°C, specify the model HAS-1204BM; for a range of −55°C to +100°C, order model number HAS-1204SM. Units screened to military requirements are available; contact the factory for details.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

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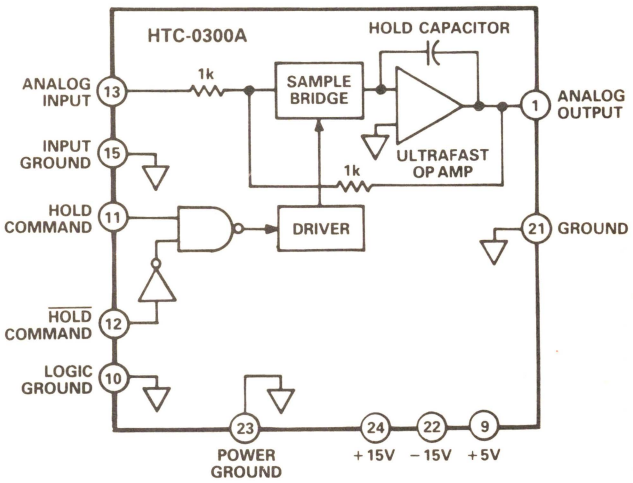
# ANALOG DEVICES

# Ultrahigh-Speed Hybrid Track-and-Hold Amplifiers

## HTC-0300A

**FEATURES**
**Aperture Jitter of 50ps**
**Input Range ±10V**
**Output Current ±50mA**
**Max Droop Rate 5μV/μs**
**Max 200ns Acquisition Time (0.01%; 10V Step)**

### HTC-0300A FUNCTIONAL BLOCK DIAGRAM




NOTES: WHEN APPLYING HOLD COMMAND TO PIN 11, CONNECT HOLD COMMAND (PIN 12) TO GROUND.
WHEN APPLYING HOLD COMMAND TO PIN 12, CONNECT HOLD COMMAND (PIN 11) TO +5V.

### PRODUCT DESCRIPTION

The HTC-0300A is a hybrid microcircuit track-and-hold (T/H) amplifier useful in a wide variety of signal processing applications, including waveform measurements, analog signal delay, and signal sampling.

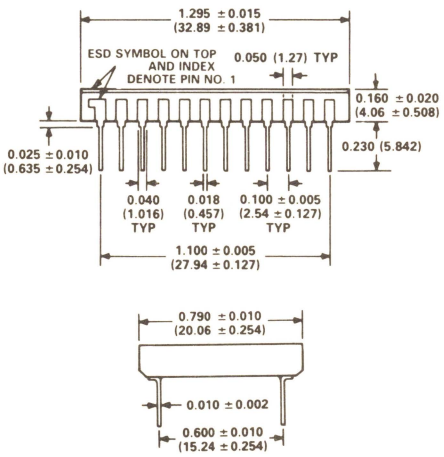
Device features include a typical aperture jitter of only 50 picoseconds rms, wide dynamic input range of ±10 volts, and laser-trimmed gain and offset which preclude a need for external adjustments. Its speed and precision are the result of innovative design techniques using a high-speed op amp and DMOSFET switches. These techniques also enhance device performance in feedthrough rejection, linearity, harmonic distortion, droop rate, and output voltage swing.

For case temperatures of −25°C to +85°C, order the HTC-0300A; it is packaged in a 24-pin hermetically sealed ceramic DIP. Military case temperatures of −55°C to +125°C are available with the HTC-0300AM, HTC-0300AM/883B, and the HTC-0300ATD/883B. The first two units are housed in 24-pin hermetic metal packages, and the latter unit is packaged in a hermetic 24-pin ceramic DIP.

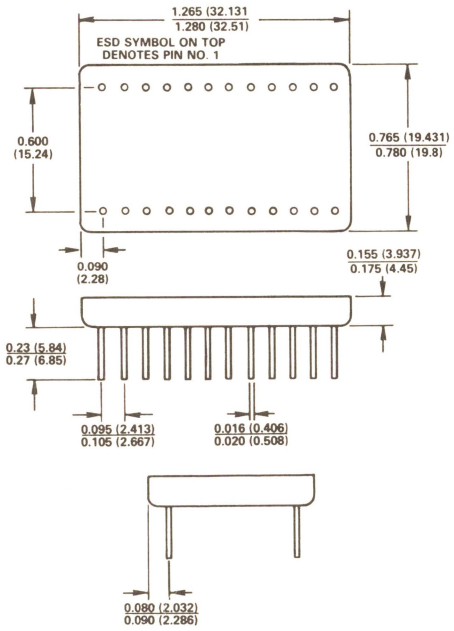
### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**HTC-0300A and HTC-0300ATD/883B**




**HTC-0300AM and HTC-0300AM/883B**

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ANALOG DEVICES

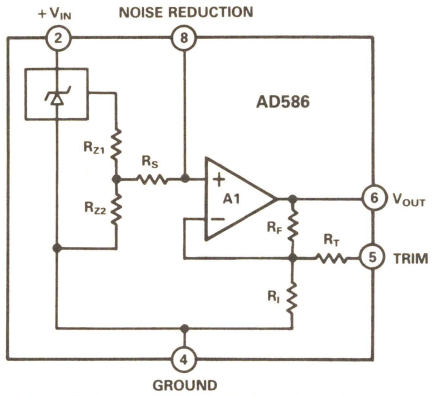
# High Precision 5-Volt Reference

# AD586

## FEATURES

**Laser Trimmed to High Accuracy:**
**5.000V ±2.5mV (L Grade)**
**Trimmed Temperature Coefficient:**
**5ppm/°C max, 0 to 70°C (L Grade)**
**10ppm/°C max, −55°C to +125°C (T Grade)**
**Noise Reduction Capability**
**Low Quiescent Current: 3mA max**
**Output Trim Capability**

## AD586 FUNCTIONAL BLOCK DIAGRAM




NOTE: PINS 1, 3 & 7 ARE INTERNAL TEST POINTS.
MAKE NO CONNECTIONS TO THESE POINTS.

## PRODUCT DESCRIPTION

The AD586 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD586 provides outstanding performance at low cost.

The AD586 offers much higher performance than most other 5V references. Because the AD586 uses an industry standard pinout, many systems can be upgraded instantly with the AD586. The buried Zener approach to reference design provides lower noise and drift than bandgap voltage references. The AD586 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD586 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD586J, K and L are specified for operation from 0 to +70°C, and the AD586S and T are specified for −55°C to +125°C operation. All grades are packaged in an 8-pin cerdip package. The AD586J and the AD586K are also available in an 8-pin plastic surface mount small outline (SO) package.

## PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD586L has a maximum deviation from 5.000V of ±3.625mV between 0 and +70°C, and the AD586T guarantees ±7.5mV maximum total error between −55°C and +125°C.
2. For applications requiring higher precision, an optional fine-trim connection is provided.
3. Any system using an industry standard pinout reference can be upgraded instantly with the AD586.
4. Output noise of the AD586 is very low, typically 4μV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.

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ANALOG DEVICES

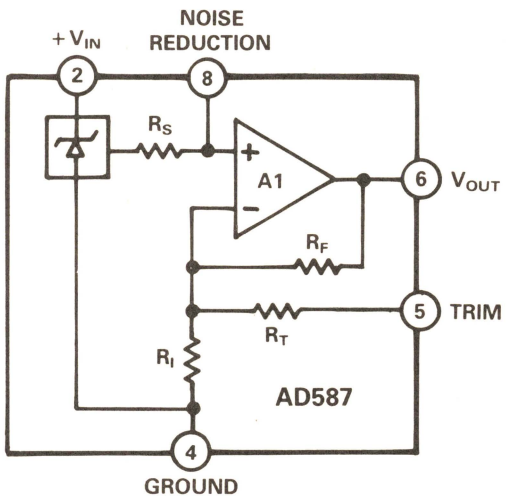
# High-Precision 10V Reference

# AD587

**FEATURES**

**Laser Trimmed to High Accuracy:**
**10.000V ±5mV (L and U Grades)**
**Trimmed Temperature Coefficient:**
**5ppm/°C max, (L and U Grades)**
**Noise Reduction Capability**
**Low Quiescent Current: 4mA max**
**Output Trim Capability**

**AD587 FUNCTIONAL BLOCK DIAGRAM**




**NOTE: PINS 1, 3, 7 & 8 ARE INTERNAL TEST POINTS. MAKE NO CONNECTIONS TO THESE POINTS.**

## PRODUCT DESCRIPTION

The AD587 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD587 provides outstanding performance at low cost.

The AD587 offers much higher performance than most other 10V references. Because the AD587 uses an industry standard pinout, many systems can be upgraded instantly with the AD587. The buried Zener approach to reference design provides lower noise and drift than band-gap voltage references. The AD587 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD587 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD587J, K and L are specified for operation from 0 to +70°C, and the AD587S, T and U are specified for −55°C to +125°C operation. All grades are available in 8-pin cerdip. The J version is also available in an 8-pin Small Outline IC (SOIC) package for surface mount applications.

## PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD587L has a maximum deviation from 10.000V of ±8.5mV between 0 and +70°C, and the AD587U guarantees ±14mV maximum total error between −55°C and +125°C.
2. For applications requiring higher precision, an optional fine-trim connection is provided.
3. Any system using an industry standard pinout 10 volt reference can be upgraded instantly with the AD587.
4. Output noise of the AD587 is very low, typically 4μV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.



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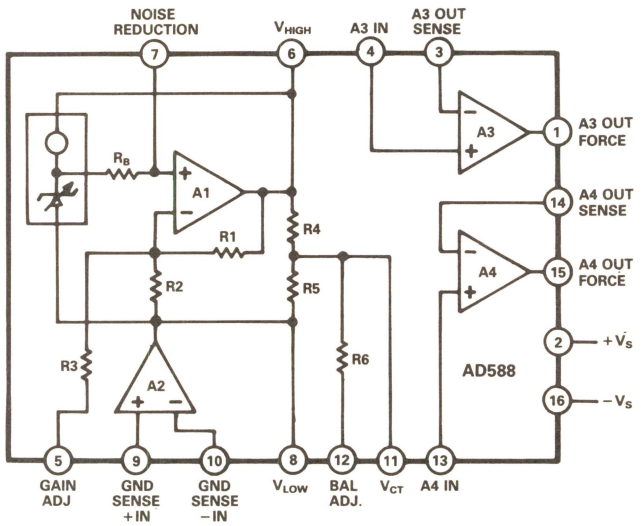
# ANALOG DEVICES

# High Precision Voltage Reference

# AD588*

**FEATURES**
**Low Drift – 1.5ppm/°C**
**Low Initial Error – 1mV**
**Pin-Programmable Output**
**+10V, +5V, ±5V Tracking, −5V, −10V**
**Flexible Output Force and Sense Terminals**
**High Impedance Ground Sense**
**Machine-Insertable DIP Packaging**
**Guaranteed Long-Term Stability – 25ppm/1000 hours**

**AD588 FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted buried zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser-trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 and autocalibration software.

The AD588 is available in five versions. AD588AD, BD, and CD grades are packaged in a 16-pin side-brazed ceramic DIP and are specified for the −25°C to +85°C industrial temperature range. The ceramic AD588SD and TD grades are specified for the full military/aerospace temperature range.

***Covered by Patent Number 4,644,253**

## PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Long-term stability is excellent and the CD and TD versions are 100% tested and guaranteed for 25 parts-per-million stability in a 1000-hour period.
3. Output noise of the AD588 is very low – typically 6μV p-p. A pin is provided for additional noise filtering using an external capacitor.
4. A precision ±5V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than one millivolt and a fine-trim is available for applications requiring exact symmetry between the +5V and −5V outputs.
5. Pin strapping capability allows configuration of a wide variety of outputs: ±5V, +5V & +10V, −5V & −10V dual outputs or +5V, −5V, +10V, −10V single outputs.

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# Complete 12-Bit A/D Converter with Programmable Gain

# AD368/AD369

## FEATURES

- Low Cost Data Acquisition Systems Including:
  - Programmable Gain Instrumentation Amplifier
  - Track-and-Hold Amplifier
  - 12-Bit A/D Converter
- Digitally Controlled Gains:
  - AD368 Gains = 1, 8, 64, 512
  - AD369 Gains = 1, 10, 100, 500
- 50kHz Throughput Rate
- Small Size: 28-Pin Hermetic Double DIP
- Guaranteed No Missing Codes Over Specified Temperature
- True 12-Bit Linear; Error ≤1/2LSB (B-Grade)
- Unipolar or Bipolar Operation
- MIL-STD–883B Screening Available

## APPLICATIONS

- Microprocessor Based Data Acquisition
- Wide Dynamic Range Measurement Systems
- Analytic and Medical Instruments
- Multichannel Systems With High/Low Level Signals

## PRODUCT DESCRIPTION

The AD368/AD369 are low cost, wide dynamic range data acquisition systems which condition and subsequently convert an analog signal into a 12-bit digital word. They include a programmable gain amplifier, a track-and-hold amplifier, and a 12-bit analog-to-digital converter – all in a 28-pin dual in-line package.

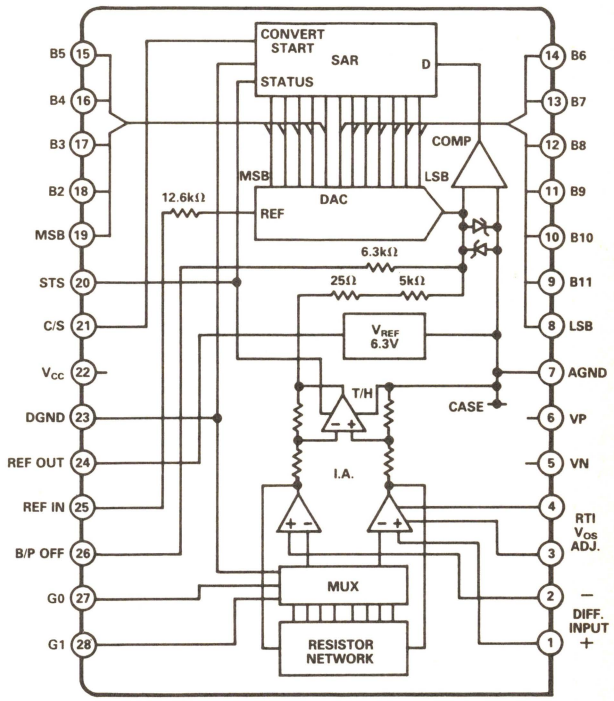
The digitally programmable-gain amplifier (PGA) of the AD368 enables the user to select binary-based gains of 1, 8, 64, and 512. These gain steps are especially useful in extending system dynamic range in DSP applications. The PGA of the AD369, with gains of 1, 10, 100, and 500, allows the user to choose full-scale input voltage ranges of 10V, 1V, 100mV, and 20mV, respectively. In addition, the precision differential input of the PGA provides the AD368/AD369 with excellent common-mode rejection.

The track-and-hold amplifier (T/H) features excellent linearity, low noise, and an internal hold capacitor.

The successive approximation analog-to-digital converter (ADC) features true 12-bit operation, with 0.012% max nonlinearity (B-grade). The user can select bipolar or unipolar operation to digitize both ac and dc input signals.

The AD368/AD369 provide a completely specified (industrial and military temperature ranges) and tested function in a space saving 28-pin hermetic package for system designers with cost, space, and time constraints.

AD368/AD369 FUNCTIONAL BLOCK DIAGRAM

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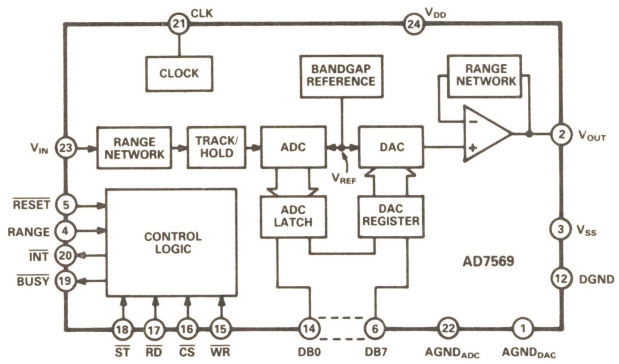
ANALOG DEVICES

# LC²MOS Complete, 8-Bit Analog I/O System

# AD7569

**FEATURES**
**2μs ADC with Track/Hold**
**1μs DAC with Output Amplifier**
**On-Chip Bandgap Reference**
**Fast Bus Interface**
**Single or Dual 5V Supplies**

AD7569 FUNCTIONAL BLOCK DIAGRAM




## GENERAL DESCRIPTION

The AD7569 is a complete, 8-bit, analog I/O system on a single monolithic chip. It contains a high-speed successive approximation ADC with 2μs conversion time, a track/hold with 200kHz bandwidth, a DAC and output buffer amplifier with 1μs settling time. A temperature-compensated 1.25V bandgap reference provides a precision reference voltage for the ADC and the DAC.

A choice of analog input/output ranges is available. Using a supply voltage of +5V, input and output ranges of zero to 1.25V and zero to 2.5 volts may be programmed using the RANGE input pin. Using a ±5V supply, bipolar ranges of ±1.25V or ±2.5V may be programmed.

Digital interfacing is via an 8-bit I/O port and standard microprocessor control lines. Bus interface timing is extremely fast, allowing easy connection to all popular 8-bit microprocessors. A separate start convert line controls the track/hold and ADC to give precise control of the sampling period.

The AD7569 is fabricated in Linear-Compatible CMOS ($LC^2MOS$), an advanced, mixed technology process combining precision bipolar circuits with low-power CMOS logic. The part is packaged in a 24-pin, 0.3″ wide "skinny" DIP and is also available in plastic leaded chip carrier (PLCC) and ceramic leadless chip carrier (LCCC).

## PRODUCT HIGHLIGHTS

1. Complete Analog I/O on a Single Chip.
   The AD7569 provides everything necessary to interface a microprocessor to the analog world. No external components or user trims are required, and the overall accuracy of the system is tightly specified, eliminating the need to calculate error budgets from individual component specifications.
2. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications the AD7569 is specified for AC parameters, including signal-to-noise ratio, distortion and input bandwidth.
3. Fast Microprocessor Interface.
   The AD7569 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 75ns and Write pulse width less than 80ns.
4. Low Power.
   Thanks to the combination of high-speed linear circuits with low-power CMOS logic, the AD7569 offers power consumption less than 60mW – considerably lower than any system of comparable performance.

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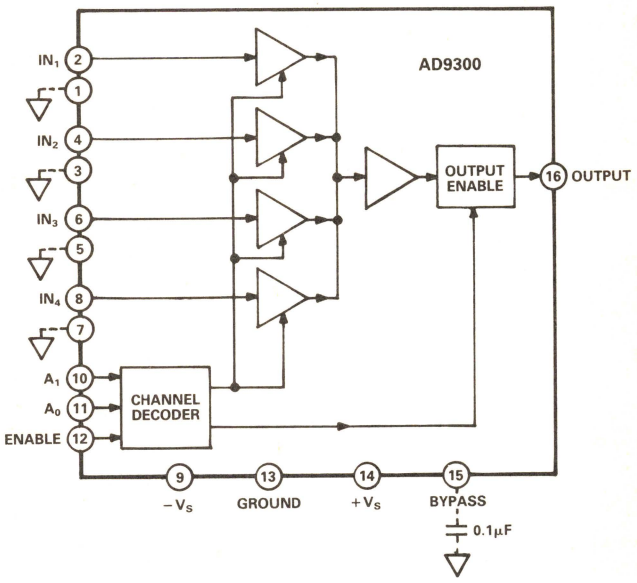
# 4 × 1 Wideband Video Multiplexer

# AD9300

**FEATURES**
- 140MHz Small-Signal Bandwidth
- 30MHz Large-Signal Bandwidth
- TTL Control Inputs
- 74dB Crosstalk Rejection @ 10MHz
- ±2V Input Range
- Operates on ±10V to ±15V Supplies

**AD9300 FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD9300 is a monolithic high-speed video signal multiplexer useable in a wide variety of applications.

Its four channels of video input signals can be randomly switched at megahertz rates to the single output. In addition, multiple devices can be configured in either parallel or cascade arrangements to form switch matrices. This flexibility in using the AD9300 is possible because the output of the device is in a high impedance state when the chip is not enabled; when the chip is enabled, the unit acts as a buffer with high input impedance and low output impedance.

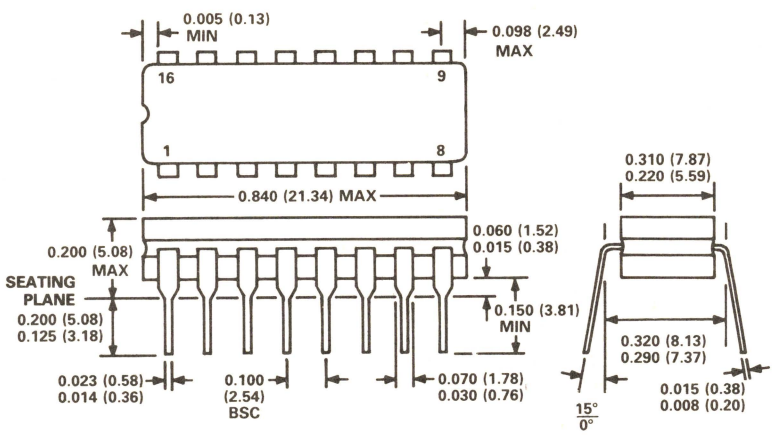
An advanced bipolar process used in the design provides fast, wideband switching capabilities while maintaining crosstalk rejection of 74dB at 10MHz. Full power bandwidth is a minimum 30MHz; this bandwidth remains constant whether the device is operated from ±10V or ±15V power, or some value between these extremes.

The AD9300JQ is packaged in a 16-pin ceramic DIP and is designed to operate over the commercial temperature range of 0 to +70°C. For extended temperatures of −55°C to +125°C, order part number AD9300SQ, which is also a 16-pin ceramic DIP.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**16-PIN CERAMIC DIP**

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# ANALOG DEVICES

# Precision Low-Power BiFET Op Amp

# AD548



## FEATURES

**DC Performance:**
- 200μA Max Quiescent Current
- 10pA Max Bias Current, Warmed Up (AD548C)
- 250μV Max Offset Voltage (AD548C)
- 2μV/°C Max Drift (AD548C)
- 2μV p-p Noise, 0.1 to 10Hz

**AC Performance:**
- 1.8 V/μs Slew Rate
- 1MHz Unity Gain Bandwidth

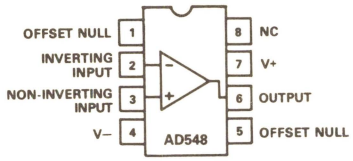
**Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages**

**MIL-STD-883B Parts Available**

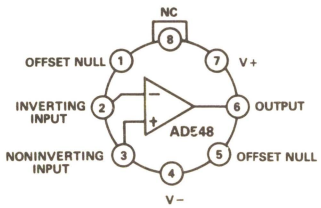
**Dual Version Available: AD648**

## AD548 CONNECTION DIAGRAMS

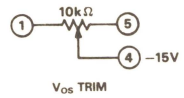
Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package




TO-99
(H) Package




NOTE: PIN 4 CONNECTED TO CASE




## PRODUCT DESCRIPTION

The AD548 is a low-power, precision monolithic operational amplifier. It offers both low bias current (10pA max, warmed up) and low quiescent current (200μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD548's entire common-mode voltage range.

The economical J grade has a maximum guaranteed input offset voltage of less than 2mV and an input offset voltage drift of less than 20μV/°C. The C grade reduces input offset voltage to less than 0.25mV and offset voltage drift to less than 2μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

The AD548 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD548's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD548 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0 to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of −40°C to +85°C. The AD548S and AD548T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available for parts specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD548 is available in an 8-pin plastic mini-DIP, cerdip, small outline or TO-99 metal can.

## PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high-performance, low-power applications.
2. The AD548 is pin compatible with industry standard op amps such as the LF441, TL061, and AD542, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2mV max) and drift (20μV/°C max) for the AD548J are achieved utilizing Analog Devices' laser drift trimming technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. A dual version, the AD648 is also available.

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# ANALOG DEVICES

# Monolithic Electrometer Operational Amplifier

# AD549*

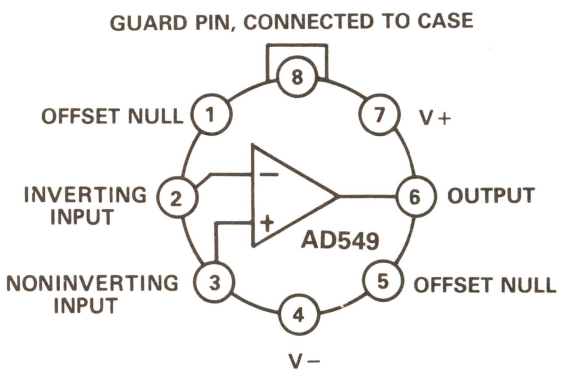
**FEATURES**

**Ultralow Bias Current: 60fA max (AD549L)**
**250fA max (AD549J)**
**Input Bias Current Guaranteed Over Common-Mode Voltage Range**
**Low Offset Voltage: 0.25mV max (AD549K)**
**1.00mV max (AD549J)**
**Low Offset Drift: 5μV/°C max (AD549K)**
**20μV/°C max (AD549J)**
**Low Power: 700μA max Supply Current**
**Low Input Voltage Noise: 4μV p-p 0.1 to 10Hz**
**MIL-STD-883B Parts Available**

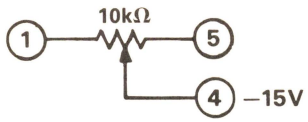
**APPLICATIONS**

**Electrometer Amplifiers**
**Photodiode Preamp**
**pH Electrode Buffer**
**Vacuum Ion Gage Measurement**

**AD549 CONNECTION DIAGRAM**




NOTE: PIN 4 CONNECTED TO CASE




$V_{OS}$ TRIM

## PRODUCT DESCRIPTION

The AD549 is a monolithic electrometer operational amplifier with very low input bias current. Input offset voltage and input offset voltage drift are laser trimmed for precision performance. The AD549's ultralow input current is achieved with "Topgate" JFET technology, a process development exclusive to Analog Devices. This technology allows the fabrication of extremely low input current JFETs compatible with a standard junction-isolated bipolar process. The $10^{15}\Omega$ common-mode impedance, a result of the bootstrapped input stage, insures that the input current is essentially independent of common-mode voltage.

The AD549 is suited for applications requiring very low input current and low input offset voltage. It excels as a preamp for a wide variety of current output transducers such as photodiodes, photomultiplier tubes, or oxygen sensors. The AD549 can also be used as a precision integrator or low droop sample and hold. The AD549 is pin compatible with standard FET and electrometer op amps, allowing designers to upgrade the performance of present systems at little additional cost.

The AD549 is available in a TO-99 hermetic package. The case is connected to Pin 8 so that the metal case can be independently connected to a point at the same potential as the input terminals, minimizing stray leakage to the case.

***Covered by Patent No. 4,639,683.**

The AD549 is available in four performance grades. The J, K, and L versions are rated over the commercial temperature range −0 to +70°C. The S grade is specified over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C. Extended reliability PLUS screening is also available. PLUS screening includes 168-hour burn in, as well as other environmental and physical tests derived from MIL-STD-883B, Rev C.

## PRODUCT HIGHLIGHTS

1. The AD549's input currents are specified, 100% tested and guaranteed after the device is warmed up. Input current is guaranteed over the entire common-mode input voltage range.
2. The AD549's input offset voltage and drift are laser trimmed to 0.25mV and 5μV/°C (AD549K), 1mV and 20μV/°C (AD549J).
3. A maximum quiescent supply current of 700μA minimizes heating effects on input current and offset voltage.
4. AC specifications include 1MHz unity gain bandwidth and 3V/μs slew rate. Settling time for a 10V input step is 5μs to 0.01%.
5. The AD549 is an improved replacement for the AD515, OPA104, and 3528.



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# Super OP-07
# Ultralow Offset Voltage Op Amp
# AD707

Analog Devices

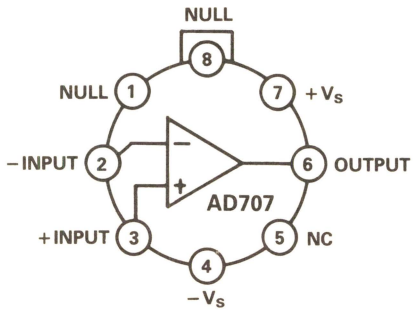
**FEATURES**

**Next Generation of the OP-07**
**Very High dc Precision**
**15μV max Offset Voltage**
**0.1μV/°C max Offset Voltage Drift**
**0.35μV p-p max Voltage Noise (0.1Hz to 10Hz)**
**Eight Million V/V min Open-Loop Gain**
**130dB min CMRR**
**120dB min PSRR**

**AC Performance**
**0.3V/μs Slew Rate**
**0.9MHz Closed-Loop Bandwidth**
**Improved Replacement for the OP-77**
**Competitively Priced to the OP-07**
**Available in 8-Pin Plastic Mini-DIPs, Small Outline, Hermetic Cerdip or Hermetic TO-99 Metal Can Packages**

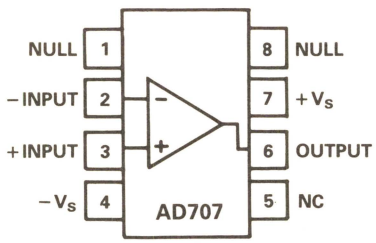
**AD707 CONNECTION DIAGRAMS**

**TO-99**
**(H) Package**




TOP VIEW

**Plastic Mini-DIP (N) Package**
**and**
**Cerdip (Q) Package**




TOP VIEW

**PRODUCT DESCRIPTION**

The AD707 is a precision, low offset voltage and low offset voltage drift, monolithic operational amplifier. *All dc characteristics are improved over the industry standard OP-07.* Most importantly, the best grade AD707's offset voltage drift of 0.1μV/°C and offset voltage of 15μV are the best available for any bipolar monolithic op amp. All important dc specifications show excellent stability over temperature. Offset current drift is typically 1pA/°C, and input bias current drift is 25pA/°C max.

The AD707 sets a new standard for low cost precision op amps by providing 8V/μV min open-loop gain and guaranteed maximum input voltage noise of 350nV p-p. Input bias current is 1.0nA max guaranteed. Both CMRR and PSRR are an order of magnitude improved over the best grade OP-07 at 130dB and 120dB, respectively.

The AD707 is available in eight performance grades. The AD707J, AD707K and AD707L are rated over the commercial temperature range of 0 to +70°C. The AD707A, AD707B and AD707C are rated over the industrial temperature range of −40°C to +85°C. The AD707S and AD707T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C. Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges.

**APPLICATION HIGHLIGHTS**

1. The AD707's 13V/μV typical open-loop gain and 140dB common-mode rejection make it ideal for precision instrumentation applications.
2. With the AD707 tighter error budgets are possible without a substantial increase in cost over previous designs.
3. The low offset voltage drift and noise of the AD707 allows the designer to amplify very small signals without sacrificing overall system preformance.
4. Unmounted chips are available for hybrid circuit applications.
5. The AD707 is an improved replacement for the OP-07, OP-77 and the LT1001.

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# Precision Low-Cost High-Speed BiFET Op Amp

# AD711

**FEATURES**

**AC PERFORMANCE:**
- **Settles to ±0.01% in 1μs**
- **16V/μs min Slew Rate (AD711J)**
- **3MHz min Unity Gain Bandwidth (AD711J)**

**DC PERFORMANCE:**
- **0.25mV max Offset Voltage: (AD711C)**
- **3μV/°C max Drift: (AD711C)**
- **200V/mV min Open-Loop Gain (AD711K)**
- **4μV p-p max Noise, 0.1Hz to 10Hz (AD711C)**

**Available In Plastic, Hermetic Cerdip, and Hermetic Metal Can Packages**

**MIL-STD-883B Parts Available**

**Dual Version Available: AD712**

## PRODUCT DESCRIPTION

The AD711 is a high-speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD711 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD711 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

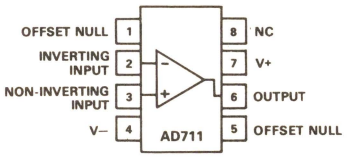
The AD711 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD711J and AD711K are rated over the commercial temperature range of 0 to +70°C. The AD711A, AD711B and AD711C are rated over the industrial temperature range of −40°C to +85°C. The AD711S and AD711T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

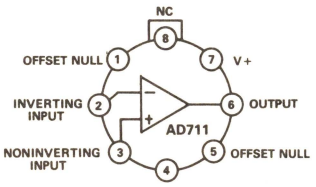
The AD711 is available in an 8-pin plastic mini-DIP, cerdip, small outline or TO-99 metal can.

## AD711 CONNECTION DIAGRAMS

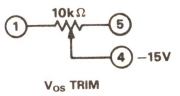
**Plastic Mini-DIP (N) Package and Cerdip (Q) Package**




**TO-99 (H) Package**




NOTE: PIN 4 CONNECTED TO CASE




## PRODUCT HIGHLIGHTS

1. The AD711 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.25mV max, C grade, 2mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 3μV/°C max on the AD711C.
3. Along with precision dc performance, the AD711 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD711 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1 to 10Hz (AD711C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 25pA max (AD711C) and an input offset current of 10pA max (AD711C). Both input bias current and input offset current are guaranteed in the warmed-up condition.

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# Precision, 500ns Settling BiFET Op Amp

# AD744

## FEATURES

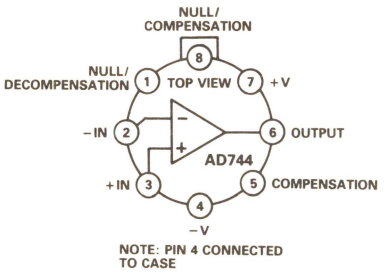
**AC PERFORMANCE**
- 500ns Settling to 0.01% for 10V Step
- 1.5μs Settling to 0.0025% for 10V Step
- 75V/μs Slew Rate
- 0.0003% Total Harmonic Distortion (THD)
- 13MHz Gain Bandwidth – Internal Compensation
- >200MHz Gain Bandwidth (G = 1000) External Decompensation
- >1000pF Capacitive Load Drive Capability with 10V/μs Slew Rate – External Compensation

**DC PERFORMANCE**
- 0.25mV max Offset Voltage (AD744C)
- 3μV/°C max Drift (AD744C)
- 250V/mV min Open-Loop Gain (AD744B)
- 4μV p-p max Noise, 0.1Hz to 10Hz (AD744C)
- Available in Plastic Mini-DIP, Hermetic Cerdip and Hermetic Metal Can Packages
- MIL-STD-883B Processing Available

**APPLICATIONS**
- Output Buffers for 12-Bit, 14-Bit and 16-Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters

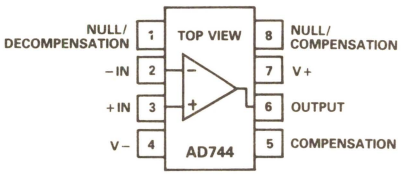
## AD744 CONNECTION DIAGRAMS

**TO-99**
**(H) Package**




NOTE: PIN 4 CONNECTED TO CASE

**Plastic Mini-DIP (N) Package**
**and**
**Cerdip (Q) Package**




## PRODUCT DESCRIPTION

The AD744 is a fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD744 also offers the option of using custom compensation to achieve exceptional capacitive load drive capability.

The single-pole response of the AD744 provides fast settling: 500ns to 0.01%. This feature combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD744's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

The AD744 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater. External compensation may be applied to the AD744 for stable operation as a unity gain follower. External compensation also allows the AD744 to drive 1000pF capacitive loads, slewing at 10V/μs with full stability. Alternatively, external decompensation may be used to increase the gain bandwidth of the AD744 to over 200MHz at high gains. This makes the AD744 ideal for use as ac preamps in digital signal processing (DSP) front ends.

The AD744 is available in seven performance grades. The AD744J and AD744K are rated over the commercial temperature range of 0 to +70°C. The AD744A, AD744B and AD744C are rated over the industrial temperature range of −40°C to +85°C. The AD744S and AD744T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes a 168-hour burn-in, as well as other environmental and physical tests.

The AD744 is available in an 8-pin plastic mini-DIP, 8-pin cerdip, or TO-99 metal can.

## PRODUCT HIGHLIGHTS

1. The AD744 is a high-speed BiFET op amp that offers excellent performance at competitive prices. It outperforms the OP42, OPA606, LF356 and LF400.
2. The AD744 offers exceptional dynamic response. It settles to 0.01% in 500ns and has a 100% tested minimum slew rate of 50V/μs (AD744B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.
4. The AD744 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1Hz to 10Hz (AD744C).

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# ANALOG DEVICES

# Wideband, Fast Settling Op Amp

# AD840

**FEATURES**
**AC PERFORMANCE**
**Gain-Bandwidth Product: 400MHz (Gain = 10)**
**Fast Settling: 110ns to 0.01%**
**Slew Rate: 400V/μs**
**Stable at Gains of 10 or Greater**
**Full Power Bandwidth: 6MHz**

**DC PERFORMANCE**
**Input Offset Voltage: 0.5mV max**
**Input Offset Drift: 5μV/°C max**
**Input Voltage Noise: 3nV/$\sqrt{Hz}$**
**Open-Loop Gain: 50V/mV min with 1kΩ Load**
**Output Current: 50mA min**
**Supply Current: 12mA max**

**APPLICATIONS:**
**Line Drivers**
**DAC and ADC Buffers**
**Video and Pulse Amplifiers**
**Available in Plastic DIP and Hermetic Cerdip Packages**
**MIL-STD-883B Parts Available**

## PRODUCT DESCRIPTION

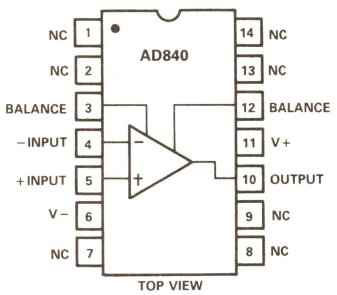
The AD840 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD841, which is unity-gain stable and the AD842, which is stable at a gain of two or greater and has 100mA output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 400MHz gain-bandwidth product, the AD840 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 110ns for a 10 volt step.

The AD840 remains stable over its full operating temperature range. It also offers a low quiescent current of 12mA, a minimum output current drive capablity of 35mA, a low input voltage noise of 3nV/$\sqrt{Hz}$, and a low input offset voltage of less than 0.5mV.

The 400V/μs slew rate of the AD840, along with its 400MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high-frequency signal conditioning circuits and high-bandwidth active filters. The extremely rapid settling time of the AD840 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD840 is also appropriate for other applications such as high-speed DAC and ADC buffer amplifiers and other wide-bandwidth circuitry.

**AD840 CONNECTION DIAGRAM**

**Plastic DIP (N) Package**
**and**
**Cerdip (Q) Package**




The AD840 is available specified to operate over either the commercial (AD840J/K) or military (AD840S) temperature range. The commercial version is available in either 14-pin plastic DIP (N) or hermetic cerdip (Q) packages. The military version is offered in hermetic cerdip (Q). Military versions are available processed to MIL-STD-883B Rev C.

## APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD840 make it ideal for DAC and ADC buffers, line drivers, and all types of video instrumentation circuitry.
2. Full differential inputs provide outstanding performance in all standard high-frequency op amp applications where circuit gain will be 10 or greater.
3. Laser-wafer trimming reduces the input offset voltage to 0.5mV max on the K grade, thus eliminating the need for external offset nulling in many applications.
4. The AD840 does not require external compensation at closed-loop gains of 10 or greater.
5. The AD840 is an enhanced replacement for the HA2540.



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# Wideband, Unity-Gain Stable, Fast Settling Op Amp

# AD841

**FEATURES**
**AC PERFORMANCE:**
**Unity-Gain-Bandwidth Product: 40MHz**
**Fast Settling: 110ns to 0.01%**
**Slew Rate: 300V/μs**
**Stable at Gains of 1 or Greater**
**Full Power Bandwidth: 4.7MHz**

**DC PERFORMANCE**
**Input Offset Voltage: 1mV max**
**Input Offset Drift: 20μV/°C max**
**Input Voltage Noise: 13nV/$\sqrt{Hz}$**
**Open-Loop Gain: 25V/mV into a 500Ω Load**
**Output Current: 50mA min**
**Supply Current: 12mA max**

**APPLICATIONS**
**Video and Pulse Amplifiers**
**Active Filters**
**High-Frequency Signal Conditioning Circuitry**
**Available in Plastic DIP, Hermetic Metal Can and Hermetic Cerdip Packages**
**MIL-STD-883B Parts Available**

## PRODUCT DESCRIPTION

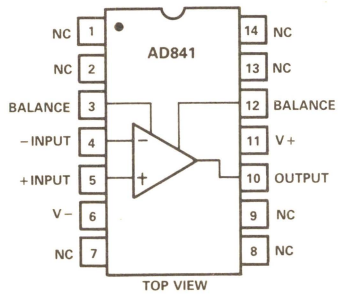
The AD841 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840, which is stable at a gain of 10 or greater, and the AD842, which is stable at a gain of two or greater and has 100mA output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to 40MHz unity-gain bandwidth, the AD841 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 110ns for a 10 volt step.

The AD841 is remarkably easy to use: it only requires two 0.01μF decoupling capacitors, one for each power supply line. External compensation is *not* required. It remains stable over its full operating temperature range. The AD841 also offers a low quiesent current (12mA), high output current drive capablity (35mA), low input voltage noise (13nV/$\sqrt{Hz}$), and low input offset voltage (1mV).

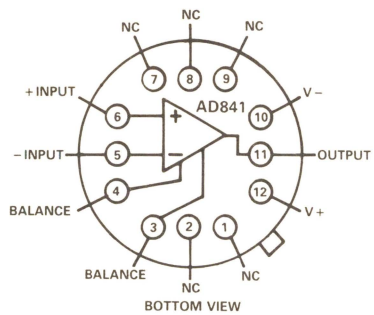
The 300V/μs slew rate of the AD841, along with its 40MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high-frequency signal conditioning circuits and high-bandwidth active filters. The extremely rapid settling time of the AD841 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD841 is also appropriate for other applications such as high-speed integrators and sample and hold circuitry.

## AD841 CONNECTION DIAGRAMS

**Plastic DIP (N) Package and Cerdip (Q) Package**




**TO-8 (H) Package**




The AD841 is available specified to operate over either the commercial (AD841J/K) or military (AD841S) temperature range. The commercial versions are offered in either the 14-pin plastic DIP (N) or cerdip (Q) or 12-pin hermetic can (H) packages. The military version is available in either the 14-pin cerdip (Q) or 12-pin hermetic can (H) packages. Military versions are available processed to MIL-STD-883B Rev C.

## APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD841 make it ideal for D/A, A/D, sample-and-hold amplifiers, high-speed integrators, and video instrumentation circuitry.
2. Full differential inputs provide outstanding performance in all standard high-frequency op amp applications such as signal conditioning and active filters.
3. Laser wafer trimming reduces the input offset voltage to 2mV max, thus eliminating the need for external offset nulling in many applications.
4. The AD841 does not require external compensation at closed-loop gains of 1 or greater.
5. The AD841 is an enhanced replacement for the HA2541.

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# Wideband, High Output Current, Fast Settling Op Amp

# AD842

## FEATURES

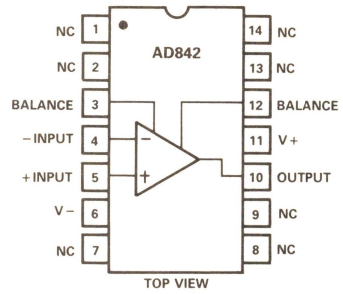
**AC PERFORMANCE**
- Gain-Bandwidth Product: 80MHz (Gain = 2)
- Fast Settling: 110ns to 0.01%
- Slew Rate: 375V/μs
- Stable at Gains of 2 or Greater
- Full Power Bandwidth: 4.7MHz

**DC PERFORMANCE**
- Input Offset Voltage: 1mV max
- Input Offset Drift: 10μV/°C max
- Input Voltage Noise: 9nV/√Hz typ
- Open-Loop Gain: 50V/mV min with 500Ω Load
- Output Current: 100mA min
- Quiesent Supply Current: 13mA max

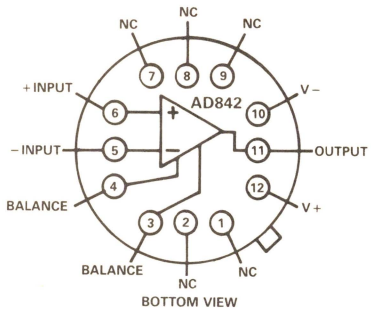
**APPLICATIONS**
- Line Drivers
- DAC and ADC Buffers
- Video and Pulse Amplifiers
- Available in Plastic DIP, Hermetic Metal Can and Hermetic Cerdip Packages
- MIL-STD-883B Parts Available.

## AD842 CONNECTION DIAGRAMS

**Plastic DIP (N) Package and Cerdip (Q) Package**




**TO-8 (H) Package**




## PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater, and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80MHz gain-bandwidth, the AD842 offers extremely fast settling,,characteristics, typically settling to within 0.01% of final value in less than 110ns for a 10 volt step.

The AD842 also offers a low quiesent current of 13mA, a high output current drive capablity (100mA min), a low input voltage noise of 9nV/√Hz, and a low input offset voltage (1mV).

The 375V/μs slew rate of the AD842, along with its 80MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high-frequency signal conditioning circuits and high-bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high-speed DAC and ADC buffer amplifiers and other wide-bandwidth circuitry.

The AD842 is available specified to operate over either the commercial (AD842J/K) or military (AD842S) temperature range. Both of the commercial versions are offered in 14-pin plastic DIP (N) or hermetic cerdip (Q) or 12-pin hermetic metal can (H) packages. The military version is available in either the 14-pin cerdip (Q) or 12-pin hermetic can (H) packages. Military versions are available processed to MIL-STD-883B Rev C.

## APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffer amplifiers, line drivers, and all types of video instrumentation circuitry.
2. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
3. Laser-wafer trimming reduces the input offset voltage to 1mV max, thus eliminating the need for external offset nulling in many applications.
4. The AD842 does not require external compensation at closed-loop gains of 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

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Analog Devices

# ANALOG DEVICES

# Very High-Speed, Operational Amplifier

# AD846

## FEATURES

**AC PERFORMANCE:**
- Small Signal Bandwidth: 46MHz ($A_V = -1$)
- Slew Rate: 450V/μs
- Full Power Bandwidth: 6.8MHz at 20V p-p, R1 = 500Ω
- Fast Settling: for 10V Step, 110ns to 0.01%, 80ns to 0.1%
- Differential Gain: <0.1%
- Differential Phase: <0.1°
- Total Harmonic Distortion (THD): 0.0002% @ 100kHz
- Open-Loop Transimpedance: 500MΩ

**DC PERFORMANCE**
- Input Offset Voltage: 75μV max (K Grade)
- Input Offset Drift: 20μV/°C max (K Grade)
- Input Voltage Noise: 2nV/$\sqrt{Hz}$
- Output Current: 50mA min
- Quiescent Supply Current: 6mA

**APPLICATIONS**
- High-Speed DAC Buffers
- Multiflash ADC Error Amplifiers
- Flash ADC Buffers
- Coaxial Cable Drivers
- High Performance Audio Circuitry
- Available in Plastic Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages
- MIL-STD-883B Parts Available

## PRODUCT DESCRIPTION

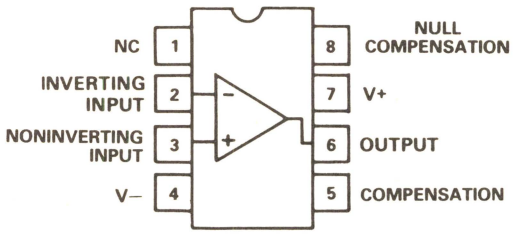
The AD846 is a monolithic, very high-speed operational amplifier offering high performance. Although technically classed as a transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.1%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high-speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog-to-digital converters.

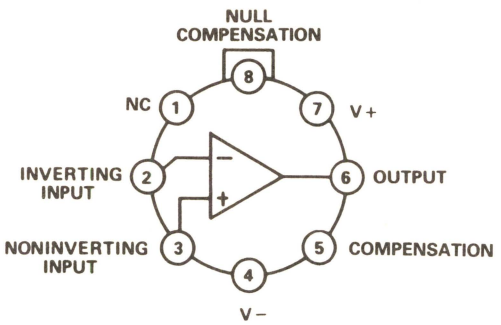
Other advantages include: low input errors and high open-loop transresistance (500MΩ) into a 500Ω load, insuring true 12-bit dc accuracy for closed-loop gains from −1 gains greater than −10. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high-speed DACs and flash ADCs.

## AD846 CONNECTION DIAGRAMS

Plastic DIP (N) Package
and
Cerdip (Q) Package




(H) Package




NOTE: PIN 4 CONNECTED TO CASE

The AD846 is available in three performance grades. The AD846J and AD846K are rated over the commercial temperature range of 0 to +70°C. The AD846S is rated over the full military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

## APPLICATION HIGHLIGHTS

1. The AD846 achieves settling times of 110ns to 0.01% for gains of −1 to −10 with a 450V/μs slew rate, while consuming only 5mA of supply current.
2. For closed loop gains of −1 to −100, the high-speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

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ANALOG DEVICES

# Ultrahigh-Frequency Operational Amplifier

# AD5539

## FEATURES

**Improved Replacement for Signetics SE/NE5539**

**AC PERFORMANCE**

- Gain Bandwidth Product: 1.4GHz typical
- Unity Gain Bandwidth: 220MHz typical
- High Slew Rate: 600V/μs typical
- Full Power Response: 82MHz typical
- Open-Loop Gain: 47dB min, 52dB typical

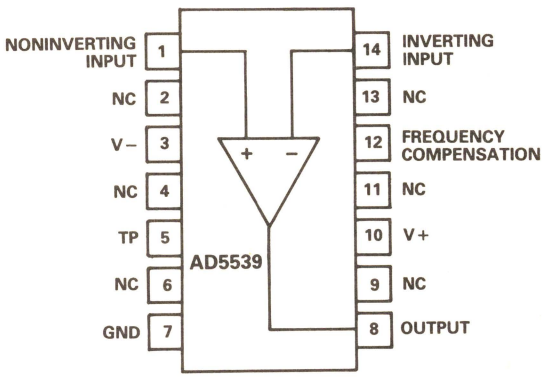
**DC PERFORMANCE**

- All Guaranteed DC Specifications Are 100% Tested For Each Device Over Its Full Temperature Range – For All Grades and Packages
- $V_{OS}$: 5mV max Over Full Temperature Range (AD5539J)
- $I_B$: 20μA max (AD5539J)
- CMRR: 70dB min, 85dB typical
- PSRR: 100μV/V typical
- MIL-STD-883B Parts Available

## AD5539 CONNECTION DIAGRAM

**Plastic DIP (N) Package**
**or**
**Cerdip (Q) Package**

**Top View**




## PRODUCT DESCRIPTION

The AD5539 is an ultrahigh-frequency operational amplifier designed specifically for use in video circuits and RF amplifiers. Requiring no external compensation for gains greater than 5, it may be operated at lower gains with the addition of external compensation.

As a superior replacement for the Signetics NE/SE5539, each AD5539 is 100% dc tested to meet all of its guaranteed dc specifications over the full temperature range of the device.

The high slew rate and wide bandwidth of the AD5539 provide low-cost solutions to many otherwise complex and expensive high-frequency circuit design problems.

The AD5539 is available specified to operate over either the commercial (AD5539JN/JQ) or military (AD5539SQ) temperature range. The commercial grade is available either in 14-pin plastic or cerdip packages. The military version is supplied in the cerdip package.

## PRODUCT HIGHLIGHTS

1. All guaranteed dc specifications are 100% tested.
2. The AD5539 drives 50Ω and 75Ω loads directly.
3. Input voltage noise is less than $4nV\sqrt{Hz}$.
4. Low-cost RF and Video speed performance.
5. ±2 volt output range into a 150Ω load.
6. Low cost.

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# Wide-Bandwidth, Fast-Settling Operational Amplifier

# AD9610

**FEATURES**
**Ultrastable Unity Gain Bandwidth (100MHz)**
**18ns Settling Time to 0.1%**
**Superior dc Performance**
**Offset Voltage ±0.3mV**
**Bias Current 2μA**
**21mA Supply Current**
**Overdrive Insensitive**

## PRODUCT DESCRIPTION

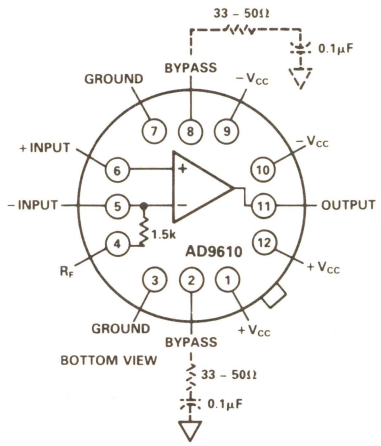
The AD9610 is a fast-settling, wide-bandwidth dc-coupled transimpedance operational amplifier which combines superior dc specifications and exceptional dynamic performance.

Thin-film technology and innovative design techniques help assure stable operation over the complete operating temperature range. Input offset voltage temperature drift is typically 5μV/°C; input bias current drift is typically 70nA/°C.

The AD9610 is inherently stable over its complete gain range and has wide bandwidth at all gain settings. With G = −1, 3dB bandwidth is 100MHz; with G = −2, bandwidth is 95MHz; with G = −20, 3dB bandwidth is 75MHz. Slew rate; rise, fall, and settling times are all independent of gain.

The design of the AD9610 makes it easy to apply. The unit is internally compensated and, under ordinary circumstances, needs no external compensation. An internal 1.5kΩ feedback resistor is available to the user by connecting Pin 4 to output Pin 11. Pins 2 and 8 are bypass pins and should be connected to ground through 33Ω-50Ω resistors and 0.1μF ceramic capacitors; effective decoupling of the power supplies is also important.

## AD9610 FUNCTIONAL BLOCK DIAGRAM

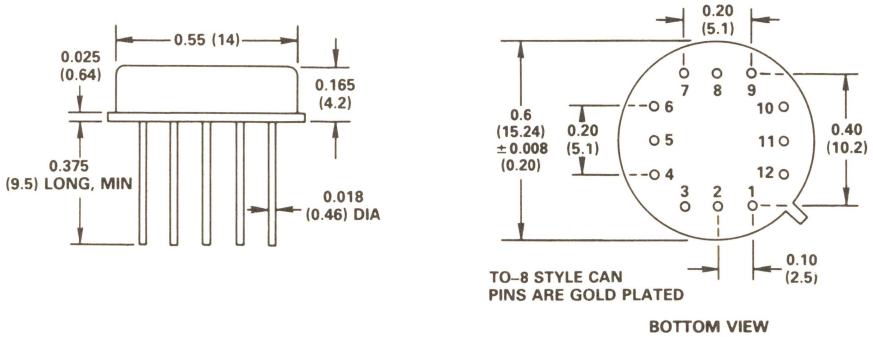



Another valuable feature of the AD9610 is the character of its recovery from overdrive upsets; this is very important in nonideal circuit environments. When the overdrive is relieved, the unit comes out of its saturation shutdown mode without damage or performance degradation.

Two temperature ranges are available. The AD9610BH is guaranteed over a case temperature range of −25°C to +85°C; the AD9610TH is for a range of −55°C to +125°C. Standard devices are produced in a MIL-STD-1772- certified facility; contact the factory for information on units screened to MIL-STD-883.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

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# Wide-Bandwidth, Fast-Settling Operational Amplifier

# AD9611

**FEATURES**
**Unity Gain Stable**
**Small-Signal Bandwidth 280MHz**
**Full Power Bandwidth 220MHz**
**Settling Time 13ns to 0.1%**
**Rise/Fall Times 1.3ns/1.45ns**
**Offset Voltage ±0.5mV**
**Bias Current ±1μA**
**Power Dissipation Independent of Load**

## PRODUCT DESCRIPTION

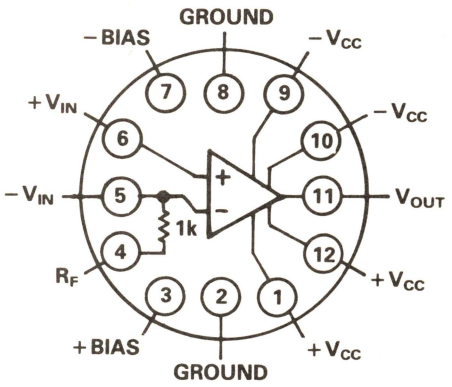
The AD9611 is an ultrafast-settling, wide-bandwidth, dc-coupled operational amplifier that combines exceptional ac and dc specifications to establish a new standard of excellence in dc-coupled amplifiers.

Rise and fall times are 1.3ns and 1.45ns, respectively. The −3dB bandwidth is 280MHz (G= −5); the full-power (3V p-p) bandwidth is 220MHz. The AD9611 settles to 0.1% in 13ns; and dc performance is also exceptional. Offset voltage is ±0.5mV and drifts only 5μV/°C. The inverting and non-inverting bias currents are 1μA.

The AD9611 requires ±5V power supplies and employs an innovative current-steering output stage that keeps the total circuit power dissipation essentially constant regardless of output drive (for loads ≤100Ω). *Circuit power dissipation does not increase as the load is increased*; the unit can be operated up to +110°C in still air without heat sinking.

Current feedback is used instead of voltage feedback to provide dynamic performance that is relatively independent of gain settings. Flat gain and phase response combine with excellent noise and distortion performance to provide a unity-gain-stable amplifier especially well suited for use in digital communication systems. The AD9611 is an excellent choice for driving the newest generation of ultrahigh-speed flash converters when system SNR and effective number of bits are important.

**AD9611 FUNCTIONAL BLOCK DIAGRAM**



BOTTOM VIEW

Harmonic distortion and noise performance are outstanding. At 60MHz input and $V_{OUT}$ = 2V p-p, second harmonics are typically 56dB down and are guaranteed to be greater than 50dB. Third harmonics are 58dB typical and 52dB minimum. Noise voltage and noise current are guaranteed ≤2.1nV/√Hz and ≤20pA/√Hz, respectively, in a frequency range of 5MHz to 280MHz.

The AD9611 is constructed with discrete transistors on a precision thin-film substrate. The AD9611BH is rated for case temperatures from −25°C to +85°C; the AD9611TH is guaranteed from −55°C to +125°C. Contact the factory for information about 883-grade parts. All units are built and tested in a MIL-STD-1772-certified facility.

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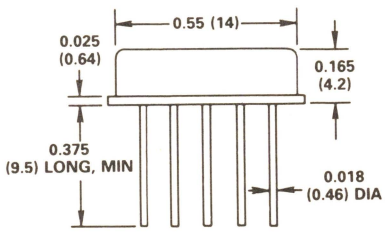
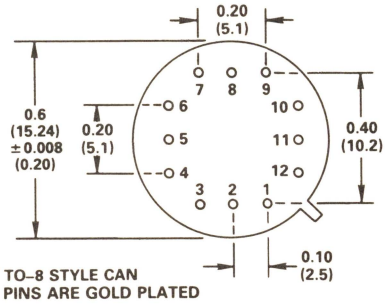
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



BOTTOM VIEW

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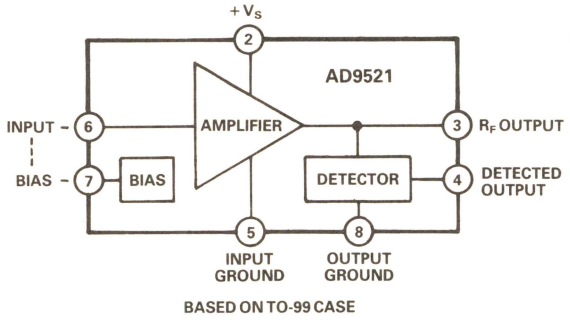
# 25MHz Wideband Logarithmic Amplifier

# AD9521

**FEATURES**
**250MHz Bandwidth**
**Monolithic Construction**
**<5dB Noise Figure**
**Excellent Detected Output Matching**
**Direct Replacement for SL521/SL1521**

**AD9521 FUNCTIONAL BLOCK DIAGRAM**



BASED ON TO-99 CASE

## PRODUCT DESCRIPTION

The AD9521 is a monolithic wideband amplifier with a logarithmic detected output which is pin compatible with the SL521 and SL1521. Minimum gain variation from 10MHz to 250MHz is assured by the high-performance bipolar process used in the design of the unit.

Its high gain tolerance of ±1.5dB remains constant over the full performance range of the device. This characteristic has the added benefit of close matching of detected output currents from one device to another. When combined with a 4dB noise figure, that matching makes it possible to construct LOG strips with 80dB-90dB of dynamic range and linearity better than ±1dB.

Two gain tolerances and two temperature ranges are available in the total of six models of the AD9521. Industrial temperature range devices are packaged in 8-pin TO-99 cans; extended temperature devices are available in TO-99 packages or 20-pin LCC format.

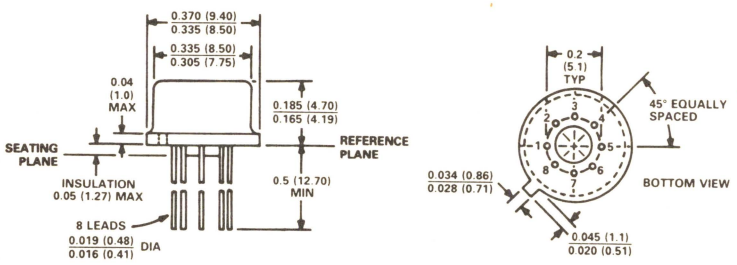
## ORDERING INFORMATION

| Device | Detected Output Matching | Temperature Range | Package |
|---|---|---|---|
| AD9521JH | 0.2mA | −25°C to +85°C | 8-Pin TO-99 |
| AD9521KH | 0.1mA | −25°C to +85°C | 8-Pin TO-99 |
| AD9521SE | 0.2mA | −55°C to +125°C | 20-Pin LCC |
| AD9521SH | 0.2mA | −55°C to +125°C | 8-Pin TO-99 |
| AD9521TE | 0.1mA | −55°C to +125°C | 20-Pin LCC |
| AD9521TH | 0.1mA | −55°C to +125°C | 8-Pin TO-99 |

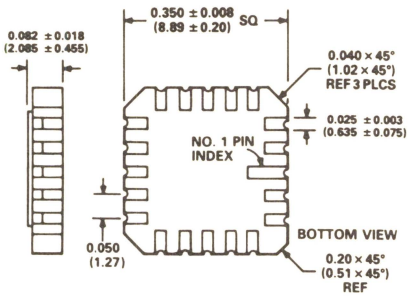
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**8-Pin Can**




**20-Pin LCC**

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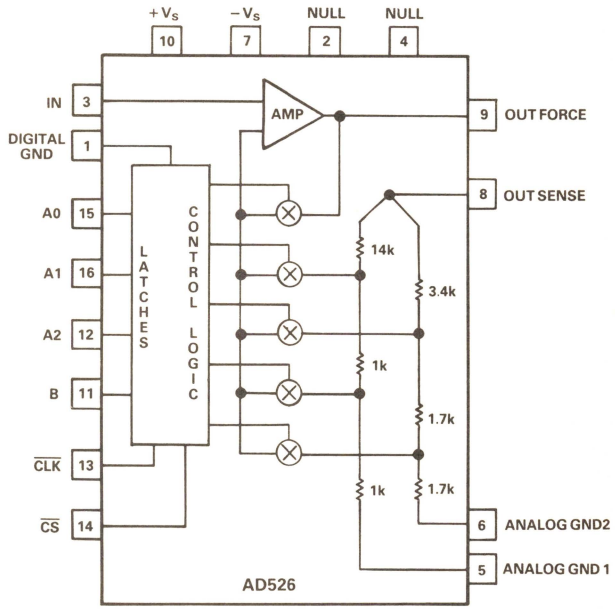
# Software Programmable Gain Amplifier

# AD526

## FEATURES

- Digitally Programmable Binary Gains from 1 to 16
- Two-Chip Cascade Mode Achieves Binary Gain from 1 to 128 with No Additional Components
- Gain Error:
  - 0.01% max, Gain = 1, 2, 4 (C Grade)
  - 0.02% max, Gain = 8, 16 (C Grade)
- Fast Settling Time
  - 10V Signal Change:
    - 0.01% in 4.5μs (Gain = 16)
  - Gain Change:
    - 0.01% in 5.6μs (Gain = 16)
- Low Nonlinearity: ±0.005% FSR max (A Grade)
- Excellent dc Accuracy:
  - Offset Voltage: 0.7mV max (A Grade)
  - Max Offset Voltage Over Temperature
    - 0.4mV (C Grade)
- TTL Compatible Digital Inputs

## AD526 FUNCTIONAL BLOCK DIAGRAM




## PRODUCT DESCRIPTION

The AD526 is a single-ended, monolithic software programmable gain amplifier (SPGA) that provides gains of 1, 2, 4, 8 and 16. It is complete, including amplifier, resistor network and TTL-compatible latched inputs, and requires no external components.

Low gain error and low nonlinearity make the AD526 ideal for precision instrumentation applications requiring programmable gain. The small signal bandwidth is 350kHz at a gain of 16. In addition, the AD526 provides excellent dc precision. The FET-input stage results in a low bias current of 50pA. A guaranteed maximum input offset voltage of 0.25mV max (C grade) and low gain error (0.01%, G=1, 2, 4, C grade) are accomplished using Analog Devices' laser trimming technology.

To provide flexibility to the system designer, the AD526 can be operated in either latched or transparent mode. The force/sense configuration preserves accuracy when the output is connected to remote or low impedance loads.

The AD526 is offered in three industrial grades, A, B and C, which are specified from −40°C to +85°C. The S grade is specified from −55°C to +125°C. The military version is available processed to MID-STD 883B, Rev C. All versions are supplied in a 16-pin hermetic side-brazed ceramic DIP.

## APPLICATION HIGHLIGHTS

1. **Dynamic Range Extension for ADC Systems:** A single AD526 in conjunction with a 12-bit ADC can provide 96dB of dynamic range for ADC systems.
2. **Gain Ranging Pre-Amps:** The AD526 offers complete digital gain control with precise gains in binary steps from 1 to 16. Additional gains of 32, 64 and 128 are possible by cascading two AD526s with *no additional components*.

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# ANALOG DEVICES

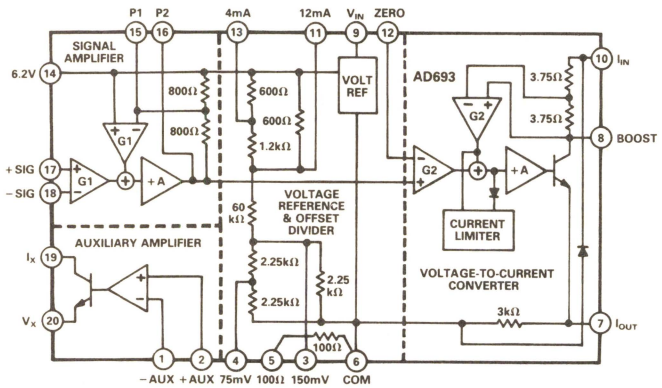
# Loop-Powered 4-20mA Sensor Transmitter

# AD693

## FEATURES

**Instrumentation Amplifier Front End**
**Loop-Powered Operation**
**Precalibrated 30mV or 60mV Input Spans**
**Independently Adjustable Output Span and Zero**
**Precalibrated Output Spans: 4-20mA Unipolar**
**0-20mA Unipolar**
**12 ± 8mA Bipolar**
**Precalibrated 100Ω RTD Interface**
**6.2V Reference with Up to 3.5mA of Current Available**
**Uncommitted Auxiliary Amp for Extra Flexibility**
**Optional External Pass Transistor to Reduce Self-Heating Errors**

## AD693 FUNCTIONAL BLOCK DIAGRAM




## PRODUCT DESCRIPTION

The AD693 is a monolithic signal conditioning circuit which accepts low-level inputs from a variety of transducers to control a standard 4-20mA, two-wire current loop. An on-chip voltage reference and auxiliary amplifier are provided for transducer excitation; up to 3.5mA of excitation current is available when the device is operated in the loop-powered mode. Alternatively, the device may be locally powered for three-wire applications when 0-20mA operation is desired.

Precalibrated 30mV and 60mV input spans may be set by simple pin strapping. Other spans from 1mV to 100mV may be realized with the addition of external resistors. The auxiliary amplifier may be used in combination with on-chip voltages to provide six precalibrated ranges for 100Ω RTDs. Output span and zero are also determined by pin strapping to obtain the standard ranges: 4-20mA, 12 ± 8mA and 0-20mA.

Active laser trimming of the AD693's thin-film resistors result in high levels of accuracy without the need for additional adjustments and calibration. Total unadjusted error is tested on every device to be less than 0.5% of full scale at +25°C, and less than 0.75% over the industrial temperature range. Residual nonlinearity is under 0.05%. The AD693 also allows for the use of an external pass transistor to further reduce errors caused by self-heating.

For transmission of low-level signals from RTDs, bridges and pressure transducers, the AD693 offers a cost-effective signal conditioning solution. It is recommended as a replacement for discrete designs in a variety of applications in process control, factory automation and system monitoring.

The AD693 is packaged in an 20-pin ceramic side-brazed DIP and is specified over the −40°C to +85°C industrial temperature range.

## PRODUCT HIGHLIGHTS

1. The AD693 is a complete monolithic low-level voltage-to-current loop signal conditioner.
2. Precalibrated output zero and span options include 4-20mA, 0-20mA, and 12 ± 8mA in two- and three-wire configurations.
3. Simple resistor programming adds a continuum of ranges to the basic 30mV and 60mV input spans.
4. The common-mode range of the signal amplifier input extends from ground to near the device's operating voltage.
5. Provision for transducer excitation includes a 6.2V reference output and an auxiliary amplifier which may be configured for voltage or current output and signal amplification.
6. The circuit configuration permits simple linearization of bridge, RTD, and other transducer signals.
7. A monitored output is provided to drive an external pass transistor. This feature off-loads power dissipation to extend the temperature range of operation, enhance reliability, and minimize self-heating errors.
8. Laser-wafer trimming results in low unadjusted errors and affords precalibrated input and output spans.
9. Zero and span are independently adjustable and noninteractive to accommodate transducers or user defined ranges.
10. Six precalibrated temperature ranges are available with a 100Ω RTD via pin strapping.

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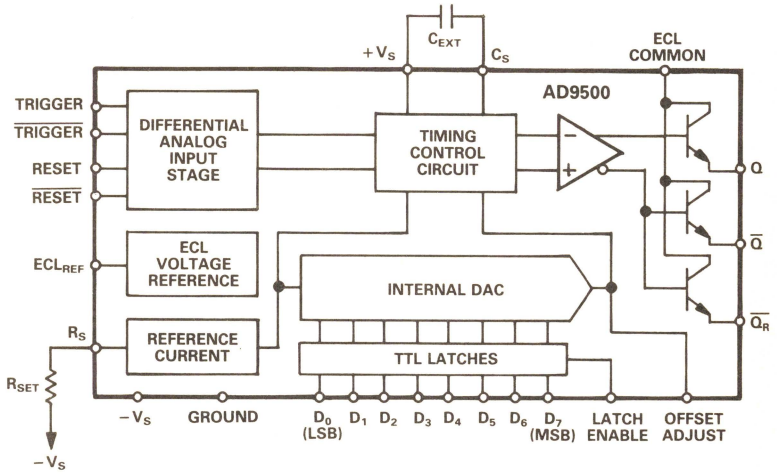
# Digitally Programmable Delay Generator

# AD9500

**FEATURES**
- 10ps Delay Resolution
- 2.5ns to 100μs Full-Scale Range
- Differential Inputs
- Separate Trigger and Reset Inputs
- 310mW Power Dissipation

**AD9500 FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD9500 is a digitally programmable delay generator which provides programmed delays in resolutions as small as 10 picoseconds on a minimum full-scale span of 2.5 nanoseconds.

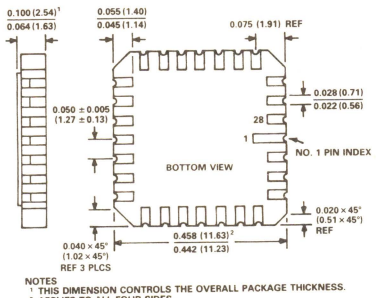
Its output is delayed from the input by a time which is directly proportional to an 8-bit digital input code. Groups of AD9500 devices are ideally suited for adjusting multiple signal timing skews and delays in various system applications. Differential TRIGGER and RESET control inputs are designed primarily for ECL signal levels but will also function with analog and TTL levels. An on-board ECL reference midpoint allows both to be driven by either single-ended or differential ECL circuits.

Two temperature ranges and three packages are available. For industrial temperatures of −25°C to +85°C, order the AD9500BP or the AD9500BQ. The "P" suffix indicates a 28-pin PLCC; the "Q" designates a 24-pin ceramic "skinny" DIP with 0.3″ package width. For extended temperatures of −55°C to +125°C, the model numbers are AD9500TE (28-pin LCC) or AD9500TQ (24-pin "skinny" DIP).

## OUTLINE DIMENSIONS

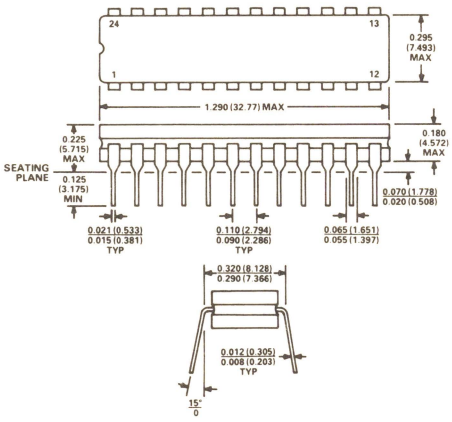
Dimensions shown in inches and (mm).

**28-Pin LCC**



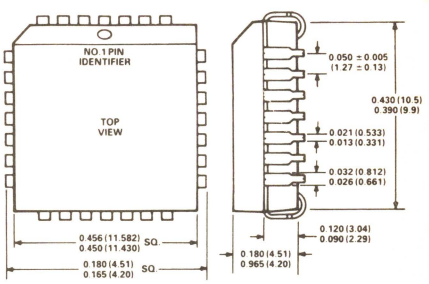

NOTES
1 THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2 APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED.

**24-Pin Ceramic "Skinny" DIP**




1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

**28-Terminal PLCC**

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# ANALOG DEVICES

# Ultrafast Voltage Comparators

# AD96685/AD96687

**FEATURES**
- 2.5ns Propagation Delay
- 0.5ns Latch Setup Time
- 90dB CMRR
- +5V, −5.2V Supply Voltages
- Low Propagation Delay Dispersion

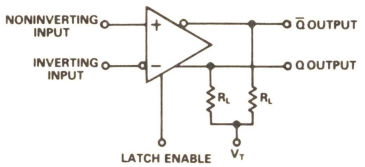
## PRODUCT DESCRIPTION

The AD96685 (single) and AD96687 (dual) are ultrafast voltage comparators with short propagation delays and setup times. They also feature extremely low propagation delay dispersion versus overdrive levels.

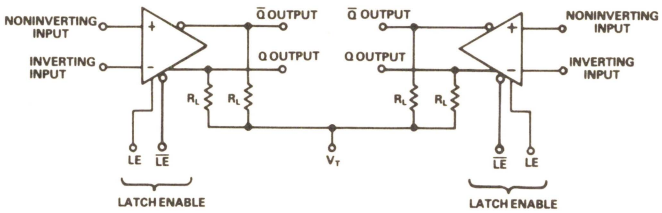
Both devices are manufactured with a high-performance bipolar process; both have differential inputs and complementary outputs which are fully compatible with ECL logic levels. Their 30mA output currents are capable of driving 50Ω terminated transmission lines; a latch enable input allows operation in either a sample mode or a track mode.

There are five models of the single AD96685 comparator; two operate over an industrial temperature of −25°C to +85°C and the other three are for extended temperatures of −55°C to +125°C. One of the three models of the dual AD96687 unit operates over industrial temperature, and the other two are for extended temperature.

## AD96685/AD96687 FUNCTIONAL BLOCK DIAGRAMS




*AD96685*




THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

*AD96687*

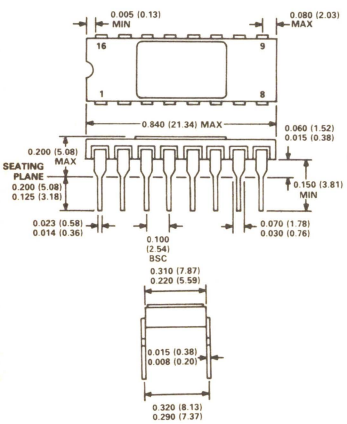
## ORDERING INFORMATION

| DEVICE | TYPE | TEMPERATURE RANGE | DESCRIPTION |
|---|---|---|---|
| AD96685BH | SINGLE | −25°C to +85°C | 10-Pin CAN, INDUSTRIAL |
| AD96685BQ | SINGLE | −25°C to +85°C | 16-Pin DIP, INDUSTRIAL |
| AD96685TE | SINGLE | −55°C to +125°C | 20-Pin LCC, EXTENDED TEMP. |
| AD96685TH | SINGLE | −55°C to +125°C | 10-Pin CAN, EXTENDED TEMP. |
| AD96685TQ | SINGLE | −55°C to +125°C | 16-Pin DIP, EXTENDED TEMP. |
| AD96687BQ | DUAL | −25°C to +85°C | 16-Pin DIP, INDUSTRIAL |
| AD96687TE | DUAL | −55°C to +125°C | 20-Pin LCC, EXTENDED TEMP. |
| AD96687TQ | DUAL | −55°C to +125°C | 16-Pin DIP, EXTENDED TEMP. |

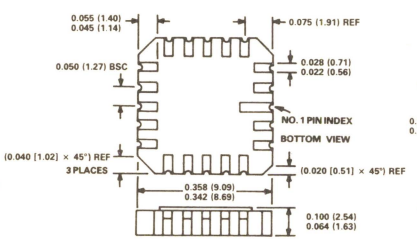
## OUTLINE DIMENSIONS

Dimensions are shown in inches and (mm).

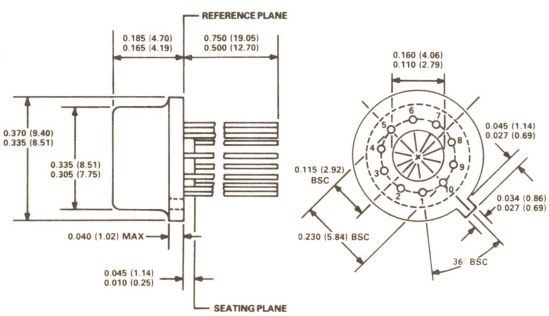
### 16-PIN CERAMIC DIP




### 20-PIN LCC




### 10-PIN TO-100 METAL CAN

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# 1987
# DSP PRODUCTS DATABOOK

**Complete Technical Data on
High-Performance-and-Functionality Fixed- and Floating-
Point Multipliers and Multiplier-Accumulators,
Word-Slice™ DSP System Components, and
DSP Microprocessors**

The pages that follow in *IC MASTER* contain brief technical data on innovative CMOS and fast bipolar chips for digital signal processing and number crunching. A 432-page Databook describes these products in detail and includes selection guides, application notes, and package information; it is available to readers of *IC MASTER* upon request.

CONTENTS

General Information
DSP Microprocessors
Microcoded Support Components
Floating-Point Components
Fixed-Point Components
Package Information
Application Notes

Analog Devices

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# ANALOG DEVICES

# IEEE Floating Point Chipsets

## ADSP-32XX

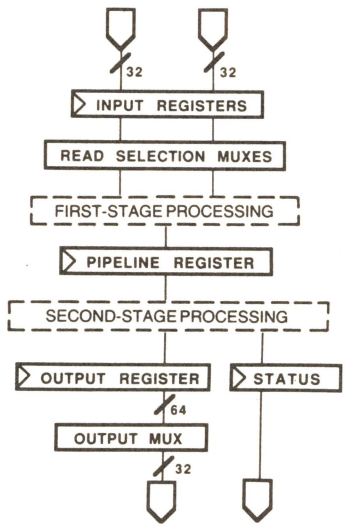
### GENERAL DESCRIPTION

Analog Devices' family of floating point chipsets (multiplier and ALU) provides a compatible, upgradable set of solutions to computation-intensive problems. These chipsets are high-speed, low-power arithmetic components conforming to IEEE Standard 754. Any multiplier can be used with any ALU. Operations are supported on several data formats including 32-bit and 64-bit IEEE floating point, 32-bit twos complement and 32-bit unsigned-magnitude fixed point. The most recent members of the family support IEEE exact divide and square root in hardware.

The high throughput of these chips is achieved with only a single level of internal pipelining, greatly simplifying program development. This results in very low latency.

All four rounding modes of IEEE Standard 754 and all five exception conditions are supported as well as the gradual underflow provisions of the standard. Alternatively, each chip offers a FAST mode which sets results less than the smallest IEEE normalized values to zero, eliminating underflow exception handling when full conformance to the standard is not essential.

The ADSP-3210 is a 100-pin, two-port device; all other members of the family are 144-pin, three-port devices. All parts are available for both commercial and extended temperature ranges, the latter also available in high-reliability PLUS versions or processed fully to MIL-STD-883B.




*ADSP-32XX General Architecture*

| PART Number (available grades) | CMOS Technology | Single-Precision Throughput | Single-Precision Latency | Double-Precision Throughput | Double-Precision Latency |
|---|---|---|---|---|---|
| ADSP-3210 (J, K, L, S, T, U) | 1.5 micron double layer metal | J - 125 ns<br>K - 100 ns<br>L - 60 ns | J - 363 ns<br>K - 290 ns<br>L - 190 ns | J - 500 ns<br>K - 400 ns<br>L - 240 ns | J - 738 ns<br>K - 590 ns<br>L - 370 ns |
| ADSP-3220 (J, K, S, T) | 1.5 micron double layer metal | J - 125 ns<br>K - 100 ns | J - 300 ns<br>K - 240 ns | J - 125 ns<br>K - 100 ns | J - 363 ns<br>K - 290 ns |
| ADSP-3211 (J, K, L, S, T, U) | 1.5 micron double layer metal | J - 125 ns<br>K - 100 ns<br>L - 50 ns | J - 300 ns<br>K - 240 ns<br>L - 140 ns | J - 500 ns<br>K - 400 ns<br>L - 200 ns | J - 738 ns<br>K - 590 ns<br>L - 315 ns |
| ADSP-3221 (J, K, S, T) | 1.5 micron double layer metal | J - 125 ns<br>K - 100 ns | J - 300 ns<br>K - 240 ns | J - 125 ns<br>K - 100 ns | J - 363 ns<br>K - 290 ns |
| ADSP-3201 (J, K, L, S, T, U) | 1.5 micron double layer metal | J - 125 ns<br>K - 100 ns<br>L - 50 ns | J - 300 ns<br>K - 240 ns<br>L - 140 ns | The ADSP-3201/3202 are single-precision only devices | |
| ADSP-3202 (J, K, S, T) | 1.5 micron double layer metal | J - 125 ns<br>K - 100 ns | J - 300 ns<br>K - 240 ns | | |
| ADSP-3212 (J, K, S, T) | 1.0 micron double layer metal | J - 60 ns<br>K - 50 ns | J - 157 ns<br>K - 130 ns | J - 60 ns<br>K - 50 ns | J - 187 ns<br>K - 155 ns |
| ADSP-3222 (J, K, S, T) | 1.0 micron double layer metal | J - 60 ns<br>K - 50 ns | J - 157 ns<br>K - 130 ns | J - 60 ns<br>K - 50 ns | J - 187 ns<br>K - 155 ns |

### ORDERING INFORMATION

**ADSP-32XXTG/883B**

- Processing
- Package
- Performance, Temp. Range
- Part Number
- Analog Devices Digital Signal Processing

**Package**

G – Pin Grid Array

**Processing**

Blank – Standard
\+ – High Reliability
883B – MIL-STD-883

**Performance/ Temperature**

J – Standard, 0 to +70°C
K – High Speed, 0 to +70°C
L – Very High Speed, 0 to +70°C
S – Standard, −55°C to +125°C
T – High Speed, −55°C to +125°C
U – Very High Speed, −55°C to +125°C

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ANALOG DEVICES

# Word-Slice Microcode Support ICs

## ADSP-1401 Program Sequencer

**FEATURES**
- **16-Bit Addressing Capability**
- **Look-Ahead™ Pipeline**
- **Extensive Interrupt Handling**
  - **Ten On-Chip Interrupt Vectors**
- **70ns Cycle Time**
- **25ns Clock-to-Address Delay**
- **64-Word RAM for Storing**
  - **Subroutine Linkage**
  - **Jump Addresses**
  - **Counters**
  - **Status Register**

### GENERAL DESCRIPTION

The ADSP-1401 is a high-speed, low-power (375mW) microprogram controller optimized for the demanding sequencing tasks found in digital signal processors and general purpose computers (e.g. looping, jumping, branching, subroutines, condition testing and interrupts). In addition to high speed and large addressing range, it has unique features that make it highly versatile:

- on-chip control of ten prioritized and maskable interrupts
- four decrementing event counters
- absolute, relative and indirect addressing capability
- download capability (writeable control store)
- a dynamically configurable 64-word RAM.

During each micro-instruction, the ADSP-1401 monitors status indicators and the current instruction to determine the next microprogram address. This address can come from one of several sources: the stack, the jump address space in the RAM, the data port, the interrupt vectors, or the microprogram counter. An extensive set of conditional instructions is available, including jumps, branches, subroutines, interrupts, and writeable control store.

The ADSP-1401's internal 64-word RAM is used for interrupt and subroutine linkage via the stack. It also provides the ability to associate counters, jump addresses, and the status register with nested interrupts and subroutines.

Interrupts are handled entirely on chip. The ADSP-1401's internal interrupt control logic includes registers for eight external interrupt vectors, a mask register, and a priority decoder. Two additional vectors are reserved for internally-generated interrupts resulting from counter underflow and stack limit violation.

The ADSP-1401's four decrementing 16-bit counters are used to track loops and events. These counters are referenced by several conditional instructions and can also trigger an internal interrupt.

The Look-Ahead (both parts) pipeline eliminates the need for an external microcode pipeline register by internally latching instructions and addresses. A complementary latching arrangement allows a new instruction to be decoded (in preparation for the following cycle) while the program memory address for the current cycle is held constant.

**Look-Ahead is a trademark of Analog Devices, Inc.**

## ADSP-1410 Address Generator

**FEATURES**
- **16-Bit Addresses with Higher Precision Options**
- **Look-Ahead Pipeline**
- **90ns Cycle Time**
- **30ns Clock-to-Address Delay**
- **Versatile Addressing Hardware:**
  - **30 16-Bit Registers**
  - **16-Bit ALU with Left/Right Shift & Carry I/O**
  - **Comparator**
  - **Bit Reverser**
- **Dual Ports**
- **Powerful Single-Cycle Looping Instructions**

### GENERAL DESCRIPTION

The ADSP-1410 is a fast, flexible address generator optimized for digital signal processors and general purpose computers. This low-power (375mW) CMOS device rapidly generates the data memory addresses required by routines such as digital filters, FFTs, matrix operations, and DMAs.

The ADSP-1410's 10-bit microcode instructions include commands for looping, register read/writes, internal data transfers, and logical/shift operations. An internal Alternate Instruction Register (AIR) can also provide the instruction under external control, allowing microcode to be conserved in many applications.

In a single instruction cycle, the ADSP-1410 can:
- output a 16-bit memory address
- modify this memory address
- conditionally reinitialize the address based on a comparison with a preset value.

Consequently, circular buffers and modulo addressing of data memories can be implemented without overhead.

The ADSP-1410's architecture features a 16-bit ALU, a comparator, and 30 16-bit registers. The registers are organized into four files: sixteen address registers, six offset registers, four compare registers, and four initialization registers.

The ADSP-1410 has a 16-bit address (Y) port for outputting addresses and a 16-bit data (D) port for I/O between internal and external registers. A value provided by the data port may serve as an input to the 1410's ALU or may be directly output over the address port.

Double-precision (30-bit), single-cycle addressing can be performed by cascading two ADSP-1410s. Alternatively, a single ADSP-1410 can provide one double-precision address every two clock cycles.

**ORDERING INFORMATION**

ADSP-14XXTD/883B
- Processing
- Package
- Performance, Temp. Range
- Part Number
- Analog Devices Digital Signal Processing

**Package**
D – Ceramic DIP
N – Plastic DIP
P – Plastic Leaded Chip Carrier

**Processing**
Blank – Standard
+ – High Reliability
883B – MIL-STD-883

**Performance/ Temperature**
J – Standard, 0 to +70°C
K – High Speed, 0 to +70°C
S – Standard, −55°C to +125°C
T – High Speed, −55°C to +125°C

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# Fixed-Point Multipliers and MACs

## GENERAL DESCRIPTION

Analog Devices offers a full line of high-speed, low-power multipliers and MACs currently fabricated in 1.5 micron CMOS. A complete selection of industry standard parts is available. In addition, a number of enhanced fixed-point components are offered. These enhanced parts include the ADSP-1101 Integer Arithmetic Unit, the ADSP-1110A Single-Port Multiplier, and the ADSP-7018 and ADSP-8018 bipolar multipliers with ultrahigh speed.

## FIXED-POINT MULTIPLIERS

| Word Size | Model No. | Multiplication[1] Time, ns Clocked Comm | Clocked MIL | Unclocked Comm | Unclocked MIL | $I_{DD}$[2] Comm | $I_{DD}$[2] MIL | Twos Comp | Data Formats Unsign Mag. | Mixed Mode | No. of Pins | Package Options[3] | Process | Logic Type |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 8×8 | ADSP-1080A | J=45<br>K=33 | S=55<br>T=45 | N/A | N/A | 45 | 55 | X | | | 40 | D,N,E[4] | CMOS | TTL |
| 8×8 | ADSP-1081A | J=45<br>K=33 | S=55<br>T=45 | N/A | N/A | 45 | 55 | | X | | 40 | D,N,E[4] | CMOS | TTL |
| 12×12 | ADSP-1012A | J=75<br>K=50 | S=90<br>T=60 | J=105<br>K=80 | S=125<br>T=95 | 60 | 70 | X | X | X | 64<br>68 | D,N<br>G,E | CMOS | TTL |
| 16×16 | ADSP-1016A | J=85<br>K=70 | S=95<br>T=80 | J=105<br>K=90 | S=120<br>T=105 | 45 | 55 | X | X | X | 64<br>68 | D,N<br>G,E | CMOS | TTL |
| 16×16 | ADSP-7018 | J=19 | Note 5 | J=25 | Note 5 | 625 | Note 5 | X | X | X | 108 | G | Bipolar | TTL |
| 16×16 | ADSP-8018 | J=15 | Note 5 | J=15.5 | Note 5 | 825 | Note 5 | X | X | X | 108 | G | Bipolar | ECL |
| 24×24 | ADSP-1024A | J=120<br>K=95 | S=150<br>T=120 | N/A | N/A | 70 | 90 | X | | | 84 | G | CMOS | TTL[6] |

## MULTIPLIER/ACCUMULATORS

| Word Size | Model No. | Multiplication[1] Accumulate Time Comm | Accumulate Time MIL | Accum. Size | No. of Accum. | $I_{DD}$[2] Comm | $I_{DD}$[2] MIL | No. of Pins | Package Options[3] |
|---|---|---|---|---|---|---|---|---|---|
| 8×8 | ADSP-1008A | J=60<br>K=50 | S=75<br>T=60 | 19 | 1 | 40 | 45 | 48 | D,N |
| 12×12 | ADSP-1009A | J=85<br>K=70 | S=100<br>T=85 | 27 | 1 | 70 | 75 | 64<br>68 | D,N<br>E,G |
| 16×16 | ADSP-1010A | J= 85<br>K=75 | S=100<br>T=90 | 35 | 1 | 80 | 100 | 64<br>68 | D,N<br>E,G |
| 16×16 | ADSP-1101 | J= 90<br>K=80 | S=105<br>T=95 | 40 | 2 | 75 | 75 | 100 | G |
| 16×16 | ADSP-1110A | J=100<br>K=85 | S=120<br>T=100 | 40 | 1 | 70 | 80 | 28 | D,N,E,P |

NOTES
[1]ns max @ $T_A$ = +70°C Comm., $T_A$ = +125°C MIL.
[2]mA max, $f_{CLK}$ = max, $V_{DD}$ = +5V @ $T_A$ = +70°C Commercial, +125°C MIL.
[3]D = ceramic DIP, N = plastic DIP, E = leadless chip carrier, G = pin grid array, P = PLCC.
[4]Contact factory.
[5]MIL versions available.
[6]TTL levels of 0.8V and +2.2V.



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ANALOG DEVICES

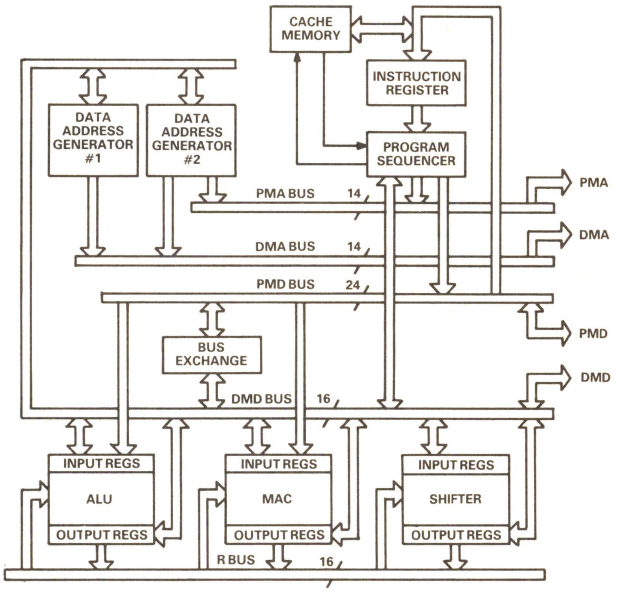
# DSP Microprocessor

# ADSP-2100

## FEATURES

- **Separate Program and Data Buses, Extended Off-Chip**
- **Single-Cycle Direct Access to 16K × 16 of Data Memory**
- **Single-Cycle Direct Access to 16K × 24 (Expandable to 32K × 24) of Program Memory**
- **Dual Purpose Program Memory for Both Instruction and Data Storage**
- **Three Independent Computational Units: ALU, Multiplier/Accumulator and Barrel Shifter**
- **Two Independent Data Address Generators**
- **Powerful Program Sequencer**
- **Internal Instruction Cache**
- **Provisions for Multiprecision Computation and Saturation Logic**
- **Single-Cycle Instruction Execution**
- **Multifunction Instructions**
- **Four External Interrupts**
- **125ns Cycle Time**
- **600mW Maximum Power Dissipation with CMOS Technology**
- **100-Pin Grid Array**

ADSP–2100 FUNCTIONAL BLOCK DIAGRAM




## GENERAL DESCRIPTION

The ADSP-2100 is a single-chip microprocessor optimized for digital signal processing (DSP) and other high-speed numeric processing applications. It integrates computational units, data address generators and a program sequencer in a single device. The ADSP-2100 makes efficient use of external memories for program and data storage, freeing silicon area for increased processor performance. The resulting architecture combines the functions and performance of a bit-slice/building block system with the ease of design and development of a general-purpose microprocessor. The ADSP-2100 operates at 8MHz. Every instruction executes in a single 125ns cycle. Fabricated in a high-speed 1.5 micron double-layer metal CMOS process, the ADSP-2100 dissipates less than 600mW.

The ADSP-2100's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. In one cycle the ADSP-2100 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

## DEVELOPMENT SYSTEM

The ADSP-2100 is supported by a complete set of tools for software and hardware system development. The Cross-Software System provides a System Builder for defining the architecture of systems under development, an Assembler, a Linker and a Simulator. The Simulator provides an interactive instruction-level simulation. A PROM Splitter generates PROM burner compatible files. An Emulator is available for hardware debugging of ADSP-2100 systems.

## ADDITIONAL INFORMATION

For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 User's Manual*. For more information about the Development System, refer to the *ADSP-2100 Cross-Software Manual* and the *ADSP-2100 Emulator Manual*.

### ORDERING INFORMATION

**ADSP-2100KG/883B**

- Processing
- Package
- Performance, Temp. Range
- Part Number
- Analog Devices Digital Signal Processing

**Package**

G – Pin Grid Array
P – Plastic Leaded Chip Carrier

**Processing**

Blank – Standard
\+ – High Reliability
883B – MIL-STD-883

**Performance/ Temperature**

J – Standard, 0 to +70°C
K – High Speed, 0 to +70°C
S – Standard, −55°C to +125°C
T – High Speed, −55°C to +125°C

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# MILITARY PRODUCTS DATABOOK

**With Specifications, Package Outlines, etc., for:**

- **QPL Parts**
- **MIL-M-38510 Slash-Sheet Parts**
- **MIL-STD-883C-Compliant Parts**

Analog Devices

The pages that follow in *IC MASTER* contain summary information and listings of products from Analog Devices available to meet the requirements of military specifications. This information was drawn from our Military Products Databook.

The Analog Devices Military Products Databook was developed to provide military systems suppliers with complete information for devices processed in accordance with MIL-STD-883 and offered under ADI's standard 883 program. All products specified in the Databook are available as catalog items from Analog Devices. The information contained in the Databook, and its format, should facilitate the preparation of Military or SCD drawings, as applicable; both its general and specific-device specifications meet or exceed the product documentation requirements outlined in paragraph 1.2.1 of MIL-STD-883C.

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ANALOG DEVICES **ONE TECHNOLOGY WAY, P.O. BOX 9106, NORWOOD, MA 02062-9106 U.S.A.**

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ANALOG DEVICES

# MIL-STD-883 Class B Products

## OPERATIONAL AMPLIFIERS

AD380 Wideband, Fast Settling, FET Op Amp
AD381 High-Speed, Low Drift, FET Op Amp
AD382 High-Speed, Low Drift, FET Op Amp, 50mA Output
AD506 FET Input IC Op Amp
AD507 Wideband, Fast-Slewing, General Purpose IC Op Amp
AD509 High-Speed, Fast-Settling IC Op Amp
AD510 Low-Cost, Laser-Trimmed Precision IC Op Amp
AD517 Precision, High Accuracy Op Amp
AD518 Fast Wideband IC Op Amp
AD542 Precision Low-Cost BiFET Op Amp
AD544 High-Speed Implanted FET Input Op Amp
AD547 Ultralow-Drift, BiFET Op Amp
AD548 Low-Power Precision BiFET Op Amp
AD642 Precision Low-Cost Dual BiFET Op Amp
AD644 Dual High-Speed Implanted FET Input Op Amp
AD647 Ultralow-Drift BiFET Op Amp
AD648 Low-Power Precision Dual BiFET Op Amp
AD711 Precision High-Speed BiFET Op Amp
AD712 Precision High-Speed BiFET Op Amp
AD741 Internally Compensated IC Op Amp
AD5539 Ultrahigh-Frequency Op Amp
ADLH0032 Ultrafast FET Op Amp
ADLH0033 High-Speed Buffer Amp
AD OP-07 Ultralow-Offset Voltage IC Op Amp
AD OP-27 Ultralow-Noise, Precision IC Op Amp
AD OP-37 Ultralow-Noise, High-Speed, Precision Op Amp
HOS-050A Fast Settling Video Op Amp
HOS-060H Fast Settling Video Op Amp

## INSTRUMENTATION AMPLIFIERS

AD521 Monolithic IC Resistor-Programmable Amp
AD522 Precision, Hybrid Instrumentation Amp
AD524 Precision Instrumentation Amp
AD624 Precision Instrumentation Amp
AD625 Precision Instrumentation Amp with Flexible Gain Setting

## ANALOG SIGNAL PROCESSING COMPONENTS

AD532 Multiplier/Divider, Fixed Scale Factor
AD534 Multiplier/Divider, Programmable Scale Factor
AD536A True RMS-to-DC IC Converter
AD538 Real-Time Analog Computational Unit
AD539 Wideband, Dual Channel, 2 Quadrant, Multiplier/Divider
AD630 Balanced Modulator/Demodulator
AD632 Internally Trimmed Precision IC Multiplier
AD637 High Precision Wideband RMS-to-DC Converter

## VOLTAGE REFERENCES

AD580 2.5V Monolithic IC Positive Voltage Ref
AD581 10V Pretrimmed, Monolithic IC Voltage Ref
AD584 Laser-Trimmed, Multi-Tap, 10V, 7.5V, 5V, 2.5V, Ref
AD2700 +10V Precision, Hybrid IC, Positive Volt Ref
AD2702 ±10V Precision, Hybrid Dual Volt Ref
ADREF02 5V Precision, IC Positive Volt Ref

## TEMPERATURE MEASUREMENT COMPONENTS

AD590 Two-Terminal Temperature Transducer

## DIGITAL-TO-ANALOG CONVERTERS

AD390 Quad 12-Bit Voltage Output D/A Converter
AD394 µP Compatible Multiplying Quad 12-Bit D/A Converter
AD395 µP Compatible Multiplying Quad 12-Bit D/A Converter
AD396 µP Compatible Multiplying Quad 14-Bit D/A Converter
AD558 Low-Cost Complete µP-Compatible 8-Bit D/A Converter
AD561 Low-Cost 10-Bit Complete Current-Output D/A Converter
AD562 High Accuracy, 12-Bit Current-Output D/A Converter
AD563 High Accuracy, 12-Bit Current-Output D/A with Reference
AD565A High-Speed 12-Bit Voltage Output D/A Converter
AD566A High-Speed 12-Bit Current Output D/A Converter
AD567 µP-Compatible 12-Bit Current Output D/A Converter
AD667 µP-Compatible 12-Bit Voltage Output D/A Converter
AD3860 Complete, Voltage-Output 12-Bit D/A Converter
AD7111 CMOS Logarithmic D/A Converter
AD7118 CMOS Logarithmic D/A Converter
AD7224 LC$^2$MOS 8-Bit DAC with Output Amplifier
AD7225 LC$^2$MOS Quad 8-Bit DAC with Separate References
AD7226 LC$^2$MOS Quad 8-Bit D/A Converter
AD7520 CMOS 10-Bit Multiplying DAC
AD7521 CMOS 12-Bit Monolithic Multiplying DAC
AD7522 CMOS 10-Bit Buffered Multiplying D/A Converter
AD7524 CMOS 8-Bit Buffered Multiplying DAC
AD7528 CMOS Dual 8-Bit Buffered Multiplying DAC
AD7533 CMOS Low-Cost 10-Bit Multiplying D/A Converter
AD7534 LC$^2$MOS µP-Compatible 14-Bit DAC
AD7536 LC$^2$MOS µP-Compatible 14-Bit DAC
AD7537 LC$^2$MOS (8+4) Loading Dual 12-Bit DAC
AD7541 CMOS 12-Bit Monolithic Multiplying DAC
AD7541A CMOS 12-Bit Monolithic Multiplying DAC
AD7542 CMOS 12-Bit µP-Compatible D/A Converter
AD7543 CMOS 12-Bit Serial Input DAC
AD7545 CMOS 12-Bit Buffered Multiplying D/A Converter
AD7547 LC$^2$MOS Parallel Loading Dual 12-Bit DAC
AD7548 CMOS 8-Bit µP-Compatible 12-Bit DAC

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# ANALOG DEVICES

# MIL-STD-883 Class B Products

AD7549 LC²MOS Dual 12-Bit µP-Compatible DAC
AD DAC85 High Performance, 12-Bit Hybrid D/A Converter
AD DAC87 Wide Temperature Range 12-Bit Hybrid D/A Converter
AD DAC87 Wide Temperature Range 12-Bit Monolithic D/A Converter

**ANALOG-TO-DIGITAL CONVERTERS**

AD376 Complete High-Speed 16-Bit A/D Converter
AD570 Low-Cost 8-Bit A/D, Complete ADC
AD571 Low-Cost, 10-Bit A/D, Complete ADC
AD572 Hybrid 12-Bit A/D Converter
AD573 Fast, Complete 10-Bit ADC with µP Interface
AD574A Complete 12-Bit ADC with µP Interface
AD575 Complete 10-Bit A/D Converter with Serial Output
AD578 Very Fast, Complete 12-Bit A/D Converter
AD579 Fast, Complete 10-Bit A/D Converter
AD670 Low-Cost, 8-Bit ADC In Amp Front End
AD673 Fast, Complete 8-Bit ADC, µP Interface
AD5200 Series 12-Bit, 50µs, Low Initial Calibration Error
AD5210 Series 12-Bit, 13µs, Low Initial Calibration Error
AD5240 12-Bit, 8µs, Low Initial Calibration Error
AD7572 LC²MOS Complete High-Speed 12-Bit ADC
AD7574 CMOS Microprocessor Compatible, 8-Bit A/D Converter
AD7575 LC²MOS 5µP-8-Bit ADC with Track/Hold
AD7576 LC²MOS 10µP-Compatible 8-Bit ADC
AD7578 CMOS 12-Bit Successive Approximation ADC
AD7582 CMOS 12-Bit Successive Approximation ADC
AD7820 LC²MOS High-Speed µP-Compatible 8-Bit ADC with Track/Hold Function
AD7824 LC²MOS High-Speed 4-Channel 8-Bit ADC
AD7828 LC²MOS High-Speed 8-Channel 8-Bit ADC
AD ADC85 Fast, Complete, 12-Bit A/D Converter

**VOLTAGE-TO-FREQUENCY & FREQUENCY-TO-VOLTAGE CONVERTERS**

AD537 General Purpose V/F Converter
AD650 1MHz Full-Scale Range V/F and F/V Converter
AD651 Synchronous V/F and F/V Converter
ADVFC32 0.5MHz Full-Scale Range V/F and F/V Converter

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**DIGITAL SIGNAL PROCESSING COMPONENTS**

ADSP-1008A Fast 8×8-Bit CMOS Multiplier/Accumulator
ADSP-1009A 12×12-Bit CMOS Multiplier/Accumulator
ADSP-1010A 16×16-Bit CMOS Multiplier/Accumulator
ADSP-1012A 12×12-Bit CMOS Multiplier
ADSP-1016A 16×16-Bit CMOS Multiplier
ADSP-1024A 24×24-Bit CMOS Multiplier
ADSP-1080A 8×8-Bit Precision Multiplier/Divider
ADSP-1081A 8×8-Bit CMOS Multiplier
ADSP-1101 Integer Arithmetic Unit
ADSP-1110A 16×16-Bit CMOS Single Port Multiplier/Accumulator
ADSP-1401 Word-Slice™ Program Sequencer
ADSP-1410 Word-Slice™ Address Generator
ADSP-2100 High Performance Monolithic Digital Signal Processor
ADSP-3210 High-Speed 64-Bit IEEE Floating Point Multiplier
ADSP-3220 High-Speed 64-Bit IEEE Floating Point ALU

**SAMPLE/TRACK HOLD AMPLIFIERS**

AD346 High-Speed Hybrid, S/H Amplifier
AD582 Low-Cost, Monolithic, S/H Amplifier
AD585 Fast Monolithic S/H Amplifier
HTC-0300A Ultrahigh-Speed Track-and-Hold Amplifier

**DATA ACQUISITION SUBSYSTEMS**

AD362 Multiplexer S/H Front End for 12-Bit A/D Converter

**CMOS SWITCHES & MULTIPLEXERS**

AD7501 8-Channel Multiplexer, High Enables
AD7502 4-Channel Differential Multiplexer
AD7503 8-Channel Multiplexer Low Enables
AD7506 16-Channel Multiplexer
AD7507 8-Channel Differential Multiplexer
AD7510DI Dielectrically Isolated Quad SPST; Address High Closes Switch
AD7511DI Dielectrically Isolated Quad SPST; Address Low Closes Switch
AD7512 Dual Single-Pole, Double-Throw Switch
AD7590DI DI CMOS Protected Analog Switch with Data Latch
AD7591DI DI CMOS Protected Analog Switch with Data Latch
AD7592DI DI CMOS Protected Analog Switch with Data Latch
ADG201A LC²MOS Quad SPST Switch
ADG202A LC²MOS Quad SPST Switch
ADG221 LC²MOS Quad SPST Switch
ADG222 LC²MOS Quad SPST Switch

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# ANALOG DEVICES

# MIL-M-38510 and Military Drawing Cross Reference

## BY FUNCTION

### D/A CONVERTERS

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| AD558 | JM38510/144 | 8-Bit D/A, Voltage Output, Internal Reference |
| AD561 | JM38510/133 | 10-Bit D/A, Current Output, Internal Reference |
| AD562 | JM38510/121 | 12-Bit D/A, Current Output, External Reference |
| AD563 | JM38510/121 | 12-Bit D/A, Current Output, Internal Reference |
| AD565 | JM38510/121 | 12-Bit D/A, Fast Current Output, Internal Reference |
| AD566 | JM38510/121 | 12-Bit D/A, Fast Current Output, External Reference |
| AD567 | (5962-87801) | 12-Bit D/A, Microprocessor Compatible |
| AD7226 | (5962-87802) | 8-Bit CMOS D/A, Quad |
| AD7520 | JM38510/127 | 10-Bit CMOS D/A, 4 Quadrant Multiplying |
| AD7524 | (5962-87700) | 8-Bit CMOS D/A, Buffered Multiplying |
| AD7528 | (5962-87701) | 8-Bit CMOS D/A, Dual Multiplying |
| AD7541 | JM38510/127 | 12-Bit CMOS D/A, 4 Quadrant Multiplying |
| AD7545 | (5962-87702) | 12-Bit CMOS D/A, Buffered Multiplying |
| AD DAC87 | JM38510/137 | 12-Bit D/A, Voltage Output, Internal Reference |

### VOLTAGE REFERENCES

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| AD580 | (5962-86861) | Precision 2.5 Volt Reference |
| AD584 | JM38510/128 | Precision Voltage Reference, Multiple Outputs |
| AD2700 | (5962-8503001, 02) | Precision, ± 10 Volt Reference |
| AD2702 | (5962-8503003, 04) | Precision, ± 10 Volt Reference |

### A/D CONVERTERS

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| AD570 | (5962-86802) | 8-Bit A/D |
| AD571 | JM38510/134 | 10-Bit A/D, Microprocessor Compatible |
| AD573 | JM38510/132 | 10-Bit A/D, Microprocessor Compatible |
| AD574 | JM38510/14001, 02 (5962-8512701, 02) | 12-Bit A/D, Microprocessor Compatible |
| AD7572 | (5962-87591) | 12-Bit A/D, Microprocessor Compatible |
| AD7820 | JM38510/146 | 8-Bit A/D, CMOS Microprocessor Compatible |

### INSTRUMENTATION AMPLIFIERS

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| AD524 | JM38510/143 | Instrumentation Amplifier |

### OP AMPS

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| AD OP-07 | JM38510/13501 | Precision Low Offset Op Amp |
| ADLH0032 | (5962-80013) | High Speed Op Amp |
| ADLH0033 | (5962-80014) | High Speed Buffer Amp |

### VOLTAGE-TO-FREQUENCY CONVERTERS

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| ADVFC32 | JM38510/138 | 100kHz V/F |
| AD650 | JM38510/138 | 1mHz V/F |

### NONLINEAR

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| AD532 | JM38510/139 | Analog Multiplier, Fixed Scale Factor |
| AD534 | JM38510/139 | Analog Multiplier, Programmable Scale Factor |

### SAMPLE AND HOLD

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| HTC-0300 | JM38510/142 | Fast Track-and-Hold Amplifier |

### DIGITAL SIGNAL PROCESSING COMPONENTS

| Generic | JAN, M385101, (Military Drawing) | Description |
|---|---|---|
| ADSP-2100 | (8773501, 02) | High Performance Digital Signal Processor |



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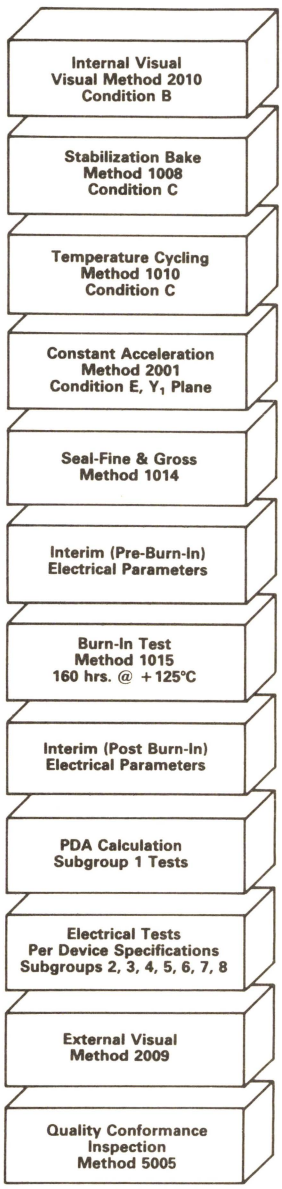
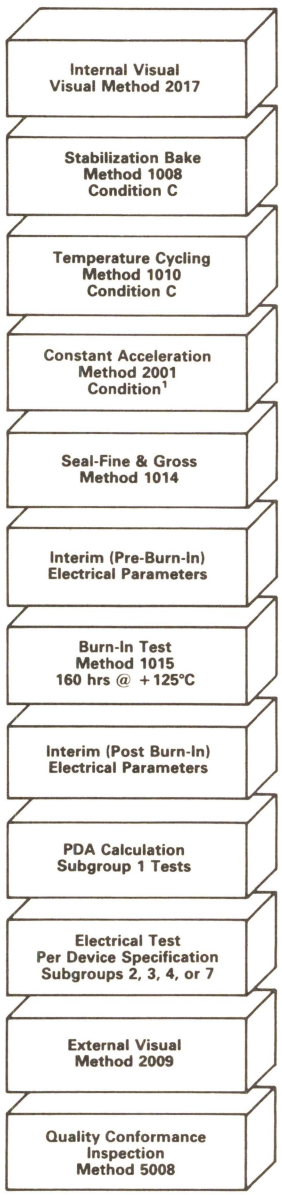
# ANALOG DEVICES

# MIL-STD-883 Class B Compliant Process Flows

## MONOLITHIC PROCESS FLOW MIL-STD-883 METHOD 5004 CLASS B DEVICE




## HYBRID PROCESS FLOW MIL-STD-883 METHOD 5008 CLASS B DEVICE




NOTE
[1]Condition A, D, E as applicable, Y1 plane.

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# MIL-STD-883 Class B Monolithic ASIC Capability

## COMBINED ANALOG AND DIGITAL APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) CAPABILITY

Analog Devices offers a full service, combined analog and digital ASIC military product capability including wafer fabrication, assembly and test. This capability provides many of the high performance analog functions found in the standard products listed in this section. These analog functions can be integrated with a family of standard combinational and sequential logic cells in a single-chip solution to many complex analog and digital system requirements.

These combined analog-digital products can be designed at several worldwide design centers by experienced design engineers using various levels of customer system design inputs. Advanced CAD hardware and software capabilities allow in-depth design simulation prior to mask making.

Manufacturing of these ASIC products can be done at several of our 38510 certified facilities in the United States and equivalent certified facilities in Europe. Available high-volume wafer process technologies include high- and low-voltage combinations of low-power, high-speed analog compatible CMOS and high-speed, precision bipolar. All of these processes incorporate precision, laser trimmable thin-film resistors. Switched capacitor filter technology is also available.

The following table summarizes the major analog and digital macrocell functions available at the time of publication. For further updates and specific information about our military ASIC product capability, please call your area sales office.

## EXAMPLES OF ASIC DESIGN FUNCTIONAL CELLS

**ANALOG:**

DATA CONVERSION – monotonic, no missing codes
D/A Converters – 8 bit, 10 bit, 12 bit and 14 bit
A/D Converters – 8 bit, 10 bit and 12 bit

INTEGRATED SAMPLE AND HOLD – 8 bit and 12 bit linear, with hold capacitor

VOLTAGE REFERENCE – bandgap and buried zener

OPERATIONAL AMPLIFIER – low noise bipolar and JFET input programmable

FILTERS – Switched capacitor biquad sections – low pass, notch, high pass, with programmable Q and center frequency
Continuous time – anti-aliasing, programmable

ANALOG SWITCHES – low RON, break before make

OSCILLATORS – trimmable, programmable, internal or external RC, crystal, voltage controlled

ANALOG SIGNAL PROCESSING – analog multiplier, delta modulators

COMPARATORS – precision, low bias current, high speed

**DIGITAL:**

COMBINATION – inverter, 2-to-4 input nor-nand, exclusive-or, buffers

SEQUENTIAL – latches, flip-flops, synchronous up/down counters, S/P, P/S and serial shift registers and one shot

OTHER FUNCTIONS –multiplexers, transmission gates, etc.

**OTHER MACRO-CELLS:** data acquisition systems, phase locked loop, power measurement, Universal Asynchronous Receiver/Transmitter (UART), etc.

Performance parameters for the above functions are dependent on the process technology chosen. See equivalent product functions in this section for an idea of the possible performance parameters available. Contact your local area sales office for more specific information.

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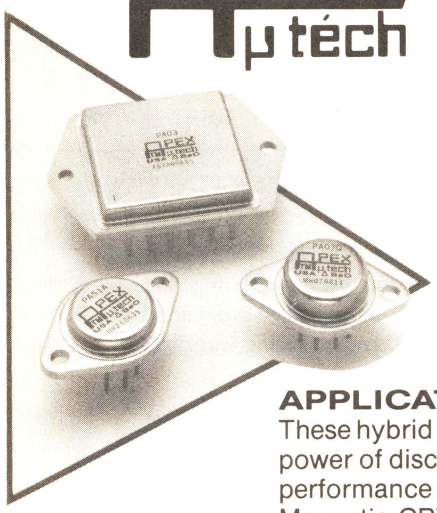
- HI-REL SCREENED (Q MODELS)
- UP TO 30 AMPS
- UP TO 450 VOLTS
- CUSTOMIZED VERSIONS



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## APPLICATION

These hybrid integrated circuits provide the precision associated with Op Amps and the power of discrete multi-component boosters all in one device. This improves reliability, performance and cost. Key applications for High Current Models include: Motor Drives, Magnetic CRT Deflection, Programmable Power Supplies, Valve Control, Pin Drivers and Compact Audio Amplifiers.

## SELECTOR GUIDE

| Model | Output Current ±A Pk Min | Output Voltage ±V Pk Min | $V_S$-Out Delta V | Supply Range ±V Max | Internal Power Watts Max | $V_{offset}$ Initial mV Max | $V_{offset}$ vs Temp μV/°C Max | I Bias nA Max | $I_q$ mA Max | PWR BW @ Nom $V_{out}$ KHz Typ | Slew Rate V/μs Typ | Unity GBW MHz Typ | $V_{os}$ Adj | Current Limit | Thermal Shutdown | Input Stage | Temp Range Max | Second Source |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA03<br>PA03A | 30<br>* | 68<br>* | 7<br>* | 15/75<br>* | 500<br>* | 3<br>1 | 30<br>10 | .05<br>.01 | 300<br>* | 30<br>* | 8<br>* | 1<br>* | Yes<br>* | Thermal<br>* | Yes<br>* | FET<br>* | 25/85<br>* | No<br>* |
| PA04 | 20 | 92 | 8 | 15/100 | 250 | 3 | 100 | .1 | 135 | 40 | 38 | 4 | No | Ext Adj | No | FET | 25/85 | No |
| PA12A<br>PA12M<br>PA12/PA12Q | 15<br>10<br>* | 43<br>39<br>* | 7<br>6<br>* | 10/50<br>10/45<br>* | 125<br>*<br>* | 3<br>6<br>* | 40<br>65<br>* | 20<br>30<br>* | 50<br>*<br>* | 20<br>*<br>* | 4<br>*<br>* | 4<br>*<br>* | No<br>*<br>* | Ext Adj<br>*<br>* | No<br>*<br>* | Bipolar<br>*<br>* | 55/125<br>*<br>25/85 | Direct<br>No<br>Direct |
| PA61A<br>PA61M<br>PA61/PA61Q | 10<br>*<br>* | 39<br>38<br>* | 6<br>7<br>* | 10/45<br>*<br>* | 97<br>*<br>* | 3<br>6<br>* | 40<br>65<br>* | 20<br>30<br>* | 10<br>*<br>* | 16<br>*<br>* | 2.6<br>*<br>* | 1<br>*<br>* | No<br>*<br>* | Ext Adj<br>*<br>* | No<br>*<br>* | Bipolar<br>*<br>* | 25/85<br>55/125<br>25/85 | No<br>*<br>* |
| PA51A<br>PA51M<br>PA51/PA51Q | 10<br>*<br>* | 32<br>*<br>28 | 8<br>*<br>* | 10/40<br>*<br>10/36 | 97<br>*<br>* | 5<br>10<br>* | 40<br>65<br>* | 20<br>40<br>* | 10<br>*<br>* | 16<br>*<br>* | 2.6<br>*<br>* | 1<br>*<br>* | No<br>*<br>* | Ext Adj<br>*<br>* | No<br>*<br>* | Bipolar<br>*<br>* | 55/125<br>*<br>25/85 | Direct<br>*<br>* |
| PA07A<br>PA07/PA07Q<br>PA07M | 5<br>*<br>* | 45<br>*<br>* | 5<br>*<br>* | 12/50<br>*<br>* | 67<br>*<br>* | .5<br>2<br>* | 10<br>30<br>* | .01<br>.05<br>* | 30<br>*<br>* | 18<br>*<br>* | 5<br>*<br>* | 1.3<br>*<br>* | Yes<br>*<br>* | Ext Adj<br>*<br>* | Yes<br>*<br>* | FET<br>*<br>* | 25/85<br>*<br>55/125 | Possible<br>*<br>* |
| PA10A<br>PA10M<br>PA10/PA10Q | 5<br>*<br>* | 44<br>37<br>* | 6<br>8<br>* | 10/50<br>10/45<br>* | 67<br>*<br>* | 3<br>6<br>* | 40<br>65<br>* | 20<br>30<br>* | 30<br>*<br>* | 23<br>*<br>* | 5<br>*<br>* | 6<br>*<br>* | No<br>*<br>* | Ext Adj<br>*<br>* | No<br>*<br>* | Bipolar<br>*<br>* | 55/125<br>*<br>25/85 | Possible<br>*<br>* |
| PA73/PA73Q<br>PA73M | 5<br>* | 22<br>* | 8<br>* | 10/30<br>* | 67<br>* | 10<br>* | 65<br>* | 40<br>* | 5<br>* | 23<br>* | 2.6<br>* | 1<br>* | No<br>* | Ext Adj<br>* | No<br>* | Bipolar<br>* | 25/85<br>55/125 | Direct<br>No |
| PA01 | 5 | 18 | 10 | 10/28 | 67 | 12 | 65 | 50 | 50 | 23 | 2.6 | 1 | No | Ext Adj | No | Bipolar | 25/85 | Possible |
| PA02A<br>PA02M<br>PA02/PA02Q | 5<br>*<br>* | 15<br>*<br>* | 4<br>*<br>* | 7/19<br>*<br>* | 48<br>*<br>* | 3<br>10<br>* | 25<br>50<br>* | .1<br>.2<br>* | 37<br>40<br>37 | 350<br>*<br>* | 20<br>*<br>* | 4.5<br>*<br>* | No<br>*<br>* | Ext Adj<br>*<br>* | No<br>*<br>* | FET<br>*<br>* | 55/125<br>*<br>25/85 | Similar<br>*<br>* |
| PA09A<br>PA09M<br>PA09/PA09Q | 2<br>*<br>* | 32<br>*<br>* | 8<br>*<br>* | 10/40<br>*<br>* | 78<br>*<br>* | 5<br>3<br>* | 10<br>30<br>* | .02<br>.1<br>* | 85<br>*<br>* | 2500<br>*<br>* | 400<br>*<br>* | 75<br>*<br>* | Yes<br>*<br>* | 4.5<br>*<br>* | Yes<br>*<br>* | FET<br>*<br>* | 25/85<br>55/125<br>25/85 | No<br>*<br>* |
| PA12H | 1 | 41 | 4 | 45 | | 6 | | 30 | 100 | | | | No | Ext Adj | No | Bipolar | 25/200 | No |
| PA08A<br>PA08M<br>PA08/PA08Q<br>PA08V | 15<br>*<br>*<br>* | 135<br>*<br>*<br>160 | 15<br>*<br>*<br>* | 15/150<br>*<br>*<br>15/175 | 17.5<br>*<br>*<br>* | .5<br>2<br>*<br>* | 10<br>30<br>*<br>* | .01<br>.05<br>*<br>* | 8.5<br>*<br>*<br>* | 90<br>*<br>*<br>* | 30<br>*<br>*<br>* | 5<br>*<br>*<br>* | Yes<br>*<br>*<br>* | Ext Adj<br>*<br>*<br>* | Yes<br>*<br>*<br>* | FET<br>*<br>*<br>* | 25/85<br>55/125<br>25/85<br>* | No<br>*<br>*<br>* |
| PA83A<br>PA83M<br>PA83/PA83Q | 075<br>*<br>* | 140<br>*<br>* | 10<br>*<br>* | 15/150<br>*<br>* | 17.5<br>*<br>* | 1<br>3<br>* | 10<br>25<br>* | 01<br>05<br>* | 8.5<br>*<br>* | 60<br>*<br>* | 30<br>*<br>* | 5<br>*<br>* | Yes<br>*<br>* | 1A<br>*<br>* | Yes<br>*<br>* | FET<br>*<br>* | 25/85<br>55/125<br>25/85 | Possible<br>No<br>Possible |
| PA80J/PA80Q | 06 | 30 | 5 | 15/35 | 11.5 | 10 | 30 | .05 | 10 | 100 | 15 | 5 | Yes | 1A | Yes | FET | 0/70 | Direct |
| PA84A<br>PA84M<br>PA84/PA84Q<br>PA84S | 04<br>*<br>*<br>* | 143<br>*<br>*<br>* | 7<br>*<br>*<br>* | 15/150<br>*<br>*<br>* | 17.5<br>*<br>*<br>* | 1<br>3<br>*<br>* | 10<br>25<br>*<br>* | .01<br>.05<br>*<br>* | 7.5<br>*<br>*<br>* | 250<br>*<br>*<br>* | 200<br>*<br>*<br>* | 75<br>*<br>*<br>* | Yes<br>*<br>*<br>* | .05A<br>*<br>*<br>* | Yes<br>*<br>*<br>* | FET<br>*<br>*<br>* | 25/85<br>55/125<br>25/85<br>* | Possible<br>No<br>Possible<br>No |
| PA81J | 03 | 70 | 5 | 32/75 | 11.5 | 3 | 25 | .05 | 8.5 | 60 | 20 | 5 | Yes | .05A | Yes | FET | 0/70 | Direct |
| PA82J/PA82Q | 015 | 145 | 5 | 70/150 | 11.5 | 3 | 25 | 05 | 8.5 | 30 | 20 | 5 | Yes | 025A | Yes | FET | 0/70 | Direct |
| WA01<br>WA01A | 4A<br>* | 12<br>* | 4<br>* | 7/16<br>* | 5<br>* | 10<br>5 | 50<br>25 | 20000<br>10000 | 35<br>* | 60000<br>* | 4500<br>* | —<br>* | Yes<br>* | 7A<br>* | No<br>* | Bipolar<br>* | 25/85<br>* | Possible<br>* |
| PA19<br>PA19A | 4A<br>* | 35<br>* | 5<br>* | 14/40<br>* | 78<br>* | 3<br>5 | 30<br>10 | 2<br>1 | 120<br>* | 3500<br>* | 900<br>* | 75<br>* | No<br>* | Ext Adj<br>* | Yes<br>* | FET<br>* | 25/85<br>* | Similar<br>* |
| PA85<br>PA85A | 2<br>* | 215<br>* | 10<br>* | 15/225<br>* | 34<br>* | 2<br>5 | 30<br>10 | .05<br>.01 | 23<br>* | 700<br>* | 1000<br>* | 20<br>* | No<br>* | Ext Adj<br>* | Yes<br>* | FET<br>* | 55/125<br>* | Similar<br>* |
| PA88<br>PA88A | 1<br>* | 215<br>* | 10<br>* | 15/225<br>* | 15<br>* | 5<br>1 | 30<br>10 | 05<br>01 | 1<br>* | 10<br>* | 4<br>* | 1<br>* | No<br>* | Ext Adj<br>* | Yes<br>* | FET<br>* | 25/85<br>* | No<br>* |
| PA18<br>PA18A | 1<br>* | 35<br>* | 5<br>* | 14/40<br>* | 10<br>* | 5<br>1 | 50<br>20 | 30<br>1 | 80<br>* | 5000<br>* | 1500<br>* | 85<br>* | No<br>* | Ext Adj<br>* | Yes<br>* | FET<br>* | 25/85<br>* | No<br>* |

*Specification is same as above.

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# DIGITAL

## DSP32, DSP32C, and DSP16

## AT&T's DSP FAMILY: The Most Advanced Digital Signal Processors

### Introduction

AT&T offers the most advanced family of single chip digital signal processors. Designed by AT&T Bell Laboratories, the *WE*® DSP16 Digital Signal Processor and the *WE* DSP32 Digital Signal Processor families offer unprecedented speed, accuracy, and ease of use.

The DSP32 was the first 32-bit single-chip floating-point DSP produced and has been in volume production since 1984. Its 32-bit floating-point format ends the need for scaling and allows easy implementation for algorithms which may be impossible to code in 16-bit fixed point due to precision or dynamic range limitations. Programming is also greatly simplified by the DSP32's C-like syntax. Equations are coded in an easy to read form which makes programs almost self-documenting. Also, the DSP32 is supported with a full Kernighan and Ritchie C compiler.

The *WE* DSP32C is AT&T's latest generation 32-bit floating point DSP. Both source and object code are upward compatible with the DSP32. A large address space (16 Mbytes), blazing speed, and easy hardware system interfaces all characterize the DSP32C. Like the DSP32, the DSP32C has its own Kernighan and Ritchie C compiler.

The DSP16 is a 16-bit fixed-point digital signal processor; it is AT&T's fourth generation DSP. It is the DSP of choice when very high speed and low power are required. It features a 55 ns instruction cycle time (multiply and accumulate) and a powerful set of microprocessor-type instructions. Hardware features include a programmed instruction cache for low overhead looping, dedicated registers for virtual shift (modulo) addressing and advanced I/O ports. Both the 16-bit parallel port and the high-speed serial port allow easy glueless interfaces to many external devices such as memories, codecs, or other DSPs.

### Hardware Development

Application system hardware and software development is supported by the *WE* DSP32-DS, DSP32C-DS, and *WE* DSP16-DS DSP Development Systems. The development systems provide real-time in-circuit emulation and real-time algorithm development. These units can be used in multiples with a single user terminal and host computer to support multiple development systems.

### Development Software

To complement the family's hardware tools, support software tools are available to help create, test, and debug application programs. The *WE* DSP32-SL and *WE* DSP16-SL Support Software Libraries run under the *MS-DOS**, *UNIX*®, or *VMS*** Operating Systems. These libraries provide an assembler, loader, and simulator. The libraries also have several utilities that aid and simplify program development.

### Application Software

Complementing the development software, AT&T offers software applications libraries containing source code for algorithms and transcendental math functions. The library currently supports the DSP32 but will soon support the DSP16 as well. All algorithms and functions have been carefully optimized for execution speed and coding efficiency.

Some of the routines included in the library are:

- sin, cost, tan, log, square root, x y
- N by N matrix routines
- Nth order FIR, IIR filters as well as Nth order real and complex adaptive FIR filters
- N-point FFT and IFFT
- Image processing routines

These are just a few of the many attributes that give the AT&T DSP family excellent performance and assurance against obsolescence in the future.

### The Floating Point Solution

The DSP32 — The first single-chip 32-bit floating-point digital signal processor. The DSP32 combines state-of-the-art technology, advanced circuit design, and extensive simulation techniques to achieve the following user-significant features.

- 12.5 MFLOP throughput
- 32-bit data bus
- 56 Kbyte off-chip memory expansion
- 4 memory accesses per instruction
- No speed penalty for using off-chip memory
- 40 powerful instruction types
- 12.5 Mb/s serial I/O rate
- 4 Mbyte/s parallel I/O rate

* Registered trademark of Microsoft Corporation
** Registered trademark of the Digital Equipment Corporation

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The DSP32 floating-point format consists of a 24-bit mantissa that encodes the fractional part of the number and an 8-bit exponent that encodes the magnitude of the number. The exponent provides greater than 1500 dB of dynamic range, making overflow or underflow unlikely. The 24-bit normalized mantissa yields a precision that is independent of the magnitude of the number. The format is very useful for high-precision calculations used in FFTs and adaptive filters; the floating point format eliminates scaling and decimal tracking and greatly reduces quantization noise during intermediate calculations. Another state-of-the-art feature of the DSP32 is its instruction set. Instead of using mnemonics, the DSP32 uses a C-like instruction set. This instruction set improves documentation by making it easier for designers to move high-level code onto the DSP.

Utilizing input from DSP32 users and Bell Laboratories design experience with the DSP32, AT&T designed the DSP32C to be the world's most advanced digital signal processor. In addition to the DSP32's impressive list of features, the DSP32C offers:

- Upward compatibility with DSP32
- 25 MFLOP throughput
- 16 Mbyte address space
- 8 vectored interrupts
- 16 Mb/s serial I/O
- IEEE 754 format conversion (single cycle)

### The Fixed-Point Solution

The *WE* DSP16 — The fastest currently available single-chip digital signal processor. An instruction cycle can include both a multiply and an accumulate and requires only 55 ns (a 75 ns version is also available).

When very high speed and low power are required, the DSP16 is the signal processor of choice. The device contains the following user-significant features:

- 55 ns parallel multiplier
- Program controlled instruction cache
- Modulo addressing for efficient vector operations
- 10 Mb/s serial I/O rate
- 18.2 Mbyte/s parallel I/O rate
- 16-bit data bus
- Hardware/software interrupt capability

The DSP16 family is ideally suited for high-speed applications which include high-speed modems, process controllers, graphics, and most computationally intensive signal processing algorithms.

Follow-on devices will also be available in the future. These devices will have speeds <50 ns with more on-chip RAM and ROM.

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# DIGITAL

## *WE*® DSP32 Digital Signal Processor

### Description

The *WE* DSP32 Digital Signal Processor is a high-speed, programmable, 32-bit digital signal processing device capable of supporting a wide range of applications. These applications include digital control, digital audio, graphics processing, image processing, speech recognition, high-speed modems, low bit-rate codecs, filtering, and multi-channel signaling systems. Support tools include a full Kernighan and Ritchie C compiler optimized for the DSP32's architecture. A pipelined architecture allows the DSP32 device to achieve high throughput. This architecture includes a 32-bit floating point arithmetic unit that performs 12.5 million floating point computations per second and a 16-bit integer arithmetic unit that executes 6.25 million instructions per second. The DSP32 device is implemented using NMOS technology and is available in a 40-pin DIP or a 100-pin pin-grid-array (PGA) package. The PGA package provides pins for an external 32-bit data bus and a 16-bit address bus for use with external memory expansion.

### Architectural Summary

The DSP32 uses two execution units to achieve its high throughput. The Control Arithmetic Unit (CAU) is used as a 16-bit microprocessor, or it may be used to generate and modify addresses for the Data Arithmetic Unit (DAU). The CAU performs ALU and data move instructions as well as conditional and unconditional branch operations. When used to generate addresses for the DAU, it can generate and post-modify four addresses in a single instruction cycle.

The DAU employs a straightforward three-stage fetch/multiply/accumulate pipeline for 32-bit floating point operands. Results are automatically normalized without additional instructions or pipeline stages. On-chip memory consists of two 512-word banks of RAM and one 512-word ROM bank. External memory is expandable to 56 Kbytes (directly addressable). Full speed execution and accesses of instructions and data is presented for the entire external address space.

Serial and parallel ports which support DMA are provided to ease interfacing.

### Features

- 25 MHz version (160 ns)
- 16 MHz version (250 ns)
- Twenty-one 16-bit general purpose registers
- Four 40-bit accumulators
- 32-bit floating point arithmetic
- 32-bit instructions
- Full C compiler
- All instructions are single-cycle
- 16-bit integer microprocessor operations for logic and control
- User-selectable memory configurations
- Data addressable as 8-, 16-, or 32-bit words
- Mask-programmable ROM
- 2048 bytes of ROM organized as 512 × 32 bits
- 4096 bytes of RAM organized as two banks of 512 × 32 bits
- 56 Kbytes of direct memory addressing off-chip with pin-grid-array package
- No speed penalty for off-chip program or data memory
- Serial and parallel I/O ports with DMA
- Interfaces to a microprocessor without any additional peripherals
- Error control logic to detect and mask errors
- Available in 40-pin DIP or 100-pin pin-array package
- Supported by:
  DSP32-SL Software Library
  DSP32-DS Development System
  DSP32-CC C compiler
  DSP32-AL Application Library
  DSP32-AG Application Guide

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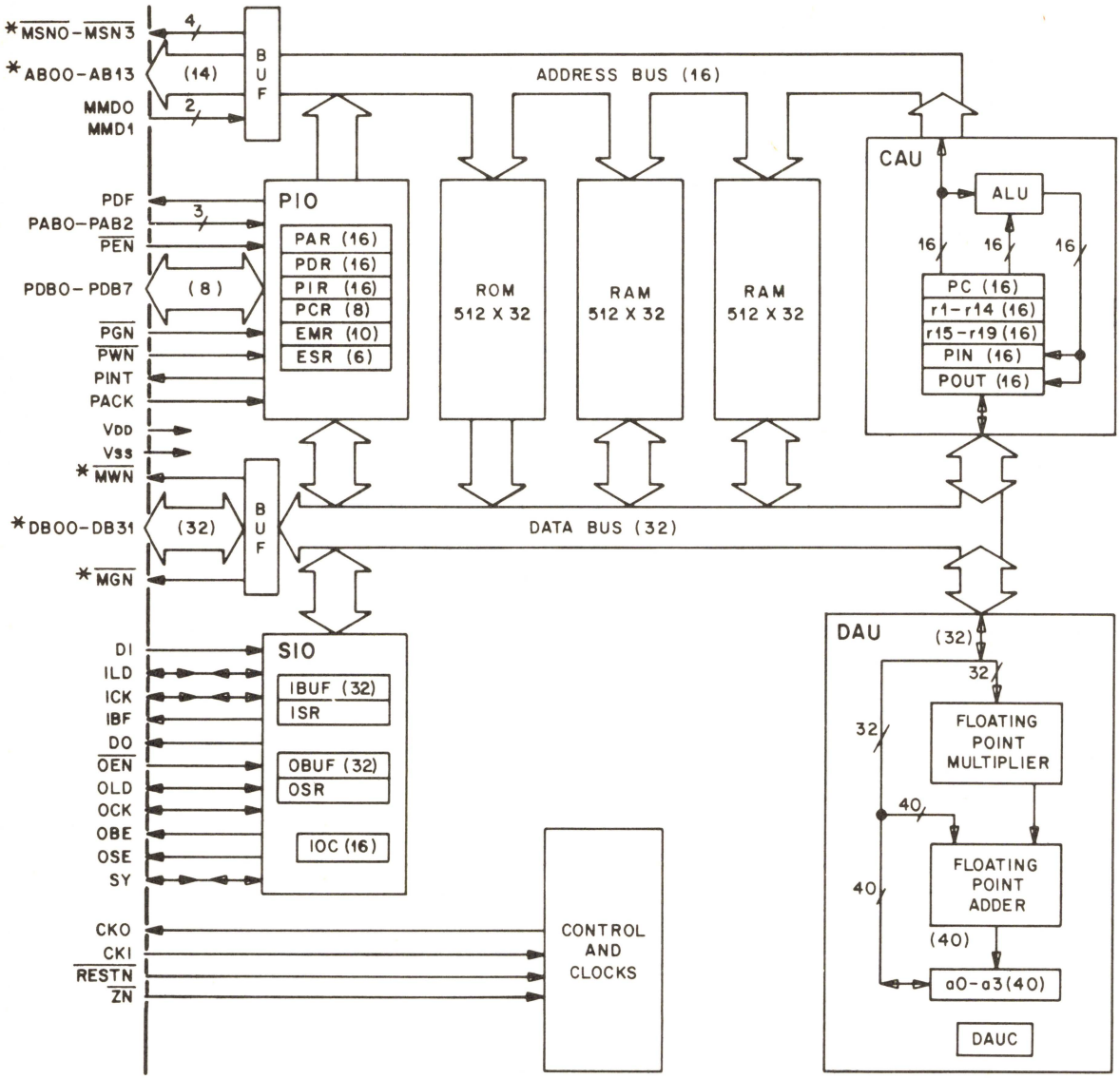
*Figure 1.* WE *DSP32 Digital Signal Processor Device Block Diagram*




*AVAILABLE ON 100-PIN PGA PACKAGE ONLY

*LEGEND:*

| | | | | | |
|---|---|---|---|---|---|
| **a0—a3** | Accumulators 0—3 | **IOC** | Input/Output Control Register | **PIO** | Parallel I/O Unit |
| **ALU** | Arithmetic Logic Unit | **ISR** | Input Shift Register | **PIR** | PIO Interrupt Register |
| **CAU** | Control Arithmetic Unit | **OBUF** | Output Buffer | **R1—r19** | Registers 1—19 |
| **DAU** | Data Arithmetic Unit | **OSR** | Output Shift Register | **PIN** | Pointer for Serial DMA Input |
| **DAUC** | Data Arithmetic Unit Control Register | **PAR** | PIO Address Register | **POUT** | Pointer for Serial DMA Output |
| | | **PC** | Program Counter | **RAM** | Read Write Memory |
| **EMR** | Error Mask Register | **PCR** | PIO Control Register | **ROM** | Read-Only Memory |
| **ESR** | Error Source Register | **PDR** | PIO Data Register | **SIO** | Serial I/O Unit |
| **IBUF** | Input Buffer | | | | |

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# DIGITAL

## *WE*® DSP32C Digital Signal Processor

### Description

The *WE* DSP32C Digital Signal Processor is the world's most advanced DSP. Targeted at high-performance applications, the DSP32C brings an unprecedented level of performance to the systems designer. Upward compatibility has been preserved with the DSP32, so current DSP32 users can easily upgrade to the DSP32C if greater performance is desired. The DSP32C features a 16 Mbyte address space, vectored interrupts, a full C compiler, enhanced instruction set, and powerful format conversions.

### Architectural Summary

The DSP32C uses two execution units to achieve its high throughput. The Control Arithmetic Unit (CAU) is used as a 16- or 24-bit microprocessor, or it may be used to generate and modify addresses for the Data Arithmetic Unit (DAU). The CAU executes conditional and unconditional ALU and branch operations as well as data move instructions. When used to generate addresses for the DAU, it can generate and post-modify four addresses in a single instruction cycle.

The DAU employs a straightforward three-stage fetch/multiply/accumulate pipeline for 32-bit floating point operands. Results are automatically normalized without additional instructions or pipeline stages.

On-chip memory consists of three banks of RAM each with 512 words. A ROM coded version is also available which substitutes a 2048-word ROM for one 512-word RAM bank. External memory is expandable to 16 Mbytes (directly addressable). A flexible wait-state generator allows efficient use of slower memories and memory-mapped peripherals. Rather than imposing full instruction cycle penalty for each wait state, the DSP32C inserts one quarter of an instruction cycle for each wait state.

Both serial and parallel ports are provided to further ease interfacing. Input and output DMA to any location in the DSP32C address space is supported by both ports.

### Features

- 25 MHz version (80 ns)
- 40 MHz version (100 ns)
- Object code compatible with DSP32
- Twenty-two 24-bit general-purpose registers
- 32-bit floating point arithmetic
- Full C compiler
- 24-bit and 16-bit integer microprocessor operations for logic and control
- Data addressable as 8-, 16-, or 32-bit words
- 2048 words of ROM and 2 banks (512 words each) of RAM, or 3 banks (512 words each) of RAM
- 16 Mbytes of directly addressable off-chip memory
- Wait states for slow memories
- Powerful single-cycle data format conversions
  - — IEEE 754 floating point
  - — 24-bit and 16-bit integer
  - — 8-bit linear byte
  - — 8-bit $\mu$-law and A-law
- Serial and parallel ports with DMA
- Interfaces to a microprocessor without glue logic
- 8 vectored interrupts
- 133-pin PGA package

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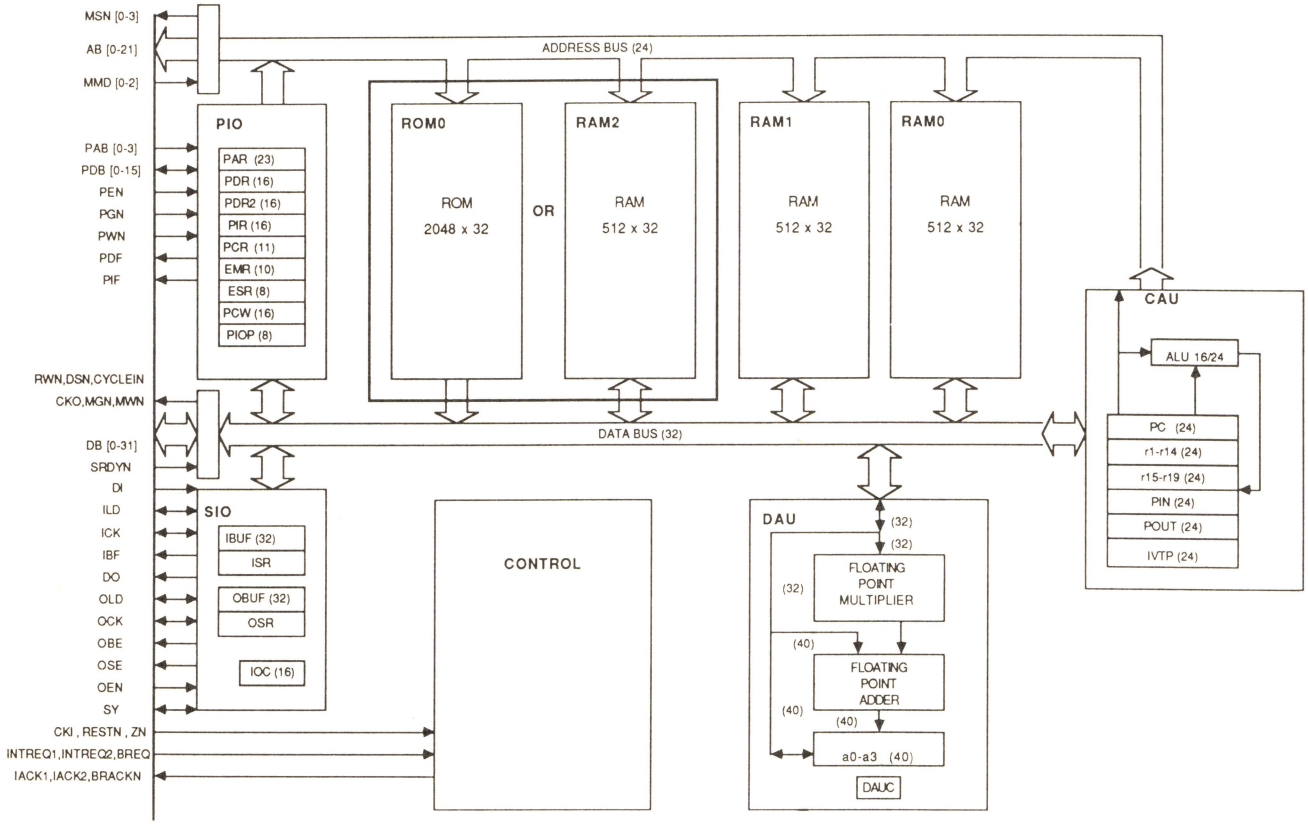
*Figure 1. Block Diagram of the DSP32C*

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*LEGEND:*

| | | | | | |
|---|---|---|---|---|---|
| **a0—a3** | Accumulators 0—3 | **IOC** | Input/Output ControlRegister | **PDR2** | PIO Data Register 2 |
| **ALU** | Arithmetic Logic Unit | **ISR** | Input Shift Register | **PIN** | Parallel Input Register |
| **CAU** | Control Arithmetic Unit | **IVTP** | Interrupt Vector Table Pointer | **PIO** | Parallel I/O Unit |
| **DAU** | Data Arithmetic Unit | **OBUF** | Output Buffer | **PIOP** | Parallel I/O Ports |
| **DAUC** | DAU Control Register | **OSR** | Output Shift Register | **PIR** | PIO Interrupt Register |
| **EMR** | Error Mask Register | **PAR** | PIO Address Register | **POUT** | Parallel Output Register |
| **ESR** | Error Source Register | **PC** | Program Counter | **r1—r19** | Registers 1—19 |
| **FPA** | Floating-Point Adder | **PCR** | PIO Control Register | **RAM** | Read/Write Memory |
| **FPM** | Floating-Point Multiplier | **PCW** | Processor Control Word | **ROM** | Read-Only Memory |
| **IBUF** | Input Buffer | **PDR** | PIO Data Register | **SIO** | Serial I/O Unit |

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# DIGITAL

## *WE*® DSP16 Digital Signal Processor

### Description

The DSP16 Digital Signal Processor integrated circuit is a 16-bit, high-speed, programmable digital signal processor. The device is fabricated in low-power CMOS technology and is available in two packages: an 84-pin plastic leaded chip carrier and an 84-pin ceramic pin grid array. It is a general-purpose building block that can be programmed to perform a wide variety of signal processing functions. It achieves high throughput with its parallel pipelined architecture without programming latencies or restrictions. The processor has an arithmetic unit capable of multiplying two 16-bit words of data and accumulating the product in a single 55 ns cycle. The arithmetic data is supplied by two independent addressing units. The DSP16 device can function in a stand-alone manner, requiring only an external clock.

### Architectural Summary

The DSP16 device contains a data arithmetic unit (DAU) that performs signal processing arithmetic; a ROM address arithmetic unit (XAAU); a RAM address arithmetic unit (XAAU); a RAM address arithmetic unit (YAAU); a 2048 by 16-bit ROM that contains program instructions and fixed data; a 512 by 16-bit RAM for variable data; an instruction cache (CACHE); a serial I/O unit (SIO); and a 16-bit parallel I/O unit (PIO).

The arithmetic unit contains a 16 × 16 bit parallel multiplier that generates a full 32-bit product in 55 ns. The product can be accumulated with one of two 36-bit accumulators. The data in these accumulators can be directly loaded from or stored to memory in two 16-bit words with automatic saturation on overflow. The ALU supports a full set of arithmetic and logical operations on either 16- or 32-bit data. A standard set of ALU conditions can be tested for conditional operations, branches, and subroutine calls. This allows the processor to perform as a powerful 16/32-bit microprocessor for logical and control applications.

Two addressing units support high-speed register-indirect memory addressing with post-modification of the register. Direct and immediate addressing is supported at a cost of only one additional instruction cycle and ROM location. Four address registers in the YAAU (r0—r3) can be used for either read or write addresses to the RAM, without restrictions. Registers j and k provide user-defined post-increments for the addresses. Fixed increments of 0, +1, −1, and +2 are also available. The YAAU also supports a flexible Modulo Addressing mode for efficient filter implementations. Registers rb and re are used to define the beginning and end of the modulo. Four compound addressing modes are provided to make read/write operations more efficient. In the XAAU, one register (pt) is used for ROM table look-up. Register i holds a user-defined post-increment. A fixed post-increment of +1 is also available. Register pc is the program counter. Registers pr and pi hold the return address for subroutine calls and interrupts.

The on-chip memory includes 4096 bytes of ROM organized as 2048 × 16 and 1024 bytes of RAM organized as 516 × 16. The ROM can be replaced with up to 64K words of external memory for prototyping or for applications that require frequent program modification.

An on-chip cache memory can be selectively used to store repetitive operations such as those found in a filter section. Up to 15 words in the cache can be repeated up to 127 times with no looping overhead. In addition, operations in the cache that require a ROM access (for example, fixed coefficients) will execute at twice the normal rate. The cache greatly reduces the need for writing repetitive code "inline" and therefore conserves ROM storage.

The DSP16 device has both serial and parallel I/O ports. The serial I/O unit is an asynchronous, full duplex, double-buffered channel operating at up to 10 Mb/s that easily interfaces with other DSP16 devices in a multiple DSP16 environment. AT&T codecs and Time Division Multiplex (TDM) channels can be interfaced to the DSP16 device with few (if any) additional components. The parallel I/O unit is capable of interfacing to a 16-bit bus containing other DSP16 devices, microprocessors, or peripheral I/O devices. Data rates of up to 145.5 Mb/s are possible through this port.

### Features

- 36.4 MHz version (55 ns)
- 26.6 MHz version (75 ns)
- Low-power CMOS technology
- Two 36-bit accumulators
- 16 × 16 multiply and 36-bit addition in 55 ns
- Instruction cache for high-speed, ROM efficient vector operations
- 2048-word ROM, 512-word RAM (on-chip)
- Off-chip ROM expansion to 64K-word
- Serial and parallel I/O ports with multi-processor capability
- Five maskable interrupts
- Single +5 V power supply
- Supported by *WE* DSP16-SL Support Software Library and *WE* DSP16-DS Digital Signal Processor Development System

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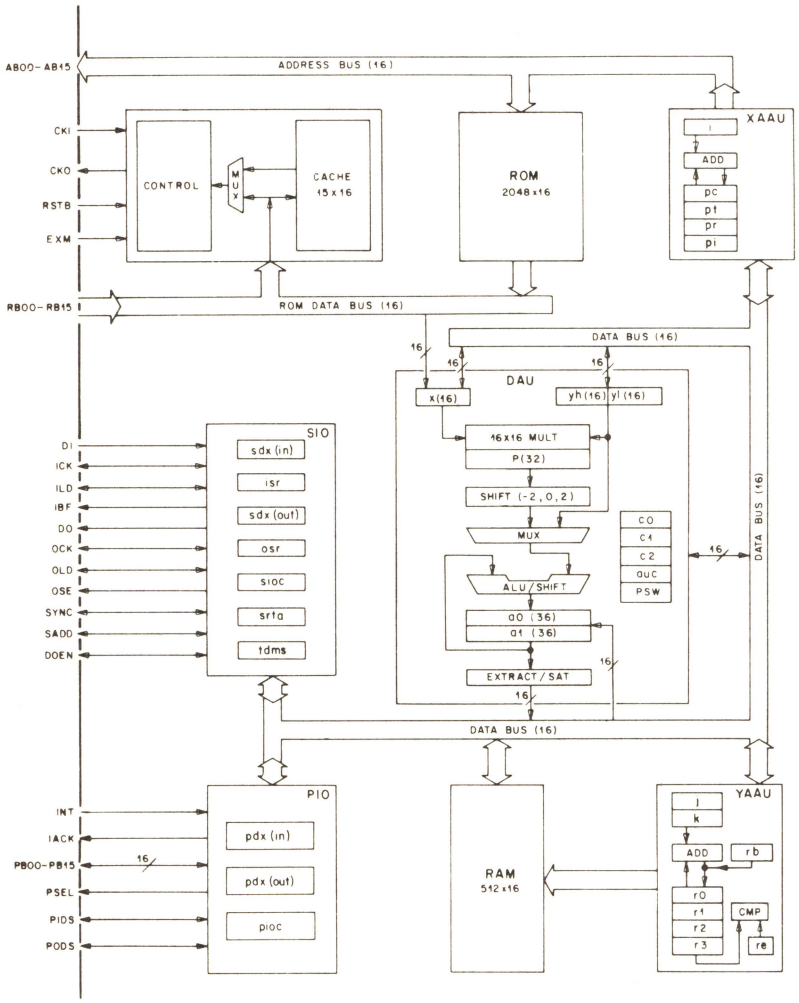
*Figure 1. Block Diagram of the DSP16*




*LEGEND:*

| | |
|---|---|
| **16 × 16 Mult** | 16-bit by 16-bit Multiplier |
| **a0—a1** | Accumulators 0—1 |
| **ADD** | Adder |
| **ALU/SHIFT** | Arithmetic Logic Unit/Shifter |
| **auc** | Arithmetic Unit Control |
| **c0—c2** | Counters 0—2 |
| **CMP** | Comparator |
| **DAU** | Data Arithmetic Unit |
| **i** | Increment Register |
| **isr** | Input Shift Register |
| **j** | Increment Register |
| **k** | Increment Register |
| **MUX** | Multiplexer |
| **osr** | Output Shift Register |
| **p** | Product Register |
| **pc** | Program Counter |
| **pdx(in)** | Parallel I/O Data Transmit Input Register |
| **pdx(out)** | Parallel I/O Data Transmit Output Register |
| **pi** | Program Interrupt Register |
| **PIO** | Parallel I/O Unit |
| **pioc** | Parallel I/O Control Register |
| **pr** | Program Return Register |
| **psw** | Processor Status Word |
| **pt** | ROM Table Pointer |
| **r0—r3** | RAM Pointer Registers 0—3 |
| **RAM** | Read/Write Memory |
| **rb** | Modulo Addressing Register |
| **re** | Modulo Addressing Register |
| **ROM** | Read Only Memory |
| **sdx(in)** | Serial Data Transmit Input Register |
| **sdx(out)** | Serial Data Transmit Output Register |
| **SIO** | Serial I/O Unit |
| **sioc** | Serial I/O Control Register |
| **srta** | Serial Receive/Transmit Address Register |
| **tdms** | Serial I/O Time Division Multiplex Signal Control Register |
| **x** | Multiplier Input Register |
| **XAAU** | ROM Address Arithmetic Unit |
| **YAAU** | RAM Address Arithmetic Unit |
| **yh** | y(high) DAU Register |
| **yl** | y(low) DAU Register |

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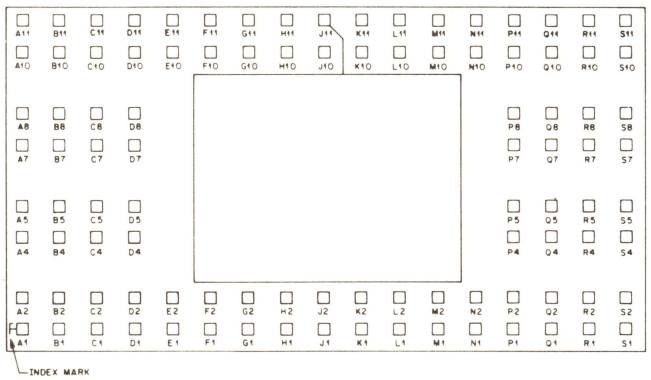
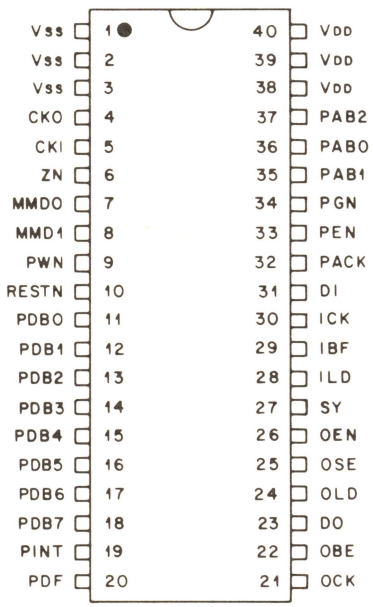
### DSP32 Pin Assignments

*100-Pin Rectangular PGA Diagram*




*40-Pin DIP*




### DSP32 Digital Signal Processor Pin Names

| Symbol | Pin |
|---|---|
| **AB00-AB07** | D11, D10, C11, C10, B11, B10, A11, A10 |
| **AB08-AB13** | D8, D7, C8, C7, B8, B7 |
| **DB00-DB07** | A1, A2, B1, B2, C1, C2, D1, D2 |
| **DB08-DB15** | E2, F1, F2, G1, G2, H1, H2, J1 |
| **DB16-DB23** | J2, K1, K2, L1, L2, M1, M2, N2 |
| **DB24-DB31** | P1, P2, Q1, Q2, R1, R2, S1, S2 |
| **MMD0-MMD1** | F11, F10 |
| **MGN** | D4 |
| **MWN** | D5 |
| **MSN0-MSN3** | A7, A5, B5, B4 |
| **PDB0-PDB7** | P11, Q11, Q10, R11, R10, S11, S10, R8 |
| **PAB0-PAB2** | L11, L10, K11 |
| **PACK** | P10 |
| **PEN** | N10 |
| **PGN** | M11 |
| **PWN** | M10 |
| **PINT** | Q8 |
| **PDF** | P8 |
| **DI** | P7 |
| **IBF** | Q5 |
| **ICK** | R7 |
| **ILD** | Q7 |
| **DO** | Q4 |
| **OBE** | P5 |
| **OCK** | S7 |
| **OLD** | S5 |
| **OSE** | R4 |
| **OEN** | P4 |
| **SY** | R5 |
| **CKI** | E10 |
| **CKO** | H11 |
| **RESTN** | G10 |
| **ZN** | G11 |
| **VDD** | E1, N1, E11, N11 |
| **Vss** | A4, S4, A8, S8, J11 |



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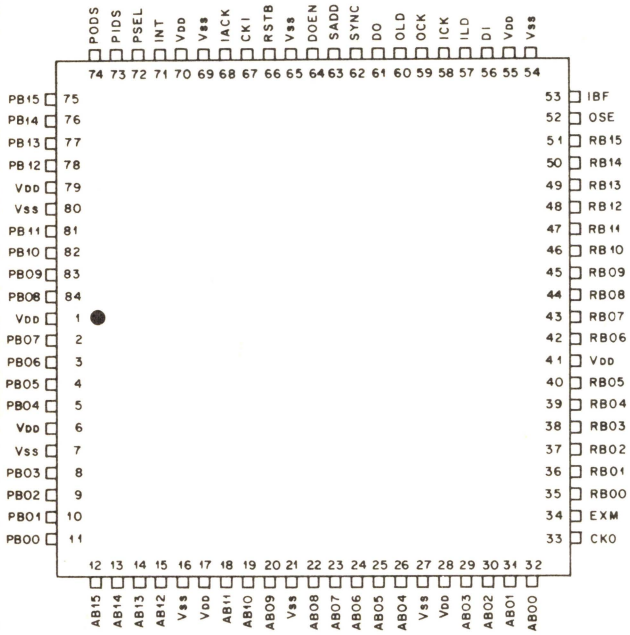
### DSP16 Pin Assignments

*84-Pin Chip Carrier Diagram*




### DSP16 Digital Signal Processor Pin Names

| Symbol | Pin |
|---|---|
| **AB00-AB07** | 32-29, 26-22 |
| **AB08-AB15** | 20-18, 15-12 |
| **CKI** | 67 |
| **CKO** | 33 |
| **DI** | 56 |
| **DO** | 61 |
| **DOEN** | 64 |
| **EXM** | 34 |
| **IACK** | 68 |
| **IBF** | 53 |
| **ICK** | 58 |
| **ILD** | 57 |
| **INT** | 71 |
| **OCK** | 59 |
| **OLD** | 60 |
| **OSE** | 52 |
| **PB00-PB07** | 2-5, 8-11 |
| **PB08-PB15** | 75-78, 81-84 |
| **PIDS** | 73 |
| **PODS** | 74 |
| **PSEL** | 72 |
| **RB00-RB05** | 35-40 |
| **RB06-RB15** | 42-51 |
| **RSTB** | 66 |
| **SADD** | 63 |
| **SYNC** | 62 |
| **VDD** | 1, 6, 17, 28, 41, 55, 70, 79 |
| **VSS** | 7, 16, 22, 27, 54, 65, 69, 80 |

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### *WE* DSP16 and *WE* DSP32 Devices

| Device Type | Pkg | Design Series | Speed (ns) | Availability | |
|---|---|---|---|---|---|
| | | | | Samples | Production |
| *WE* DSP16 | M | 02 | 075 | Now | Now |
| | | | 055 | Now | Now |
| *WE* DSP32 | C | 08 | 250 | Now | Now |
| | | | 160 | Now | Now |
| | G | 08 | 250 | Now | Now |
| | | | 160 | Now | Now |
| | R | 08 | 250 | 1Q88 | 3Q88 |
| | | | 160 | 1Q88 | 3Q88 |
| *WE* DSP32C | R | 10* | 100 | 3Q88 | — |
| | | | 080 | 3Q88 | — |
| | R | 11* | 100 | 4Q88 | 1Q89 |
| | | | 080 | 4Q88 | 1Q89 |

Packages: M = Plastic Leaded Chip Carrier
C = Hermetic Ceramic DIP
G = Hermetic Ceramic Rectangular PGA
R = Hermetic Ceramic Square PGA

* These are the CMOS (DSP32C) devices.

### *WE* DSP16 and *WE* DSP32 Development Tools

| Device Type | Tool Type | O.S./Host | Media | Availability |
|---|---|---|---|---|
| *WE* DSP16 | SL | MS-DOS | F | Now |
| | | UN5VX | T | Now |
| | | UN5B2 | F | Now |
| | | VMS | T | Now |
| | | UNB42 | T | Now |
| | | BKSUN | C | Now |
| | AL | MS-DOS | F | Now |
| | DS | — | — | Now |
| *WE* DSP32 | SL | MS-DOS | F | Now |
| | | UN5VX | T | Now |
| | | UN5B2 | F | Now |
| | | UNB42 | T | Now |
| | | BKSUN | C | Now |
| | CC | * | — | 2Q88 |
| | AL | MS-DOS | F | Now |
| | DS | — | — | Now |
| *WE* DSP32C | SL | MS-DOS | F | 1Q88 |
| | | UN5VX | T | 1Q88 |
| | | UN5B2 | F | 1Q88 |
| | | UNB42 | T | 1Q88 |
| | | BKSUN | C | 1Q88 |
| | CC | * | — | 2Q88 |
| | AL | MS-DOS | F | 1Q88 |
| | DS | — | — | 3Q88 |

O.S./Host: MS-DOS = *MS-DOS* (AT&T PC6300 and Compatibles)
UN5VX = *UNIX* V (VAX 11/780 Series)
UN5B2 = *UNIX* V (3B2 Series)
VMS = *VMS* (VAX 11/780 Series)
UNB42 = *UNIX* Berkeley 4.2 (VAX 11/780 Series)
BKSUN = *UNIX* Berkeley 4.2 (Sun Series)

Media: T = 1600 BPI Magnetic Tape
F = 5¼" DSDD Diskettes

* Operating Systems Supported
— *MS-DOS*
— *UNIX* V
— *UNIX* Berkeley 4.2

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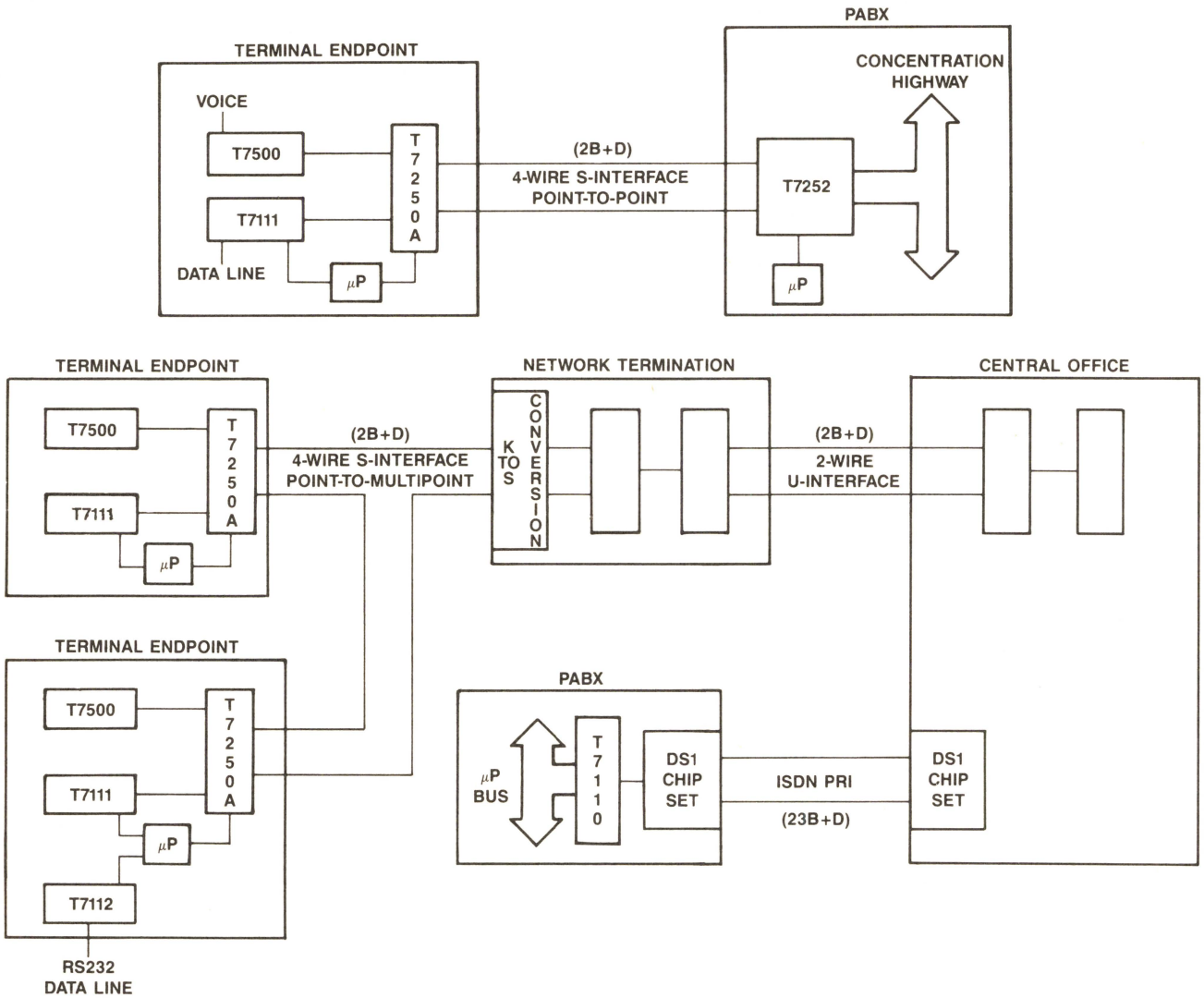
## Typical ISDN Interface Using AT&T Integrated Circuits

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# INTERFACE

## Digital Encryption Processor — T7000A

### Description

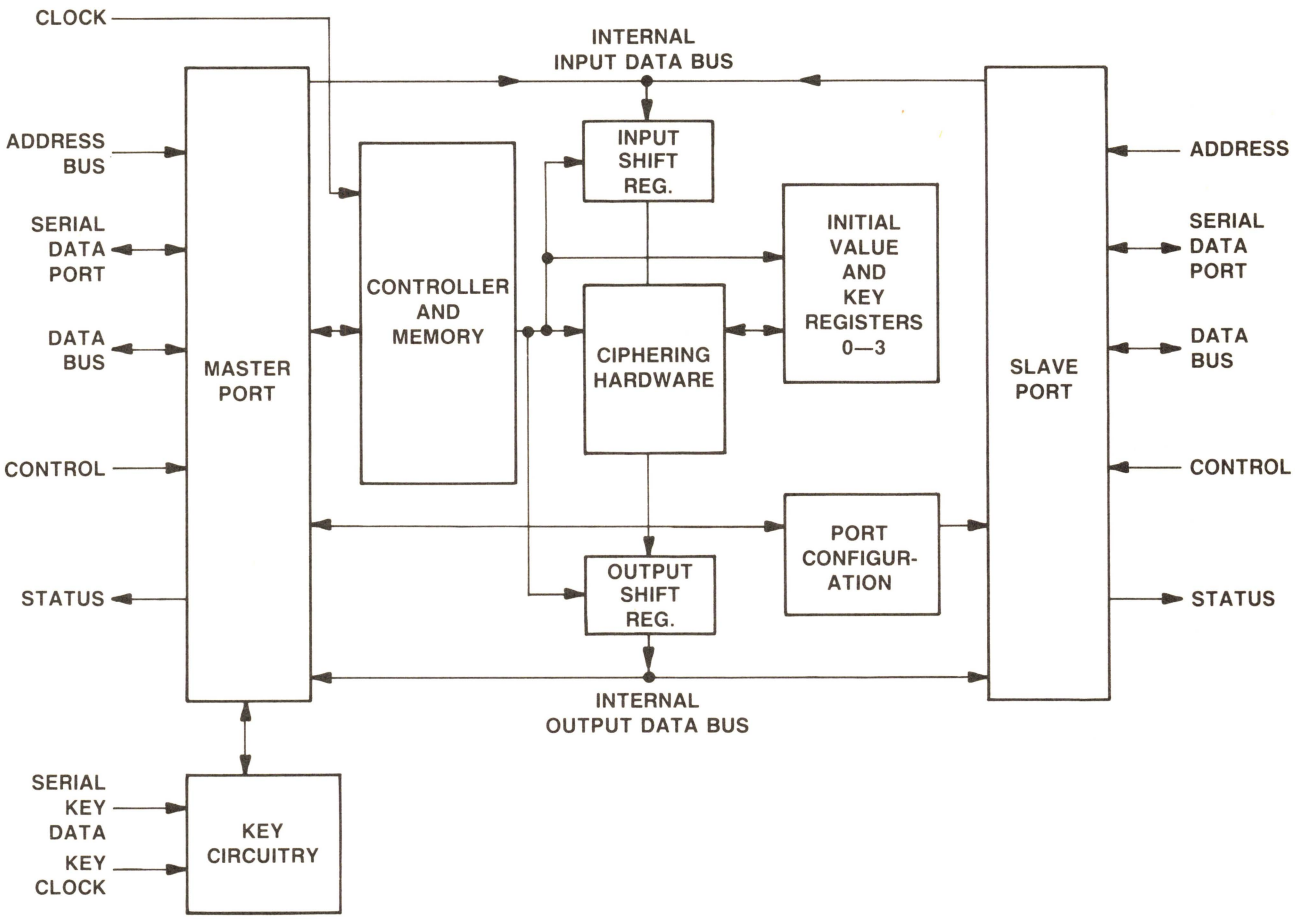
The Digital Encryption Processor (DEP) provides a low-cost, high security cryptographic system for encrypting and decrypting digital signals. It implements the four data encryption standard (DES) modes specified by the National Bureau of Standards (NBS), and is capable of performing multiple encryption operations or multiplexed key and initial value ciphering.

This programmable device provides a ciphering rate of 235,000 operations/second for any of the DES modes. It is manufactured using CMOS technology, requires a single +5 volt supply, and is packaged in a 40-pin plastic DIP.

### Features

- Programmable DES ciphering modes
- Programmable multiple or multiplexed ciphering
- On-chip RAM and ROM
- Separate parallel and/or serial plain-text and cipher-text ports
- Separate serial key input port
- Data throughput of 1.882 Mbytes/s using the entire DES output block
- Validated by the NBS

### T7000A DEP Block Diagram

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### Description

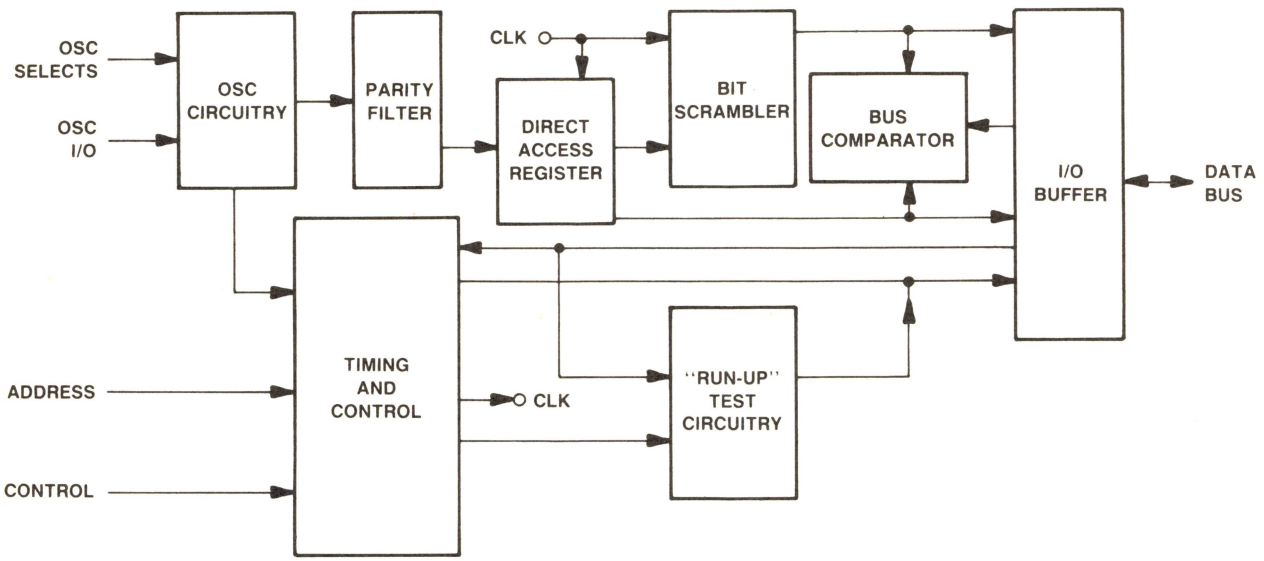
The Random Number Generator (RNG) produces random bits based on the phase jitter of a free-running oscillator. The output data stream of this device is truly random (not pseudorandom). In the data encryption unit, the RNG generates a random number that can be used as a session key.

This device is fabricated in CMOS technology, requires a single +5 volt supply, and is available in a 32-pin plastic DIP.

### Features

- On-chip or external HF oscillator source option
- On-chip or external jitter oscillator source option
- Generation of a 536-bit random number available in 8-bit bytes
- Internal elementary randomness check with external access to generated statistics

### T7001A RNG Block Diagram

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# INTERFACE

## Clock Recovery Circuits — T7032 & T7033

### Description

The T7032 and T7033 Clock Recovery Circuits operate over a 1 MHz to 50 MHz frequency range. The T7032 device provides clock recovery, data retiming, and a polynomial-based descrambler. The T7033 device is similar but without the descrambler and associated output mux. These devices accept TTL-NRZ data from a receiver (optical or electrical), recover the clock, and retime the data to the recovered clock. The inputs and outputs are TTL-compatible and the circuits require a single +5 V supply. The clock recovery circuits are manufactured using CMOS technology and are available in a 300 mil, 20-pin plastic DIP.

### Features

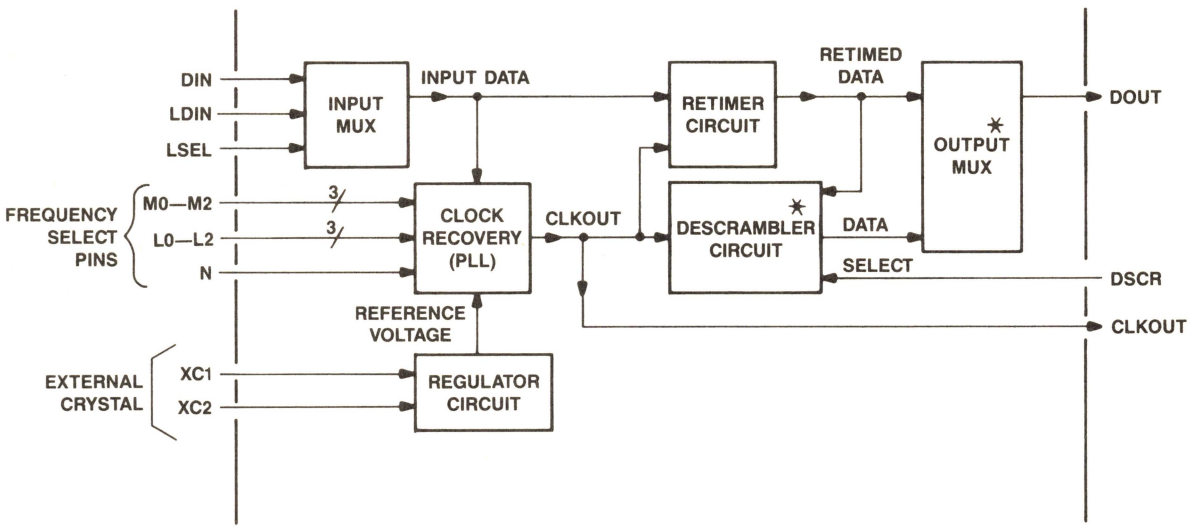
- Pin-programmable for 1 MHz to 50 MHz operation
- Fiber and wire applications
- Single +5 V supply
- Only one external component required: 3.58 MHz crystal

### System Applications

The clock recovery circuits are used for a variety of applications:

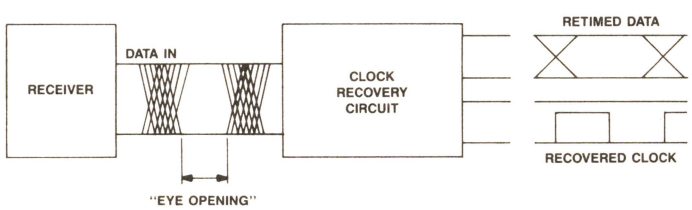
- Optical data links
- Multiplexers
- Digital PBXs
- Cluster concentrators
- Local area networks
- Front end processors
- Terminals and workstations
- Communications test equipment

### Clock Recovery Circuit Block Diagram




* The T7033 device does not contain the descrambler or output mux.

### Application Diagram

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# INTERFACE

## X.25 Protocol Controller — T7100A

### Description

The T7100A X.25 Protocol Controller, also known as XPC-8, implements the data link control functions defined in the X.25 packet switching communication standard for an 8-bit data bus. The level-2 protocol controller is fabricated using NMOS silicon gate technology, is TTL-compatible, and may be interfaced with an 8-bit microprocessor. It is available in a 48-pin nonhermetic ceramic DIP.

### Features

- DMA with standard interface including DMA request, DMA acknowledge, DMA read, and DMA write
- Programmable timers and window size
- Serial data rate of 250 kb/s
- Wait-state generator (on DMA side) for slow memory
- Two independent test modes to verify the XPC-8 and its link

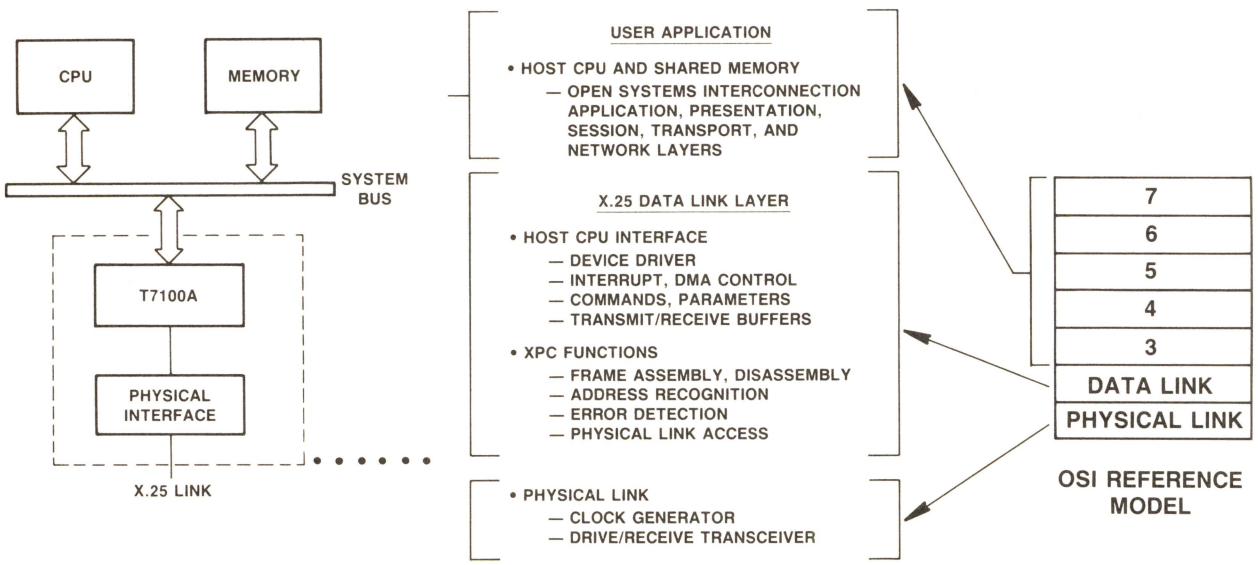
### System Applications

The X.25 Protocol Controller provides a building block for data communications in a packet switching environment.

The XPC-8 transmits and receives frames using the X.25 packet switching network access protocol. (A frame is defined as a block of information transferred over an access link.) It implements level 2 link interface, so minimum intervention by the central processing unit (CPU) is needed when sending and receiving frames.

In this common bus application, the XPC-8 is used as a peripheral off the main system bus. The diagram also indicates the mapping between the seven X.25 levels and defines which functions are performed and where they are performed.

### XPC-8 Typical Application Diagram (with Mapping)

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# INTERFACE

## X.25/X.75 Protocol Controller — T7102A

### Description

The T7102A XPC device satisfies the X.25 link layer (level 2) requirements for a balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex serial data link. This device also implements X.75 level 2 protocol used in inter-network applications. It is bit-oriented with a maximum transmit and receive speed of 333 kb/s. A set of programmable registers control and record vital events during data transmission.

This single-chip LSI device, available in a 70-pin pin-grid-array package, is fabricated using NMOS silicon gate technology.

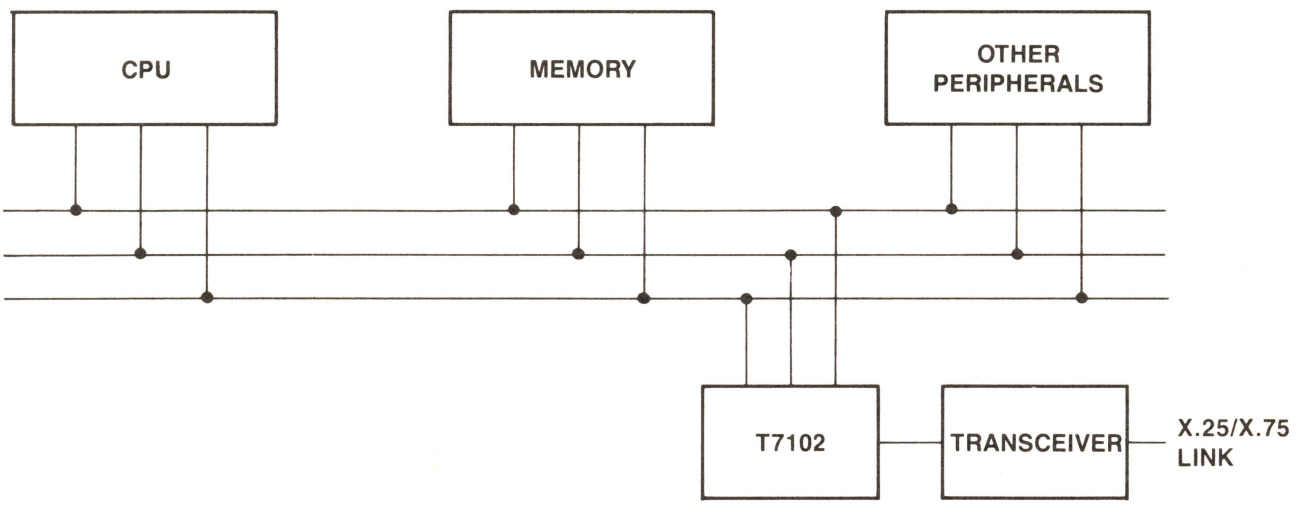
### Features

- 24-bit address bus to address 16-Mbyte address space
- Dual-channel DMA with standard interface including DMA request, DMA acknowledge, DMA read, and DMA write
- Independently programmable timers, retransmission counter, window size (transmit and receive), and Modulo 8 or 128 frame sequence numbering
- Daisy chain DMA for priority-controlled CPU interface
- Event counters and registers
- Supports 8-bit or 16-bit data buses

### System Applications

As with the other protocol controllers, the T7102A Protocol Controller is used for transmitting and receiving, and interpreting information between system elements. In addition, this device can read and write memory using either Intel or Motorola data byte ordering convention. Shown in the diagram below is an example of the XPC used in a common bus application.

### XPC Common Bus Application Diagram

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# INTERFACE

## Synchronous Protocol Data Formatter with Serial Interface — T7110

### Description

The T7110 Synchronous Protocol Data Formatter with Serial Interface (SPYDER-S) is a synchronous packet data communications controller. It is used to interface physical link level lines using bit-synchronous (HDLC/SDLC) protocols to 16-bit and 32-bit microprocessor systems. All inputs and outputs are TTL-compatible. The device is fabricated using CMOS technology, requires a single +5 volt power supply, and is packaged in a 68-pin plastic leaded chip carrier (PLCC).

### Features

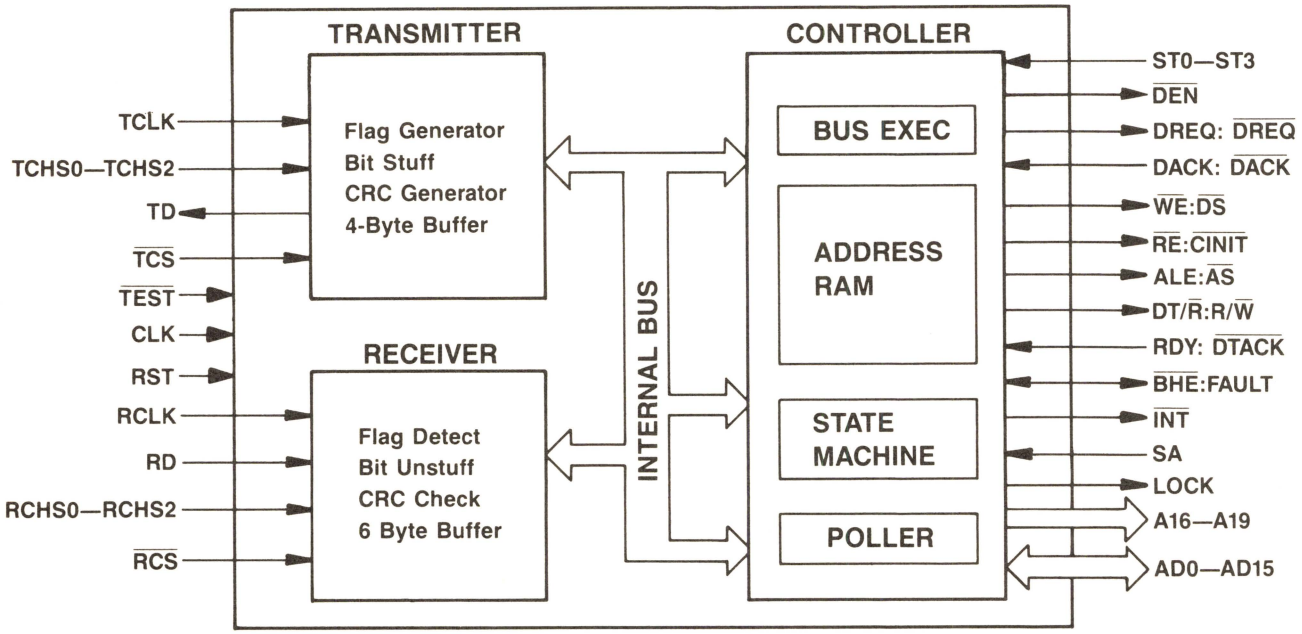
*Host Interface*

- Compatible with iAPX86, MC68000, or *WE*® 32100 Microprocessor systems
- On-chip 16-channel DMA memory address generator and buffer management with a 4 Mbyte/s maximum transfer rate
- Software register interface for maximum flexibility

*Serial Interface*

- 8-channel multiplexed serial input/output
- Automatic flag transmission and detection
- Zero bit insertion and deletion
- CRC generation and checking
- 2 Mb/s continuous serial data rate, 4 Mb/s instantaneous data rate

### T7110 SPYDER-S Block Diagram




LEGEND INTEL: MOTOROLA

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# INTERFACE

## Synchronous Packet Data Formatter — T7111

### Description

The T7111 Synchronous Packet Data Formatter (ANT) integrated circuit is used to interface physical link level lines using bit-synchronous HDLC/SDLC protocols to 8-bit microprocessor or microcontroller systems. All inputs and outputs of the T7111 ANT are TTL-compatible. It is implemented using CMOS technology and requires a single 5 V supply. The device is available in a 28-pin plastic DIP for standard through-hole mounting, or in a 28-pin plastic small-outline J-lead (SOJ) for surface mounting.

### Features

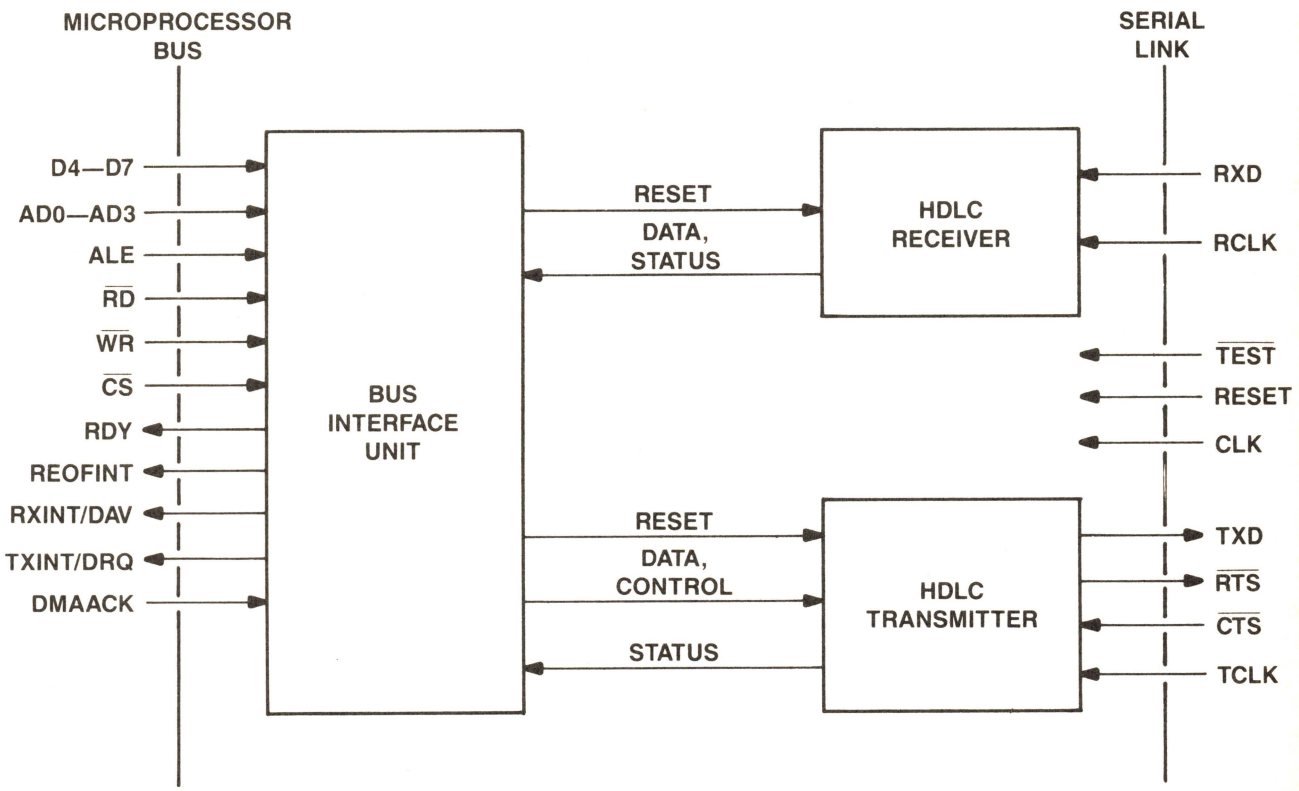
*Host Interface*

- Compatible with 8088 and 80188 microprocessor-based systems and 8051 microcontroller
- Compatible with 8237 and 8257 DMA controllers in extended write mode
- Programmable receive and transmit queue interrupts with variable fill levels
- Programmable receive and transmit DMA requests with variable fill levels

*Serial Interface*

- Separate receive and transmit clocks
- 4 Mb/s maximum data rate
- 6-byte receive queue
- Automatic flag transmission and detection
- Zero bit insertion and deletion for data transparency
- CRC-CCITT 16-bit polynomial generation and check with inhibit option

### T7111 ANT Block Diagram

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# INTERFACE

## Asynchronous Receiver/Transmitter Interface — T7112

### Description

The T7112 ARTI is an asynchronous, single-channel, full-duplex receiver/transmitter interface for terminals and modems. The ARTI is compatible with the bus protocol and timing specifications of both the 8051 microcontroller and the 8088 microprocessor. It may be used in a polled or interrupt driven system. The transmitter is quadruple buffered and the receiver has six buffers to reduce the interrupt overhead and the potential for overruns. The device is implemented in low-power, CMOS technology and is available in a 24-pin plastic DIP or a 28-pin plastic SOJ surface-mount package.

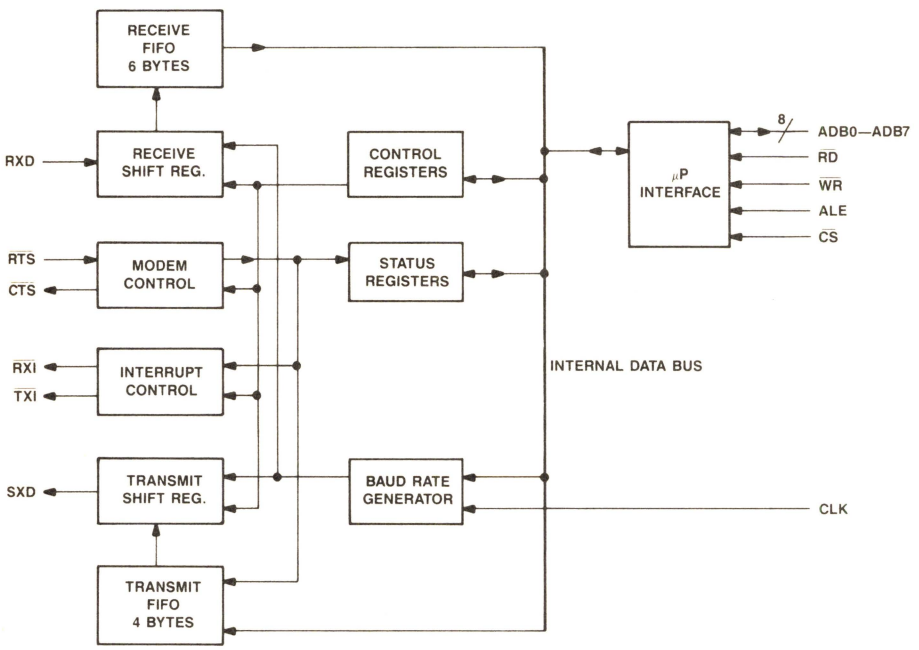
### Features

- Programmable data format:
  - — Seven data bits plus parity
  - — Odd, even, no parity
  - — One or two stop bits
- Six receive and four transmit data buffers
- 8088 (8 MHz) and 8051 (16 MHz) microprocessor interface without wait states
- Clear-to-send/request-to-send selectable signals for DTE or DCE modes and flow control
- Programmable interrupt systems:
  - — Full level interrupt of receive FIFOs (first-in, first-out)
  - — Receive break detection and error interrupt
  - — Empty level of transmit FIFO and error interrupt
- Transmit/receive FIFO status bits indicate FIFO levels
- Flexible polling capabilities
- On-chip baud rate generator
- Speedmatching (autobaud capability)

### System Application

As an asynchronous interface to customer terminals or modems, the ARTI provides standard UART functions with additional data buffering. In the illustrations below, the ARTI is used with EIA drivers and receivers to interface with data communications equipment (DCE) and with data terminal equipment (DTE).

### T7112 ARTI Block Diagram

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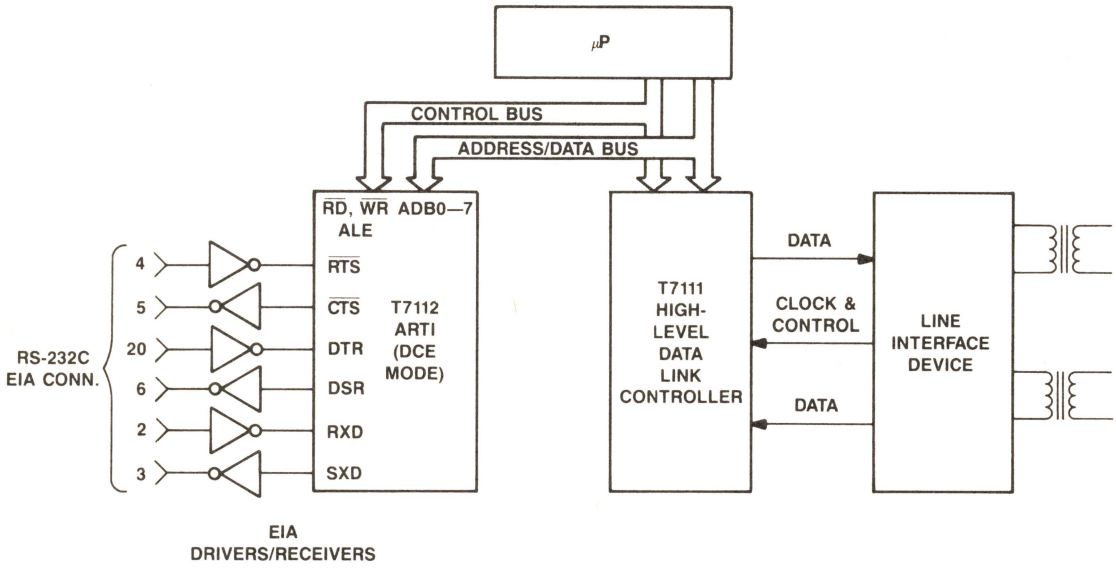
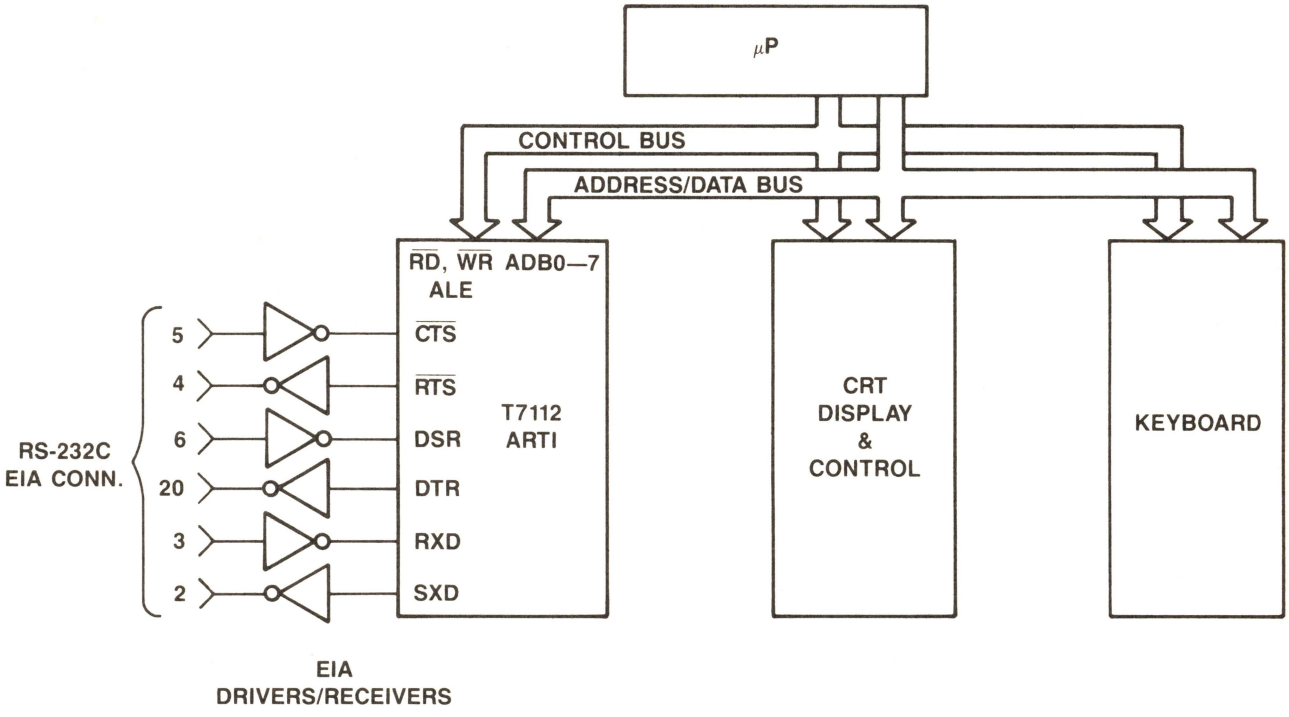
### Digital Communications Protocol/ISDN Data Module Application Diagram




### Terminal Application Diagram

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### Description

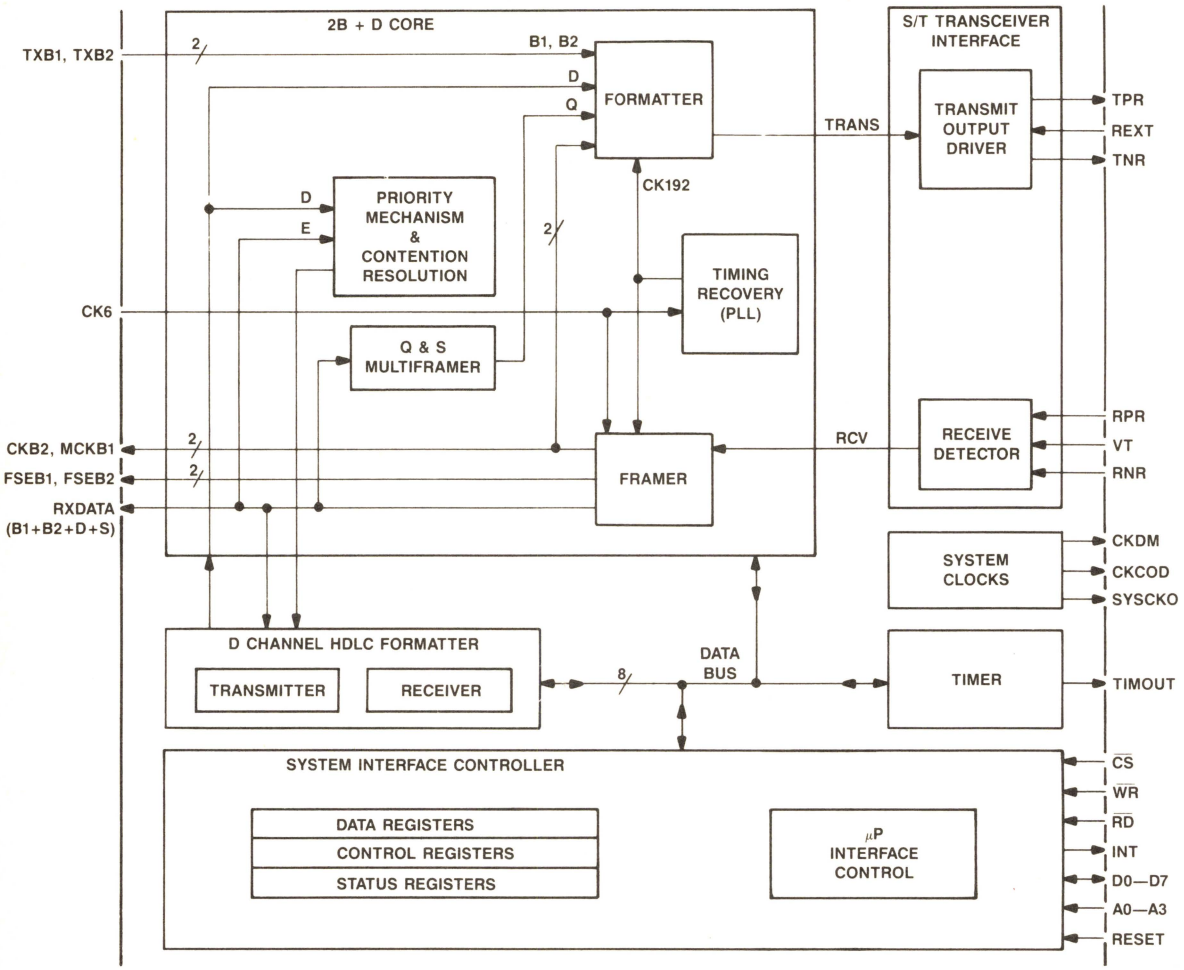
The T7250A S/T Interface circuit provides the line interface used for basic access service offered by the Integrated Services Digital Network (ISDN). The device conforms to all CCITT I.430 recommendations for point-to-multipoint configuration. Priority, contention resolution, multiframing, and activation/deactivation processes are fully supported. With a simple line interface circuit, I.430 impedance and voltage requirements can be met. An HDLC formatter and a sophisticated queue manager are provided to simplify the D channel interface.

This device is manufactured using CMOS technology, and is available in either a 40-pin plastic DIP or in a 44-pin plastic leaded chip carrier (PLCC). The 44-pin chip carrier provides additional 16/8 kHz and 6.149 MHz/192 kHz clocks that the 40-pin DIP does not have. The T7250A uses a nominal 5 volt supply and has a maximum power consumption of 100 mW.

### Features

- Built-in HDLC formatter for the D channel
- Programmable synchronization signal for codecs
- Power-up reset with a programmable timer for system interface control
- Interchangeable B channels for voice or data
- 16 bytes for transmit and receive buffer
- Local and remote loopback test modes

### T7250A S/T Interface for ISDN Block Diagram

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# INTERFACE

## User Network Interface Termination for Switches (UNITS) — T7252

### Description

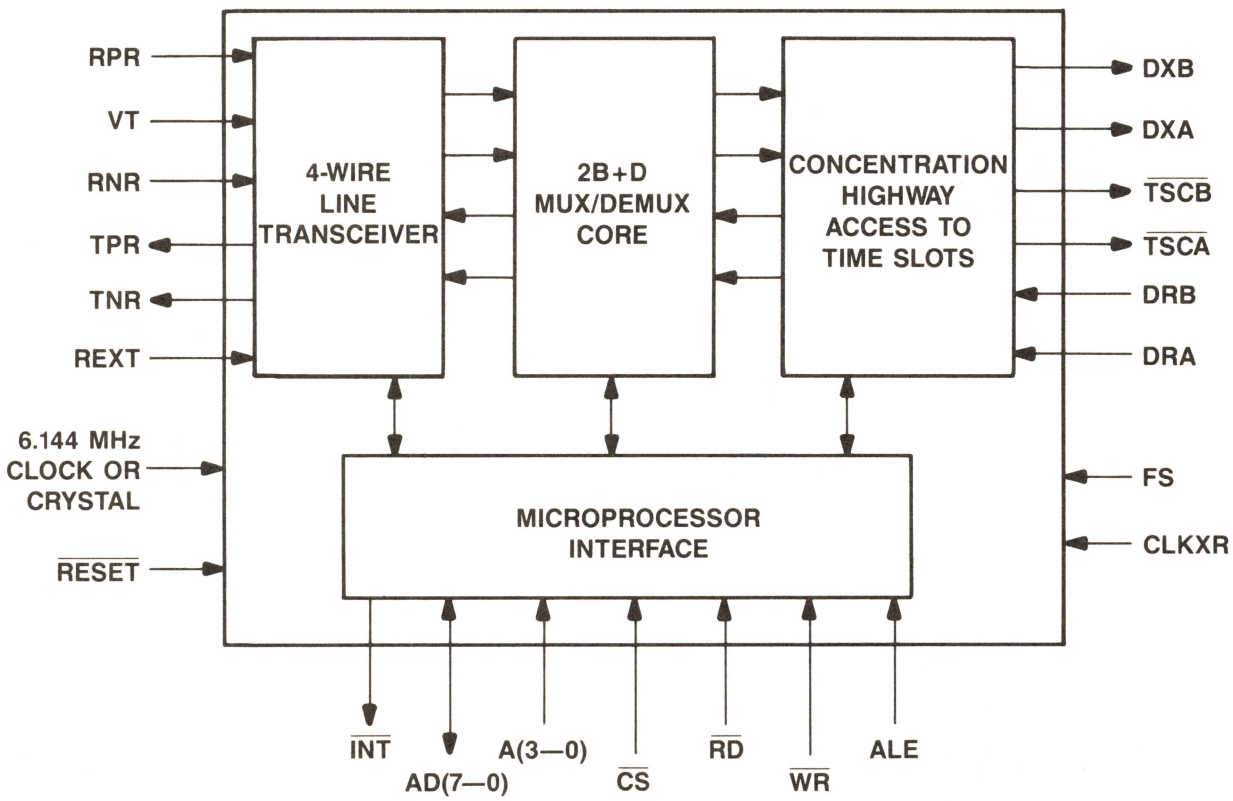
The T7252 User Network Interface Termination for Switches is a silicon integrated circuit that provides the user with level 1 network termination (NT) functions for ISDN. The T7252 UNITS provides full-duplex 2B+D communication at 192 kb/s over a four-wire digital subscriber loop. Channels B1 and B2 are 64 kb/s voice or data channels, and the D channel is a 16 kb/s control or data channel. All point-to-point and point-to-multipoint (passive bus) configurations are supported as defined in the 1986 version of CCITT Recommendation I.430 and the November, 1986 Draft US Specification. The T7252 UNITS communicates with a switching network over a user-configured time-division multiplexed (TDM) highway. A generic microprocessor interface is also provided.

The T7252 UNITS is manufactured in low-power 1.25 micron CMOS technology, and is available in either a 44-pin plastic leaded chip carrier or a 40-pin DIP. The T7252 UNITS operates on a 5 V power supply and has a maximum power consumption of less than 100 mW.

### Features

- Full-duplex 2B+D interface for point-to-point and point-to-multipoint (passive bus) configurations with automatic threshold adjustment
- B1, B2, and D channels separated from and combined into a 192 kb/s stream
- Two independent transmit/receive serial highways, with assignable time slots for voice/data transfer
- Generic parallel microprocessor interface, with either multiplexed or demultiplexed address/data lines and maskable interrupts
- Capability of direct microprocessor control of B1, B2, or D channel through the microprocessor interface
- Multiframing support, with access to the S (NT-to-TE) and Q (TE-to-NT) channels through microprocessor registers
- Provides I.430 interface for 2B+D applications in digital switches (PBXs, etc.)
- Selectable speeds on serial highway: 256 kHz (4 time slots) to 4.096 MHz (64 time slots)

### T7252 UNITS Block Diagram

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### Description

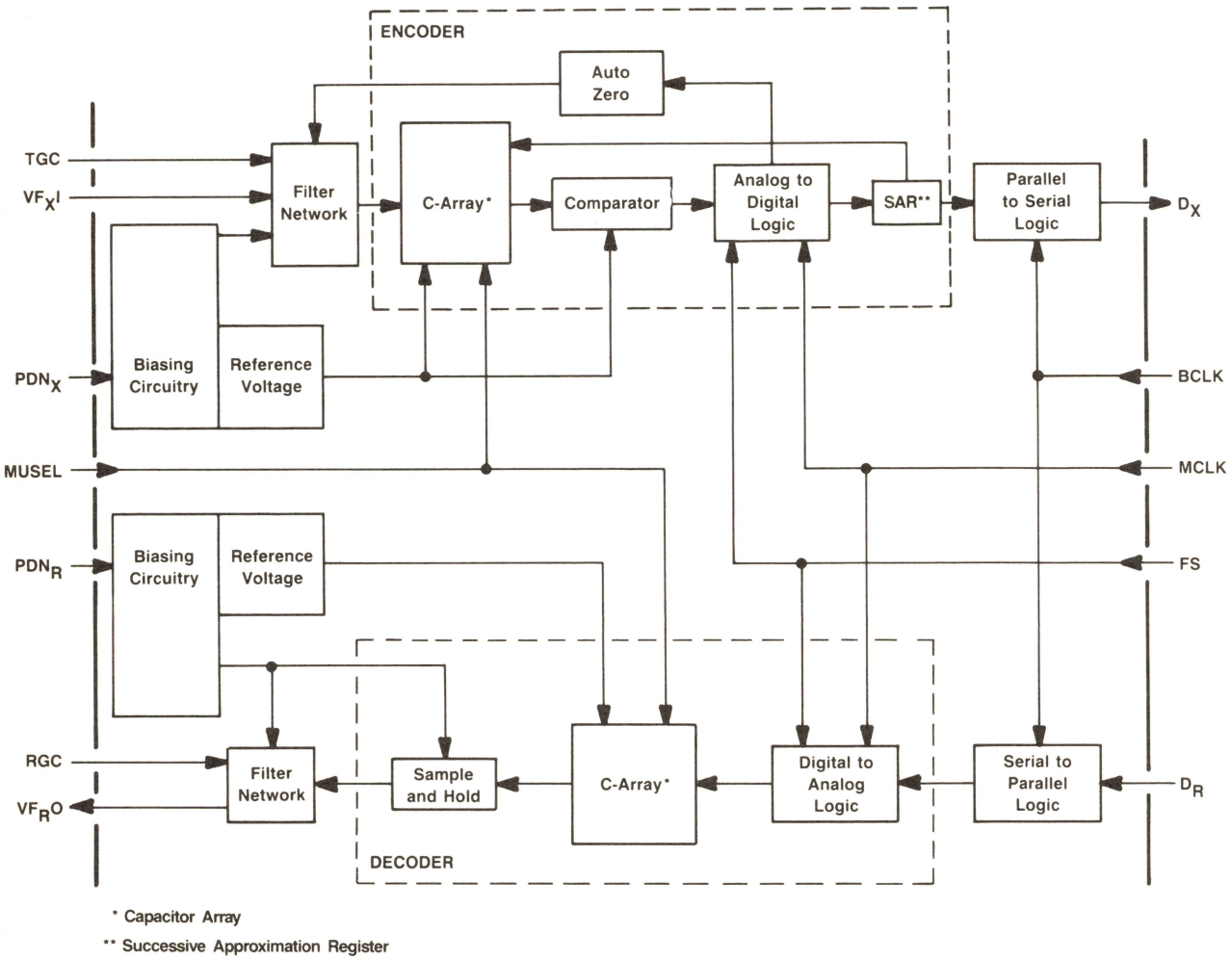
The T7500 PCM Codec with Filters integrated circuit performs the analog-to-digital and digital-to-analog translation functions in a circuit. It incorporates the transmit and receive filtering necessary to interface a voice telephone circuit to a time division multiplexed (TDM) system. The device is a full-duplex, 8-bit codec that operates from a ±5 volt power supply and provides A-law and/or μ-law conversion algorithms.

The T7500 codec is synchronized off the positive-going edge and has separate power-down for the transmitter and receiver. The device is manufactured using CMOS technology and is available in an 18-pin plastic DIP or in a 20-pin plastic SOJ. Custom configurations and/or special packages may be available on request.

### Features

- AT&T/CCITT compatible
- Pin selectable μ-law or A-law operation
- Pin selectable transmit and receive gain
- Variable data rate (128 kHz to 4.096 MHz)
- On-chip voltage reference
- Low power dissipation
- TTL-compatible inputs and outputs
- Low power dissipation
  - □ 20 mW typical power-down
  - □ 80 mW typical operation

### T7500 PCM Codec Block Diagram




* Capacitor Array

** Successive Approximation Register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# PCM Codec with Filters — T7512

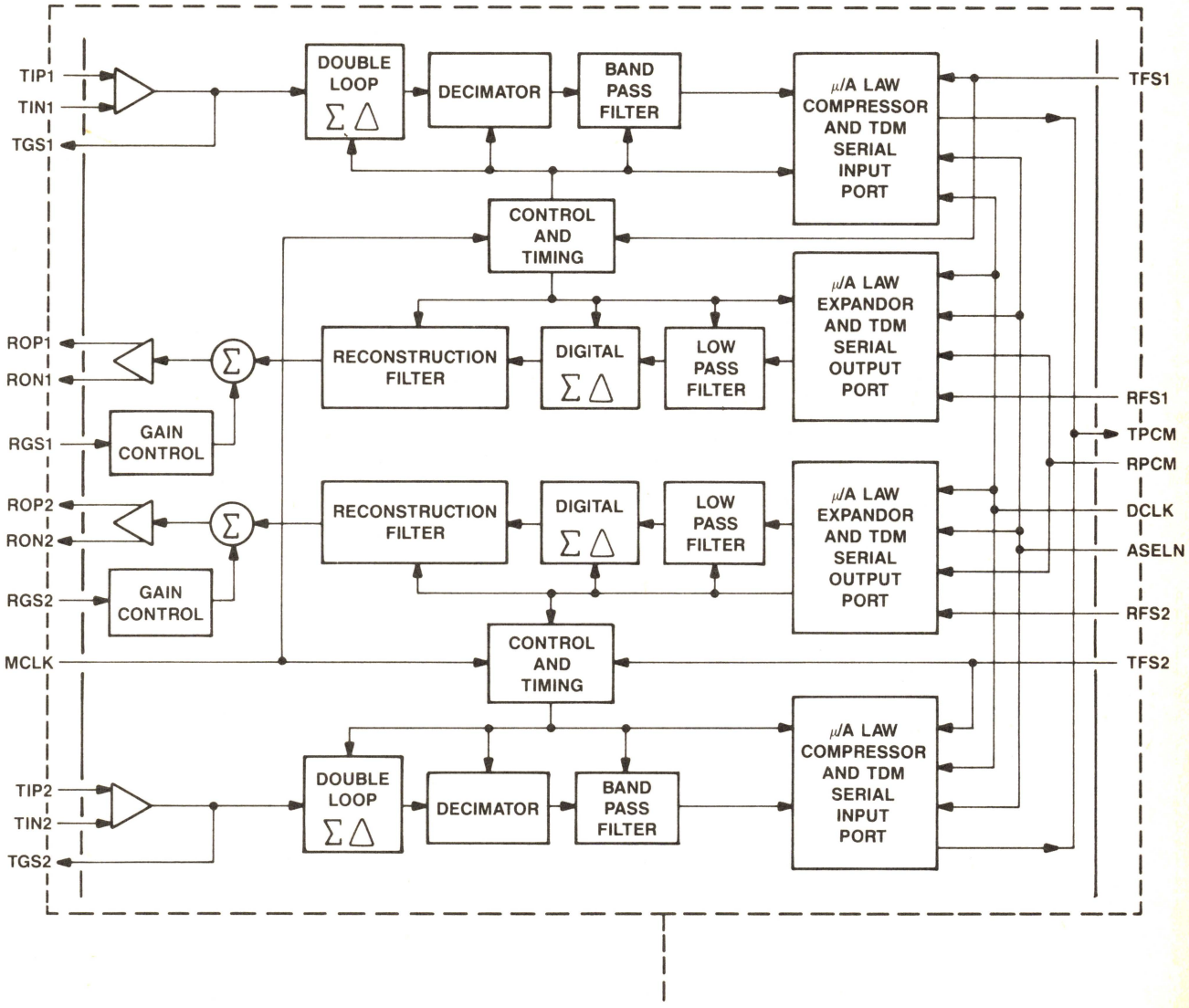
## Description

The AT&T T7512 integrated circuit is a dual PCM sigma-delta codec with transmit/receive filters. It provides two channels of analog-to-digital and digital-to-analog conversion as well as the transmit and receive filtering necessary to interface two voice telephone circuits to a time division multiplexed system. The device is fabricated using a low-power CMOS technology and requires a single +5 volt supply. It is available in either a 28-pin plastic DIP package or 28-pin plastic SOJ package.

## Features

- AT&T/CCITT-compatible
- Pin selectable $\mu$-law or A-law operation
- Transmit and receive gain control with external resistors
- Two timing modes
  - — Fixed data rate mode at 2.048 MHz
  - — Variable data rate mode — 128 kHz to 2.048 MHz
- On-chip voltage reference
- Differential output amplifier
- TTL-compatible inputs and outputs

## T7512 PCM Codec Block Diagram

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### Description

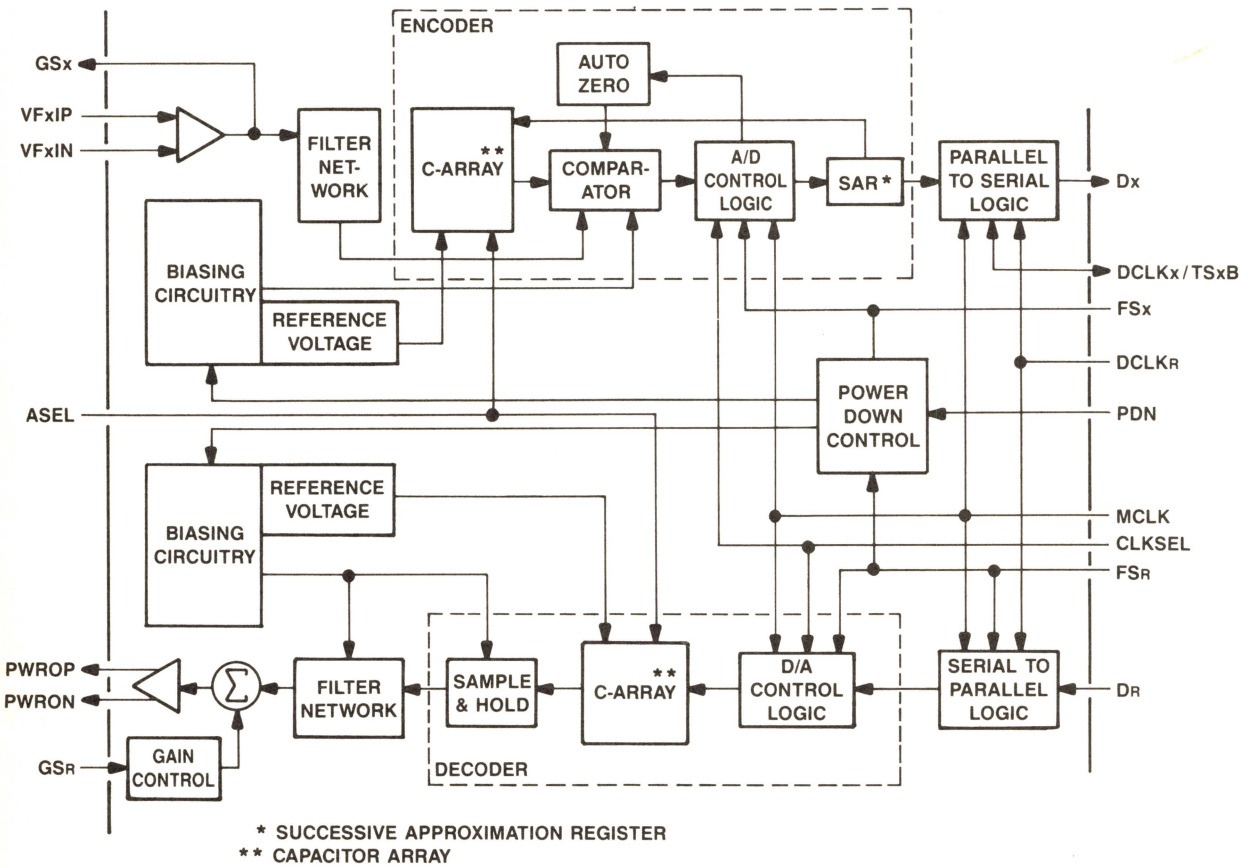
The T7513 PCM Codec with Filters integrated circuit performs the analog-to-digital and digital-to-analog translation functions in a circuit. It incorporates transmit and receive filtering of voice information for transmission via a digital network. The device is a full-duplex, 8-bit codec that operates from a ±5 volt power supply and provides A-law and/or μ-law conversion algorithms.

The T7513 codec is synchronized off the positive-going edge and has a chip power-down. The T7513 codec features differential analog inputs and outputs using an uncommitted on-chip operational amplifier. The device is manufactured using CMOS technology and is available in a 20-pin plastic DIP or 20-pin plastic SOJ. Custom configurations and/or special packages may be available on request.

### Features

- AT&T/CCITT compatible
- Pin-selectable μ-law or A-law operation
- 600 Ω drive capabilities
- Variable data rate (64 kHz to 2.048 MHz)
- On-chip voltage reference
- Low-power CMOS technology
- TTL-compatible inputs and outputs
- Replacement for industry-standard 2913 and 29C13 codecs

### T7513 PCM Codec Block Diagram

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# INTERFACE

## High-Precision PCM Codec with Filters — T7522

### Description

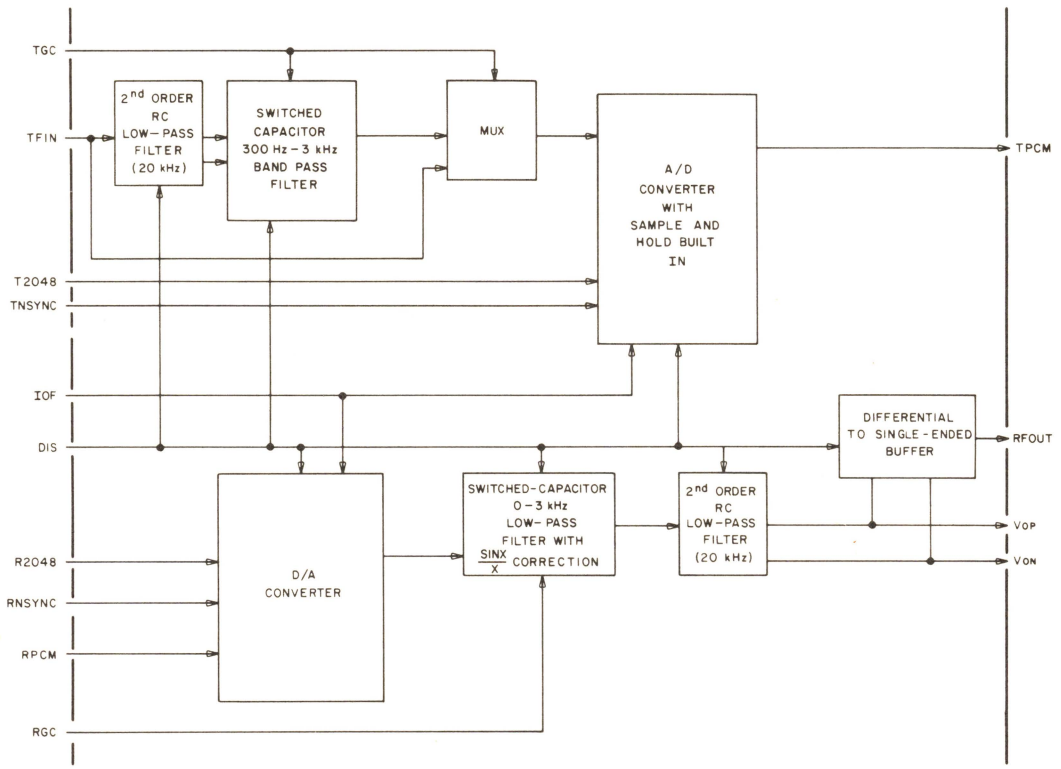
The T7522 High-Precision PCM Codec with Filters integrated circuit performs analog-to-digital and digital-to-analog conversion with 15-bit resolution and 10-bit linearity. The device provides anti-aliasing and reconstruction filters and a precision voltage reference. The device is designed for use in signal-processing applications that require PCM data with a higher resolution than PCM $\mu$-law data. The T7522 codec is a linear device with 16-bit PCM I/O data in 2's complement binary format. Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. This chip has programmable capabilities as LSB or MSB first I/O. The T7522 codec is manufactured using CMOS technology and is available in a 24-pin hermetic, ceramic DIP.

The T7522 can directly replace the T7520 and T7521 in applications not requiring independent A/D and D/A power-down options, and is recommended for all new designs. Designs requiring the independent A/D and D/A power-down options should use the T7523.

### Features

- Encoder and decoder with on-chip filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 120 mW nominal power
- Easy interface to a DSP device
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- Data format: 16-bit PCM in 2's complement binary (LSB or MSB first)
- Gain selection — transmit: 0 or −3 dB
  receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved power supply rejection ratio (PSRR)
- A/D filter/without filter selection
- A/D has sample and hold built in

### T7522 High-Precision PCM Codec Block Diagram

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# High-Precision PCM Codec with Filters — T7523

## Description

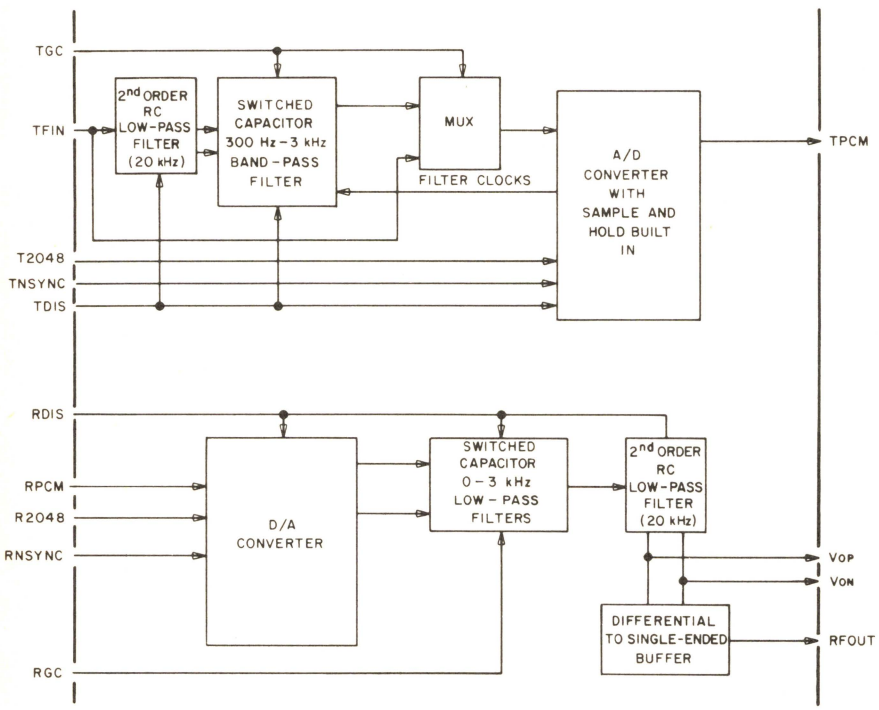
The T7523 High-Precision PCM Codec with Filters integrated circuit performs analog-to-digital and digital-to-analog conversion with 15-bit resolution and 10-bit linearity. The device is designed for use in signal-processing applications that require PCM data with a higher resolution than PCM $\mu$-law data. The T7523 Codec is a linear device with 16-bit PCM I/O data in 2's complement binary format (LSB first). Typical applications include the use of this Codec with echo cancelers, digital signal processors, and in data sets. The T7523 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic, ceramic DIP.

The T7023 is a pin-for-pin replacement and upgrade for the T7520 and T7521 Codecs, and is recommended as their replacement for all new designs. Applications requiring MSB first PCM I/O should use the T7522 Codec.

## Features

- Encoder and decoder with on-chip filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 120 mW nominal power
- Independent transmit and receive power-down
- Easy interface to industry-standard DSP devices
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- Data format: 16-bit PCM in 2's complement binary (LSB first)
- Gain selection — transmit: 0 or −3 dB
  receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved power supply rejection ratio (PSRR)
- A/D filters can be bypassed; A/D has sample and hold built in

## T7523 High-Precision PCM Codec Block Diagram

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## Description

The DS1 chip set performs the various multiplexing and framing functions required by a digital multiplexed interface (DMI). This chip set consists of a 229CG Framer, 229FB Maintenance Buffer, 257AL Transmit Formatter, 257AU Receive Synchronizer, and the LC1046 Digital Signaling Interface (DSI). For DMI applications the 229GB Framer is an excellent alternative. The two transformers provide impedance matching to the twisted pair cable. The received information is input to the LC1046 DSI in alternate mark inversion (AMI) format. The DSI then converts this signal into a TTL-level signal that is output to the 229GB Framer. The DSI also uses an internal phase-locked loop (PLL) to extract the receive line clock (RCLK) from the signal. This clock is output to the framer and the 257AU Receive Synchronizer. The framer detects frame boundaries and monitors the received data stream for facility trouble conditions and alarms. The 257AU Receive Synchronizer then receives the data signal from the framer and converts this serial data stream into parallel time-division multiplexed (TDM) data while extracting signaling information. The parallel data and signaling information are output on a per time slot basis to a PBX switching network or a host computer. The data and signaling information to be transmitted from the PBX or host computer is input to the 257AL Transmit Formatter. The transmit formatter converts this parallel data and signaling information back into a serial data stream. The information is input to the framer for in-line processing and output to the LC1046 DSI for conversion back to a digital AMI signal and output to the transformers. The 229FB Maintenance Buffer provides an interface between the controlling processor and the serial report and control streams of the framer, transmit formatter, and the receive synchronizer.

## 229FB Maintenance Buffer

*Description*

The 229FB Maintenance Buffer integrated circuit provides the microprocessor interface for the serial report and control streams of the 229CG or 229GB Framer, 257AU Receive Synchronizer, and 257AL Transmit Formatter. The device also processes facility alarms received from the framer and provides additional latched inputs and outputs for microprocessor use. The maintenance buffer is manufactured using depletion-mode NMOS technology, requires a single +5 V supply, and is available in a 40-pin plastic DIP.

*Features*

- 8-bit interface bus
- Microprocessor access to control/report streams
- Ten general-purpose latched outputs
- Two error-source latched inputs
- Preprocessing counters for facility error conditions updated by the framer
- Built-in operational testing capability
- TTL-compatible

## 229GB Framer

*Description*

The 229GB Framer integrated circuit provides the line format and frame format interfaces for DS1 (1.544 Mb/s) digital carrier systems. It performs on-line and off-line frame-oriented functions in both the receive and transmit directions. In addition, the device provides an auxiliary signaling format known as DMI Bit-Oriented Signaling (BOS). The 229GB Framer is TTL-compatible and is packaged in a 40-pin ceramic DIP.

*Features*

- Bipolar and B8ZS line format capability
- Multiple TDM frame formats
  - — Independent formats — D4, *SLC*® Carrier, ESF, and DDS T1DM
  - — Auxiliary signaling format — DMI BOS
- Off-line, defensive, and fast frame synchronization
- *SLC* Carrier, ESF, and DDS T1DM facility data-link insertion and extraction
- Remote frame/multiframe alarm activation and detection
- Transmission performance monitoring capability:
  - — Bipolar and B8ZS violations
  - — Frame-alignment signal (frame bit) errors
  - — Loss-of-frame/multiframe alignment
  - — CRC-6 errors (ESF mode)
  - — Change-of-frame alignment

## 229CG Framer

*Description*

The 229CG Framer integrated circuit provides the line format and frame format interfaces for both DS1 (1.544 Mb/s) and CEPT (2.048 Mb/s) digital carrier systems. It performs on-line and off-line frame-oriented functions in both the receive and transmit directions. The 229CG Framer is TTL-compatible and is packaged in a 40-pin ceramic DIP.

*Features*

- Bipolar and B8ZS line format capability
- Multiple TDM frame formats
  - — Independent formats — D4, *SLC* Carrier, ESF, and DDS T1DM

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— CCITT 30-channel format with optional TS-16 signaling

- Off-line, defensive, and fast frame synchronization
- *SLC* Carrier, ESF, and DDS T1DM facility data-link insertion and extraction
- Remote frame/multiframe alarm activation and detection
- Transmission performance monitoring capability:
  — Bipolar and B8ZS violations
  — Frame-alignment signal (frame bit) errors
  — Loss-of-frame/multiframe alignment
  — CRC-6 errors (ESF mode)
  — Change-of-frame alignment

## 257AU Receive Synchronizer

*Description*

The 257AU Receive Synchronizer performs serial-to-parallel conversion, slip compensation, and signaling extraction on the serial data received from the framer. The receive synchronizer is a part of an LSI digital facility interface chip set that also includes the 257AL Transmit Formatter, the 229CG or 229GB Framer, and the 229FB Maintenance Buffer. The receive synchronizer is manufactured using NMOS technology and is available in a 32-pin plastic DIP.

*Features*

- Selectable DS1 (1.544 Mb/s) or CEPT (2.048 Mb/s) formats
- 4- or 16-state, RSM signal extraction
- Internal maintenance circuits
- Single +5 V supply
- TTL-compatible inputs and outputs

## 257AL Transmit Formatter

*Description*

The 257AL Transmit Formatter integrated circuit converts 14 bits of parallel data (8 traffic bits, 5 signaling bits, 1 parity bit), received from a time slot interchanger, into a serial stream. The device is manufactured using NMOS technology, requires a single +5 volt supply, and is available in a 32-pin plastic DIP.

*Features*

- Selectable DS1 (1.544 Mb/s) or CEPT (2.048 Mb/s) formats
- 2-, 4-, 16-state signaling or inhibit signaling insertion
- Variable F bit and parity bit delays
- TTL-compatible

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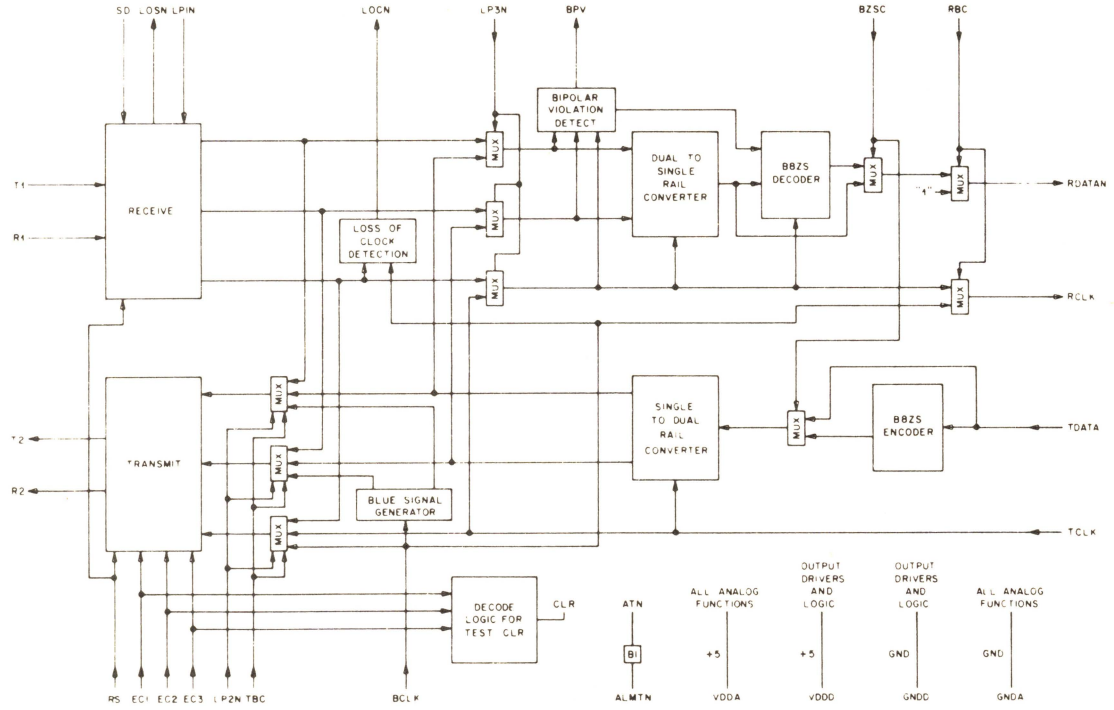
### Description

The LC1046 Digital Signaling Interface (DSI) is an integrated circuit that provides a line interface between the DS1 or DS1C cross-connect and terminal equipment circuits for cable distances of up to 655 feet for 22-gauge plastic insulated cable. The device performs receive pulse regeneration, timing recovery, and transmit pulse shaping and equalization functions. The LC1046 DSI device is manufactured using 1.75 micron CMOS technology and is available in a 28-pin plastic DIP or 28-pin plastic small-outline J-leaded (SOJ) package for surface mounting.

### Features

- Fully integrated DS1/DS1C line interface
- Compatible with Technical Advisory #34 (TA34) and PUB 43802 specifications
- On-chip transmit equalization
- Monolithic clock recovery
- Pin-selectable B8ZS encoder and decoder
- Loopback modes for fault isolation
- Multiple link-status and alarm features
- Minimal external circuitry required

### LC1046 DSI Block Diagram



# Quad Differential Line Receiver — 41LF

## Description

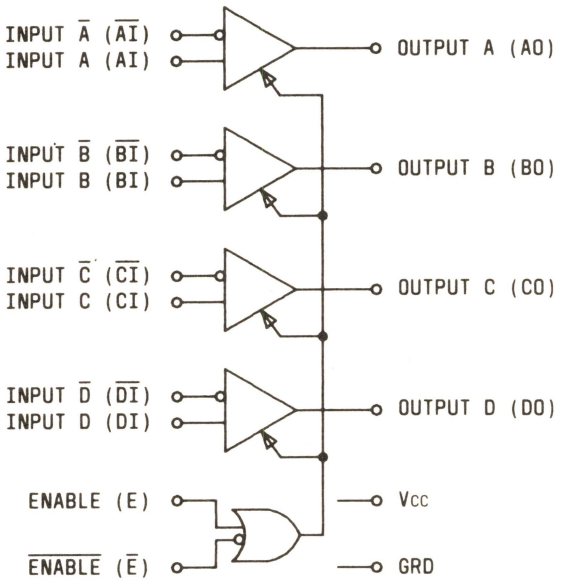
The 41LF Quad Differential Line Receiver integrated circuit is a quad differential input to TTL output line receiver. This OXIL technology device contains four receiver clusters and enable circuitry. The average propagation delay is 4 ns, and the common mode operating range is ±4 V. The 41LF line receiver is pin-equivalent to the general-trade AM26LS32 device, but has improved speed and decreased power consumption.

The quad differential line receiver is available in a 16-pin plastic DIP (41LF), a 16-pin SOJ (1041LF), and a 16-pin SOIC-GW (1141LF).

## Features

- Pin-equivalent to general-trade AM26LS32, with increased speed and reduced power
- Single +5 V supply
- 0 to 85°C operating temperature
- Four line receivers per package
- Complementary inputs for each line receiver
- 250 mW maximum power dissipation
- 7 ns maximum propagation delay
- 0.20 V input sensitivity
- ±4 V common mode rejection

*Logic Diagram*

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### Electrical Characteristics

*$T_A$ = 0 to 85°C, $V_{CC}$ = 5.0 ±0.5 V*

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage, $V_{CC}$ = 4.5 V | | | | | |
| Low, $I_{OL}$ = 8 mA | $V_{OL}$ | — | — | 0.5 | V |
| High, $I_{OH}$ = −400 μA | $V_{OH}$ | 2.5 | — | — | V |
| Input Voltages (E, $\overline{E}$) | | | | | |
| Low, $V_{CC}$ = 5.5 V | $V_{IL}$** | — | — | 0.7 | V |
| High, $V_{CC}$ = 4.5 V | $V_{IH}$** | 2.0 | — | — | V |
| Clamp, $V_{CC}$ = 4.5 V; $I_{IN}$ = −18 mA | $V_{IK}$ | — | — | −1.5 | V |
| Differential Input Voltages* (AI, $\overline{AI}$, BI, $\overline{BI}$, CI, $\overline{CI}$, DI, $\overline{DI}$) | | | | | |
| $V_O$ = $V_{OL}$ or $V_{OH}$** −0.80 V < $V_{IH}$ < 7.2 V, −1.2 V < $V_{IL}$ < 6.8 V | $V_{TH}$** | 0.20 | 0.1 | — | V |
| Output Currents, $V_{CC}$ = 5.5 V | | | | | |
| Off-State (High Z), $V_O$ = 0.4 V | $I_{OZL}$ | — | — | 20.0 | μA |
| Off-State (High Z), $V_O$ = 2.4 V | $I_{OZH}$ | — | — | 20.0 | μA |
| Short-Circuit | $I_{SC}$ | −25.0 | — | −100.0 | mA |
| Input Currents (E, $\overline{E}$) $V_{CC}$ = 5.5 V | | | | | |
| Low, $V_{IN}$ = 0.4 V | $I_{IL}$ | — | — | −360 | μA |
| High, $V_{IN}$ = 2.7 V | $I_{IH}$ | — | — | 20.0 | μA |
| Reverse, $V_{IN}$ = 5.5 V | $I_{IH}$ | — | — | 100 | μA |
| Input Currents (AI, $\overline{AI}$, BI, $\overline{BI}$, CI, $\overline{CI}$, DI, $\overline{DI}$) | | | | | |
| Low, $V_{IN}$ = −1.2 V | $I_{IL}$ | — | — | −1.0 | mA |
| High, $V_{IN}$ = 7.2 V | $I_{IH}$ | — | — | 1.0 | mA |
| Power Supply Current, $V_{CC}$ = 5.5 V | | | | | |
| All outputs disabled | $I_{CC}$ | — | 35.0 | 45.0 | mA |

* Unused differential input pairs should be biased alternately to $V_{CC}$ and GND. No protection resistor required.

** These input levels and difference voltage provide zero noise immunity and should only be tested in a static, noise-free environment.

### Maximum Ratings

| Rating | Value | Unit |
|---|---|---|
| DC Power Supply Voltages ($V_{CC}$) | 7.0 | V |
| Ambient Operating Temperature ($T_A$) | 0 to 125 | °C |
| Storage Temperature ($T_{stg}$) | −40 to +125 | °C |

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300°C.

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## Quad Differential Line Driver — 41LG

### Description

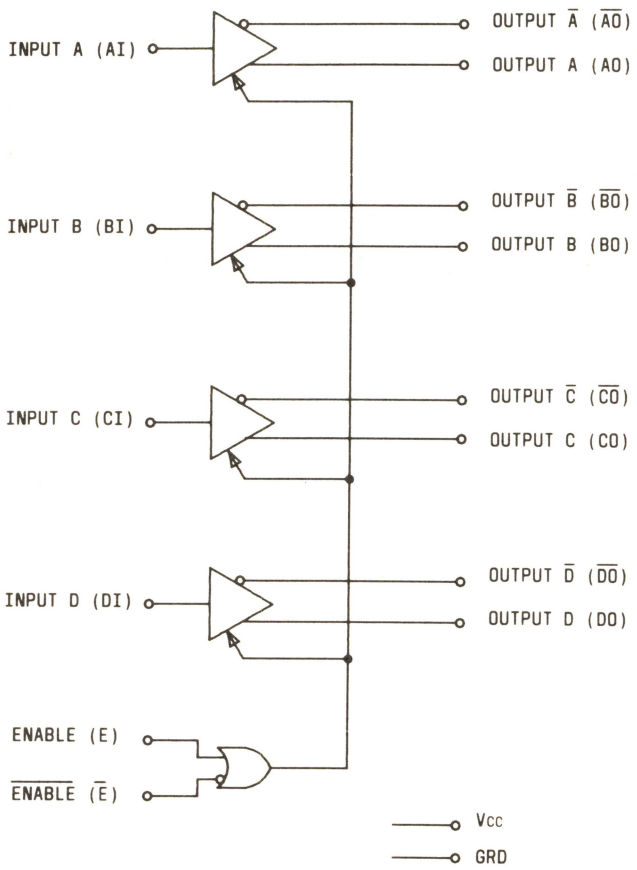
The 41LG Quad Differential Line Driver integrated circuit transmits digital data over balanced transmission lines. It translates input TTL logic levels to ECL-like output levels that directly drive the line. This OXIL technology device is pin-equivalent to the general-trade 26LS31 device; however, it has decreased power consumption and generates lower levels of electromagnetic interference (EMI). By having four drivers in one 41LG device, circuit board package count is reduced. All four line drivers in the device have common enable and disable functions. The 41LG line driver is compatible with many line receivers including the AT&T 41LF and 858B HIC (built-in terminations) devices, and the general-trade AM26LS32 device.

The quad differential line driver is available in a 16-pin plastic DIP (41LG), a 16-pin SOJ (1041LG), and a 16-pin SOIC-GW (1141LG).

### Features

- Pin-equivalent to general-trade AM26LS31 device with increased speed, reduced power, and reduced EMI
- Single +5 V supply
- Four line drivers per package
- Complementary outputs from each line driver
- No line loading when Vcc = 0
- 40 mA drive capability
- High output drive for 50 Ω lines
- 100 mA minimum output short-circuit current
- 300 mW maximum power dissipation
- 6 ns maximum propagation delay
- 0.2 ns output skew, typical
- 0 to 85°C operating temperature

*Logic Diagram*

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### Electrical Characteristics

*$T_A$ = 0 to 85°C, $V_{CC}$ = 5.0 ±0.5 V*

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltages, $V_{CC}$ = 4.5 V | | | | | |
| Low, $I_{OL}$ = −40.0 mA | $V_{OL}$ | — | — | $V_{OH}$ − 0.8* | V |
| High, $I_{OH}$ = −40.0 mA | $V_{OH}$ | 3.0 | — | — | V |
| High Z, $I_{OZ}$ = −1.0 mA, $V_{CC}$ = 4.5 V | $V_{OZ}$ | — | 2.0 | $V_{OL}$ − 0.05 | V |
| $V_{CC}$ = 4.75 V | | | 2.0 | $V_{OL}$ − 0.2 | V |
| Input Voltages | | | | | |
| Low, $V_{CC}$ = 5.5 V | $V_{IL}$** | — | — | 0.8 | V |
| High, $V_{CC}$ = 4.5 V | $V_{IH}$** | 2.0 | — | — | V |
| Clamp, $V_{CC}$ = 4.5 V; $I_{IN}$ = −18.0 mA | $V_{IK}$ | — | — | −1.5 | V |
| Output Currents | | | | | |
| Short-Circuit | $I_{SC}$ | −100.0 | −20.0 | −300.0 | mA |
| Input Currents, $V_{CC}$ = 5.5 V | | | | | |
| Low, $V_{IN}$ = 0.4 V | $I_{IL}$ | — | — | −400 | μA |
| High, $V_{IN}$ = 2.7 V | $I_{IH}$ | — | — | 20.0 | μA |
| Reverse, $V_{IN}$ = 5.5 V | $I_{IH}$ | — | — | 100 | μA |
| Power Supply Current, $V_{CC}$ = 5.5 V | | | | | |
| All outputs disabled | $I_{CC}$ | — | 60.0 | 75.0 | mA |
| All outputs enabled | $I_{CC}$ | — | 35.0 | 55.0 | mA |

* $V_{OL}$ must be a minimum of 0.8 V (800 mV) less than its complementary output.
** These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

### Maximum Ratings

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage ($V_{CC}$) | 7.0 | V |
| Ambient Operating Temp. Range ($T_A$) | 0 to 125 | °C |
| Storage Temp. Range ($T_{stg}$) | −40 to +125 | °C |

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300°C.

# INTERFACE

## Dual Differential Line Driver & Receiver Pairs — 41LK, 41LL, and 41LM

### Description

The 41LK, 41LL, and 41LM devices are dual differential line driver and line receiver pairs, consisting of two differential ECL-to-TTL converters and two TTL-to-differential ECL converters. These OXIL technology devices contain individual enabling circuitry for the driver and receiver pairs. The average propagation delay for the driver and receiver is 3.0 ns and 4.0 ns, respectively. By having two receivers and two drivers in one package, the serial data and control clock are transmitted and received using a single integrated circuit.

The 41LK device is intended for use where the minimization of electromagnetic interference is required. The 41LL device has internal 200 Ω discharge resistors on each driver output and is equivalent to the DS8923A. The 41LM device has resistor terminations for both the driver (200 Ω) and receiver (100 Ω) and is intended for use with 100 Ω impedance (Z) twisted pair or flat cable — since this device eliminates the need for external resistors.

The 41LK, 41LL, and 41LM dual line driver and line receiver pairs are available in a choice of packaging: 16-pin plastic DIP, 16-pin SOJ, or 16-pin SOIC-GW.

### Features

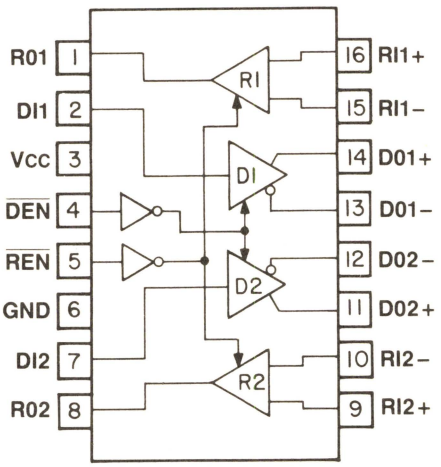
*Driver*

- Single +5 V supply
- Two line drivers per package
- Complementary outputs for each line driver
- No line loading when Vcc = 0 V
- 100 mA minimum output short-circuit current
- 6 ns maximum propagation delay
- 0.2 ns output skew, typical
- 0 to 85°C operating temperature

*Receiver*

- Two line receivers per package
- Complementary outputs for each line receiver
- 7 ns maximum propagation delay
- 0.20 V input sensitivity
- ±4 V common mode rejection
- 0 to 85°C operating temperature

*Pin Function Diagram*




*Logic Table*

| $\overline{DEN}$ | $\overline{REN}$ | R01 | R02 | D01 | D02 |
|---|---|---|---|---|---|
| 0 | 0 | ACTIVE | ACTIVE | ACTIVE | ACTIVE |
| 1 | 0 | ACTIVE | ACTIVE | HI-Z | HI-Z |
| 0 | 1 | HI-Z | HI-Z | ACTIVE | ACTIVE |
| 1 | 1 | HI-Z | HI-Z | HI-Z | HI-Z |

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### Electrical Characteristics

*$T_A$ = 0 to 85°C, $V_{CC}$ = 5.0 ±0.5 V*

*Driver*

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltages, $V_{CC}$ = 4.5 V | | | | | |
| Low, $I_{OL}$ = −40.0 mA | $V_{OL}$ | — | — | $V_{OH}$ − 0.8* | V |
| High, $I_{OH}$ = −40.0 mA | $V_{OH}$ | 3.0 | — | — | V |
| High Z, $I_{OZ}$ = −1.0 mA, $V_{CC}$ = 4.5 V | $V_{OZ}$ | — | 2.0 | $V_{OL}$ − .05 | V |
| $V_{CC}$ = 4.75 V | $V_{OZ}$ | — | 2.0 | $V_{OL}$ − 0.2 | V |
| Input Voltages | | | | | |
| Low, $V_{CC}$ = 5.5 V | $V_{IL}$ | — | — | 0.7 | V |
| High, $V_{CC}$ = 4.5 V | $V_{IH}$ | 2.0 | — | — | V |
| Clamp, $V_{CC}$ = 4.5 V; $I_{IN}$ = −18.0 mA | $V_{IK}$ | — | — | −1.5 | V |
| Output Currents | | | | | |
| Short-Circuit | $I_{SC}$ | −100.0 | — | −300.0 | mA |
| Input Currents, $V_{CC}$ = 5.5 V | | | | | |
| Low, $V_{IN}$ = 0.4 V | $I_{IL}$ | — | — | −400 | μA |
| High, $V_{IN}$ = 2.7 V | $I_{IH}$ | — | — | 20.0 | μA |
| Reverse, $V_{IN}$ = 5.5 V | $I_{IH}$ | — | — | 100 | μA |
| Power Supply Current, $V_{CC}$ = 5.5 V | | | | | |
| 41LK: All outputs disabled | $I_{CC}$ | — | 40.0 | 75.0 | mA |
| All outputs enabled | $I_{CC}$ | — | 30.0 | 50.0 | mA |
| 41LL, 41LM: All outputs disabled | $I_{CC}$ | — | 60.0 | 90.0 | mA |
| All outputs enabled | $I_{CC}$ | — | 90.0 | 135.0 | mA |

* $V_{OL}$ must be a minimum of 0.8 V (800 mV) less than its complementary output.

One input of unused differential input pairs should be based to $V_{CC}$. No protection resistor required.





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*Receiver*

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage, $V_{CC}$ = 4.5 V | | | | | |
| Low, $I_{OL}$ = 8 mA | $V_{OL}$ | — | — | 0.5 | V |
| High, $I_{OH}$ = −40.0 μA | $V_{OH}$ | 2.5 | — | — | V |
| Input Voltages (E, $\bar{E}$) | | | | | |
| Low, $V_{CC}$ = 5.5 V | $V_{IL}$* | — | — | 0.7 | V |
| High, $V_{CC}$ = 4.5 V | $V_{IH}$* | 2.0 | — | — | V |
| Clamp, $V_{CC}$ = 4.5 V; $I_{IN}$ = −18 mA | $V_{IK}$ | — | — | −1.5 | V |
| Differential Input Voltages | | | | | |
| $V_O$ = $V_{OL}$ or $V_{OH}$* | $V_{TH}$* | 0.20 | 0.1 | — | V |
| −0.80 V < $V_{IH}$ < 7.2 V, −1.2 V < $V_{IL}$ < 6.8 V | | | | | |
| Output Currents, $V_{CC}$ = 5.5 V | | | | | |
| Off-State (High Z), $V_O$ = 0.4 V | $I_{OZL}$ | — | — | 20.0 | μA |
| Off-State (High Z), $V_O$ = 2.4 V | $I_{OZH}$ | — | — | 20.0 | μA |
| Short-Circuit | $I_{SC}$ | −25.0 | — | −100.0 | mA |
| Input Currents (E, $\bar{E}$) | | | | | |
| $V_{CC}$ = 5.5 V | | | | | |
| Low, $V_{IN}$ = 0.4 V | $I_{IL}$ | — | — | −400 | μA |
| High, $V_{IN}$ = 2.7 V | $I_{IH}$ | — | — | 20.0 | μA |
| Reverse, $V_{IN}$ = 5.5 V | $I_{IH}$ | — | — | 100 | μA |
| Input Currents | | | | | |
| Low, $V_{IN}$ = −1.2 V | $I_{IL}$ | — | — | −1.0 | mA |
| High, $V_{IN}$ = 7.2 V: 41LK, 41LM (Only) | $I_{IH}$ | — | — | 1.0 | mA |

* The input levels and difference voltage provide zero noise immunity and should only be tested in a static, noise-free environment.

One input of unused differential input pairs should be based to $V_{CC}$. No protection resistor required.

### Maximum Ratings

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage ($V_{CC}$) | 7.0 | V |
| Ambient Operating Temp. Range ($T_A$) | 0 to 125 | °C |
| Storage Temp. Range ($T_{stg}$) | −40 to +125 | °C |

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300°C.



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# INTERFACE

## 8 × 8 Bipolar Bilateral Crosspoint Array — 129EH-P

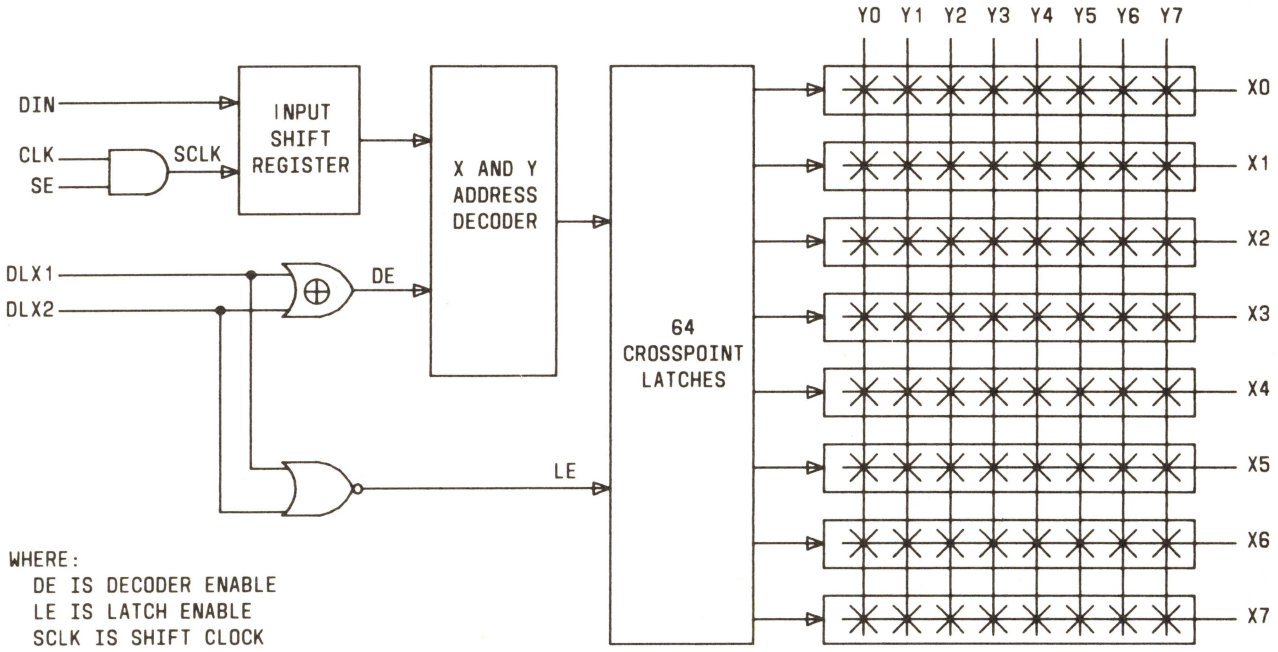
### Description

The 129EH-P 8 × 8 Bipolar Bilateral Crosspoint ($B^2X$) Array integrated circuit is a high-density, high-performance, bipolar space division switch. It is organized as an 8 × 8 crosspoint array, with crosspoints consisting of 64 symmetrical, lateral $P^+NP^+$ transistors. Each crosspoint is a nearly ideal switch, capable of conducting current in both directions with an insertion impedance of less than 20 Ω. The on-board $I^2L$ control and interface logic is TTL-compatible. The 129EH-P $B^2X$ device is available in a 24-pin molded plastic DIP.

### Features

- Crosstalk < −90 dB @ 3 kHz, 900 Ω
- Off isolation < −90 dB @ 3 kHz, 900 Ω
- Crosspoint-on resistance: 7 Ω ≤ $R_{ON}$ ≤ 20 Ω
- Crosspoint signal bandwidth > 5 MHz
- Power dissipation < 100 mW, all crosspoints off
- TTL-compatible

*129EH-P 8 × 8 Bipolar Bilateral Crosspoint Array Simplified Block Diagram*

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# 8 × 8 Bipolar Bilateral Crosspoint Array — 129EH-P

## Electrical Characteristics

*$T_A$ = 0 to 70°C, $V_{CC}$ = 5.0 ±0.5 V, $V_{EE}$ = −4 ±0.4 V, GND = 0 V*

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltages | | | | |
| Low | $V_{IL}$ | — | 1.0 | V |
| High | $V_{IH}$ | 1.8 | — | V |
| Input Clamp Diode Voltage | | | | |
| ($I_I$ = −18 mA) | $V_{IK}$ | −0.5 | −1.35 | V |
| Input Currents | | | | |
| Low, $V_{IN}$ = 0.0 V | $I_{IL}$ | 10 | −30 | μA |
| High, $V_{IN}$ = 2.7 V | $I_{IH1}$ | −1 | 2 | μA |
| High, $V_{IN}$ = 4.0 V | $I_{IH2}$ | −1 | 10 | μA |
| Power Supply Current | | | | |
| $V_{CC}$ = 5.5 V, $V_{EE}$ = −4.4 V | $I_{CC}$ | 23 | 40 | mA |
| For 8 Crosspoints On | $I_{EE}$ | −23 | −45 | mA |
| Power Dissipation | | | | |
| For 8 Crosspoints On | $PD_{on}$ | 200 | 420 | mW |
| For All Crosspoints Off | $PD_{off}$ | 40 | 100 | mW |

## Maximum Ratings

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage ($V_{CC}$) | 7.0 | V |
| Input Voltage ($V_{IH}$) | 5.5 | V |
| Operating Temp. Range ($T_J$) | 0 to 70 | °C |
| Storage Temp. Range ($T_{stg}$) | −40 to +125 | °C |

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300°C.

## Crosspoint Characteristics

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Bandwidth | BW | — | 5.0* | MHz |
| On Resistance | $R_{ON}$ | 7 | 20 | Ω |
| Offset Voltage | $V_{OF}$ | −30 | 30 | mV |
| Offset Current | $I_{OF}$ | −200 | 200 | μA |
| Crosstalk (3 kHz, 900 Ω) | — | — | −90 | dB |
| Off Isolation (3 kHz, 900 Ω) | — | — | −90 | dB |
| Signal Bias Voltage (Off) | — | −3.0 | 3.0 | V |
| Signal Bias Voltage (On) | — | −2.0 | 2.0 | V |
| Signal Bias Current (On) | — | −4.5 | 4.5 | mA |

* This device has been tested to 5 MHz. Higher frequencies may be acceptable, depending on application.

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# Quad Line Driver — AM26LS31C

## Description

The AM26LS31C Quad Line Driver is an integrated circuit (IC) consisting of four independent line drivers with a common control for both ENABLE, $\overline{\text{ENABLE}}$. It provides high-speed differential drive to transmission lines having an impedance of at least 100 ohms. Each of the four drivers has a complementary tristate output. The AM26LS31C requires only a 5 volt supply (±10%) for operation.

## Features

- Meets EIA RS-422A requirements
- Propagation delay is less than 20 ns
- Power supply current is reduced to less than 40 mA when device is disabled
- TTL-compatible ENABLE, $\overline{\text{ENABLE}}$ inputs
- ENABLE, $\overline{\text{ENABLE}}$ to output delay is less than 40 ns
- Output skew (time delay between direct output and inverse output) is typically 2 ns

## Electrical Characteristics

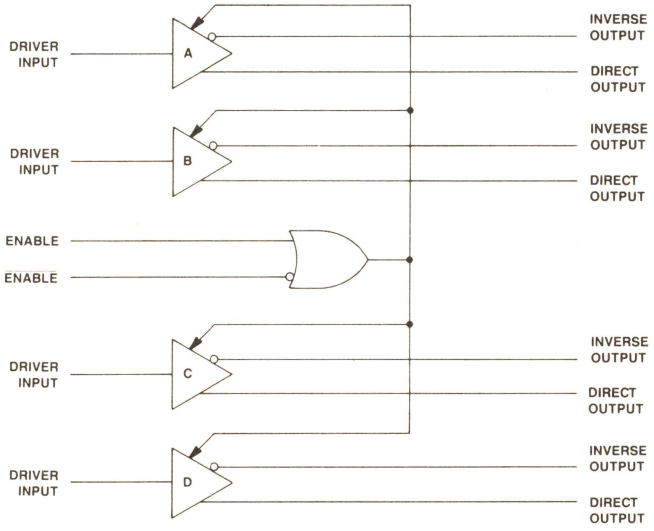
*$T_A$ = 25°C unless otherwise specified*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| Power Supply Voltage, Operating | | 4.5 | 5.5 | V |
| Output Voltage ($V_+$ = 4.5 V, $I_O$ = 20 mA) | High | 2.5 | 3.5 | V |
| ($V_{IH}$ = 2.0 V, $V_{IL}$ = 0.8 V) | Low | 0.05 | 0.5 | V |
| Input Clamp Voltage ($V_+$ = 4.5 V, $I_{IN}$ = −18 mA) | | 0 | −1.5 | V |
| Power Supply Current, No Load ($V_+$ = 5.5 V, $V_{IN}$ = 0) | | 45 | 90 | mA |
| Power Supply Current, Disabled ($V_+$ = 5.5 V, $V_{IN}$ = 2.0 V) | | 20 | 40 | mA |
| Output Current, Disabled ($V_O$ = 0.5 V or 2.5 V) | | — | ±20 | μA |
| Output Current, Power Off ($V_O$ = −0.25 or +6.0 V) | | — | ±100 | μA |
| Output Current, Short Circuit ($V_+$ = 5.5 V) | | — | −150 | mA |
| Input Current, Low ($V_{IN}$ = 0.4 V) | | 0 | −0.36 | mA |
| Input Current, High ($V_{IN}$ = 2.7 V) | | — | ±20 | μA |
| Input Current, Reverse ($V_{IN}$ = 7.0 V) | | 0 | 0.1 | mA |

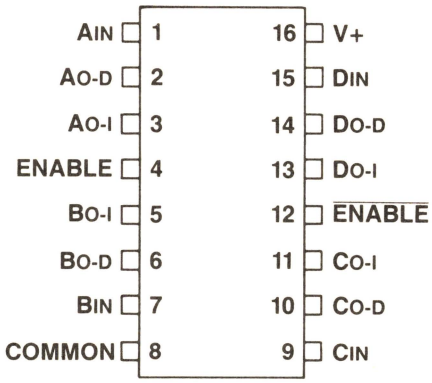
## Maximum Ratings

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage ($V_+$) | 7.0 | V |
| Input Operating Voltages, $V_+$, Driver Inputs, (ENABLE, $\overline{\text{ENABLE}}$) | 5.5 | V |
| Ambient Operating Temperature Range | 0 to +70 | °C |
| Storage Temperature Range | −40 to +125 | °C |
| Driver Output Current | ±35 | mA |
| Pin Temperature (Soldering, 15 sec) | 300 | °C |

*AM26LS31C Functional Diagram*




*16-Pin Plastic DIP*

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# Quad Line Receivers — AM26LS32C, AM26LS33C

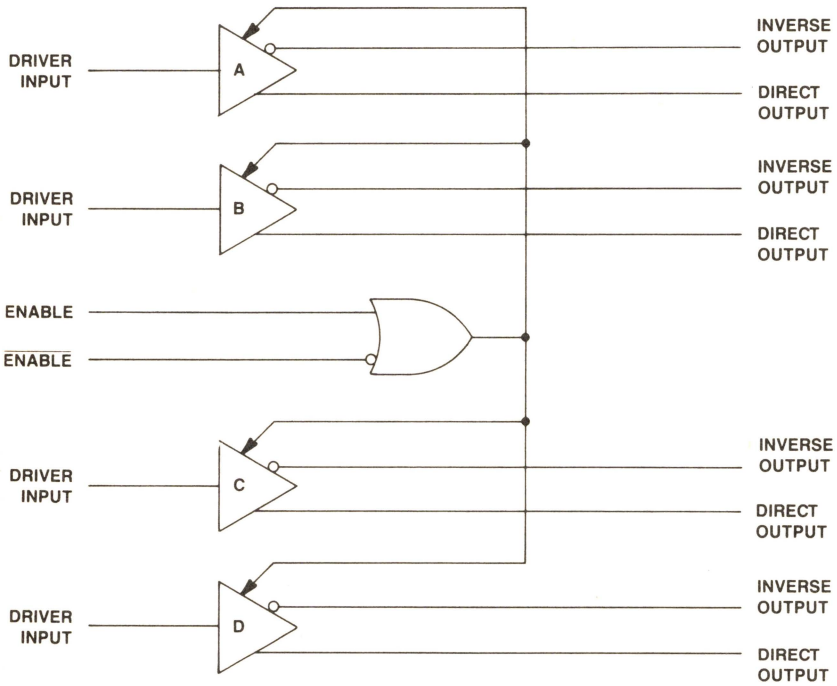
## Description

The AM26LS32C and AM26LS33C Quad Line Receivers are general purpose quad line receivers for balanced and unbalanced data transmission. A TTL-compatible ENABLE, $\overline{\text{ENABLE}}$ is common to all four receivers in the device package. The ENABLE, $\overline{\text{ENABLE}}$ allows the output to assume a high impedance state for output busing. Each device is encapsulated in a 16-pin plastic dual in-line package (DIP) and designed to meet industry standard EIA RS-422A specifications for the AM26LS32C and EIA RS-423A specifications for the AM26LS33C.

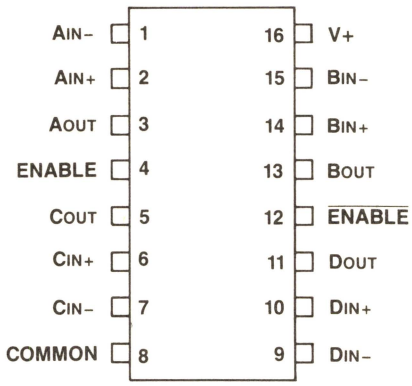
## Features

- Meets EIA RS-422A/423A specifications
- Four independent receivers with common strobe TTL-compatible input
- Electrostatic discharge protection on receiver inputs
- Requires only a single 5 V (±10%) power supply
- Input sensitivity:
  AM26LS32C ±200 mV
  AM26LS33C ±500 mV
- Minimum input hysteresis:
  AM26LS32C ±15 mV
  AM26LS33C ±30 mV
- Internal fail safe forces the output high for an open input condition
- Typical propagation delay of 17 ns
- 16-pin plastic DIP, with industry standard pinout

*AM26LS32C, AM26LS33C Functional Diagram*




*16-Pin Plastic DIP*

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## Maximum Ratings

| Rating | Value | Unit |
|---|---|---|
| Supply Voltage (V+) | 7.0 | V |
| Control Input Voltage (ENABLE, $\overline{\text{ENABLE}}$) | 7.0 | V |
| Input Common Mode Range | ±25 | V |
| Input Differential Voltage | ±25 | V |
| Storage Temperature Range | −40 to +125 | °C |
| Power Dissipation (Package Limitation) | 400 | mW |
| Pin Temperature (Soldering, 15 sec) | 300 | °C |

## Characteristics

| Characteristic and Conditions | | | Min | Max | Unit |
|---|---|---|---|---|---|
| Differential Input Threshold Voltage | $I_O$ = −0.4 mA, $V_{OH}$ ≥2.7 V | | | | V |
| | AM26LS32C, −7.0 V < $V_{CM}$ <7.0 V | | — | 0.2 | |
| | AM26LS33C, −15.0 V < $V_{CM}$ <15.0 V | | — | 0.5 | |
| | $I_O$ = 4.0 mA, $V_{OL}$ ≤0.5 V | | | | |
| | AM26LS32C, −7.0 V < $V_{CM}$ <7.0 V | | — | −0.2 | |
| | AM26LS33C, −15.0 V < $V_{CM}$ <15.0 V | | — | −0.5 | |
| Dynamic Input Resistance | −15.0 V < $V_{CM}$ <15.0 V<br>One input AC GND | | 6.0 | — | kΩ |
| Input Current | $V_{IN}$ = 15.0 V | | — | 2.3 | mA |
| | $V_{IN}$ = −15.0 V | | — | −2.8 | |
| Input Hysteresis Voltage | V+ = 5.0 V<br>$T_A$ = 25°C | AM26LS32C, $V_{CM}$ = ±7.0 V<br>AM26LS33C, $V_{CM}$ = ±15.0 V | ±15<br>±30 | —<br>— | mV |
| High Level Output Voltage | V+ = 4.5 V, $V_{ID}$ = 1.0 V<br>$V_{\overline{EN}}$ = 0.8 V<br>$I_{OH}$ = −440 μA | | 3.6 | — | V |
| Low Level Output Voltage | V+ = 4.5 V<br>$V_{ID}$ = 0.8 V | $I_{OL}$ = 5.0 mA | — | 0.4 | |
| | $V_{\overline{EN}}$ = 0.8 V | $I_{OL}$ = 8.0 mA | — | 0.45 | |

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# LINEAR

## Octal High-Voltage N-Channel MOSFET Array — AN0130NA

### Monolithic N-Channel Enhancement-Mode — Advanced Information

#### Description

The AT&T Octal High-Voltage N-Channel MOSFET Array provides the interface between MOS logic and loads requiring high voltages and intermediate currents. Each Circuit consists of eight channels in a common source configuration with open drains. These devices are fabricated in AT&T's proprietary BCDMOS technology with dielectric isolation. This process offers unprecedented freedom from latchup and parasitic device interaction.

A most important feature is the ESD protection provided on-chip. This is a feature not provided by similar arrays presently available in the industry. Initial devices will be available for operation up to 300 volts. Inquire about the availability of higher voltage-rated devices. This device is packaged in an 18-pin plastic DIP.

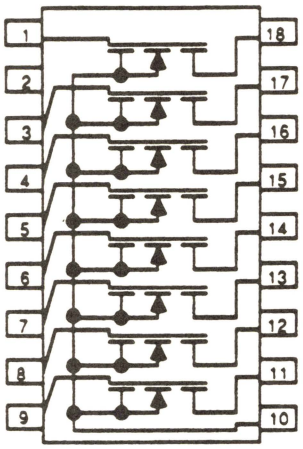
#### Features

- On-chip ESD protection
- Operating voltage up to 300 volts
- Processed with BCDMOS technology
- Freedom from secondary breakdown
- Interfaces directly to CMOS logic
- PIN compatible with industry standard driver arrays
- Low crosstalk between channels

#### Applications

- Test Systems
- Industrial controls
- Telecommunications
- Electrostatic array drivers
- Electroluminescent panel drivers
- General multi-channel driver array

*Functional and Pin Configuration*




| $BV_{DS}$ | $R_{DS(ON)}$ | $I_{D(ON)}$ |
|---|---|---|
| 300 V | 300 Ω | 25 mA |

#### Maximum Ratings

*At 25°C unless otherwise specified*

| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | −40 to +85 | °C |
| Storage Temperature Range | −55 to +150 | °C |
| Pin Soldering Temperature (t=15 sec max.) | 300 | °C |
| Drain Current, DC | 30 | mA |
| Drain Current, Pulsed (tP=200 μs; duty cycle=2%) | 75 | mA |
| Gate-to-Source Voltage | ±20 | V |
| Drain-to-Source Voltage | | $BV_{DS}$ |

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# Octal High-Voltage P-Channel MOSFET Array — AP0130NA

## Monolithic P-Channel Enhancement-Mode — Advanced Information

### Description

The AT&T Octal High-Voltage P-Channel MOSFET Array provides the interface between MOS logic and loads requiring high voltages and intermediate currents. Each Circuit consists of eight channels in a common-source configuration with open drains. These devices are fabricated in AT&T's proprietary BCDMOS technology with dielectric isolation. This process offers unprecedented freedom from latchup and parasitic device interaction.

A most important feature is the ESD protection provided on-chip. This is a feature not provided by similar arrays presently available in the industry. Initial devices will be available for operation up to 300 volts. Inquire about the availability of higher voltage-rated devices. This device is packaged in an 18-pin plastic DIP.

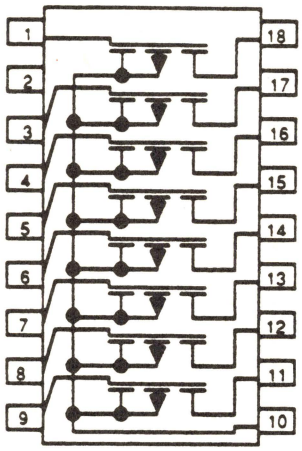
### Features

- On-chip ESD protection
- Operating voltage up to 300 volts
- Processed with BCDMOS technology
- Freedom from secondary breakdown
- Interfaces directly to CMOS logic
- PIN compatible with industry standard driver arrays
- Low crosstalk between channels

### Applications

- Test Systems
- Industrial controls
- Telecommunications
- Electrostatic array drivers
- Electroluminescent panel drivers
- General multi-channel driver array

*Functional and Pin Configuration*




| $BV_{DS}$ | $R_{DS(ON)}$ | $I_{D(ON)}$ |
|---|---|---|
| −300 V | 600 Ω | −15 mA |

### Maximum Ratings

*At 25°C unless otherwise specified*

| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | −40 to +85 | °C |
| Storage Temperature Range | −55 to +150 | °C |
| Pin Soldering Temperature (t=15 sec max.) | 300 | °C |
| Drain Current, DC | −15 | mA |
| Drain Current, Pulsed (tP=200 μs; duty cycle=2%) | −40 | mA |
| Gate-to-Source Voltage | ±20 | V |
| Drain-to-Source Voltage | | $BV_{DS}$ |

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# General-Purpose Telephone Tone Ringers — LB1005-Type

## Description

These integrated circuits provide the telephone alerter function. The output tone warbles between the base frequency and 1.25 times the base frequency at a 15 or 20 Hz modulation rate (see Table 1 under Applications for specific tone options). These devices meet all known standard criteria for telephone alerters. Piezoelectric transducers can be driven directly.

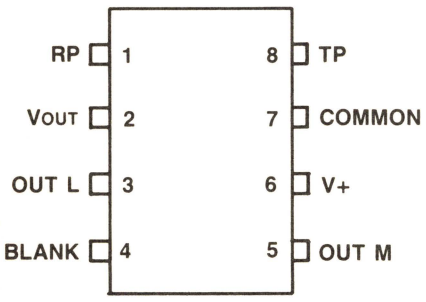
## Applications

Each LB1005 device requires only two capacitors, one resistor, and an alerter to provide tone ringing functions from any standard Tip-Ring telephone pair. These devices operate over widely varying ringing waveforms (15 to 68 Hz at 40 to 150 Vrms). The LB1005 derives its power by rectifying the AC ringing signal from the Tip-Ring pair of a telephone loop. It uses this power to activate a tone generator, and then transfers most of this power to an alerter after the ringing has been detected. There is essentially no loading under non-ringing conditions. Selectable on-chip resistors allow the volume of the alerter output to be adjusted (see Application diagram). These devices do not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V+ will also allow the devices to operate in what is described as "stand alone applications." The tone generator circuitry includes an oscillator and frequency divider which produce specified tones and the tone modulation rate. The output warble frequency ranges and modulation rates are shown in Table 1.

*Table 1. Tone Generation (Design Values)*

| Device Number | Output Warble Frequency Range | Modulation Rate |
|---|---|---|
| LB1005AB | 1800/2250 Hz | 20 Hz |
| LB1005BB | 1200/1500 Hz | 20 Hz |
| LB1005CB | 900/1125 Hz | 15 Hz |

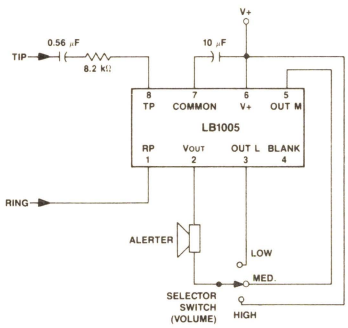
*8-Pin Plastic DIP*



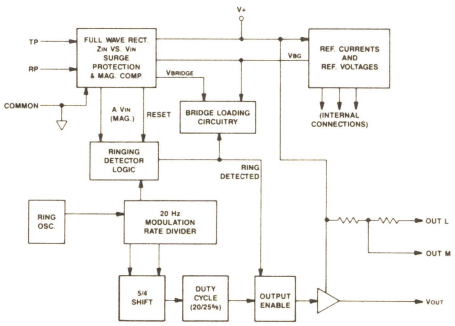

## Features

- Tight output frequency control (±3%)
- An internal polarity guard provides 2000 V lightning surge protection when connected as shown in the Application Diagram
- Meets both Type A and B ringing requirements (40 Vrms <VIN <15 Hz <fin <68 Hz) as specified by EIA RS-470 on FCC Part 68
- Provides essentially no loading under non-ringing conditions
- External components required are two capacitors, one resistor, and a transducer
- Meets input impedance criteria specified by EIA RS-470 and AT&T technical publication 47001
- Immune to rotary dial pulsing (bell tap)
- Ringer equivalency: 0.8 B when configured as shown in the Application Diagram
- On-chip volume control resistors are provided

*LB1005 Typical Application*




*Functional Diagram*

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# Telephone Ringing Detector — LB1006AB

## Description

The LB1006AB Telephone Ringing Detector provides ringing detection functions from the Tip-Ring pair of a telephone loop. This device provides a nominal output current (up to approximately 1 mA) for two types of output drives. The output can be connected to either an opto-isolator device or to a logic interface with a microprocessor.

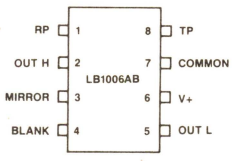
## Applications

The LB1006AB detector derives its power by rectifying the AC ringing signal from the Tip-Ring pair of a telephone loop. It operates over widely varying ringing waveforms (15 to 68 Hz at 40 to 150 Vrms). It uses this derived power to activate ringing-detector logic, and then transfers most of this power to an output current driver. There is essentially no loading under non-ringing conditions. This device has two outputs, OUT H and OUT L. The OUT H output is used source output current when ringing is detected. The OUT L output becomes functional when the OUT H output is connected to the mirror input. The OUT L output will sink current when ringing is detected (see Simplified Output Diagram). This device does not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V+ will also allow the device to operate in what is described as "stand alone applications." Applications for the two types of outputs (source or sink current) are shown in the Application Diagrams.

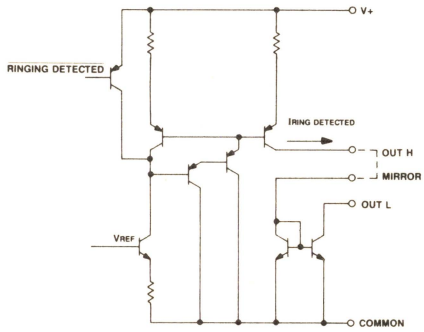
## Features

- Provides an inexpensive means of ringing detection
- Operates on less than 1.0 mA from the telephone loop
- Internal polarity guard and 2000 V lightning surge protection
- Immune to rotary dial pulsing (bell tap)
- Meets both Type A and B ringing requirements (40 Vrms $<V_{IN}<$150 Vrms, 15 Hz $<$fin $<$68 Hz) as specified by EIA RS-470 and FCC Part 68
- Ringer equivalency: 0.8 B when configured as shown in the Application Diagrams

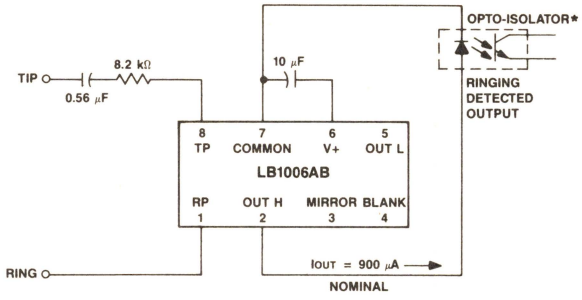
*8-Pin Plastic DIP*




*Simplified Output Diagram*

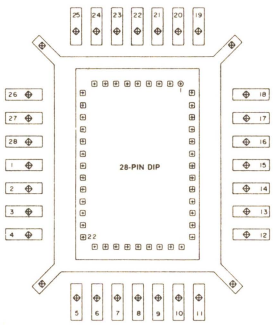



*Typical Application for Opto-isolator Drive*

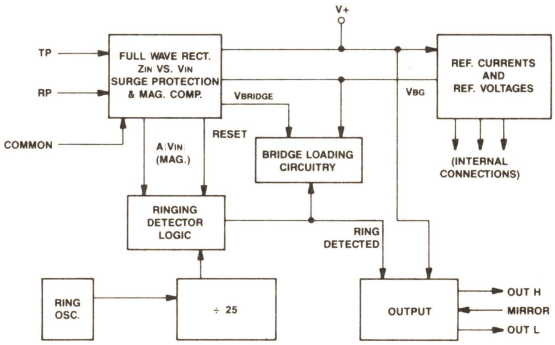



* AT&T 4U, GI MCT210Q4898 OR SIMILAR DEVICES

*Typical Application for Interface Direct to Logic*




*Functional Diagram*

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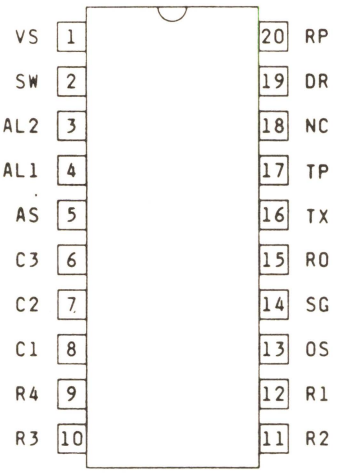
# LINEAR

## Keyboard Controlled Single-Chip Telephone — LB1008AE

### Description

The LB1008AE integrated circuit requires only a few external components to provide all of the touch-tone electronic functions. This integrated circuit furnishes ac and dc loop termination for both switchhook states, transmits and receives voice signals to the central office, provides dual-tone multi-frequency (DTMF) signals to the central office, and properly distinguishes between spurious noise and genuine ringing signals, providing a distinctive audible alerter output.

*20-Pin Plastic DIP*




### Features

- An alerter select function of 1200/1500 Hz
- Capable of speech transmission down to 3.0 mA loop current
- Compatible with electret and carbon microphones
- Signal ground pin eliminates external capacitor for dial-in-handset designs
- 700 ohm line matching impedance, 600 ohm receiver impedance
- Provides a power port for driving an LED

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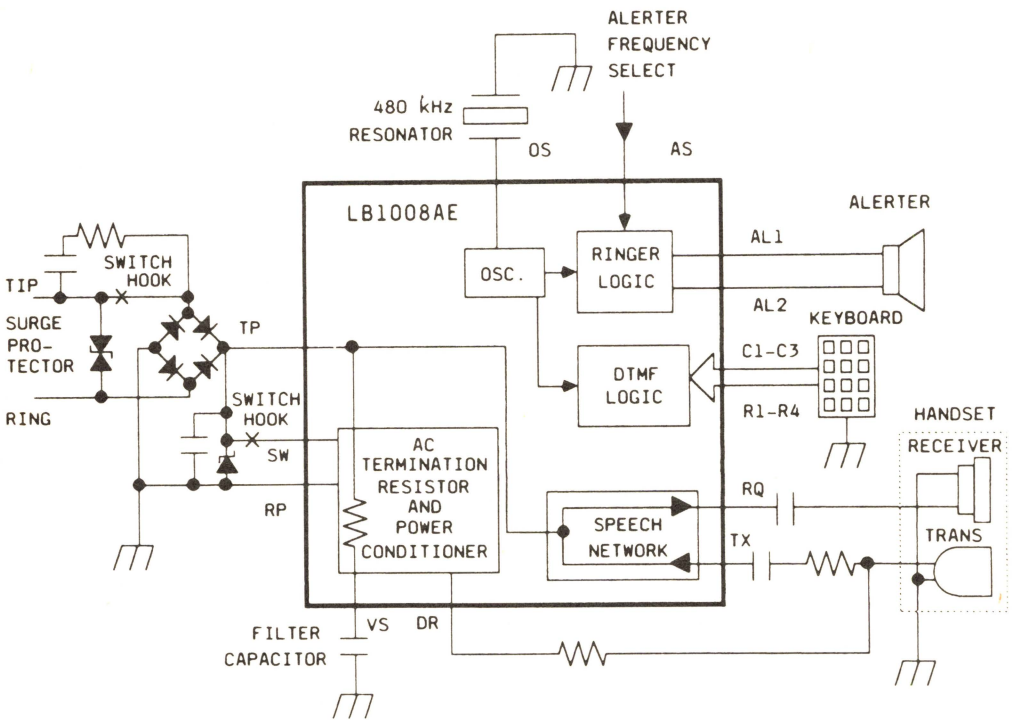
*LB1008AE Functional Diagram (4-Wire Handset Interface)*

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# Keyboard Controlled Single-Chip Telephone — LB1008AE

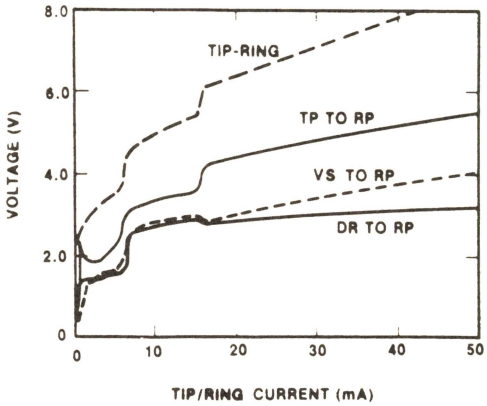
## Maximum Ratings

*At 25°C unless otherwise specified*

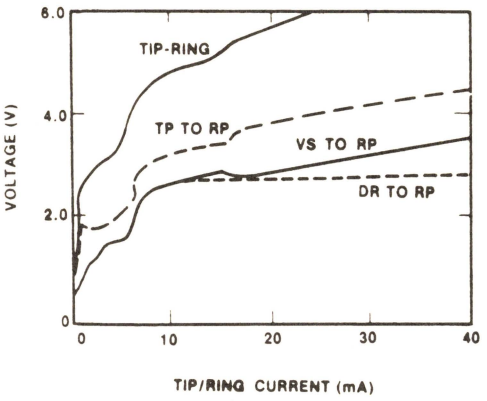
| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | 0 to +60 | °C |
| Storage Temperature Range | −40 to +125 | °C |
| Pin Soldering Temperature (t=15 sec max.) | 300 | °C |
| Voltage (TP) | 20 | V |
| Current (TP) | 120 | mA |

## Characteristics

*Typical V-1 Characteristics (Dial Mode)*




*Typical V-1 Characteristics (Speech Mode)*

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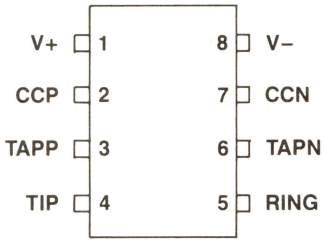
### Description

The LB1011AB integrated circuit is an electronic battery feed circuit which supplies DC currents to a telephone line with minimal loading on the AC signals. The LB1011AB is integrated as two complementary chips to supply DC currents of both negative and positive polarities to either balanced or unbalanced lines. In the balanced line application, this device helps suppress undesirable common-mode signals.

### Features

- Basic battery feed function at a low cost
- High AC impedance characteristics for balanced line, differential-mode, voice-band signals
- Full internal lightning surge protection
- DC voltage drops can be adjusted to accommodate different peak signal levels

*8-Pin Plastic Power DIP*




### Maximum Ratings

| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | −20 to +70 | °C |
| Storage Temperature Range | −40 to +125 | °C |
| Pin Temperature (Soldering, 15 sec) | 300 | °C |
| Operating Voltages (DC Voltage Drop)* | −4.00 to +4.85 | V |

* See Electrical Characteristics

### Electrical Characteristics

*$T_A$ = 25°C unless otherwise specified*

| Characteristics | Min | Max | Unit |
|---|---|---|---|
| DC Voltage Drop, Positive Line Feed<br>V+ Current = 50 mA | 2.50 | 3.50 | V |
| DC Voltage Drop, Positive Line Feed, High-Level Mode<br>V+ Current = 50 mA<br>TAPP Shorted to CCP | 3.75 | 4.85 | V |
| DC Voltage Drop, Negative Line Feed<br>V– Current = −50 mA | −2.50 | −3.50 | V |
| DC Voltage Drop, Negative Line Feed, High-Level Mode<br>V– Current = −50 mA<br>TAPN Shorted to CCN | −3.60 | −4.00 | V |
| Shunt Impedance | 18 | — | kΩ |
| Common-Mode (Longitudinal) Rejection<br>$V_{IN}$ = 1.0 Vrms, f = 1 kHz<br>RP1 = RN1 | 45 | — | dB |
| Common-Mode (Longitudinal) Rejection, High-Level Mode<br>TAP Shorted to CC<br>$V_{IN}$ = 1.0 Vrms, f = 1 kHz<br>RP1 = RN1 | 45 | — | dB |
| Distortion<br>V(TIP to RING) = 1.0 Vrms | — | 2.0 | % |
| Distortion, High-Level Mode<br>TAP Shorted to CC<br>V(TIP to RING) = 2.0 Vrms | — | 2.0 | % |

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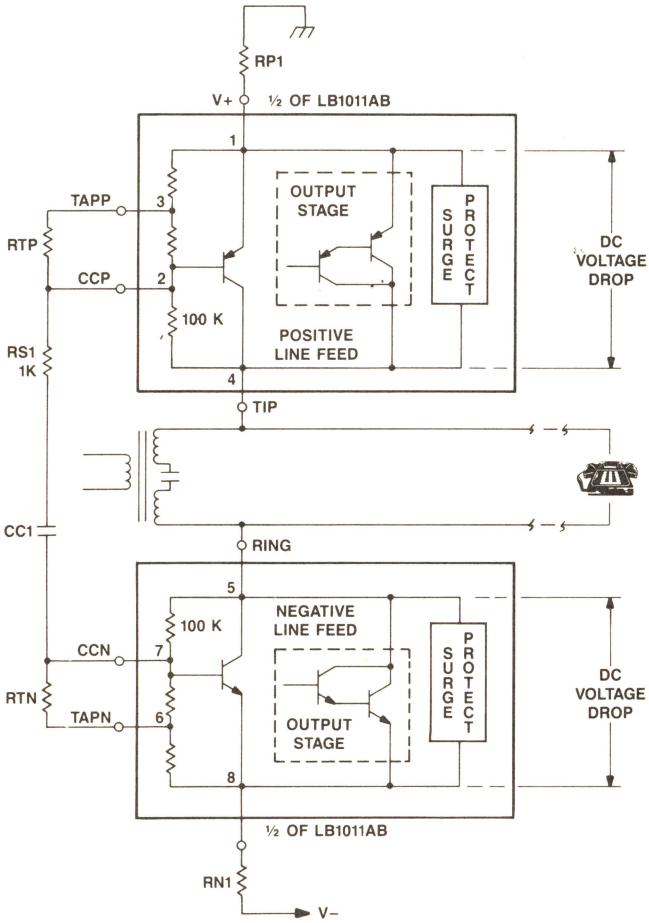
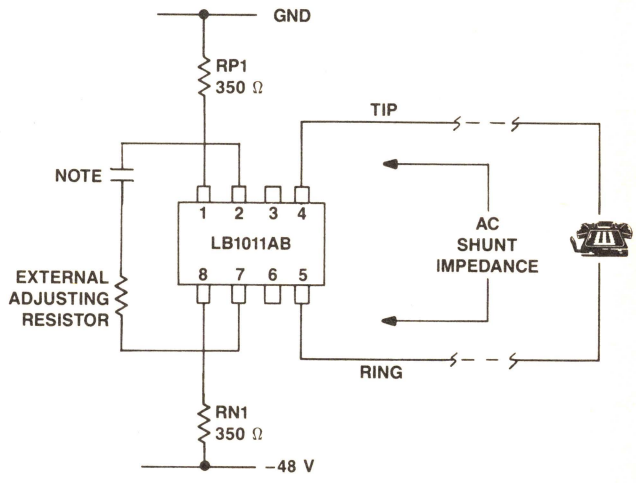
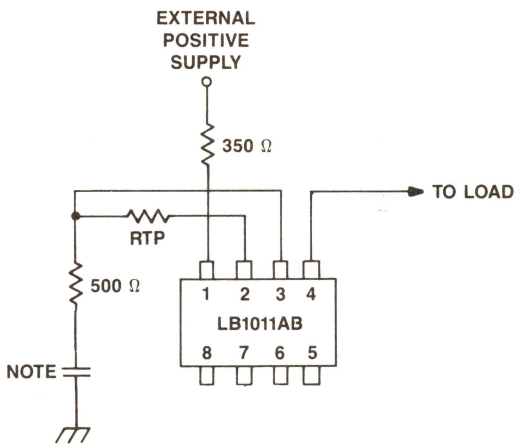
*Functional Diagram*




*Battery Feed Application Diagram (Balanced Configuration)*




*AC Blocking, DC Current Feed Applications*

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## Description

The LB1012AD integrated circuit device is an electronic battery feed circuit which supplies a controlled DC current to the Tip-Ring pair of a telephone system. The battery feed circuitry presents a low impedance to DC current, while presenting a high impedance to the AC signal. The LB1012AD device contains input and output ports for voice-frequency signals and a hook status output signal.

## Maximum Ratings

*At $T_A$ = 25°C unless otherwise specified*

| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | −20 to +70 | °C |
| Storage Temperature Range | −40 to +125 | °C |
| Lead Soldering Temperature (5=15 sec max) | 300 | °C |
| Power Dissipation* | 2.0 | W |
| Voltage, HOOK STATUS to V− | 60 | V |
| Voltage, GND to V− | 60 | V |
| Voltage (HOOK STATUS to GND) | 5.5 | V |
| Current (TIP DRIVE) | 50 | mA |

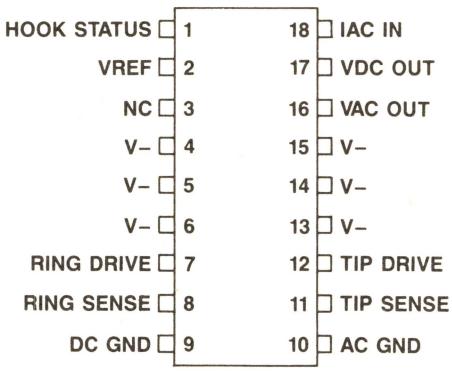
* Care in mounting and proper environmental conditions are required to keep the operating temperature acceptably low. The package of this device has a thermal resistance of approximately 12°C/W to its mounting plane. The remainder of its environment (thermal resistance of wiring board mounting plane to ambient) should not exceed an additional 30°C/W. Forced air circulation over the IC or high-thermal-conductivity wiring boards may be needed.

Thermal impedance between the package and the connecting mounting path may be minimized by connecting the V− pins to as large a thermally conductive land area as is practical to place on the mounting board. See the V− pin description for additional information.

## Features

- Drives loop lengths up to 1300 ohms
- Common-mode rejection (longitudinal balance) better than 60 dB (AC)
- Longitudinal balance and amplifier gains are laser trimmed
- TTL-compatible "hook status" indicator
- Proper line matching can be provided with a 50:1 scaled network; 30k ohms provide a 600 ohm termination
- 18-pin plastic power DIP

*18-Pin Plastic DIP*

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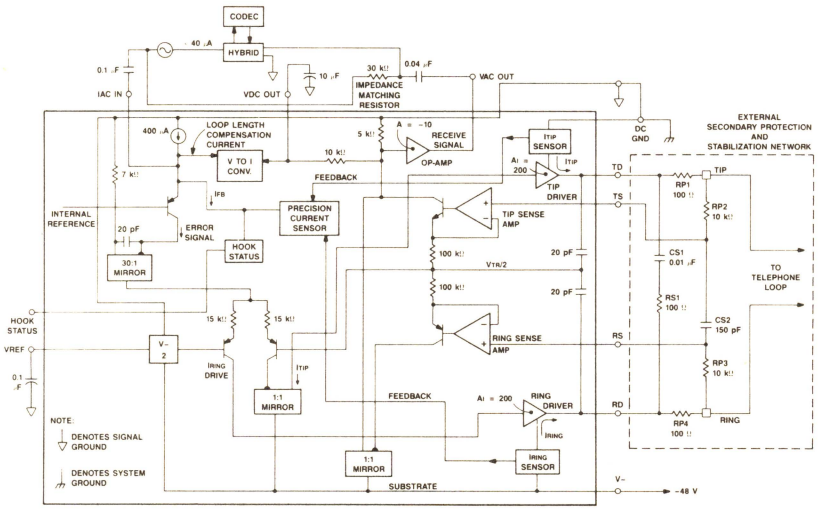
## Electrical Characteristics

*V– = –53 V and TA = 25°C unless otherwise specified*

The characteristics shown below are expressed in circuit functional terms. They are insured as the result of production testing measurements.

| Characteristics | Min | Max | Unit |
|---|---|---|---|
| Power Supply Current, OFF-HOOK (V– = –53 to –60 V), (Loop = 275 Ω | 43 | 49.5 | mA |
| Power Supply Current, ON-HOOK (V– = –48 V), (Loop = Open Circuit) | 0.2 | 3.5 | mA |
| Ringing Current Capability, RING Lead Open | 100 | — | mA |
| TIP Current for Power Gate Threshold | 3.0 | 8.0 | mA |
| Loop Current for Hook Status Threshold (Loop = 500 Ω) | 11 | 16 | mA |
| Loop Current: 150 Ω | 38.3 | 41.3 | mA |
| 500 Ω | 38.5 | 41.5 | mA |
| 800 Ω | 30.5 | 34.5 | mA |
| 1300 Ω | 19.0 | 23.0 | mA |
| Transmit Loop Current Gain, IAC IN to TIP-RING | 95.5 | 101 | — |
| Receive Voltage Gain, TIP-RING to VAC OUT | 0.476 | 0.506 | — |
| Longitudinal Balance (ac) (Common-Mode Current <10 mA) | 60 | — | dB |
| Power-Supply Rejection: (Loop = 400 Ω) | 52 | — | dB |
| Noise Voltage, TIP/RING: (Loop = 500 Ω) | — | 8.0 | dBrnc |
| IAC IN, Input Resistance | — | 100 | Ω |
| VAC OUT, Output Resistance: (2.0 kΩ between VAC OUT & GND) | — | 50 | Ω |
| Longitudinal Resistance | 50 | 100 | Ω |
| TIP-TO-RING Shunt Resistance: (ΔLoop = 150 Ω – 400 Q) | 30 | — | KΩ |
| Input Current Capability of "IAC IN" without Clipping | — | 100 | μAp-p |
| Output Voltage Capability of "VAC OUT" without Clipping | — | 2.0 | Vp-p |

*Battery Feed Functional Diagram*

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# LINEAR

## Voice Path Switch Power Conditioner/Amplifier — LB1020AF, LB1021AD

### Description

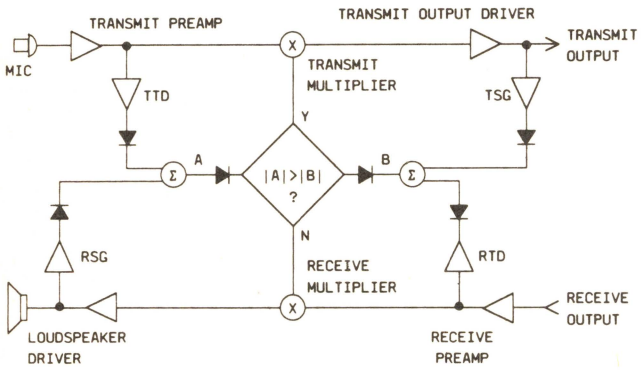
The LB1020AF performs the switching function needed for Speaker phone operation by accepting transmit and receive signals as input, and providing transmit and receive variolosser control signals as output. Timing of these switching functions is selectable using external RC combinations. The LB1020AF also provides a noise guard feature which permits steady background noise to be ignored in making the transmit/receive switching decision. It is normally used in conjunction with the LB1021AD to which it provides variolosser control currents.

The LB1021AD provides the linear amplification for a full-feature Speakerphone system, including switchable controllable gain for the transmit and receive voice paths, speaker and line drive capabilities, and switchguard/talkdown gain. It provides a stable, low-noise signal reference from a single 12 volt supply needed to power the circuit. It is normally used in conjunction with the LB1020AF.

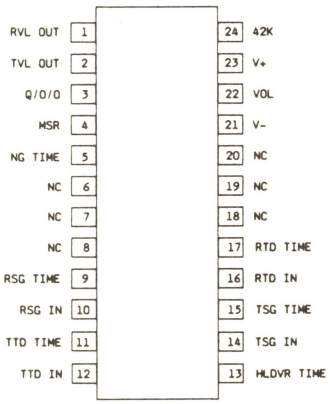
### Features

- 70 mA speaker driver capability
- High-gain receive preamplifier accommodates variety of microphones
- 40 dB typical receive path gain
- Quiet, on/off volume control
- Receive in default
- Switching unaffected by constant background noise
- Slow attack/quick decay noise guard does not interfere with forced switching
- All switching time constants independently controllable
- Holdover timing independent of forced switching time constants

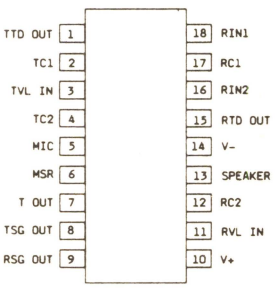
*Simplified Speakerphone Circuit*




*LB1020AF 24-Pin Plastic DIP*




*LB1021AD 18-Pin Plastic DIP*

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## Multipurpose Solid-State Relays — LH1056A-Type

**Preliminary Information**

### Description

The LH1056A-Type Multipurpose Solid-State Relays are low-cost, bi-directional, SPST switches which can replace mechanical relays in many applications. Output is rated at 350 volts and can handle loads up to 100 mA. The MSR is available in a 6-pin plastic DIP or a surface-mount package. The MSR will switch both dc and ac loads and is UL-approved for 1500 Vrms of input/output isolation.

The circuit consists of one GaAlAs LED to optically couple the control signal to a dielectrically isolated high-voltage integrated circuit. The typical ON-Resistance is 30 ohms at 25 mA, and is exceptionally linear up to 50 mA. Beyond 50 mA, the incremental resistance becomes even less, thereby minimizing internal power dissipation. The MSR also has internal current limiting which clamps the load current to 150 mA to insure that the device survives during power surges. The MSR will survive FCC lightning test number 68-302 when it is properly protected.

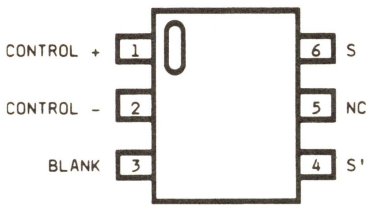
### Features

- Low ON-Resistance
- Clean, bounce-free switching
- 1500 Vrms input/output isolation (optically coupled)
- High solid-state reliability
- dv/dt typically better than 500 V/$\mu$s
- High-surge capability
- Low-power consumption
- Noise-free operation
- No electromagnetic interference
- High-voltage monolithic IC fabricated in a dielectric isolation process

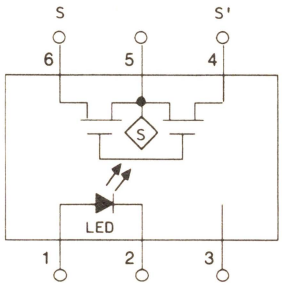
### Applications

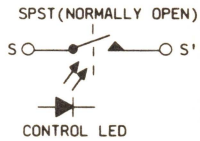
- Telephone switchhook
- High-voltage testers
- Industrial controls
- Triac driver
- Isolation switching

*6-Pin Configuration (Plastic DIP or Surface Mount)*




*Functional and Equivalent Relay Diagrams*




### Maximum Ratings

*At 25°C unless otherwise specified*

| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | 0 to 70 | °C |
| Storage Temperature Range | −40 to +100 | °C |
| Pin Soldering Temperature (t=15 sec max) | 300 | °C |
| Input/Output Voltage Isolation | 1500 | Vrms |
| LED Input Ratings | | |
| Continuous Forward Current | 20 | mA |
| Reverse Voltage | 10 | V |
| Output Operation | | |
| Operating Voltage | 350 | V |
| DC or RMS Load Current | 100 | mA |
| LED Forward Current for Turn-on | 1.3 | mA (typ) |

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## Multipurpose Solid-State Relays — LH1061A-Type

**Preliminary Information**

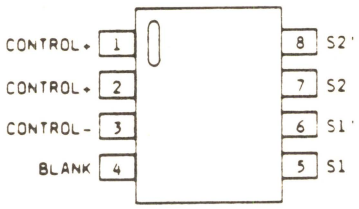
### Description

The LH1061A-Type Multipurpose Solid-State Relays are low-cost, bi-directional, double-pole, single-throw (DPST) switches which can replace mechanical relays in many applications. Output is rated at 200 volts per pole and can handle loads up to 200 mA. The LH1061A-Type is packaged in an 8-pin plastic DIP. It provides up to 1500 Vrms of input/output isolation and will switch both ac and dc loads. This device consists of a single LED to optically couple the control signal to a dielectrically isolated high-voltage integrated circuit. The typical ON-Resistance is 12 ohms per pole at 50 mA, and is exceptionally linear to 100 mA. Beyond 100 mA, the incremental ON-Resistance becomes even less, thereby minimizing internal power dissipation. The LH1061A-Type also has internal current limiting which clamps the load current to 250 mA to insure that the device survives during power surges.

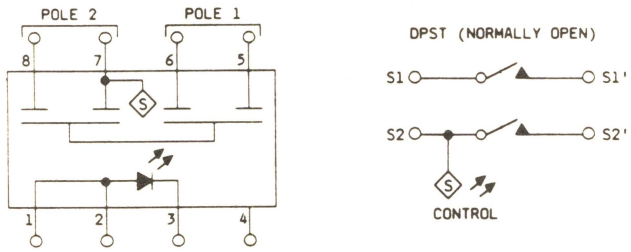
### Features

- Low ON-Resistance
- Clean, bounce-free switching
- 1500 Vrms input/output isolation (optically coupled)
- High solid-state reliability
- dv/dt typically better than 500 V/$\mu$s
- High-surge capability
- Low-power consumption
- Noise-free operation
- No electromagnetic interference
- High-voltage monolithic IC fabricated in a dielectric isolation process
- Surface mount version available

*8-Pin Plastic DIP*




*Functional and Equivalent Relay Diagrams*




### Maximum Ratings

*At 25°C unless otherwise specified*

| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | 0 to 70 | °C |
| Storage Temperature Range | −40 to +100 | °C |
| Pin Soldering Temperature (t=15 sec max) | 300 | °C |
| Input/Output Voltage Isolation | 1500 | Vrms |
| LED Input Ratings | | |
| Continuous Forward Current | 20 | mA |
| Reverse Voltage | 10 | V |
| Recommended Maximum Output Operation | | |
| Operating Voltage (per pole) | 200 | V |
| Load Current (each pole, two poles operating simultaneously) | 200 | mA |
| Surge Voltage (1.0 ms square wave, non-current) | 200 | V |
| LED Forward Current for Turn-on | 3.5 | mA (typ) |



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## Solid-State Relay — LH1085AT

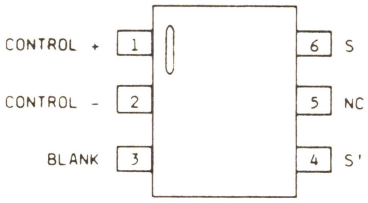
**Preliminary Information**

### Description

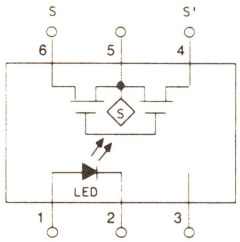
The LH1085AT Solid-State Relay is a low-cost, bi-directional, SPST switch which can replace mechanical relays in many applications. The output is rated for 350 volts and is similar to the LH1056AT (MSR) except that the typical value of internal current limiting has been increased from 150 mA to 300 mA. The LH1085AT is available in a 6-pin plastic DIP. The LH1085AT will switch both dc and ac loads and is UL approved for 1500 Vrms of input-to-output isolation.

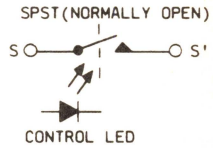
This device uses one GaAlAs LED to optically couple the control signal to a dielectrically isolated high-voltage integrated circuit. The typical ON-Resistance is 30 ohms at 25 mA and is exceptionally linear up to 50 mA. Beyond 50 mA, the incremental resistance becomes even less, thereby minimizing internal power dissipation. The LH1085AT is rated for dc load (operating) currents up to 150 mA and peak currents up to 225 mA. Internal current limiting will protect the device in many applications. However, the LH1056AT is recommended for those applications where operating currents are below 100 mA.

*6-Pin Plastic DIP*




*Functional and Equivalent Relay Diagrams*




### Features

- Low ON-Resistance
- Clean, bounce-free switching
- 1500 Vrms input/output isolation (optically coupled)
- High solid-state reliability
- dv/dt typically better than 500 V/$\mu$s
- High-surge capability
- Low-power consumption
- Noise-free operation
- No electromagnetic interference
- High-voltage monolithic IC fabricated in a dielectric isolation process

### Applications

- Telephone switchhook
- High-voltage testers
- Industrial controls
- Triac driver
- Isolation switching

### Maximum Ratings

*At 25°C unless otherwise specified*

| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | 0 to 70 | °C |
| Storage Temperature Range | −40 to +100 | °C |
| Pin Soldering Temperature (t=15 sec max) | 300 | °C |
| Input/Output Voltage Isolation | 1500 | Vrms |
| LED Input Ratings | | |
| Continuous Forward Current | 20 | mA |
| Reverse Voltage | 10 | V |
| Output Operation | | |
| Operating Voltage | 350 | V |
| Peak Load Current (t ≤10 milliseconds) | 225 | mA |
| DC or RMS Load Current | 150 | mA |

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# Dual Sample-and-Hold Amplifiers — LB1127AAK

## Description

The LB1127AAK is a silicon integrated circuit consisting of two separate sample-and-hold circuits, with differential inputs, combined in one 24-pin, hermetic-sealed, leadless ceramic chip carrier. It consists of FET input amplifiers in series with switched, high performance operational amplifiers. Internal holding capacitors are connected to the switch output, but provisions have been made so that external capacitors may be connected in parallel. This provides for application flexibility. This device is ideal for data systems where fast acquisition time, low sample-to-hold offset and low droop rate are critical.

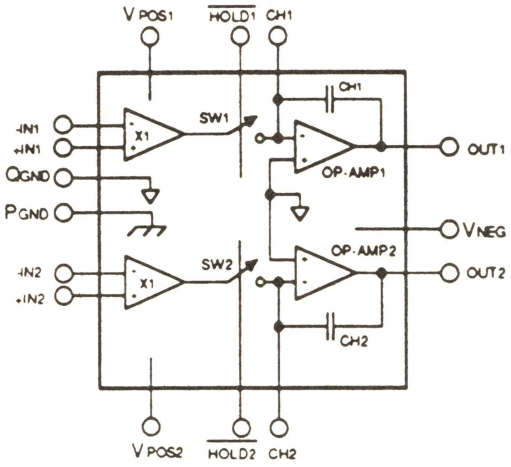
## Features

- Fast acquisition time (10 V step to ±0.01%) ≤3 μs
- Low droop rate (CH = 100 pF) ≤1.0 mV/ms
- Sample-hold offset step ≤3 mV
- Low aperture jitter ≈ 0.5 ns
- TTL-compatible control inputs
- 100 pF internal hold capacitor. External capacitance can be added to reduce droop rate when long hold times and high accuracy are required.

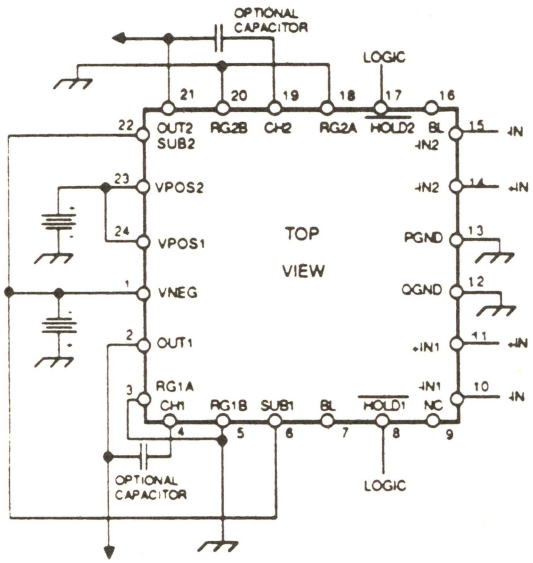
## Applications

- Data acquisition systems
- Peak detection
- Data distribution systems
- Analog delay and storage
- A/D conversion systems

*Functional Diagram*




*Basic Connections*

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# Dual Sample-and-Hold Amplifiers — LB1127AAK

## Maximum Ratings

*At 25°C unless otherwise specified*

| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Range | 15 to 75 | °C |
| Storage Temperature Range | −40 to +125 | °C |
| Pin Soldering Temperature (t=15 sec max.) | 300 | °C |
| Supply Voltage (VPOS to VNEG) | 30 | V |
| Short Circuit Output Current | 40 | mA |
| Logic Input Voltage (Pins 7 and 17) | VPOS, VNEG | |

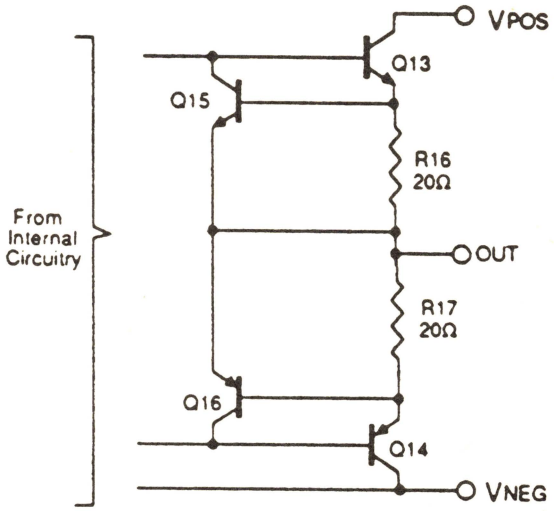
## Operating Characteristics

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Operating Supply Voltage (VPOS, VNEG) | +5, −12 | ±16.5 | V |
| Output Current (Source or Sink) | — | 15 | mA |

## Logic Input Levels

| Parameter | Min | Max | Unit |
|---|---|---|---|
| HOLD1 (Pin 8) and HOLD2 (Pin 17) | | | |
| High Input Voltage | 2.0 | — | V |
| Low Input Voltage | — | 0.8 | V |

*Sample-and-Hold Op-Amp Outputs (Simplified)*



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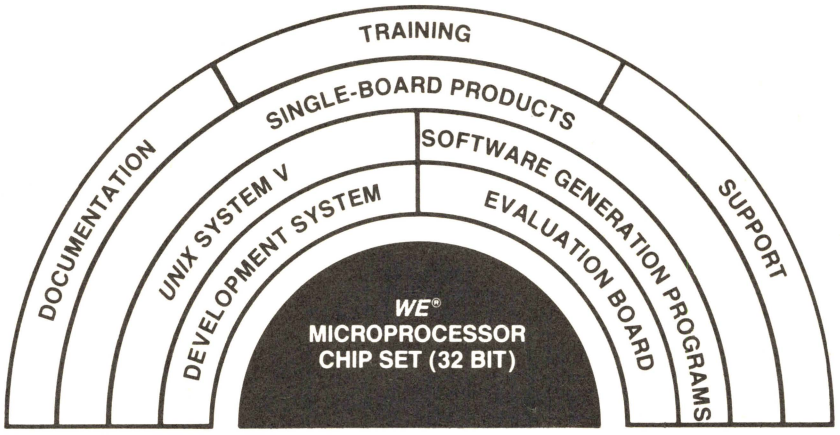
# MICROPROCESSOR

## *WE*® 32-Bit Microprocessors and Peripherals




The AT&T *WE* 32-Bit Microprocessors and Peripherals are a complete, integrated family of 32-bit microprocessor-based hardware, software, development, and application products. The chip set is specifically designed to support process-oriented operating systems such as the *UNIX*® Operating System and provides both building block and board level solutions to system design. The CPU devices have specific capabilities for both low-level assembly language and direct high-level language software development. The *WE* 32-Bit Microprocessors and Peripherals further consist of a complete family of peripherals, including memory management units, floating-point coprocessors, DMA and DRAM controllers, evaluation boards, development systems, software generation programs, and complete VME board products. Devices are available in 10-, 14-, 18-, 24-MHz, and higher frequency versions and are compatible with other general-trade peripherals.

### *WE* 32100 Microprocessor

- Low-power, 1.5-micron, CMOS technology
- 10-, 14-, and 18-MHz operation
- 125-pin square, ceramic pin grid array package
- Full 32-bit address and data buses
- Nine 32-bit general purpose registers and seven 32-bit special-purpose registers
- Direct support for process-oriented operating systems, such as *UNIX* System V
- Multiuser system support of *UNIX* System V
- Powerful and versatile instruction set
- Efficient high-level language execution
- Dynamically selectable two-word block fetch for instruction cache fill
- 4 Gbytes of direct memory addressing
- General coprocessor interface
- Monadic, dyadic, and triadic instructions
- Four levels of execution privilege
- 15-level interrupt structure
- Autovector and nonmaskable interrupt facilities
- On-chip 64 × 32-bit instruction cache
- Synchronous and asynchronous interfacing
- DMA and multiprocessor environment support

The *WE* 32100 Microprocessor (CPU) is a second-generation, high-performance, single-chip, 32-bit central processing unit. It is optimized to support modern process-oriented operating systems and execute high-level language programs. It performs all of the system address generation, control, memory access, and processing functions required in a full 32-bit microcomputer system. Special instructions allow the use of coprocessors such as the *WE* 32106 Math Acceleration Unit.

System memory is addressed over a 32-bit address bus using either virtual or physical addresses. The resulting memory space — over four billion bytes — greatly increases the flexibility of memory organization and provides ample space for program and data storage. Data is written over the 32-bit bidirectional data bus in word (32-bit), halfword (16-bit), or byte (8-bit) lengths. Extensive addressing modes result in a symmetric, powerful, and extensive instruction set. The *WE* 32100 Microprocessor supports an extremely powerful assembly language. In addition, the sixteen user-accessible registers are designed for efficient support of procedure-oriented high-level languages, such as C, and process-oriented operating systems, such as the *UNIX* Operating System. Nine of these registers can be used in any addressing mode for accumulations, addressing, or temporary data storage.

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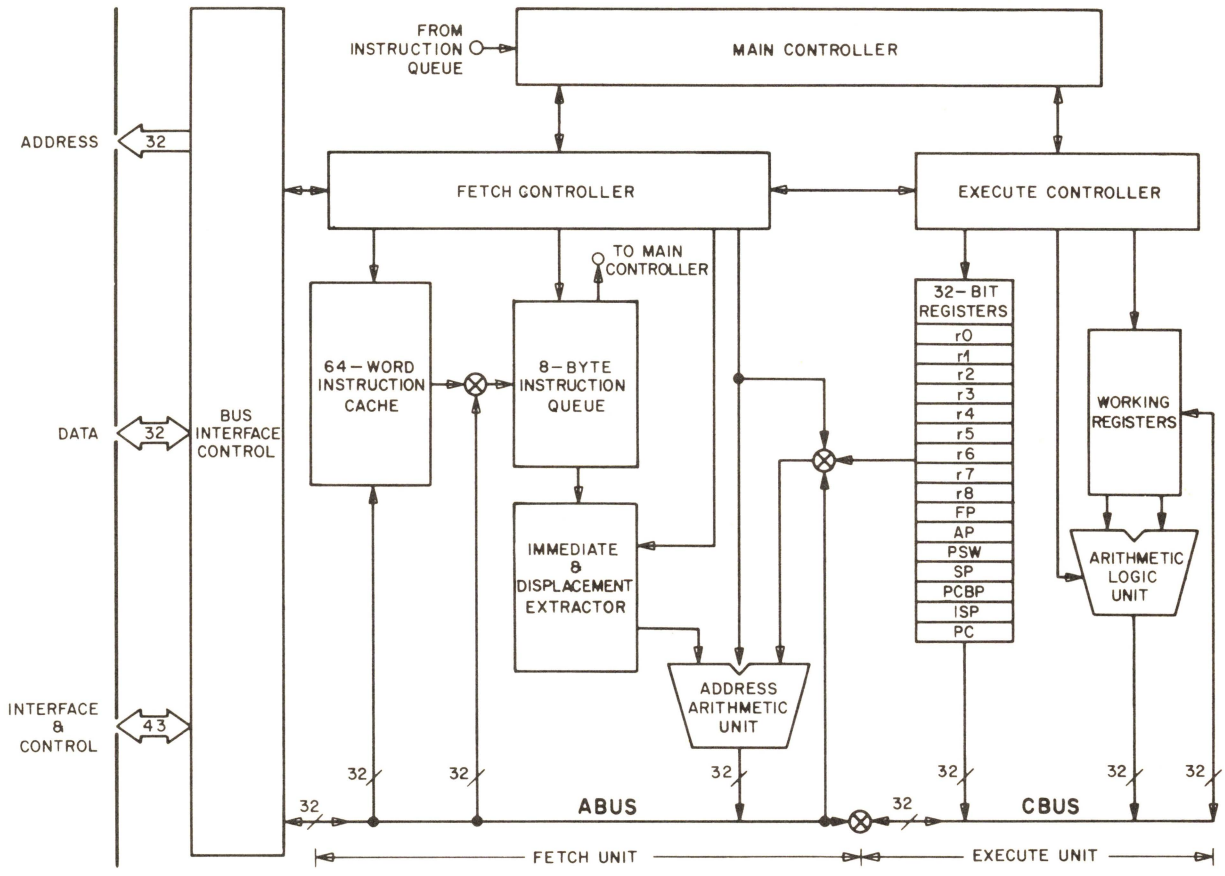
WE *32100 Microprocessor Block Diagram*




### *WE* 32101 Memory Management Unit

- Low-power, 1.5-micron, CMOS technology
- 10-, 14-, and 18-MHz operation
- 125-pin square, ceramic pin grid array package
- Manages mapping of up to 4 Gbytes of virtual address space and up to 4 Gbytes of physical address space
- On-chip segment descriptor cache and two-way, set-associative page descriptor cache
- Paged and nonpaged segmentation support
- Hardware support for *UNIX* System demand paging with automatic referenced/modified (R/M) bit update
- On-chip cache miss-processing
- Extensive fault detection and resolution capability
- Fully supports multiple MMU configuration

The *WE* 32101 Memory Management Unit (MMU) is a 32-bit, bus-structured device that provides logical-to-physical address translation memory organization, control, and access protection for the *WE* 32100 Microprocessor. The MMU performs address translation by mapping virtual memory addresses to physical memory addresses. It supports both demand paged and demand segmented virtual memory systems, allowing 4 Gbytes of virtual memory and up to 4 Gbytes of physical memory per process.

The 4 Gbyte virtual address space is subdivided into four sections with as many as 8K segments per section. Segments may be as large as 128 Kbytes of contiguous space, or may be further subdivided into as many as sixty-four 2-Kbyte pages. Each virtual memory section has a segment descriptor cache, page descriptor cache, base address register, and section length register associated with it. Segments are mapped by the MMU into physical address space. For each of four execution levels, there are four access permissions associated with segments — execute only, read/execute, read/write/execute, and no access.

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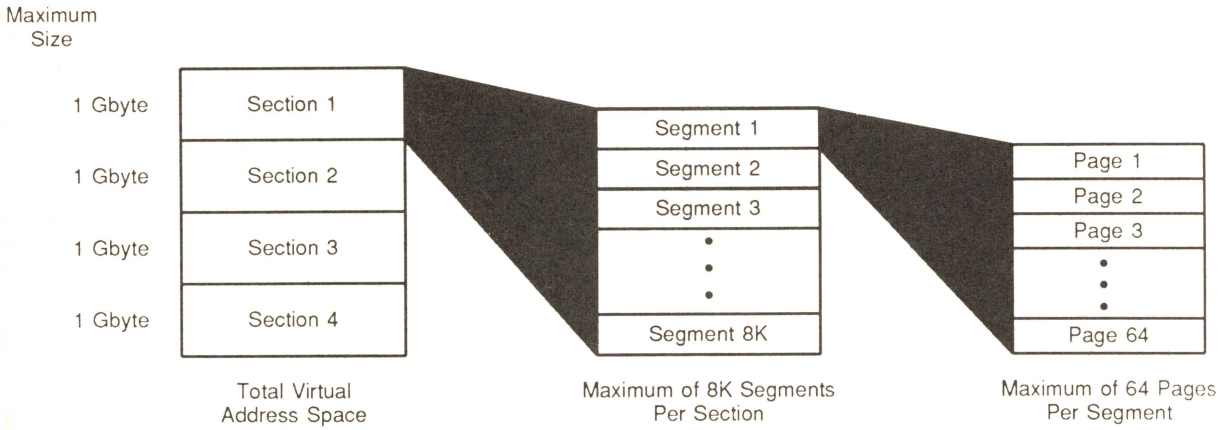
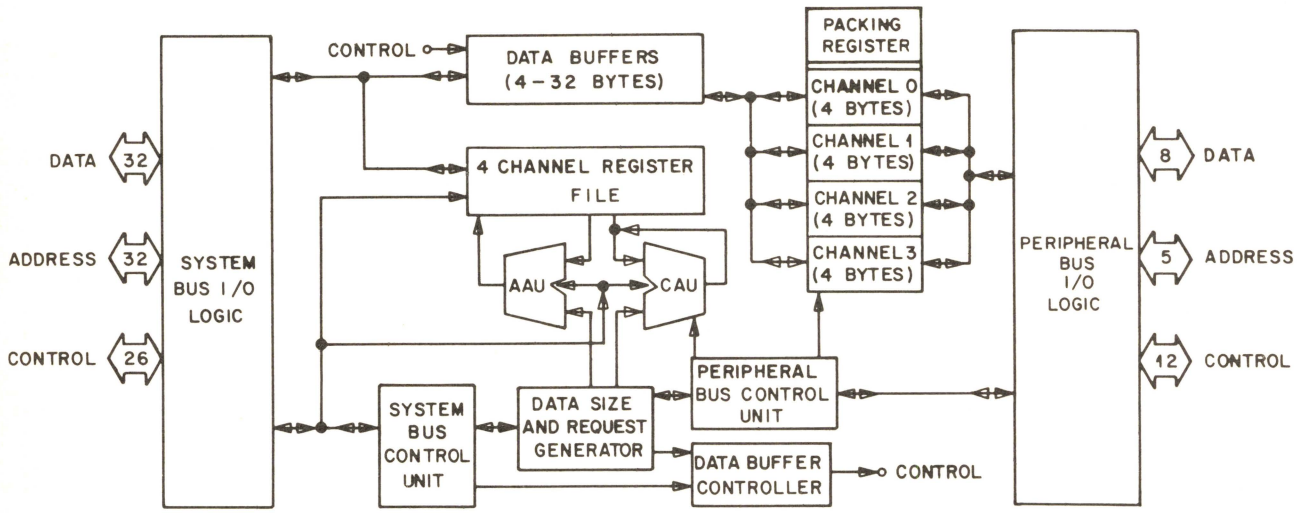
WE *32101 MMU: Paged Virtual Address Space*




WE *32104 DMA Controller Block Diagram*




AAU–ADDRESS ARITHMETIC UNIT
CAU–COUNT ARITHMETIC UNIT

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### *WE* 32102 Clock

- Available in 10-, 14-, 18-, and 24-MHz
- All outputs capable of handling up to 130 pF of capacitive loading
- Input for an external clock source
- CMOS-level inputs and outputs

The *WE* 32102 Clock supplies the two-phase, CMOS-level, frequency source required by the *WE* 32-Bit Microprocessors and Peripherals. Two of the three clock outputs are of the same basic frequency (10-, 14-, 18-, or 24-MHz), but 90° out-of-phase. The third output is twice the basic frequency. The *WE* 32102 Clock can be controlled by either its internal crystal or by an external frequency source for testing purposes. The clock is packaged in a hermetically sealed, metal can (double-width DIP) and requires a single +5 V supply.

### *WE* 32103 DRAM Controller

- Low-power, 1.5-micron, CMOS technology
- 10-, 14-, and 18-MHz operations
- Overlaps memory accesses with MMU address translation
- Provides 5-cycle access for CPU, CPU/MMU, and CPU/MMU/DMAC systems
- Supports double- and quad-word memory access
- Full support for error detection and correction devices
- Drives up to 88 DRAM devices without external buffers
- Controls a variety of DRAM configurations including 1-Mbit DRAM devices
- Internal refresh timer and refresh address counter
- Programmable DRAM access times
- Programmable support for page and nibble mode DRAM
- Supports dual-ported memory configurations using two DRAM controllers

The *WE* 32103 DRAM Controller provides the control and interface required between the *WE* 32100 CPU and commercially available dynamic RAM memories. It can be used with DRAMs as large as the AT&T 1-Mbit memory device, control 16 Mbytes of DRAM, and drive as many as 88 DRAM devices without external buffers. The *WE* 32103 DRAM Controller uses a pre-translation technique allowing it to work in parallel with a memory management unit (MMU). With an MMU in the system, the DRAM controller can respond to a CPU-initiated read in five clock cycles. While the MMU is translating a paged virtual address into a corresponding physical address, the DRAM controller initiates the actual memory access. This is possible because the low order bits of the virtual address do not change during virtual-to-physical address translation.

#### *Data Sizes*

The *WE* 32103 DRAM Controller supports byte, half-word, word, double-word, and quad-word accesses. The designer can interface any commercially available DRAMs using the controller's configuration registers to match the design properties of the selected DRAM.

#### *Error Detection and Correction*

High-performance fault-tolerant systems can be designed using commercially available error detection and correction units (EDCs) with the DRAM controller. The controller provides all of the signals needed to interface to an EDC unit. For high reliability applications, programmable support is provided for periodic error scrubbing and automatic check-bit initialization.

#### *Other Features*

A dual-ported memory can be configured using two DRAM controllers and ordinary DRAM devices. Additionally, the controller can be programmed to provide a wide variety of refresh schemes using an internal programmable refresh timer and an external refresh request input.

### *WE* 32104 DMA Controller

- Low-power, 1.5-micron, CMOS technology
- 10-, 14-, and 18-MHz operation
- Full 32-bit address and data buses
- 8-bit peripheral bus for decoupling I/O devices from the system bus
- Double- and quad-word bus cycles available for high system throughput
- Internal data buffers to support burst data peripherals
- Four independent prioritized DMA channels
- Two programmable interrupt vectors per channel
- Memory-to-memory transfers at rates up to 14.4 Mbytes/s at 18 MHz
- Memory-to-peripheral transfers at rates up to 9.0 Mbytes/s at 18 MHz (with burst mode)



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The *WE* 32104 DMA Controller provides the ability to transfer large amounts of data quickly and efficiently between the main memory subsystem and I/O devices or between different memory locations. The DMA controller permits the full 32-bit system bus to be used without external logic and provides a separate 8-bit peripheral bus to decouple I/O devices from the system bus. This allows concurrent operation with the CPU as well as greater system throughput. Four independent prioritized DMA channels are provided. Request chaining allows multiple transfer requests to be serviced without CPU intervention.

The DMA controller has four independent channels that allow it to serve four unrelated requests simultaneously. Each channel has a set of registers that configures and controls its operations. In addition there is one mask register shared by four channels.

System Bus Interface — provides address, data, and control signals needed to interface the *WE* 32104 DMA Controller to the *WE* 32100 Microprocessor.

Data Buffers — each of the four channels has a 32-byte data buffer. The lowest address data buffer is used as the memory fill data register (MFDR). This register contains the data written to consecutive locations during memory fill operations.

Register File — contains eight control registers for each DMA channel and one global register. The control registers consist of source address, destination address, transfer count, base address, mode, device control, interrupt vector, and status and control registers. The global register is a mask register used to disable particular channel activity.

Address Arithmetic Unit (AAU) — calculates addresses of source and destination using information from the per channel registers and the data size and request generator.

Count Arithmetic Unit (CAU) — calculates number of bytes to be transferred using information from the per channel registers and the data size and request generator.

Packing Registers — used to pack bytes into larger operands when transferring from the peripheral bus to the system bus. Also, to unpack large system bus operands to bytes when transferring to the peripheral bus.

Peripheral Bus — used to communicate with 8-bit I/O devices

### *WE* 32106 Math Acceleration Unit

- Compatible with ANSI/IEEE Standard 754-1985 for Binary Floating Point Arithmetic
- Single (32-bit), double (64-bit), and double-extended (80-bit) precision capability
- Add, subtract, multiply, divide, remainder, negate, absolute value, and square root functions
- 32-bit I/O interface
- Support of transcendental functions via the *WE* 321SG Software Generation Programs
- Symmetric integer, decimal, and floating-point conversions

The *WE* 32106 Math Acceleration Unit (MAU) provides ANSI/IEEE standard floating-point coprocessing capability for the CPU. The MAU can operate in peripheral mode, allowing operation with general-trade microprocessors, or as a coprocessor for the *WE* 32100 Microprocessor. It provides single (32-bit), double (64-bit), and double-extended (80-bit) precision for add, subtract, multiply, divide, remainder, square root, and compare operations. The operand, result, status, and command information transfers take place over a 32-bit bidirectional data bus that provides the interface to the host microprocessor.

*Data Formats*

The MAU supports floating-point numbers with single precision, double precision, and double-extended precision formats. It also provides signed decimal number (BCD) and signed integer representation.

### *WE* 32200 Microprocessor

- Low-power, 1-micron, CMOS technology
- 24-MHz and higher frequency operation
- 133-pin square, hermetic, ceramic pin grid array package
- Full 32-bit address and data paths
- 32 on-chip 32-bit registers
- *WE* 32100 CPU protocol and object code compatible
- Direct support for process-oriented operating systems, such as *UNIX* System V
- Multiuser system support of *UNIX* System V
- Extensive and orthogonal instruction set
- Efficient high-level language execution
- Dynamically selectable two-word blockfetch for instruction cache fill
- 25 addressing modes
- 4 Gbytes of direct memory addressing
- General-purpose coprocessor interface
- Monadic, dyadic, and triadic instructions
- Four levels of execution privilege
- 15-level interrupt structure
- Autovector and nonmaskable interrupt facilities

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- On-chip 64 × 32-bit instruction cache
- Arbitrary byte alignment for data and instructions
- Dynamic bus sizing
- Byte replication

The *WE* 32200 Microprocessor is the next generation of the single-chip, 32-bit *WE* 32100 Microprocessor. It is protocol and upward object code compatible with the *WE* 32100 CPU. In conjunction with the *WE* 322SG Software Generation Programs, the *WE* 32200 CPU provides a two-time performance improvement over the *WE* 32100 CPU. The new features of the *WE* 32200 CPU include:

- Arbitrary byte alignment for data and instructions
- New addressing modes to support more efficient array access
- Additional kernel and user registers
- Enhanced quick interrupt
- Enhanced loop control
- BCD arithmetic instructions
- Enhanced semaphore support
- Dynamic bus sizing
- Byte replication

### *WE* 32201 Memory Management Unit

- Low-power, 1-micron, CMOS technology
- 24-MHz and higher frequency operation
- 133-pin square, hermetic, ceramic pin grid array package
- Manages mapping of up to 4 Gbytes of virtual address space and up to 4 Gbytes of physical address space
- One and a half cycle virtual-to-physical address translation
- Fully associative, CAM based, 64-entry page descriptor cache
- Support for paged and contiguous segments
- On-chip, 4-Kbyte, two-way, set-associative instruction/data cache
- Transparent multiple context support, with internal management of context identification
- Variable page size
- Four execution levels with access rights checking
- On-chip cache miss-processing
- Hardware support for *UNIX* System demand paging with automatic referenced/modified bit update
- Indirect segment descriptors for support of shared segments
- Comprehensive fault detection and resolution
- Protocol compatible with the *WE* 32101 Memory Management Unit

The *WE* 32201 Memory Management Unit (MMU) provides high-performance memory management support for *WE* 32200 Microprocessor based systems. The VLSI device provides logical-to-physical address translation and access protection for the *WE* 32200 Microprocessor. It has 32-bit data and address buses and is upward protocol compatible with the *WE* 32101 MMU. The MMU can map 4 Gbytes of virtual memory into a maximum of 4 Gbytes of physical memory. Paged segments are supported with access rights checking for system protection. A 64-entry, fully associative page descriptor cache provides a 99.8% hit rate. Transparent multiple contexts are supported for faster context switching. The MMU also allows the use of shared segments for interprocess communication.

The on-chip, 4-Kbyte, two-way, set-associative instruction/data cache returns data with zero wait states on *WE* 32200 CPU virtual and physical memory accesses. Transparent data cache miss-processing and zero wait-state hits significantly reduce overall system access wait states. The physical cache stores multiple contents and performs bus monitoring to maintain cache integrity.

### *WE* 32204 DMA Controller

- Low-power, CMOS technology
- 24-MHz frequency operation
- Full 32-bit address and data buses
- 8-bit peripheral bus for decoupling I/O devices from the system bus
- Double- and quad-word bus cycles available for high system throughput
- Internal data buffers to support burst data peripherals
- Four independent prioritized DMA channels
- Two programmable interrupt vectors per channel
- Memory-to-memory transfers at rates of up to 19.2 Mbytes/s at 24 MHz
- Memory-to-peripheral transfers at rates of up to 12.0 Mbytes/s at 24 MHz (with burst mode)
- Memory fill operations available for writing an arbitrary constant to a block of memory



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The *WE* 32204 DMA Controller is a memory-mapped peripheral device that performs memory-to-memory, memory-to-peripheral, peripheral-to-memory, and memory fill data transfers quickly and efficiently. The DMA controller contains specialized hardware that permits transfers at a much faster rate than possible under microprocessor control. When used with the *WE* 32200 Microprocessor, the *WE* 32204 DMA Controller permits the full 32-bit width of the system bus to be used without external interfacing logic. In addition, a peripheral bus is provided to decouple 8-bit input/output devices from the system bus.

The DMA controller has four independent channels, which allow it to serve four unrelated transfer requests simultaneously. Each channel has a set of registers that configures and controls its operation. In addition, there is one mask register that is shared between the four channels. When the DMA controller is in peripheral mode, registers within the DMA controller and registers within devices connected to the peripheral bus are accessed by the CPU. This procedure provides the CPU an access path to the peripheral bus. The seven functional elements of the DMA controller are:

System Bus Interface — provides the address, data, and control signals needed to interface the DMA controller to the *WE* 32200 Microprocessor.

Data Buffers — each of the four channels has a 32-byte data buffer. The lowest address data buffer is used as the memory fill data register (MFDR). This register contains the data that is written to consecutive locations during memory fill operations.

Register File — contains eight control registers for each DMA channel and one global register. The control registers consist of source address, destination address, transfer count, base address, mode, device control, interrupt vector, and status and control registers. The global register is a mask register used to disable particular channel activity.

Address Arithmetic Unit (AAU) — calculates the addresses of source and destination using information from the per channel registers and the data size and request generator.

Count Arithmetic Unit (CAU) — calculates the number of bytes to be transferred using information from the per channel registers and the data size and request generator.

Packing Registers — used to pack bytes into larger operands when transferring from the peripheral bus to the system bus. Also, it is used to unpack large system operands to bytes when transferring to the peripheral bus.

Peripheral Bus — used to communicate with 8-bit I/O devices.

### *WE* 32206 Math Acceleration Unit

- Low-power, 1-micron, CMOS technology
- 24-MHz and higher frequency operation
- 133-pin square, hermetic, ceramic pin grid array package
- Full compliance with ANSI/IEEE standard 754-1985 for Binary Floating-Point Arithmetic
- Single (32-bit), double (64-bit), and double-extended (80-bit) precision capability
- Eight 80-bit user registers
- Add, subtract, multiply, divide, remainder, negate, absolute value, square root, sine, cosine, arctan, and pi operations
- Compare, move, and rounding to integral value functions
- On-chip trigonometric functions
- Coprocessor and peripheral mode interfaces
- Symmetric integer, decimal, and floating-point conversions
- 32-bit I/O interface

The *WE* 32206 Math Acceleration Unit (MAU) is an enhanced coprocessor that provides high-speed, ANSI/IEEE floating-point processing support for the *WE* 32200 Microprocessor. The MAU can operate in peripheral mode, allowing operation with general-trade microprocessors, or as a coprocessor for the *WE* 32200 CPU. Microprocessor systems using the *WE* 32206 MAU will have a two-times performance improvement over systems using the *WE* 32106 MAU. The *WE* 32206 MAU is protocol and upward object code compatible with the *WE* 32106 MAU.

### *WE* 321SG C-Software Generation Programs

*Utilities*

- C Compiler
- Assembler
- Link Editor
- Disassembler
- Object Code Optimizer
- Archiver and Library Maintainer
- Object File Host Converter


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- Object and Archive File Converter
- Object File Dumper
- Source Code Lister
- Object File Orderer
- Symbol Table Printer
- Object File Stripper

*Libraries*

- Math Libraries
- Floating-Point Emulation Library
- Common Object File Access Library
- *UNIX* System Libraries
  - — Standard C Library
  - — PW Library
  - — Debug Library
  - — LEX Library
  - — Memory Allocation Library
  - — YACC Library

The *WE* 321SG C-Software Generation Programs (C-SGPs) allow the computing power of a host *UNIX* System to be used in the creation, debugging, and downloading of software to a *WE* 32100 Microprocessor. This support software provides utility programs that enable the user to write applications software in both C and assembly languages. The C-SGP supports both software floating-point emulation (FPE) and hardware math acceleration units (MAUs). The hardware mode provides enhanced floating-point performance through the use of in-line compilation of the MAU instruction set. The software mode allows for emulation of floating-point capabilities using floating-point emulation library routines.

### *WE* 321DS Microprocessor Development System

- Emulation of the *WE* 32100 Microprocessor, *WE* 32101 Memory Management Unit, and the *WE* 32102 Clock in a target system with no wait states
- 52 Kbytes of user available static RAM
- Assembly-level debugger and optional C-level symbolic debugger
- Physical and virtual mode debugging capability
- Memory map option switch to select pod-based or target-based interrupt and exception pointers
- Hardware and software breakpointing
- Software support for the *WE* 32106 Math Acceleration Unit
- Two RS-232C serial I/O ports
- Logic analyzer access connectors
- Stand-alone pod that can operate without additional support
- Target signal isolation
- Reset and abort pushbuttons
- On-board or external clock
- Eight-character alphanumeric LED display
- System self-test firmware
- Optional software support package for a Hewlett-Packard 64000 Logic Development System

The *WE* 321DS Microprocessor Development System is an integrated hardware and software system used to develop, test, and debug *WE* 32100 Microprocessor based applications. It consists of items that can be ordered individually. The main component of the development system is the *WE* 321AP Microprocessor Analysis Pod.

The analysis pod can emulate the functions of the *WE* 32100 Microprocessor, *WE* 32101 Memory Management Unit, and *WE* 32102 Clock in the target system under development, and is essential for diagnosing target hardware and software problems. The analysis pod contains a complete firmware-based interactive monitor program (IMP) for assembly-level debugging and the firmware portion of Ferret, a C-level symbolic debugger.

The development system also includes the *WE* 321SD Development Software Programs, a package of *UNIX* System based software that runs on either an AT&T 3B2/300 or 400 Computer or *VAX* 11/780 Computer. This package includes utility programs for downloading from a host system using IMP, I/O routines, and optional software for the Ferret C-level symbolic debugger. An additional software package is available that supports logic analysis with the Hewlett-Packard 64000 Logic Development System.

The *WE* 321DS Microprocessor Development System can operate in any of four configurations: as a stand-alone system, as a hardware development station, as a software development station, or as an integrated hardware and software development station.

### *WE* 321DM/*WE* 322DM CPU & MMU Device Monitors

- Signal observation of target systems operating at frequencies up to 24 MHz with zero wait states
- Eight logic analyzer access connectors (one connector is user definable)
- Timing connectors for direct access to all CPU and MMU signals
- Software support package for the Hewlett-Packard 64000 Logic Development System



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- Supports blockfetch accesses at target system frequencies up to 24 MHz
- Switches to select transparent or latched operation mode and single or multiple sampling points per bus cycle

The *WE* 321DM/*WE* 322DM CPU & MMU Device Monitors provide a low-cost solution for debugging *WE* 32100/*WE* 32200 Microprocessor and *WE* 32101/*WE* 32201 Memory Management Unit based applications operating at frequencies up to 24 MHz with a logic analyzer that is limited to a maximum sample rate of 10 MHz.

The device monitor consists of a logic retiming unit, a CPU cable system, an MMU cable system, and seven 25-wire ribbon cables that provide a standard interface to a logic analyzer. The CPU and MMU cable systems contain footprint connectors that replace the CPU and MMU devices in the target system. The device monitor can be used for target systems with or without an MMU. The footprint connectors plug directly into the CPU and MMU sockets in the target systems and are linked by umbilical cables to two buffer boards (one each for the CPU and MMU). The device(s) replaced in the target system by the footprint connector(s) plug directly into zero insertion force sockets on the buffer board(s). These boards connect via cables to the logic retiming unit.

The device monitor allows signal observation of high-speed target systems with a logic analyzer that has 10 MHz sampling rates by:

- Generating logic analyzer sample points based on bus cycle activity and guaranteeing a minimum of 100 ns between sample points at target system operating frequencies as high as 24 MHz
- Sampling and holding signals as necessary to assure 30 ns signal set-up and 0 ns hold times with respect to selected sampling points and a target system operating frequency up to 24 MHz
- Providing the flexibility of observing a narrow window of bus activity in detail or a larger window with reduced detail and greater perspective of system bus activity

These device monitors support zero wait-state block fetch accesses at frequencies of 18 MHz and 24 MHz, respectively.

### *WE* 321EB Microprocessor Evaluation Board

- *WE* 32100 Microprocessor
- *WE* 32101 Memory Management Unit
- *WE* 32106 Math Acceleration Unit
- *WE* 32102 Clock (18 MHz)
- 64 Kbytes of high-speed static RAM
- 32 Kbytes of additional RAM
- 64-Kbyte ROM-resident interactive monitor program (IMP) and system self-test program
- Program trace and breakpoint capability
- Seven individually maskable interrupts
- Twenty-four programmable parallel I/O lines
- Two RS-232C serial I/O ports with selectable baud rates (300-9600)
- Communication with terminal and with *UNIX* System host
- Three programmable 16-bit interval timers
- Eight-character LED display (17-segment)
- Push-button reset and abort switches
- *WE* 32106 Math Acceleration Unit software support

The *WE* 321EB Microprocessor Evaluation Board is a *WE* 32100 Microprocessor-based single-board microcomputer evaluation system. It allows evaluation of the hardware and software capabilities and performance of the *WE* 32100 Microprocessor, *WE* 32101 Memory Management Unit, and the *WE* 32106 Math Acceleration Unit in an application environment. In addition to these components, the board contains a *WE* 32102 Clock (18 MHz), a ROM-based interactive monitor and system self-test programs, 96 Kbytes of RAM, and I/O circuitry.

### *WE* 321SB VMEbus Single Board Computer

- Full capability for supporting *UNIX* System V/VME
- *WE* 32100 Microprocessor (CPU) operating at 14 MHz and 18 MHz
- *WE* 32101 Memory Management Unit (MMU) operating at 14 MHz and 18 MHz
- *WE* 32106 Math Acceleration Unit (MAU) operating at 14 MHz and 18 MHz
- 1 Mbyte of DRAM with byte parity
- Up to 256 Kbytes of EPROM or ROM
- Two RS-232C serial I/O ports
- Three user-programmable counter/timers
- On-board debug monitor and self-test firmware
- VMEbus master/slave capabilities
- Optional cross software generation programs
- Optional selected peripheral device drivers

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The *WE* 321SB VMEbus Single Board Computer (SBC) is a high-performance, 32-bit, single board computer that facilitates the user-defined VMEbus computer systems. Using the SBC with the *UNIX* System V/VME users can design and assemble open-architecture, demand-paged *UNIX* Systems that are object file and floppy disk format compatible with the AT&T 3B Computer family. Thus, many hundreds of applications and language packages available for the 3B computer will execute directly on a VMEbus computer built using the SBC and *UNIX* System V/VME. This compatibility gives SBC users immediate access to one of the largest collections of off-the-shelf *UNIX* System software available today.

### *UNIX* System V Release 2/3

- Multi-user/multi-tasking
- Enhanced C software generation system with symbolic debugging includes shared library
- Demand-paged virtual memory gives at least 16 Mbytes of linear address space per process; includes U page
- File and record locking system calls provide user data protection
- Self-configuration allows installation of new drivers without regenerating the system
- Simplified system administration eliminates the need for a full-time, on-site systems expert
- Job control language
- Cross-compilers allow program development in a large computer environment
- Exploits *UNIX* System oriented features of the *WE* 32100 Microprocessor chip set, such as full 32-bit architecture, efficient process switching, memory management, and optional hardware floating-point capability
- Facilitates personalization to user-developed hardware configurations
- Easy to use documentation
- Remote file sharing using Ethernet local area network
- Improved signal mechanisms
- Incremental back-up of nested systems

### Additional Features for *UNIX* System V Release 3

- Internationalization, includes support for 8-bit code set, alternate date/time formats, and character class/ conversion rules
- Assists menu/forms interface
- Faster Curses/Terminfo support the writing of terminal-dependent applications
- Remote file sharing (RFS)
- STREAMS Mechanism and Tools
- AT&T Transport Interface
- Media-independent uucp
- Executable shared libraries
- ASSIST Interface
- Performance improvements, including paging the user area, remote file sharing client caching, and smaller and faster curses
- Complies completely with the *UNIX* System V Interface Definition Issue 2 (SVID) (i.e., passes the *UNIX* System V Verification Suite Release 3)

*UNIX* System V Release 2/3 source code provides the operating system and user interfaces for the 32-bit *WE* 32100/32200 Microprocessor chip set. Optionally, this software may be compiled by the user with an optimized version of the *WE* 321SG C-Software and Cross C-Software Generation Programs for the *WE* 32100 Microprocessor chip set. The optimized Cross C-Software Generation Programs provide several levels of optimization and different types of floating-point support as runtime options.

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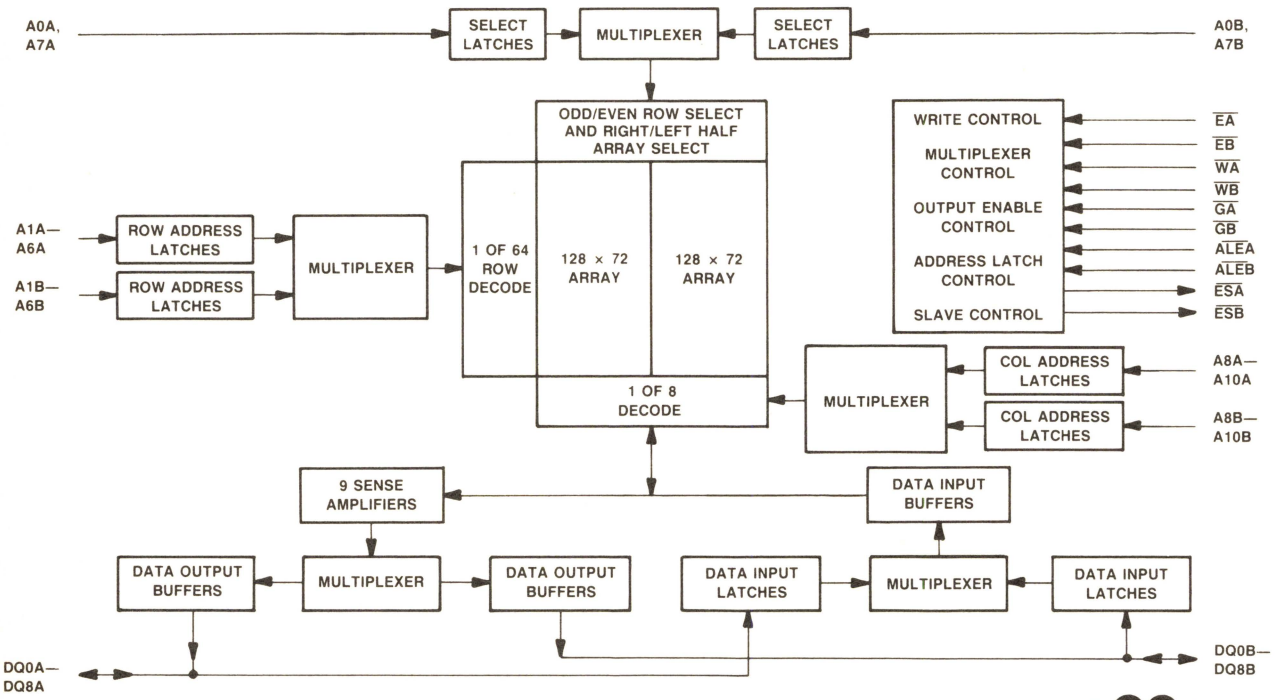
### Description

The M79018DX-15 integrated circuit is a 2048-word by 9-bit, clocked, static Dual Port RAM. It can be viewed as shared memory in that any cell can be accessed from either of two ports. Each port has its own address bus, data bus, and control leads. All contention between the two ports is arbitrated internally. The M79018DX-15 is TTL compatible, requires a single 5 volt supply, is manufactured using CMOS technology, and is available in a 68-pin leaded plastic chip carrier.

### Features

- 2048 words × 9-bit organization
- Full internal contention resolution transparent to the user
- Guaranteed access time with contention for either port of 150 ns
- Guaranteed uncontested access time of 75 ns
- Guaranteed cycle time for either port of 180 ns
- Power dissipation less than 330 mW
- 550 μW standby power, max.
- Two independent bidirectional data buses
- Two independent sets of address buses
- Data and read/write information gated and latched by Enable ($\overline{E}$)
- Addresses gated and latched by Address Latch Enable ($\overline{ALE}$)
- Word-size expansion capability
- CMOS static memory array
- TTL-compatible inputs and outputs

*Figure 1. M79018DX-15 Dual Port RAM Block Diagram*

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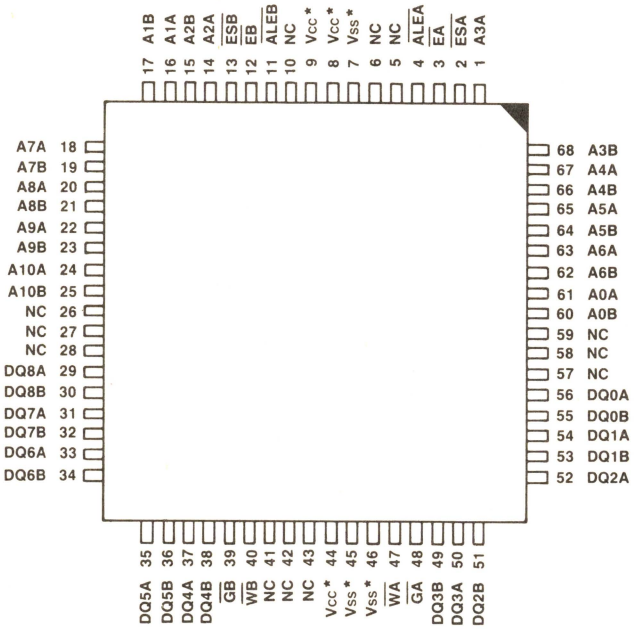
### Pin Descriptions

*Figure 2. Pin Function Diagram*




* All Vcc and Vss pins must be connected for proper operation.

*Pin Description Key*

| Symbol | Type | Name |
|---|---|---|
| Vcc | — | +5 V Supply |
| DQ(#)** | I/O | Data In/Data Out |
| A(#)** | I | Address Input |
| $\overline{W}$** | I | Write Enable |
| $\overline{E}$** | I | Enable |
| Vss | — | Ground |
| $\overline{ES}$** | O | Enable Slave |
| $\overline{ALE}$** | I | Address Latch Enable |
| NC | — | No Connection |
| $\overline{G}$** | I | Output Enable |

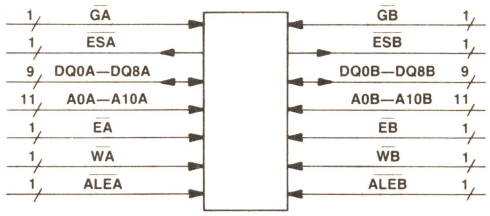
** Letter "A" or "B" follows the terminal designation indicating which port is being referenced.

### Overview

The M79018DX-15 is an 18K-bit, clocked, static, read/write CMOS memory device which provides access to any cell through either of two ports. Each port has eleven address input leads, nine bidirectional 3-state I/O leads, an output enable lead, an address latch enable lead, an enable slave output lead, an enable lead, and a write enable lead. Figure 3 is a logic diagram of the M79018DX-15 DPRAM device.

The feature of asynchronous access from two ports makes this device useful in a wide variety of applications in which a "mail box" type of function is needed or where shared RAM is required. The M79018DX-15 DPRAM also features word size expansion capability.

*Figure 3. Logic Symbol*




### Device Operation

Ports A and B are totally independent of each other, with a worst case guaranteed access time specified at 150 ns. This worst case access time specification includes a memory access, a precharge, and a second memory access. All contention between the ports is arbitrated internally. Single port access requests, or the first serviced access requests, are completed in one-half the worst case access time.

The port Enable ($\overline{E}$) input starts every memory cycle. Input data (write cycle) and the write enable information associated with the port are gated and latched with this signal. This information must be valid at the falling edge of the appropriate enable signal.

A read cycle occurs when $\overline{E}$ goes low with Write Enable ($\overline{W}$) high. $\overline{W}$ must be high when $\overline{E}$ goes low and must remain high for at least 20 ns. A write cycle occurs if $\overline{W}$ is low when $\overline{E}$ goes low. During a write cycle, the data output pins are disabled (high impedance state). The data bus is also disabled whenever its associated $\overline{E}$ or Output Enable ($\overline{G}$) lead is high.

On the falling edge of Address Latch Enable ($\overline{ALE}$), the address information associated with the port is gated and latched internally. Address information must be valid on the falling edge of this lead. Address latching with the $\overline{ALE}$ lead is independent of $\overline{E}$ and is also independent of any action taken on the other port. The only requirement on $\overline{ALE}$ with respect to $\overline{E}$ is that $\overline{ALE}$ must latch address information for the desired cycle before or coincident with $\overline{E}$.

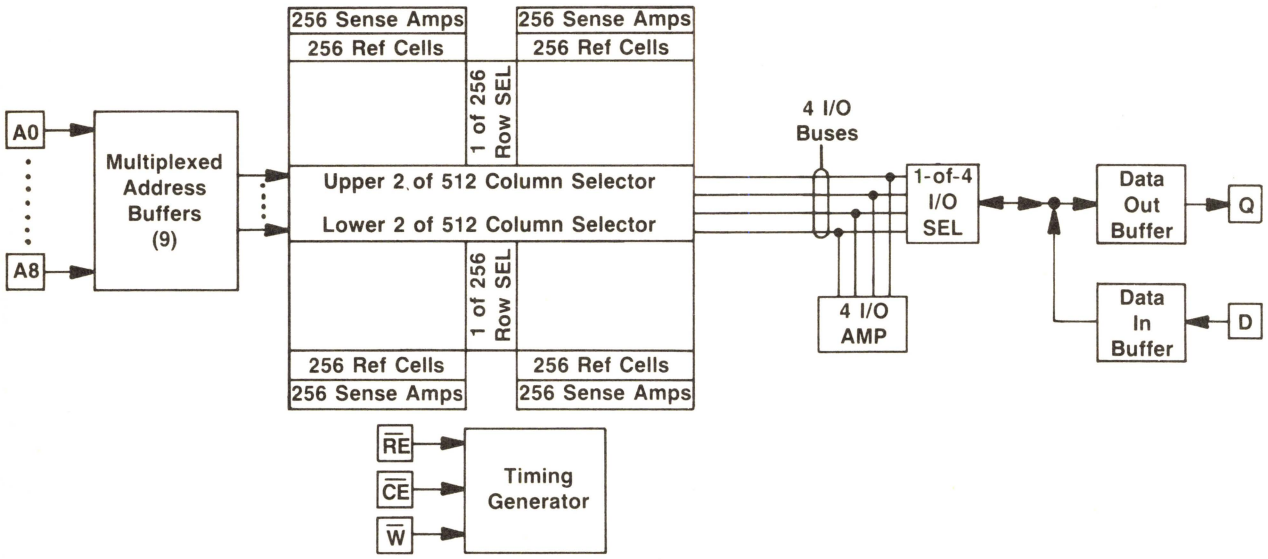
### Description

The M41256xxM15B integrated circuit is a high-speed, low-power 262,144 words by 1-bit dynamic random access memory (DRAM) device. The device is manufactured according to the general requirements of MIL-STD-883, is screened according to Method 5004 for a class B device, and meets the qualification and quality conformance requirements of Method 5005.

### Features

- Military temperature range, Tc = −55°C to +110°C
- Complies with MIL-STD-883
- 262,144 words × 1-bit organization
- 150 ns access time from $\overline{RE}$
- 75 ns access time from $\overline{CE}$
- 360/330 mW active power, Page Mode at minimum cycle time
- 55 mW standby power
- Multiplexed address inputs
- ±10% power supply tolerance
- Read-Modify-Write capabilities
- $\overline{RE}$ Only refresh/Hidden Refresh
- Latched or high-impedance output during refresh
- 256 refresh cycles
- Page Mode operation
- Available in a hermetic ceramic DIP

*Figure 1. Page Mode Block Diagram*



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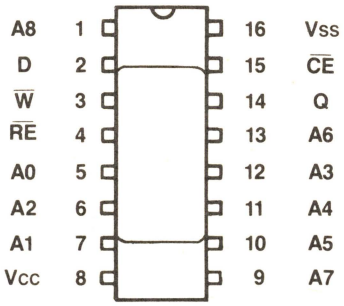
### Pin Descriptions

*Figure 2. Pin Function Diagram*




*Pin Description Key*

| Symbol | Name |
|---|---|
| Vcc | +5 V Supply |
| D | Data In |
| Q | Data Out |
| A(0-8) | Address Input(0-8) |
| $\overline{W}$ | Write Enable |
| $\overline{RE}$ | Row Enable |
| $\overline{CE}$ | Column Enable |
| Vss | Ground |
| NC | No Connect |

### Operating Conditions

*(Tc = −55°C to +110°C)*

| Parameter | Symbol | Min | Nom | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltages | Vcc | 4.5 | 5.0 | 5.5 | V |
| | Vss | 0 | 0 | 0 | V |
| Input Voltages* | | | | | |
| High Level — All Inputs (Logic 1) | VIH | 2.4 | — | 7.0 | V |
| Low Level — All Inputs (Logic 0) | VIL | −1.0 | — | 0.8 | V |
| Refresh Cycle Time** | tREF | — | — | 4.0 | ms |

* Application of invalid levels may destroy stored information during that cycle as well as the first cycle using valid levels. Data out is indeterminate.

** Addresses A0—A7 are used for refresh. A8 must be a valid one or zero.

**This part is also available in a JAN B version, which is in full compliance with MIL-M-38510.**

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# HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

## GENERAL PURPOSE

| Description | Model | Offset Voltage, max: At 25°C, (±mV) | Offset Voltage, max: Temp Drift, (±μV/°C) | Bias Current (25°C), max (nA) | Open Loop Gain, min (dB) | Frequency Response: Unity Gain (MHz) | Frequency Response: Slew Rate (V/μsec) | Rated Output, min: (±V) | Rated Output, min: (±mA) | Temp Range[1] | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Low Power | OPA21GZ | 0.5 | 5 | 50 | 114 | 0.3 | 0.2 | 13.6 | 1.3 | Ind | DIP |
| | OPA21EZ | 0.1 | 1 | 25 | 120 | 0.3 | 0.2 | 13.7 | 1.4 | Ind | DIP |
| Switchable Input | OPA201AG | 0.5 | 5 | 50 | 114 | 0.5 | 0.1 | 13.5 | 5 | Com | DIP |
| | OPA201BG | 0.2 | 2 | 40 | 114 | 0.5 | 0.1 | 13.5 | 5 | Com | DIP |
| | OPA201CG | 0.1 | 1 | 25 | 120 | 0.5 | 0.1 | 13.5 | 5 | Com | DIP |
| | OPA201SG | 0.2 | 2 | 40 | 114 | 0.5 | 0.1 | 13.5 | 5 | MIL | DIP |
| Low Cost FET | OPA121KP* | 3 | 10 | ±0.010 | 106 | 2 | 2 | 10 | 5 | Com | DIP |
| | OPA121KM | 2 | 10 | ±0.005 | 110 | 2 | 2 | 10 | 5 | Com | TO-99 |
| Wide Temp Range | OPA11HT | 5 | 5[2] | ±25 | 94 | 12.0 | 7.0 | 10 | 15 | −55°C to +175°C | TO-99 |
| | OPA27HT | 0.05 | 0.25[2] | 1μA | 120 | 6 | 1.9 | 12 | 16[2] | −55°C to +200°C | TO-99 |
| | OPA37HT | 0.05 | 0.25[2] | 1μA | 120 | 36 | 11.9 | 12 | 16[2] | −55°C to +200°C | TO-99 |
| | OPA111HT | 0.5 | 8[2] | 0.002 | 114 | 2 | 2 | 10 | 5 | −55°C to +200°C | TO-99 |

* Indicates product is available in 20-pin ceramic leadless chip carriers.
NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (2) Typical.

## LOW DRIFT (≤5μV/°C)

| Description | Model | Offset Voltage, max: At 25°C (±mV) | Offset Voltage, max: Temp Drift (±μV/°C) | Bias Current (25°C), max (nA) | Open Loop Gain, min (dB) | Frequency Response: Unity Gain (MHz) | Frequency Response: Slew Rate (V/μsec) | Rated Output, min: (±V) | Rated Output, min: (±mA) | Temp Range[1] | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FET | OPA111AM* | 0.5 | 5 | ±0.002 | 114 | 2 | 2 | 11 | 5 | Ind | TO-99 |
| | OPA111BM | 0.25 | 1 | ±0.001 | 120 | 2 | 2 | 11 | 5 | Ind | TO-99 |
| | OPA111SM | 0.5 | 5 | ±0.002 | 114 | 2 | 2 | 11 | 5 | MIL | TO-99 |
| Wideband | OPA156AM | 2 | 5 | 0.05 | 94 | 6 | 14 | 10 | 5 | MIL | TO-99 |
| | OPA356AM | 2 | 5 | 0.05 | 94 | 6 | 14 | 10 | 5 | Com | TO-99 |
| | OPA606LM | 0.5 | 5 | ±0.01 | 100 | 13 | 35 | 12 | 5 | Com | TO-99 |
| Dual FET | OPA2111BM* | 0.5 | 2.8 | ±0.004 | 114 | 2 | 2 | 11 | 5 | Ind | TO-99 |
| Bipolar | OPA27A* | 0.025 | 0.6 | ±40 | 120 | 8 | 1.9 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA37A* | 0.025 | 0.6 | ±40 | 120 | 63[2] | 11.9 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA27B | 0.060 | 1.3 | ±55 | 120 | 8 | 1.9 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA37B | 0.060 | 1.3 | ±55 | 120 | 63[2] | 11.9 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA27C | 0.100 | 1.8 | ±80 | 117 | 8 | 1.9 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA37C | 0.100 | 1.8 | ±80 | 117 | 63[2] | 11.9 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA27E | 0.025 | 0.6 | ±40 | 120 | 8 | 1.9 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA37E | 0.025 | 0.6 | ±40 | 120 | 63[2] | 11.9 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA27F | 0.060 | 1.3 | ±55 | 120 | 8 | 1.9 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA37F | 0.060 | 1.3 | ±55 | 120 | 63[2] | 11.9 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA27G | 0.100 | 1.8 | ±80 | 117 | 8 | 1.9 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA37G | 0.100 | 1.8 | ±80 | 117 | 63[2] | 11.9 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA27GP | 0.100 | 1.8 | ±80 | 117 | 8 | 1.9 | 12 | 16.6 | Com | DIP |
| | OPA37GP | 0.100 | 1.8 | ±80 | 117 | 63[2] | 11.9 | 12 | 16.6 | Com | DIP |
| Low Power | OPA21EZ | 0.1 | 1 | 25 | 120 | 0.3 | 0.2 | 13 | 5 | Ind | DIP |
| | OPA21GZ | 0.5 | 5 | 50 | 114 | 0.3 | 0.2 | 13 | 5 | Ind | DIP |

* Indicates product is available in 20-pin ceramic leadless chip carriers.
NOTES: (1) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (2) Gain-bandwidth product for OPA37. $A_V$ = 5 minimum.

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# HIGH PERFORMANCE OPERATIONAL AMPLIFIERS (cont.)

| LOW BIAS CURRENT (≤50pA) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Offset Voltage, max | | Bias Current | Open Loop | Frequency Response | | Rated Output, min | | | |
| Description | Model[1] | At 25°C, (±mV) | Temp Drift, (±μV/°C) | (25°C), max (pA) | Gain, min (dB) | Unity Gain (MHz) | Slew Rate (V/μsec) | (±V) | (±mA) | Temp Range[2] | Package |
| Premium Performance | OPA111AM* | 0.5 | 5 | ±2 | 114 | 2 | 2 | 11 | 5 | Ind | TO-99 |
| | OPA111BM | 0.25 | 1 | ±1 | 120 | 2 | 2 | 11 | 5 | Ind | TO-99 |
| | OPA111SM | 0.5 | 5 | ±2 | 114 | 2 | 2 | 11 | 5 | MIL | TO-99 |
| Low Noise | OPA101AM | 0.50 | 10 | −15 | 94 | 10 | 6.5 | 12 | 12 | Ind | TO-99 |
| | OPA101BM | 0.25 | 5 | −10 | 94 | 10 | 6.5 | 12 | 12 | Ind | TO-99 |
| | OPA102AM | 0.50 | 10 | −15 | 94 | 40 | 14 | 12 | 12 | Ind | TO-99 |
| | OPA102BM | 0.25 | 5 | −10 | 94 | 40 | 14 | 12 | 12 | Ind | TO-99 |
| Ultra-Low Bias Current | OPA128JM* | 1 | 20 | ±0.300 | 94 | 1 | 3 | 10 | 5 | Com | TO-99 |
| | OPA128KM | 0.5 | 10 | ±0.150 | 110 | 1 | 3 | 10 | 5 | Com | TO-99 |
| | OPA128LM | 0.5 | 5 | ±0.075 | 110 | 1 | 3 | 10 | 5 | Com | TO-99 |
| | OPA128SM | 0.5 | 10 | ±0.150 | 110 | 1 | 3 | 10 | 5 | MIL | TO-99 |
| Dual FET | OPA2111AM* | 0.75 | 6 | ±8 | 110 | 2 | 2 | 11 | 5 | Ind | TO-99 |
| | OPA2111BM | 0.5 | 2.8 | ±4 | 114 | 2 | 2 | 11 | 5 | Ind | TO-99 |
| | OPA2111SM | 0.75 | 6 | ±8 | 110 | 2 | 2 | 11 | 5 | MIL | TO-99 |
| | **OPA2111KM** | **2** | **15** | **±15** | **106** | **2** | **2** | **11** | **5** | **Com** | **TO-99** |
| | **OPA2111KP** | **2** | **15** | **±15** | **106** | **2** | **2** | **11** | **5** | **Com** | **DIP** |
| Quad FET | OPA404AG* | 1 | 3[3] | ±8 | 88 | 6.4 | 35 | 11.5 | 5 | Ind | DIP |
| | OPA404BG | 0.75 | 3[3] | ±4 | 92 | 6.4 | 35 | 12 | 5 | Ind | DIP |
| | OPA404SG | 1 | 3[3] | ±8 | 88 | 6.4 | 35 | 11.5 | 5 | MIL | DIP |
| | **OPA404KP** | **2.5** | **5[3]** | **±12** | **88** | **6.4** | **35** | **11.5** | **5** | **Com** | **DIP** |
| Low Cost | OPA121KM* | 2 | 10 | ±5 | 110 | 2 | 2 | 11 | 5 | Com | TO-99 |
| | OPA121KP | 3 | 10 | ±10 | 106 | 2 | 2 | 11 | 5 | Com | DIP |
| Wideband | **OPA602AM** | **1** | **15** | **10** | **75** | **6.5** | **20** | **10** | **15** | **Ind** | **TO-99** |
| | **OPA602BM** | **0.5** | **5** | **2** | **88** | **6.5** | **24** | **10** | **15** | **Ind** | **TO-99** |
| | **OPA602CM** | **0.25** | **2** | **1** | **92** | **6.5** | **28** | **10** | **15** | **Ind** | **TO-99** |
| | **OPA602SM** | **0.5** | **5** | **2** | **88** | **6.5** | **24** | **10** | **15** | **MIL** | **TO-99** |
| | OPA606KM | 1.5 | 5[3] | ±15 | 95 | 12.5 | 33 | 11 | 5 | Com | TO-99 |
| | OPA606LM | 0.5 | 5 | ±10 | 100 | 13 | 35 | 12 | 5 | Com | TO-99 |
| | OPA606SM | 1.5 | 5[3] | ±15 | 95 | 12.5 | 33 | 11 | 5 | MIL | TO-99 |
| | OPA606KP | 3 | 10[3] | ±25 | 90 | 12 | 30 | 11 | 5 | Com | DIP |
| Low Cost, Ultra-Low Bias Current | AD515JH | 3 | 50 | 0.300 | 86 | 0.35 | 1 | 10 | 5 | Com | TO-99 |
| | AD515KH | 1 | 15 | 0.150 | 92 | 0.35 | 1 | 10 | 5 | Com | TO-99 |
| | AD515LH | 1 | 25 | 0.075 | 88 | 0.35 | 1 | 10 | 5 | Com | TO-99 |

* Indicates product is available in 20-pin ceramic leadless chip carriers.

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Typical.



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# HIGH PERFORMANCE OPERATIONAL AMPLIFIERS (cont.)

| LOW NOISE (Guaranteed $e_n$) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Offset Voltage, max | | | Frequency Response | | | | | |
| Description | Model | Noise Voltage at 10kHz, max ($nV/\sqrt{Hz}$) | Bias Current (25°C), max (pA) | At 25°C (±mV) | Temp Drift (±μV/°C) | Open Loop Gain, min (dB) | Gain Bandwidth (MHz) | Slew Rate, min (V/μsec) | Rated Output, min (±V) | Rated Output, min (±mA) | Temp Range [1] | Package |
| Bipolar | OPA27A* | 3.8 | ±40nA | 0.025 | 0.6 | 120 | 8 | 1.7 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA37A* | 3.8 | ±40nA | 0.025 | 0.6 | 120 | 63 | 11 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA27B | 3.8 | ±55nA | 0.060 | 1.3 | 120 | 8 | 1.7 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA37B | 3.8 | ±55nA | 0.060 | 1.3 | 120 | 63 | 11 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA27C | 4.5 | ±80nA | 0.100 | 1.8 | 117 | 8 | 1.7 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA37C | 4.5 | ±80nA | 0.100 | 1.8 | 117 | 63 | 11 | 12 | 16.6 | MIL | TO-99, DIP |
| | OPA27E | 3.8 | ±40nA | 0.025 | 0.6 | 120 | 8 | 11 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA37E | 3.8 | ±40nA | 0.025 | 0.6 | 120 | 63 | 11 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA27F | 3.8 | ±55nA | 0.060 | 1.3 | 120 | 8 | 1.7 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA37F | 3.8 | ±55nA | 0.060 | 1.3 | 120 | 63 | 11 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA27G | 4.5 | ±80nA | 0.100 | 1.8 | 117 | 8 | 1.7 | 12 | 16.6 | Ind | TO-99, DIP |
| | OPA37G | 4.5 | ±80nA | 0.100 | 1.8 | 117 | 63 | 11 | 12 | 16.6 | Ind | TO-99, DIP |
| Wide Bandwidth | OPA101AM | 8 | −15 | 0.5 | 10 | 94 | 20 | 5 | 12 | 12 | Ind | TO-99 |
| | OPA101BM | 8 | −10 | 0.25 | 5 | 94 | 20 | 5 | 12 | 12 | Ind | TO-99 |
| | OPA102AM | 8 | −15 | 0.5 | 10 | 94 | 40 | 10 | 12 | 12 | Ind | TO-99 |
| | OPA102BM | 8 | −10 | 0.25 | 5 | 94 | 40 | 10 | 12 | 12 | Ind | TO-99 |
| FET | OPA111AM* | 8 | ±2 | 0.5 | 5 | 114 | 2 | 1 | 11 | 5 | Ind | TO-99 |
| | OPA111BM | 8 | ±1 | 0.25 | 1 | 120 | 2 | 1 | 11 | 5 | Ind | TO-99 |
| | OPA111SM | 8 | ±2 | 0.5 | 5 | 114 | 2 | 1 | 11 | 5 | MIL | TO-99 |
| | OPA606LM | 13 | ±10 | 0.5 | 5 | 100 | 13 | 25 | 12 | 5 | Com | TO-99 |
| Low Cost | OPA27GP | 4.5 | ±80nA | 0.100 | 1.8 | 117 | 8 | 1.9 [2] | 10 | 16.6 | Com | DIP |
| | OPA37GP | 4.5 | ±80nA | 0.100 | 1.8 | 117 | 63 | 11.9 [2] | 10 | 16.6 | Com | DIP |
| Dual FET | OPA2111AM* | 8 | ±8 | 0.75 | 6 | 110 | 2 | 1 | 11 | 5 | Ind | TO-99 |
| | OPA2111BM | 8 | ±4 | 0.5 | 2.8 | 114 | 2 | 1 | 11 | 5 | Ind | TO-99 |
| | OPA2111SM | 8 | ±4 | 0.75 | 6 | 110 | 2 | 1 | 11 | 5 | MIL | TO-99 |
| | **OPA2111KM** | **6** [2] | **±15** | **2** | **15** | **106** | **2** | **1** | **11** | **5** | **Com** | **TO-99** |
| | **OPA2111KP** | **6** [2] | **±15** | **2** | **15** | **106** | **2** | **1** | **11** | **5** | **Com** | **DIP** |

* Indicates product is available in 20-pin ceramic leadless chip carriers.

NOTES: (1) Ind = −25°C to +85°C, MIL = −55°C to +125°C, Com = 0°C to +70°C. (2) Typical.

| UNITY-GAIN BUFFER | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Rated Output, min | | Frequency Response | | | | | | |
| Description | Model | (±V) | (±mA) | −3dB (MHz) | Full Power BW (MHz) | Slew Rate (V/μsec) | Gain (V/V) | Input Impedance (Ω) | Temp Range [1] | Package |
| High Performance | 3553AM | 10 | 200 | 300 | 32 | 2000 | ≈1 | $10^{11}$ | Ind | TO-3 |
| Low Cost | **OPA633AH** | **10** | **80** | **275** | **65** | **1000** | **≈1** | **$10^6$** | **Ind** | **TO-8** |
| | **OPA633SH** | **10** | **80** | **275** | **65** | **1000** | **≈1** | **$10^6$** | **MIL** | **TO-8** |
| | **OPA633KP** | **10** | **80** | **275** | **65** | **1000** | **≈1** | **$10^6$** | **Com** | **DIP** |

NOTES: (1) Ind = −25°C to +85°C, MIL = −55°C to +125°C, Com = 0°C to +70°C.

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# HIGH PERFORMANCE OPERATIONAL AMPLIFIERS (cont.)

WIDE BANDWIDTH (≥5MHz)

| Description | Model[1] | Frequency Response: Gain Bandwidth (MHz) | Frequency Response: Slew Rate, min (V/μsec) | $t_S$ ±0.1% (nsec) | Compensation | Rated Output, min (±V) | Rated Output, min (±mA) | Offset Voltage, max: At 25°C (±mV) | Offset Voltage, max: Temp Drift (±μV/°C) | Open Loop Gain, min (dB) | Temp Range[2] | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FET | 3554AM, (Q) | 1700, A = 1000 | 1000 | 120 | ext. | 10 | 100 | 2 | 50 | 100 | Ind | TO-3 |
| | 3554BM, (Q) | 1700, A = 1000 | 1000 | 120 | ext. | 10 | 100 | 1 | 15 | 100 | Ind | TO-3 |
| | 3554SM, (Q) | 1700, A = 1000 | 1000 | 120 | ext. | 10 | 100 | 1 | 25 | 100 | MIL | TO-3 |
| | 3551J | 50, A = 10 | 250 | 400 | ext. | 10 | 10 | 1 | 50[3] | 88 | Com | TO-99 |
| | 3551S, (Q) | 50, A = 10 | 250 | 400 | ext. | 10 | 10 | 1 | 50[3] | 88 | MIL | TO-99 |
| | 3550J | 10, A = 10 | 65 | 400 | int. | 10 | 10 | 1 | 50[3] | 88 | Com | TO-99 |
| | 3550K | 20, A = 1 | 100 | 400 | int. | 10 | 10 | 1 | 50[3] | 88 | Com | TO-99 |
| | 3550S, (Q) | 10, A = 1 | 65 | 400 | int. | 10 | 10 | 1 | 50[3] | 88 | MIL | TO-99 |
| Bipolar | 3508J | 100, A = 100 | 0 | — | ext. | 10 | 10 | 5 | 30[3] | 98 | Com | TO-99 |
| | 3507J, (Q) | 20, A= 10 | 80 | 200 | ext. | 10 | 10 | 10 | 30[3] | 83 | Com | TO-99 |
| FET | OPA156AM | 6, A = 1 | 10 | 1.5μsec | int. | 10 | 5 | 2 | 5 | 94 | MIL | TO-99 |
| | OPA356AM | 6, A = 1 | 10 | 1.5μsec | int. | 10 | 5 | 2 | 5 | 94 | Com | TO-99 |
| Advance Information | **OPA602AM** | **6.5** | **20** | **600** | **int.** | **10** | **15** | **1** | **15** | **75** | **Ind.** | **TO-99** |
| | **OPA602BM** | **6.5** | **24** | **600** | **int.** | **10** | **15** | **0.5** | **5** | **88** | **Ind.** | **TO-99** |
| | **OPA602CM** | **6.5** | **28** | **600** | **int.** | **10** | **15** | **0.25** | **2** | **92** | **Ind.** | **TO-99** |
| | **OPA602SM** | **6.5** | **24** | **600** | **int.** | **10** | **15** | **0.5** | **5** | **88** | **MIL** | **TO-99** |
| | OPA605H | 200, A=1000 | 300[3] | 300 | ext. | 10 | 30 | 1 | 25 | 96[3] | Com | DIP |
| | OPA605A | 200, A=1000 | 300[3] | 300 | ext. | 10 | 30 | 1 | 25 | 96[3] | Ind | DIP |
| | OPA605K | 200, A=1000 | 300[3] | 300 | ext. | 10 | 30 | 0.5 | 5 | 96[3] | Com | DIP |
| | OPA605C | 200, A=1000 | 300[3] | 300 | ext. | 10 | 30 | 0.5 | 5 | 96[3] | Ind | DIP |
| | OPA606KM | 12.5 | 22 | 1μsec | int. | 11 | 5 | 1.5 | 5[3] | 95 | Com | TO-99 |
| | OPA606LM | 13 | 25 | 1μsec | int. | 12 | 5 | 0.5 | 5 | 100 | Com | TO-99 |
| | OPA606SM | 12.5 | 22 | 1μsec | int. | 11 | 5 | 1.5 | 5[3] | 95 | MIL | TO-99 |
| | OPA606KP | 12 | 20 | 1μsec | int. | 11 | 5 | 3 | 10[3] | 90 | Com | TO-99 |
| Quad FET | OPA404AG | 6.4 | 24 | 600 | int. | 11.5 | 5 | 1 | 3[3] | 88 | Ind | DIP |
| | OPA404BG | 6.4 | 28 | 600 | int. | 11.5 | 5 | 0.75 | 3[3] | 92 | Ind | DIP |
| | OPA404SG | 6.4 | 24 | 600 | int. | 11.5 | 5 | 1 | 3[3] | 88 | MIL | DIP |
| | **OPA404KP** | **6.4** | **24** | **600** | **int.** | **11.5** | **5** | **2.5** | **5[3]** | **88** | **Com** | **DIP** |
| Low Noise Bipolar | OPA27A* | 8, A = 1 | 1.7 | — | int.[4] | 12 | 16.6 | 0.025 | 0.6 | 120 | MIL | TO-99, DIP |
| | OPA37A* | 63, A = 5 | 11 | — | int.[4] | 12 | 16.6 | 0.025 | 0.6 | 120 | MIL | TO-99, DIP |
| | OPA27B | 8, A = 1 | 1.7 | — | int.[4] | 12 | 16.6 | 0.060 | 1.3 | 120 | MIL | TO-99, DIP |
| | OPA37B | 63, A = 5 | 11 | — | int.[4] | 12 | 16.6 | 0.060 | 1.3 | 120 | MIL | TO-99, DIP |
| | OPA27C | 8, A = 1 | 1.7 | — | int.[4] | 12 | 16.6 | 0.100 | 1.8 | 117 | MIL | TO-99, DIP |
| | OPA37C | 63, A = 5 | 11 | — | int.[4] | 12 | 16.6 | 0.100 | 1.8 | 117 | MIL | TO-99, DIP |
| | OPA27E | 8, A = 1 | 1.7 | — | int.[4] | 12 | 16.6 | 0.025 | 0.6 | 120 | Ind | TO-99, DIP |
| | OPA37E | 63, A = 5 | 11 | — | int.[4] | 12 | 16.6 | 0.025 | 0.6 | 120 | Ind | TO-99, DIP |
| | OPA27F | 8, A = 1 | 1.7 | — | int.[4] | 12 | 16.6 | 0.060 | 1.3 | 120 | Ind | TO-99, DIP |
| | OPA37F | 63, A = 5 | 11 | — | int.[4] | 12 | 16.6 | 0.060 | 1.3 | 120 | Ind | TO-99, DIP |
| | OPA27G | 8, A = 1 | 1.7 | — | int.[4] | 12 | 16.6 | 0.100 | 1.8 | 117 | Ind | TO-99, DIP |
| | OPA37G | 63, A = 5 | 11 | — | int.[4] | 12 | 16.6 | 0.100 | 1.8 | 117 | Ind | TO-99, DIP |
| Low Noise FET | OPA101AM | 20, A=100 | 5 | 2.5μsec | int. | 12 | 12 | 0.5 | 10 | 94 | Ind | TO-99 |
| | OPA101BM | 20, A=100 | 5 | 2.5μsec | int. | 12 | 12 | 0.25 | 5 | 94 | Ind | TO-99 |
| | OPA102AM | 40, A=100 | 10 | 1.5μsec | int. | 12 | 12 | 0.5 | 10 | 94 | Ind | TO-99 |
| | OPA102BM | 40, A=100 | 10 | 1.5μsec | int. | 12 | 12 | 0.25 | 5 | 94 | Ind | TO-99 |
| Fast Settling | OPA600UM | 6000, A=1000 | 500 | 80 | ext. | 9 | 180 | 5 | 100 | 86 | MIL | DIP |
| | OPA600VM | 6000, A=1000 | 500 | 80 | ext. | 9 | 180 | 4 | 20 | 86 | MIL | DIP |
| | OPA600BM | 5000, A = 1000 | 500 | 80 | ext. | 9 | 180 | ±5 | ±80 | 86 | Ind | DIP |
| | OPA600CM | 5000, A = 1000 | 500 | 80 | ext. | 9 | 180 | ±4 | ±40 | 86 | Ind | DIP |
| | OPA600SM | 5000, A = 1000 | 500 | 80 | ext. | 9 | 180 | ±5 | ±100 | 86 | MIL | DIP |
| | OPA600TM | 5000, A = 1000 | 500 | 80 | ext. | 9 | 180 | ±4 | ±80 | 86 | MIL | DIP |

* Indicates product is available in 20-pin ceramic leadless chip carriers.

(This table continued on next page.)

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# HIGH PERFORMANCE OPERATIONAL AMPLIFIERS (cont.)

## WIDE BANDWIDTH (≥5MHz) (cont.)

| Description | Model[1] | Frequency Response: Gain Bandwidth (MHz) | Frequency Response: Slew Rate, min (V/μsec) | $t_s$ ±0.1% (nsec) | Compensation | Rated Output, min (±V) | Rated Output, min (±mA) | Offset Voltage, max: At 25°C (±mV) | Offset Voltage, max: Temp Drift (±μV/°C) | Open Loop Gain, min (dB) | Temp Range[2] | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unity-Gain Buffer | 3553AM, (Q) | 32 | 2000 | — | — | 10 | 200 | 50 | 300[3] | NA | Ind | TO-3 |
| Low Cost | OPA27GP | 8, A = 1 | 1.9[3] | — | int. | 12 | 16.6 | 0.100 | 1.8 | 117 | Com | DIP |
| | OPA37GP | 63, A = 5 | 11.9[3] | — | int.[4] | 12 | 16.6 | 0.100 | 1.8 | 117 | Com | DIP |
| Wide Temp Range | OPA27HT | 6, A = 1 | 1.9 | — | int. | 12 | 16.6[3] | 0.050 | 0.25[3] | 120 | −55°C to +200°C | TO-99 |
| | OPA37HT | 36, A = 5 | 11.9 | — | int.[4] | 12 | 16.6[3] | 0.050 | 0.25[3] | 120 | | TO-99 |
| | OPA11HT | 12, A=1 | 4 | 1.5μsec | ext. | 10 | 15 | 5[3] | 5 | 98 | −55°C to +200°C | TO-99 |

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Typical. (4) G = 5 min for OPA37.

## HIGH VOLTAGE—HIGH CURRENT

| Description | Model[1] | Rated Output, min (±V) | Rated Output, min (±mA) | Offset Voltage, max: At 25°C, (±mV) | Offset Voltage, max: Temp Drift, (±μV/°C) | Bias Current (25°C), max (pA) | Frequency Response: Unity Gain (MHz) | Frequency Response: Slew Rate (V/μsec) | Open Loop Gain (dB) | Temp Range[2] | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| High Power | OPA501AM | 20 | 10A | 10 | 65 | 40nA | 1 | 1.35 | 94 | Ind | TO-3 |
| | OPA501BM | 26 | 10A | 5 | 40 | 20nA | 1 | 1.35 | 98 | Ind | TO-3 |
| | OPA501RM | 20 | 10A | 10 | 65 | 40nA | 1 | 1.35 | 94 | MIL | TO-3 |
| | OPA501SM | 26 | 10A | 5 | 40 | 20nA | 1 | 1.35 | 98 | MIL | TO-3 |
| | OPA511AM | 22 | 5A | 10 | 65 | 40 | 1 | 1 | 91 | Ind | TO-3 |
| | OPA512BM | 35 | 10A | 6 | 65 | 30 | 4 | 2.5 | 110 | Ind | TO-3 |
| | OPA512SM | 35 | 15A | 3 | 40 | 20 | 4 | 2.5 | 110 | MIL | TO-3 |
| | **OPA541AM** | **30** | **5A** | **10** | **40** | **50** | **1.6** | **8** | **90** | **Ind.** | **TO-3** |
| | **OPA541BM** | **35** | **5A** | **1** | **30** | **50** | **1.6** | **8** | **90** | **Ind.** | **TO-3** |
| | **OPA541SM** | **35** | **5A** | **1** | **30** | **50** | **1.6** | **8** | **90** | **MIL** | **TO-3** |
| | 3573AM | 20 | 2A[5] | 10 | 65 | 40nA | 1 | 2.6 | 94 | Ind | TO-3 |
| | 3572AM | 30 | 2A[5] | 2 | 40 | −100 | 0.5 | 3 | 94 | Ind | TO-3 |
| | 3571AM, (Q) | 30 | 1A[4] | 2 | 40 | −100 | 0.5 | 3 | 94 | Ind | TO-3 |
| Wideband | 3554AM, (Q) | 10 | 100 | 2 | 50 | −50 | 1700[3] | 1200 | 100 | Ind | TO-3 |
| | 3554BM, (Q) | 10 | 100 | 1 | 15 | −50 | 1700[3] | 1200 | 100 | Ind | TO-3 |
| | 3554SM, (Q) | 10 | 100 | 1 | 25 | −50 | 1700[3] | 1200 | 100 | MIL | TO-3 |
| High Voltage | 3584JM, (Q) | 145 | 15 | 3 | 25 | −20 | 20[3] | 150 | 126 | Com | TO-3 |
| | 3583AM | 140 | 75 | 3 | 25 | −20 | 5 | 30 | 118 | Ind | TO-3 |
| | 3583JM | 140 | 75 | 3 | 25 | −20 | 5 | 30 | 118 | Com | TO-3 |
| | 3582J | 145 | 15 | 3 | 25 | −20 | 5 | 20 | 118 | Com | TO-3 |
| | 3581J | 70 | 30 | 3 | 25 | −20 | 5 | 20 | 112 | Com | TO-3 |
| | 3580J | 30 | 60 | 10 | 30 | −50 | 5 | 15 | 106 | Com | TO-3 |
| Advance Information | **OPA445BM** | **35** | **15** | **3** | **10** | **50** | **2** | **10** | **100** | **Ind** | **TO-99** |
| | **OPA445SM** | **35** | **15** | **1** | **10** | **50** | **2** | **10** | **100** | **MIL** | **TO-99** |
| Booster | 3553AM, (Q) | 10 | 200 | 50 | 300[6] | −200 | 300 | 2000 | NA | Ind | TO-3 |
| | **OPA633AH** | **10** | **80** | **15** | **33[6]** | **35μA** | **275[6]** | **1000** | **NA** | **Ind** | **TO-8** |
| | **OPA633SH** | **10** | **80** | **15** | **33[6]** | **35μA** | **275[6]** | **1000** | **NA** | **MIL** | **TO-8** |
| | **OPA633KP** | **10** | **80** | **15** | **33[6]** | **35μA** | **275[6]** | **1000** | **NA** | **Com** | **DIP** |

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) 2A peak. (5) 5A peak. (6) Typical.

**For additional details. refer to the Burr-Brown *Product Data Book* and *Supplement*, or contact your nearest Burr-Brown sales office.**

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# INSTRUMENTATION AMPLIFIERS AND PROGRAMMABLE GAIN AMPLIFIERS

## INSTRUMENTATION AMPLIFIERS

| Description | Model | Gain Range | Gain Accuracy, G = 100, 25°C, max (%) | Gain Drift, G = 100 (ppm/°C) | Non-Linearity, G = 100, max (%) | Input Parameters: CMR, DC to 60Hz, G = 10, 1kΩ Unbal., min (dB) | Input Parameters: Offset Voltage vs Temp, max (μV/°C) | Dynamic Response, G = 100, ±3dB BW (kHz) | Temp Range [1] | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| Very-High Accuracy | INA104HP | 1-1000[2] | 0.15 | 22 | ±0.007 | 96 | ±(2 ± 20/G) | 25 | Com | DIP |
| | INA104JP | 1-1000[2] | 0.15 | 22 | ±0.003 | 96 | ±(0.25 ± 10/G) | 25 | Com | DIP |
| | INA104KP | 1-1000[2] | 0.15 | 22 | ±0.003 | 96 | ±(0.75 ± 10/G) | 25 | Com | DIP |
| | INA104AM | 1-1000[2] | 0.15 | 22[3] | ±0.007 | 96 | ±(2 ± 20/G) | 25 | Ind | DIP |
| | INA104BM | 1-1000[2] | 0.15 | 22[3] | ±0.003 | 96 | ±(0.75 ± 10/G) | 25 | Ind | DIP |
| | INA104CM | 1-1000[2] | 0.15 | 22[3] | ±0.003 | 96 | ±(0.25 ± 10/G) | 25 | Ind | DIP |
| | INA104SM | 1-1000[2] | 0.15 | 22[3] | ±0.003 | 96 | ±(0.75 ± 10/G) | 25 | MIL | DIP |
| | INA101AM* | 1-1000[2] | 0.03 | 22[4] | ±0.007 | 96 | ±(2 + 20/G) | 25 | Ind | TO-100 |
| | INA101CM | 1-1000[2] | 0.03 | 22[4] | ±0.004 | 96 | ±(0.25 + 10/G) | 25 | Ind | TO-100 |
| | INA101SM | 1-1000[2] | 0.03 | 22[4] | ±0.004 | 96 | ±(0.25 + 10/G) | 25 | MIL | TO-100 |
| | INA101AG | 1-1000[2] | 0.03 | 22[3] | ±0.007 | 96 | ±(2 + 20/G) | 25 | Ind | DIP |
| | INA101CG | 1-1000[2] | 0.03 | 22[3] | ±0.003 | 96 | ±(0.25 + 10/G) | 25 | Ind | DIP |
| | INA101SG | 1-1000[2] | 0.03 | 22[3] | ±0.003 | 96 | ±(0.25 + 10/G) | 25 | MIL | DIP |
| | INA101HP | 1-1000[2] | 0.3 | 22[3] | ±0.007 | 90 | ±(2 + 20/G) typ | 25 | Com | DIP |
| | **INA101KU** | **1-1000[2]** | **0.3** | **22[3]** | **±0.007** | **90** | **±(2 + 20/G) typ** | **25** | **Com** | **SOIC** |
| Low Quiescent Power | INA102AG* | 1, 10, 100, 1000 | 0.25 | 20 | ±0.05 | 80 | ±(5 + 10/G) | 3 | Ind | DIP |
| | INA102CG | | 0.15 | 15 | ±0.02 | 90 | ±(2 + 5/G) | 3 | Ind | DIP |
| Fast Settling FET Input | INA110AG* | 1, 10, 100, 200, 500 | 0.2 | 40 | ±0.02 | 87 | ±(5 + 100/G) | 470 | Ind | DIP |
| | INA110BG | | 0.1 | 20 | ±0.01 | 96 | ±(2 + 50/G) | 470 | Ind | DIP |
| | **INA110SG** | **1, 10, 100** | **0.1** | **20** | **0.01** | **96** | **±(2 + 50/G)** | **470** | **MIL** | **DIP** |
| | **INA110KP** | **200,** | **0.2** | **6 typ** | **0.02** | **87** | **±(2 + 20/G) typ** | **470** | **Com** | **DIP** |
| | **INA110KU** | **500** | **0.2** | **6 typ** | **0.02** | **87** | **±(2 + 20/G) typ** | **470** | **Com** | **SOIC** |
| Buffer, Unity-Gain Differential | 3627AM | 1V/V, fixed | 0.01 | 5 | ±0.001[3] | 90 | 30 | 800[3] | Ind | TO-99 |
| | 3627BM | 1V/V, fixed | 0.01 | 5 | ±0.001[3] | 100 | 20 | 800[3] | Ind | TO-99 |
| | INA105AM* | 1V/V, fixed | 0.01 | 5 | ±0.001[3] | 80[6] | 20 | 1000[3] | Ind | TO-99 |
| | INA105BM | 1V/V, fixed | 0.01 | 5 | ±0.001[3] | 86[6] | 10 | 1000[3] | Ind | TO-99 |
| | INA105KP | 1V/V, fixed | 0.025 | 5 | ±0.001[3] | 72[6] | 5 typ | 1000[3] | Com | DIP |
| | **INA105KU** | **1V/V, fixed** | **0.025** | **5** | **±0.001[3]** | **72[6]** | **5** | **1000[3]** | **Com** | **SOIC** |
| Gain of 10 Differential | **INA106AM** | **10V/V fixed** | **0.01** | **10** | **0.001** | **94[6]** | **5** | **500[5]** | **Ind** | **DIP** |
| | **INA106BM** | **10V/V fixed** | **0.01** | **10** | **0.001** | **100[6]** | **2** | **500[5]** | **Ind** | **DIP** |
| | **INA106KP** | **10V/V fixed** | **0.025** | **4 typ** | **0.001** | **86[6]** | **0.2 typ** | **500[5]** | **Com** | **DIP** |
| High Common Mode Voltage Differential (200VDC CMV) | **INA117AG** | **1V/V fixed** | **0.05[3]** | **10[3]** | **0.001[3]** | **74[3,6]** | **40** | **200[3]** | **Ind** | **TO-99** |
| | **INA117BG** | **1V/V fixed** | **0.02[3]** | **10[3]** | **0.001[3]** | **86[3,6]** | **20** | **200[3]** | **Ind** | **TO-99** |
| | **INA117P** | **1V/V fixed** | **0.05[3]** | **10[3]** | **0.001[3]** | **74[3,6]** | **40** | **200[3]** | **Com** | **DIP** |

## PROGRAMMABLE GAIN AMPLIFIERS

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Noninverting Multiplexed Input | PGA100AG | Gain set with 4-bit word 1, 2, 4, 8 . . . 128 | 0.05 | 10 | ±0.01 | NA | 6 typ | 5MHz | Ind | DIP |
| | PGA100BG | | 0.02 | 10 | ±0.005 | NA | 6 typ | 5MHz | Ind | DIP |
| | PGA102AG | Gain set with 2-bit word 1, 10 100 | 0.02 | 20 | 0.01 | — | 3, G = 100 | 250 | Ind | DIP |
| | PGA102BG | | 0.01 | 20 | 0.01 | — | 3, G = 100 | 250 | Ind | DIP |
| | PGA102SG | | 0.01 | 20 | 0.01 | — | 3, G = 100 | 250 | Ind | DIP |
| | PGA102KP | | 0.02 | 50 | 0.01 | — | 3, G = 100 | 250 | Com | DIP |
| Instrumentation Amplifier Input | PGA200AG | Gain set with 2-bit word 1, 10, 100, 1000 | 0.05 | 20 | ±0.007 | 96 | 2, G = 100 | 30 | Ind | DIP |
| | PGA200BG | | 0.02 | 10 | ±0.003 | 96 | 0.4, G = 100 | 30 | Ind | DIP |
| Differential Input | 3606AG | Gain set with 3-bit word 1, 2, 4 8 . . . 1024 | 0.05 | 10 | 0.004 | 90, G = 1 | ±(3 + 50/G) | 40 | Ind | DIP |
| | 3606AM | | 0.05 | 10 | 0.004 | 90, G = 1 | ±(3 + 50/G) | 40 | Ind | DIP |
| | 3606BG | | 0.02 | 10 | 0.004 | 90, G = 1 | ±(1 + 20/G) | 40 | Ind | DIP |
| | 3606BM | | 0.02 | 10 | 0.004 | 90, G = 1 | ±(1 + 20/G) | 40 | Ind | DIP |

* Indicates product is available in 20-pin ceramic leadless chip carriers.

NOTES: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (2) Set with external resistor. (3) Unity-gain. (4) With zero TC external resistor. (5) Gain = 10. (6) No source imbalance.

**For additional details, refer to the Burr-Brown *Product Data Book* and *Supplement*, or contact your nearest Burr-Brown sales office.**



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# INSTRUMENTATION AMPLIFIERS AND PROGRAMMABLE GAIN AMPLIFIERS (cont.)

## PRECISION TRANSMITTERS

| Description | Model | Span: Untrimmed Error, max (%) | Span: Non-Linearity, max (%) | Span: Temp Drift[1] (ppm/°C) | Input Parameters: Offset Voltage, max (μV) | Input Parameters: Offset Voltage vs Temp, max (μV/°C) | Input Parameters: CMR, DC, min (dB) | Output Parameters: Current Range (mA) | Output Parameters: Offset Current Error, max (μA) | Output Parameters: FS Output Current Error, max (μA) | Temp Range [2] | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Two-Wire | XTR100AM | −3 | 0.01 | ±100 | ±50 | ±1 | 90 | 4–20 | ±4 | ±20 | Ind | DIP |
| | XTR100AP | −3 | 0.01 | ±100 | ±50 | ±1 | 90 | 4–20 | ±4 | ±20 | Ind | DIP |
| | XTR100BM | −3 | 0.01 | ±100 | ±25 | ±0.5 | 90 | 4–20 | ±4 | ±20 | Ind | DIP |
| | XTR100BP | −3 | 0.01 | ±100 | ±25 | ±0.5 | 90 | 4–20 | ±4 | ±20 | Ind | DIP |
| | XTR101AG* | −5 | 0.01 | ±100 | ±60 | ±1.5 | 90 | 4–20 | ±10 | ±40 | Ind | DIP |
| | XTR101BG | −5 | 0.01 | ±100 | ±30 | ±0.75 | 90 | 4–20 | ±6 | ±30 | Ind | DIP |
| | **XTR101AP** | **−5** | **0.01** | **±100** | **±100** | **±1.5** | **90** | **4–20** | **±19** | **±60** | **Ind[3]** | **DIP** |
| | **XTR101AU** | **−5** | **0.01** | **±100** | **±100** | **±1.5** | **90** | **4–20** | **±19** | **±60** | **Ind[3]** | **SOIC** |
| Three-Wire and Current Source | XTR110AG* | 0.6 | 0.025 | 50 | — | — | — | 4–20, 0–20, 5–25 [4] | ±64 | ±96 | Ind | DIP |
| | XTR110BG | 0.2 | 0.005 | 30 | — | — | — | | ±16 | ±32 | Ind | DIP |
| | XTR110KP | 0.6 | 0.025 | 50 | — | — | — | | ±64 | ±96 | Com | DIP |
| | **XTR110KU** | **0.6** | **0.025** | **50** | — | — | — | | **±64** | **±96** | **Com** | **SOIC** |

* Indicates product is available in 20-pin ceramic leadless chip carriers.

NOTES: (1) With zero TC span resistor. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) −40°C to +85°C. (4) Many more ranges with appropriate circuit.

# ISOLATION PRODUCTS

## TRANSFORMER COUPLED AMPLIFIERS

| Description | Model | Isolation Voltage (V): Continuous, peak | Isolation Voltage (V): Pulse/Test, peak | Isolation Mode Rejection, typ.: DC (dB) | Isolation Mode Rejection, typ.: 60Hz (dB) | Leakage Current at Test Voltage (μA) | Isolation Impedance: (Ω) | Isolation Impedance: (pF) | Gain Nonlinearity: max (%) | Gain Nonlinearity: typ. (%) | Voltage Drift, (±μV/°C) max | Bias Current, max | ±3dB Freq. (kHz) | External Isolation Power Required | Temp. Range [1] | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Low Drift[2] | 3450 | ±500 | ±2000 | 160 | 120 | 1 | $10^{12}$ | 16 | ±0.005 | ±0.0015 | 100 | 50nA | 1.5 | No | Com | Module |
| Low Bias FET | 3451 | ±500 | ±2000 | 160 | 120 | 1 | $10^{12}$ | 16 | ±0.025 | ±0.005 | 100 | 25pA | 2.5 | No | Com | Module |
| | 3452 | ±2000 | ±5000 | 160 | 120 | 1 | $10^{12}$ | 16 | ±0.025 | ±0.005 | 100 | 10pA | 2.5 | No[4] | Com | Module |
| | 3455 | [3] | [3] | 160 | 120 | [3] | $10^{12}$ | 16 | ±0.025 | ±0.005 | 100 | 20pA | 2.5 | No[4] | Com | Module |
| Highest Isolation Voltage | 3656AG | ±3500 | ±8000 | 160 | 125 | 0.5 | $10^{12}$ | 6 | ±0.1 | ±0.03 | 25 + (500/$G_1$) | 100nA | 30 | No | Ind | DIP |
| | 3656BG | ±3500 | ±8000 | 160 | 125 | 0.5 | $10^{12}$ | 6 | ±0.05 | ±0.03 | 5 + (1000/$G_1$) | 100nA | 30 | No | Ind | DIP |
| | 3656HG | ±3500 | ±8000 | 160 | 125 | 0.5 | $10^{12}$ | 6 | ±0.15 | ±0.03 | 200 + (1000/$G_1$) | 100nA | 30 | No | Com | DIP |
| | 3656JG | ±3500 | ±8000 | 160 | 125 | 0.5 | $10^{12}$ | 6 | ±0.1 | ±0.03 | 50 + (750/$G_1$) | 100nA | 30 | No | Com | DIP |
| | 3656KG | ±3500 | ±8000 | 160 | 125 | 0.5 | $10^{12}$ | 6 | ±0.1 | ±0.03 | 10 + (350/$G_1$) | 100nA | 30 | No | Com | DIP |

## OPTICALLY COUPLED AMPLIFIERS

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Balanced Current Input | 3650HG | ±2000 | ±5000 | 140 | 120 | 0.25[5] | $10^{12}$ | 1.8 | ±0.2 | ±0.05 | 25 | 10nA | 15 | Yes[6] | Ind | DIP |
| | 3650JG | ±2000 | ±5000 | 140 | 120 | 0.25[5] | $10^{12}$ | 1.8 | ±0.1 | ±0.03 | 10 | 10nA | 15 | Yes[6] | Ind | DIP |
| | 3650KG | ±2000 | ±5000 | 140 | 120 | 0.25[5] | $10^{12}$ | 1.8 | ±0.05 | ±0.02 | 5 | 10nA | 15 | Yes[6] | Ind | DIP |
| | 3650MG | ±2000 | ±5000 | 140 | 120 | 0.25[5] | $10^{12}$ | 1.8 | ±0.2 | ±0.05 | 100 | 10nA | 15 | Yes[6] | Ind | DIP |
| Balanced FET Input | 3652HG | ±2000 | ±5000 | 140 | 120 | 0.25[5] | $10^{12}$ | 1.8 | ±0.2 | ±0.05 | 50 | 50nA | 15 | Yes | Ind | DIP |
| | 3652JG | ±2000 | ±5000 | 140 | 120 | 0.25[5] | $10^{12}$ | 1.8 | ±0.1 | ±0.05 | 25 | 50nA | 15 | Yes | Ind | DIP |
| | 3652MG | ±2000 | ±5000 | 140 | 120 | 0.25[5] | $10^{12}$ | 1.8 | ±0.2 | ±0.05 | 100 | 50nA | 15 | Yes | Ind | DIP |
| Low Drift Wide Bandwidth | ISO100AP | 750 | 2500 | 146[6] | 108[6] | 0.3 | $10^{12}$ | 2.5 | 0.4 | 0.1 | 10[6] | 10nA | 60 | Yes | Ind | DIP |
| | ISO100BP | 750 | 2500 | 146[6] | 108[6] | 0.3 | $10^{12}$ | 0.1 | 0.01 | 4[6] | 10nA | 60 | Yes | Ind | DIP | |
| | ISO100CP | 750 | 2500 | 146[6] | 108[6] | 0.3 | $10^{12}$ | 2.5 | 0.07 | 0.02 | 4[6] | 10nA | 60 | Yes | Ind | DIP |

## CAPACITOR COUPLED, HERMETICALLY SEALED AMPLIFIERS

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **1500VAC Isolation** | **ISO102** | **±2121** | **±4000** | **160** | **120** | **1.0** | **$10^{14}$** | **6** | **0.075** | **0.04** | **±500** | **100μA** | **70** | **Yes** | **Ind** | **DIP** |
| | **ISO102B** | **±2121** | **±4000** | **160** | **120** | **1.0** | **$10^{14}$** | **6** | **0.025** | **0.02** | **±250** | **100μA** | **70** | **Yes** | **Ind** | **DIP** |
| **3500VAC Isolation** | **ISO106** | **±4950** | **±8000** | **160** | **130** | **1.0** | **$10^{14}$** | **6** | **0.075** | **0.04** | **±500** | **100μA** | **70** | **Yes** | **Ind** | **DIP** |
| | **ISO106B** | **±4950** | **±8000** | **160** | **130** | **1.0** | **$10^{14}$** | **6** | **0.025** | **0.02** | **±250** | **100μA** | **70** | **Yes** | **Ind** | **DIP** |

NOTES: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C. (2) Bipolar. (3) Isolation voltage tested at 2500Vrms, 60Hz; leakage current tested for 2μA max at 240Vrms, 60Hz. (4) ±15V at ±15mA isolated power available to power external circuitry. (5) At 240V/60Hz. (6) $R_{IN}$ = 10k, Gain = 100.

**For additional details, refer to the Burr-Brown *Product Data Book* and *Supplement*, or contact your nearest Burr-Brown sales office.**





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# ISOLATION PRODUCTS (cont.)

| ISOLATION POWER SUPPLIES[1] | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Isolation Voltage (V) | | Input Voltage (VDC) | | Leakage Current, 240VAC, 60Hz | Isolation Impedance | | Rated Current, Balanced Loads On All | Max Current,[1] Balanced Loads On All | Sensitivity To Input Voltage | Temp | |
| Description | Model | Continuous Peak | Pulse/ Test Peak | Min | Max | (μA) | (Ω) | (pF) | Outputs (mA) | Outputs (mA) | Change (V/V) | Range [2] | Package |
| Single ±15V Output | 700 | 1500 | 4200 | 10 | 18 | 1 | $10^{10}$ | 5 | ±3-30 | ±60 | 1.08 | Ind | Module |
| | 700U | 2000 | 5000 | 10 | 18 | 1 | $10^{10}$ | 3 | ±3-30 | ±60 | 1.08 | Ind | Module |
| | **725** | **2121** | **4000** | **7** | **18** | **1.2** | $\mathbf{10^{12}}$ | **9** | **±15** | **±40** | **1.15** | **Ind** | **DIP** |
| | **726** | **4950** | **8000** | **7** | **18** | **1.2** | $\mathbf{10^{12}}$ | **9** | **±15** | **±40** | **1.15** | **Ind** | **DIP** |
| Dual ±15V Output | 722 | 4950 | 8000 | 5 | 16 | 1 | $10^{10}$ | 6 | ±3-40 | ±50 | 1.13 | Ind | Module |
| Quad ±15V Output | 710 | 1000 | 3100 | 10 | 18 | 1 | $10^{10}$ | 8 | ±9.5 | ±60 | 1.08 | Ind | Module |
| Quad ±8V Output | 724 | 1000 | 3000 | 5 | 16 | 1 | $10^{10}$ | 6 | ±3-16 | ±60 | 0.63 | Ind | Module |

NOTE: (1) See complete data sheet for full specifications, especially regarding output current capabilities. (2) Ind = −25°C to +85°C.

# ANALOG CIRCUIT FUNCTIONS

| MULTIPLIERS/DIVIDERS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Model | Transfer Function | Error at +25°C, max (%) | Temperature Coefficient (%/°C) | Feed-through (mV) | Offset Voltage (mV) | 1% Bandwidth (kHz) | Temp Range [1] | Package |
| MPY100A* | $[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$ | ±2 | 0.017 | 100 | 50 | 70 | Ind | TO-100 |
| MPY100B | ǂ | ±1 | 0.008 | 30 | 10 | 70 | Ind | TO-100 |
| MPY100C | ǂ | ±0.5 | 0.008 | 30 | 7 | 70 | Ind | TO-100 |
| MPY100S | ǂ | ±0.5 | 0.025 | 30 | 7 | 70 | MIL | TO-100 |
| MPY534JH* | ǂ | ±1.0 | 0.022 | 0.3% | 5 | 3MHz | Com | TO-100 |
| MPY534JD | ǂ | ±1.0 | 0.022 | 0.3% | 5 | 3MHz | Com | DIP |
| MPY534KH | ǂ | ±0.5 | 0.015 | 0.15 | 2 | 3MHz | Com | TO-100 |
| MPY534KD | ǂ | ±0.5 | 0.015 | 0.15% | 2 | 3MHz | Com | DIP |
| MPY534LH | ǂ | ±0.25 | 0.008 | 0.05% | 2 | 3MHz | Com | TO-100 |
| MPY534LD | ǂ | ±0.25 | 0.008 | 0.05% | 2 | 3MHz | Com | DIP |
| MPY534SH | ǂ | ±1.0 | 0.02 | 0.3% | 5 | 3MHz | MIL | TO-100 |
| MPY534SD | ǂ | ±1.0 | 0.02 | 0.3% | 5 | 3MHz | MIL | DIP |
| MPY534TH | ǂ | ±0.5 | 0.01 | 0.15% | 2 | 3MHz | MIL | TO-100 |
| MPY534TD | ǂ | ±0.5 | 0.01 | 0.15% | 2 | 3MHz | MIL | DIP |
| MPY634AM* | ǂ | ±1.0 | 0.022 | 0.3% | 5 | 10MHz | Ind | TO-100 |
| MPY634BM | ǂ | ±0.5 | 0.015 | 0.15% | 2 | 10MHz | Ind | TO-100 |
| MPY634SM | ǂ | ±1.0 | 0.02 | 0.3% | 5 | 10MHz | MIL | TO-100 |
| MPY634KP | ǂ | ±2.0 | 0.03 | 0.3% | 25 | 10MHz | Ind | DIP |
| **MPY634KU** | ǂ | **±2.0** | **0.03** | **0.3%** | **25** | **10MHz** | **Com** | **SOIC** |
| **AD632A** | ǂ | 1 | 0.02 | 0.3 | 30 | 50 | Ind | |
| **AD632B** | ǂ | 0.5 | 0.01 | 0.15 | 15 | 50 | Ind | TO-100, |
| **AD632S** | ǂ | 1 | 0.02 | 0.3 | 30 | 50 | MIL | DIP |
| **AD632T** | ǂ | 0.5 | 0.01 | 0.15 | 15 | 50 | MIL | |

* Indicates product is available in 20-pin ceramic leadless chip carriers. ǂ Same as model above.
NOTE: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C.



**For additional details, refer to the Burr-Brown *Product Data Book* and *Supplement*, or contact your nearest Burr-Brown sales office.**

# ANALOG CIRCUIT FUNCTIONS (cont.)

| SPECIAL FUNCTIONS | | | | | |
|---|---|---|---|---|---|
| Function | Model | Description | Comments | Temp Range[1] | Package |
| Multifunction Converter | 4302 | $Y\ (Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions. | Plastic package. | Ind | DIP |
| | LOG100JP | K Log ($I_1/I_2$) | Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity. | Com | DIP |
| Logarithmic Amplifier | 4127JG<br>4127KP | K Log ($I_1/I_{REF}$) | A more versatile part which contains an internal reference and a current inverter. 1% and 0.5% accuracy. | Com<br>Com | DIP<br>DIP |
| $\sqrt{\frac{1}{T}\int_o^T E_{IN}^2\,(t)\,dt}$ | 4341 | True rms-to-DC conversion based on a log-antilog occupational approach. | Some external trimming required. Lower cost in plastic package. Pin compatible with 4340. | Ind | DIP |
| Peak Detector | 4085BM<br>4085KG<br>4085SM | These are analog memory circuits which hold and provide read-out of a DC voltage equal to peak value of a complex input waveform. | Digital mode control provides reset capability and allows selection of peaks within a desired time interval. May be used to make peak-to-peak detector. | Com<br>Ind<br>MIL | DIP<br>DIP<br>DIP |

NOTE: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C.

| DIVIDERS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Model | Transfer Function | Input Range | Accuracy, max D = 250mV (%) | Temperature Coefficient (%/°C) | 0.5% Bandwidth (kHz) | Rated Output, min | Temp Range[1] | Package |
| DIV100HP | N/D 10 | 250mV | 1.0 | 0.2 | 15 | ±10V, ±5mA | Ind | DIP |
| DIV100JP | N/D 10 | to | 0.5 | 0.2 | 15 | ±10V, ±5mA | Ind | DIP |
| DIV100KP | N/D 10 | 10V | 0.25 | 0.2 | 15 | ±10V, ±5mA | Ind | DIP |

NOTE: (1) Ind = −25°C to +85°C.

| FREQUENCY PRODUCTS | | | | | |
|---|---|---|---|---|---|
| Function | Model | Description | Comments | Temp Range[1] | Package |
| Oscillator | 4423 | Very-low cost in plastic package. Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available). | Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%. | Com | DIP |
| Universal Active Filter | UAF41<br>UAF21 | These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass and bandpass outputs are available. | Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses. | Ind<br>Ind | DIP<br>DIP |

NOTE: (1) Com = 0 to +70°C, Ind = −25°C to +85°C.

| VOLTAGE REFERENCE | | | | | | | |
|---|---|---|---|---|---|---|---|
| Model | Output (V) | Minimum Output (mA) | Maximum Drift (ppm/°C) | Power Supply (V) | Power Supply (mA) | Temp Range[1] | Package |
| REF10KM* | +10.00 ±0.005 | 10 | 1 | +13.5/35 | 4.5 | Com | TO-99 |
| REF10JM* | +10.00 ±0.005 | 10 | 2 | +13.5/35 | 4.5 | Com | TO-99 |
| REF10SM* | +10.00 ±0.005 | 10 | 3 | +13.5/35 | 4.5 | MIL | TO-99 |
| REF10RM* | +10.00 ±0.005 | 10 | 6 | +13.5/35 | 4.5 | MIL | TO-99 |
| REF101KM* | +10.00 ±0.005 | 10 | 1 | +13.5/35 | 4.5 | Com | TO-99 |
| REF101JM* | +10.00 ±0.005 | 10 | 2 | +13.5/35 | 4.5 | Com | TO-99 |
| REF101SM* | +10.00 ±0.005 | 10 | 3 | +13.5/35 | 4.5 | MIL | TO-99 |
| REF101RM* | +10.00 ±0.005 | 10 | 6 | +13.5/35 | 4.5 | MIL | TO-99 |

* Indicates product is available in 20-pin ceramic leadless chip carriers.
NOTE: (1) Com = 0 to +70°C, MIL = −55 to +125°C.

**For additional details, refer to the Burr-Brown *Product Data Book* and *Supplement*, or contact your nearest Burr-Brown sales office.**




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# DATA CONVERSION AND DATA ACQUISITION

## ANALOG-TO-DIGITAL CONVERTERS

| Description | Model | Q[1] Screen | Resolution (Bits) | Linearity Error (% FSR) | Conversion Time (μs) | Gain Tempco (ppm/°C) | Temp Range[2] | Input Range[3] (V) | Package |
|---|---|---|---|---|---|---|---|---|---|
| Very High Speed | ADC803 | Q | 12 | ±0.012 | 1.5 | 30 | MIL, Ind | 10, 20, U/B | Hermetic Metal DIP |
| Ultra High Speed | **ADC600** | | **12** | **±0.015** | **0.1** | **30** | **Com** | **1.25 B** | **Module** |
| Serial Out | ADC804 | Q | 12 | ±0.012 | 17 | 30 | MIL, Com, Ind | 5, 10, 20 U/B | Hermetic Ceramic DIP |
| Low Cost, Microprocessor Interface | ADC574<br>ADC674 | Q<br>Q | 12<br>12 | ±0.012<br>±0.012 | 25<br>15 | 25<br>25 | MIL, Com, Ind | 10, 20 U/B<br>10, 20 U/B | Hermetic Ceramic DIP<br>Hermetic Ceramic DIP |
| Low Cost | ADC80AG<br>**ADC80MAH** | Q<br>**QM** | 12<br>**12** | ±0.012<br>**±0.012** | 25<br>**25** | 30<br>**30** | Ind<br>**Ind** | 5, 10, 20 U/B<br>**5, 10, 20 U/B** | Hermetic Ceramic DIP<br>**Hermetic Ceramic DIP** |
| High Temp | ADC10HT | | 12 | ±0.012 | 50 | 35 | −55°C to +200°C | 10, 20, U/B | Hermetic Ceramic DIP |
| High Speed, Low Cost | **ADC84** | **Q** | **12** | **±0.012** | **10** | **30** | **Com** | **5, 10, 20 U/B** | **Hermetic Ceramic DIP** |
| High Speed, Wide Temp | **ADC85H**<br>**ADC87H** | **Q**<br>**Q** | **12**<br>**12** | **±0.012**<br>**±0.012** | **10**<br>**10** | **30**<br>**30** | **Ind**<br>**MIL** | **5, 10, 20 U/B**<br>**5, 10, 20 U/B** | **Hermetic Ceramic DIP**<br>**Hermetic Ceramic DIP** |
| High Resolution | ADC71<br>ADC72<br>ADC76 | Q<br>Q<br>Q | 16<br>16<br>16 | ±0.003<br>±0.003<br>±0.003 | 50<br>50<br>17 | 15<br>15<br>15 | Ind, Com<br>Ind, Com<br>Ind, Com | 5, 10, 20 U/B<br>5, 10, 20 U/B<br>5, 10, 20 U/B | Ceramic DIP<br>Hermetic Metal DIP<br>Ceramic DIP |
| Audio | PCM75 | | 16 | 0.006% THD | 17 | 20 | Com | 5, 10, 20 U/B | Ceramic DIP |

NOTES: (1) "Q" or "QM" indicates product available with screening for enhanced reliability. (2) Com = 0°C to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) U = Unipolar, B = Bipolar.

## DIGITAL-TO-ANALOG CONVERTERS

| Description | Model | Q[1] Screen | Resolution (Bits) | Linearity Error (% FSR) | Settling Time (μs) | Gain Tempco (ppm/°C) | Temp Range[2] | Output Range[3] | Package |
|---|---|---|---|---|---|---|---|---|---|
| Very High Resolution | **DAC729** | **Q** | **18** | **±0.00075** | **5** | **15** | **Com** | **10V, 20V U/B** | **Hermetic Ceramic DIP** |
| High Resolution | DAC700<br>DAC701<br>DAC702<br>DAC703 | QM<br>QM<br>QM<br>QM | 16<br>16<br>16<br>16 | ±0.0015<br>±0.0015<br>±0.0015<br>±0.0015 | 1<br>8<br>1<br>8 | 10<br>10<br>10<br>10 | MIL, Com, Ind<br>MIL, Com, Ind<br>MIL, Com, Ind<br>MIL, Com, Ind | −1mA<br>10V, 20V U/B<br>±1mA<br>10V, 20V U/B | Hermetic Ceramic DIP, Plastic DIP, LCC, Die |
| Bus Interface, High Resolution | DAC705<br>DAC706 | QM<br>QM | 16<br>16 | ±0.003<br>±0.003 | 8<br>1 | 15<br>15 | MIL, Com, Ind<br>MIL, Com, Ind | 10V, 20V U/B<br>±1mA | Hermetic Ceramic DIP<br>Hermetic Ceramic DIP |
| | DAC707 | QM | 16 | ±0.003 | 8 | 15 | MIL, Com, Ind | 10V, 20V U/B | Hermetic Ceramic DIP, Plastic DIP |
| | DAC708<br>DAC709 | QM<br>QM | 16<br>16 | ±0.003<br>±0.003 | 1<br>8 | 15<br>15 | MIL, Com, Ind<br>MIL, Com, Ind | 2mA, ±1mA<br>10V, 20V U/B | Hermetic Ceramic DIP<br>Hermetic Ceramic DIP |
| High Resolution | DAC70BH<br>DAC71<br>DAC72BH | QM<br>QM<br>QM | 16<br>16<br>16 | ±0.003<br>±0.003<br>±0.003 | 1, 10<br>1, 10<br>1, 10 | 20<br>20<br>20 | Ind<br>Com<br>Ind | 10V, 20V, 2mA U/B<br>10V, 20V, 2mA U/B<br>10V, 20V, 2mA U/B | Hermetic Ceramic DIP<br>Hermetic Ceramic DIP<br>Hermetic Ceramic DIP |
| Low Cost, High Resolution | DAC710<br>DAC711 | | 16<br>16 | ±0.003<br>±0.003 | 1<br>8 | 50<br>50 | Com<br>Com | ±1mA<br>10V, 20V U/B | Hermetic Ceramic DIP, Plastic DIP |
| Low Cost, Bus Interface | DAC811 | QM | 12 | ±0.006 | 4 | 20 | MIL, Com, Ind | 10V, 20V U/B | Hermetic Ceramic DIP, Plastic DIP, SOIC, Die |
| CMOS | **DAC 7541** | **QM** | **12** | **±0.012** | **2** | **5** | **MIL, Com, Ind** | **Multiplying** | **Hermetic Ceramic DIP, Plastic DIP, SOIC, Die** |
| CMOS, Bus Interface | **DAC7545**<br>**DAC8012** | **QM**<br>**QM** | **12**<br>**12** | **±0.012**<br>**±0.012** | **2**<br>**1** | **5**<br>**5** | **MIL, Com, Ind**<br>**MIL, Com, Ind** | **Multiplying**<br>**Multiplying** | **Hermetic Ceramic DIP, Plastic DIP, SOIC, Die** |

(This table continued on next page.)

**For additional details, refer to the Burr-Brown *Product Data Book* and *Supplement*, or contact your nearest Burr-Brown sales office.**

# DATA CONVERSION AND DATA ACQUISITION (cont.)

| DIGITAL-TO-ANALOG CONVERTERS (cont.) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Description | Model | Q[1] Screen | Resolution (Bits) | Linearity Error (% FSR) | Settling Time (μs) | Gain Tempco (ppm/°C) | Temp Range[2] | Output Range[3] | Package |
| Low Cost, Industry Standard | DAC80 | | 12 | ±0.012 | 0.3, 3 typ | 30 | Com | 10V, 20V, 2mA U/B | Hermetic Ceramic DIP, Plastic DIP, Die |
| | DAC85H | QM | 12 | ±0.012 | 0.3, 3 typ | 20 | Ind | 10V, 20V, 2mA U/B | Hermetic Ceramic DIP |
| Military Temp, Industry Standard | DAC87H | QM | 12 | ±0.012 | 0.3, 3 typ | 20 | MIL | 10V, 20V, 2mA U/B | Hermetic Ceramic DIP |
| Ultra High Speed ECL | DAC63 | Q | 12 | ±0.012 | 0.05 | 30 | MIL, Ind | 10mA, U/B | Ceramic DIP, Metal Can |
| Ultra High Speed TTL | DAC812 | Q | 12 | ±0.012 | 0.065 | 20 | Ind | 10mA, U/B | Ceramic DIP, Metal Can |

NOTES: (1) "Q" or "QM" indicates product available with screening for enhanced reliability. (2) MIL = −55°C to +125°C, Com = 0°C to +70°C, Ind = −25°C to +85°C. (3) U = Unipolar, B = Bipolar.

| VOLTAGE-TO-FREQUENCY CONVERTERS | | | | | | | |
|---|---|---|---|---|---|---|---|
| Description | Model[1] | Frequency Range (kHz) | $V_{IN}$ Range (V) | Linearity, max (% of FSR) | Tempco, max (ppm of FSR/°C) | Temp Range[2] | Package |
| Low Cost, Monolithic | VFC32KP* | User-selected, 500kHz, max | User-selected | ±0.01 at 10kHz | 75 typ | Com | DIP |
| | VFC32BM, (Q) | | | ±0.05 at 100kHz | ±100 | Ind | TO-100 |
| | VFC32SM, (Q) | | | ±0.2 at 500kHz | ±150 | MIL | TO-100 |
| Low Cost Complete | VFC42BP | 0 to 10 | 0 to +10 | ±0.01 | ±100 | Ind | DIP |
| | VFC42SM | 0 to 10 | 0 to +10 | ±0.01 | ±100 | MIL | DIP |
| | VFC52BP | 0 to 100 | 0 to +10 | ±0.05 | ±150 | Ind | DIP |
| | VFC52SM | 0 to 100 | 0 to +10 | ±0.05 | ±150 | MIL | DIP |
| Precision Monolithic | VFC62BG* | User-selected, 1MHz max | User-selected | ±0.005 at 10kHz | ±50 | Ind | DIP |
| | VFC62BM | | | ±0.005 at 10kHz | ±50 | Ind | TO-100 |
| | VFC62SM | | | ±0.005 at 10kHz | ±50 | MIL | TO-100 |
| | VFC62CG | | | ±0.002 at 10kHz | ±20 | Ind | DIP |
| | VFC62CM | | | ±0.002 at 10kHz | ±20 | Ind | TO-100 |
| | VFC320BG* | User-selected, 1MHz max | User-selected | ±0.005 at 10kHz | ±50 | Ind | DIP |
| | VFC320BM | | | ±0.005 at 10kHz | ±50 | Ind | TO-100 |
| | VFC320SM | | | ±0.005 at 10kHz | ±50 | MIL | TO-100 |
| | VFC320CG | | | ±0.002 at 10kHz | ±20 | Ind | DIP |
| | VFC320CM | | | ±0.002 at 10kHz | ±20 | Ind | TO-100 |
| Synchronized Monolithic | VFC100AG* | Clock Programmed, 2MHz max | 0 to +10 | 0.025 at 100kHz | ±100 | Ind | DIP |
| | VFC100BG | | 0 to +10 | 0.1 at 1MHz | ±50 | Ind | DIP |
| | VFC100SG | | 0 to +10 | 0.025 at 100kHz | ±100 | MIL | DIP |

*Available in 20-pin ceramic leadless chip carriers.
NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C.



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# DATA CONVERSION AND DATA ACQUISITION (cont.)

| SAMPLE/HOLD AMPLIFIERS | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Description | Model | Q[1] Screen | Gain Error (% FSR) | Offset Error (mV) | Charge Offset (mV) | Amplifier Bandwidth, −3dB (MHz) | Hold Transient Settling (μs to 1mV) | Acquisition Time (μs) (0.01% FSR) | Aperture Time (ns) | Aperture Jitter (ns) | Input Range (Vp-p) | Package |
| Ultra High Speed | SHC600 | Q | 0.1 | 5 | 10 max | 70 | 0.015 | 0.05 | 8 | 0.009 | 2.5 | Ceramic DIP |
| High Speed With Buffer | SHC803 | Q | 0.1 | 3 | 5 max | 16 | 0.15 | 0.35 | 25 | 0.025 | 20 | Hermetic Metal DIP |
| High Speed | SHC804 | Q | 0.1 | 3 | 5 max | 16 | 0.15 | 0.35 | 25 | 0.025 | 20 | Hermetic Metal DIP |
| Low Cost | SHC5320 | Q | | 0.5 | 1 typ | 1.5 | 0.25 | 1.5 | 25 | 0.3 | 20 | Hermetic Ceramic DIP |
| | SHC85 | Q | 0.01 | 2 | 2 max | | 0.5 | 4.5 | 30 | 1.5 | 20 | Hermetic Metal DIP |
| | SHC298 | | 0.01 | 7 | 25 max | | 1.5 | 10 | 200 | 15 | 20 | TO-99 |

NOTE: (1) "Q" indicates product available with screening for enhanced reliability.

| MULTIPLEXERS | | | | | | | |
|---|---|---|---|---|---|---|---|
| Description | Model | Channels | Input Range (V) | On Resistance, max (Ω) | Crosstalk (% of Off Channel) | Settling Time (to 0.01%) | Package |
| Protected Inputs | MPC8S | 8 Single | ±15 | 1.8k | 0.005 | 5μs | DIP |
| | MPC4D | 4 Differential | ±15 | 1.8k | 0.005 | 5μs | DIP |
| | MPC16S | 16 Single | ±15 | 1.8k | 0.005 | 4μs | DIP |
| | MPC8D | 8 Differential | ±15 | 1.8k | 0.005 | 4μs | DIP |
| High Speed | MPC800KG | 16 Single or 8 Differential | ±15 | 750 | 0.004 | 800ns | DIP |
| | MPC800SG | 16 Single or 8 Differential | ±15 | 750 | 0.004 | 800ns | DIP |
| | MPC801KG | 8 Single or 4 Differential | ±15 | 750 | 0.004 | 800ns | DIP |
| | MPC801SG | 8 Single or 4 Differential | ±15 | 750 | 0.004 | 800ns | DIP |

# MILITARY PRODUCTS

| ANALOG-TO-DIGITAL CONVERTERS | | | | | | | |
|---|---|---|---|---|---|---|---|
| Model | Resolution (Bits) | Linearity, max (±LSB) | Conversion Time, max (μs) | Gain Drift, max (±ppm/°C) | Input Range (V) | Operating Temperature Range | Package |
| ADC87/883B | 12 | 1/2 | 10 | 15 | ±2.5, ±5, ±10, 0 to +5, 0 to +10 | MIL | 32-pin DIP |
| ADC87 | 12 | 1/2 | 10 | 15 | | MIL | 32-pin DIP |
| ADC87U/883B | 12 | 1/2 | 10 | 15 | | MIL | 32-pin DIP |
| ADC87U | 12 | 1/2 | 10 | 15 | | MIL | 32-pin DIP |
| ADC87V/883B | 12 | 1/2 | 10 | 15 | | MIL | 32-pin DIP |
| ADC87V | 12 | 1/2 | 10 | 15 | | MIL | 32-pin DIP |

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# MILITARY PRODUCTS (cont.)

| DIGITAL-TO-ANALOG CONVERTERS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Model | Resolution (Bits) | Linearity, max (±LSB) | Monotonicity (°C) | Gain Drift, max (±ppm/°C) | Settling Time, max | Output Ranges (V) | Operating Temperature Range | Package |
| DAC87-CBI-V/B | 12 | 1/2 | −55 to +125 | 20 | 7μsec | ±2.5, ±5, ±10, +5, +10 | MIL | 24-pin DIP |
| DAC87-CBI-V | 12 | 1/2 | −55 to +125 | 20 | 7μsec | | MIL | 24-pin DIP |
| DAC87U-CBI-V/B | 12 | 1/2 | −25 to +85 | 20 | 7μsec | | MIL | 24-pin DIP |
| DAC87U-CBI-V | 12 | 1/2 | −25 to +85 | 20 | 7μsec | | MIL | 24-pin DIP |
| DAC87-CBI-I/B | 12 | 1/2 | −55 to +125 | 20 | 400nsec | 0 to 2mA, ±1mA | MIL | 24-pin DIP |
| DAC87-CBI-I | 12 | 1/2 | −55 to +125 | 20 | 400nsec | | MIL | 24-pin DIP |
| DAC87U-CBI-I/B | 12 | 1/2 | −25 to +85 | 20 | 400nsec | | MIL | 24-pin DIP |
| DAC87U-CBI-I | 12 | 1/2 | −25 to +85 | 20 | 400nsec | | MIL | 24-pin DIP |
| DAC870V/883B | 12 | 1/2 | −55 to +125 | 25 | 7μsec | ±2.5, ±5, ±10, 0 to +5, 0 to +10 | MIL | 24-pin DIP ceramic |
| DAC870V | 12 | 1/2 | −55 to +125 | 25 | 7μsec | | MIL | |
| DAC870U/883B | 12 | 1/2 | −25 to +85 | 20 | 7μsec | | MIL | |
| DAC870U | 12 | 1/2 | −25 to +85 | 20 | 7μsec | | MIL | |
| DAC870VL/883B | 12 | 1/2 | −55 to +125 | 25 | 7μsec | | MIL | 28-term. leadless chip carrier |
| DAC870VL | 12 | 1/2 | −55 to +125 | 25 | 7μsec | | MIL | |
| DAC870UL/883B | 12 | 1/2 | −25 to +85 | 20 | 7μsec | | MIL | |
| DAC870UL | 12 | 1/2 | −25 to +85 | 20 | 7μsec | | MIL | |
| **DAC703VG/883B** | **16** | **±.003% FSR** | **−55 to +125[1]** | **20** | **8μsec** | **±10** | **MIL** | **24-pin DIP** |
| **DAC703VG** | **16** | **±.003% FSR** | **−55 to +125[1]** | **20** | **8μsec** | **±10** | **MIL** | **24-pin DIP** |
| **DAC703VL/883B** | **16** | **±.003% FSR** | **−55 to +125[1]** | **20** | **8μsec** | **±10** | **MIL** | **28-term. LCC** |
| **DAC703VL** | **16** | **±.003% FSR** | **−55 to +125[1]** | **20** | **8μsec** | **±10** | **MIL** | |

NOTE: (1) Monotonicity to 14-bit accuracy.

| VOLTAGE-TO-FREQUENCY CONVERTERS | | | | | | |
|---|---|---|---|---|---|---|
| Model | $V_{IN}$ Range (V) | $F_{OUT}$ Range, max (kHz) | Linearity, max at 10kHz (% FSR) | Full-Scale Drift, max (ppm FSR/°C) | Operating Temperature Range | Package |
| VFC32WM/883B | ±10 | 200 | ±0.006 | ±100 at 10kHz | MIL | TO-100 |
| VFC32WM | ±10 | 200 | ±0.006 | ±100 at 10kHz | MIL | TO-100 |
| VFC32VM/883B | ±10 | 200 | ±0.01 | −400, +150 at 200kHz | MIL | TO-100 |
| VFC32VM | ±10 | 200 | ±0.01 | −400, +150 at 200kHz | MIL | TO-100 |
| VFC32UM/883B | ±10 | 200 | ±0.01 | ±150 at 10kHz | MIL | TO-100 |
| VFC32UM | ±10 | 200 | ±0.01 | ±150 at 10kHz | MIL | TO-100 |

| MULTIPLIERS | | | | | | | |
|---|---|---|---|---|---|---|---|
| Model | Accuracy at 25°C, max (±%) | Accuracy at 125°C, max (±%) | Feedthrough, max (±mV) | Output Offset, max (±mV) | Output, min (V, mA) | Operating Temperature Range | Package |
| 4213WM/883B | 1/2 | 4 | 50 | 25 | ±10, ±5 | MIL | TO-100 |
| 4213WM | 1/2 | 4 | 50 | 25 | ±10, ±5 | MIL | TO-100 |
| 4213VM/883B | 1 | 4 | 100 | 30 | ±10, ±5 | MIL | TO-100 |
| 4213VM | 1 | 4 | 100 | 50 | ±10, ±5 | MIL | TO-100 |
| 4213UM/883B | 1 | 2[1] | 100 | 50 | ±10, ±5 | MIL | TO-100 |
| 4213UM | 1 | 2[1] | 100 | 50 | ±10, ±5 | MIL | TO-100 |

NOTE: (1) At +85°C.

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# MILITARY PRODUCTS (cont.)

## OPERATIONAL AMPLIFIERS

| Description | Model | Offset Voltage: At 25°C, max (±mV) | Offset Voltage: Drift, max (±μV/°C) | Bias Current, max (nA) | Bandwidth Unity Gain, min (MHz) | Slew Rate, min (V/μs) | $t_s$ ±0.01% (ns) | Compensation | Output, min (V, mA) | Operating Temp. Range | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Wideband | OPA600VM/883B | 2 | 20 | −100pA | 5000, [1] A = 1000 | 400 | 125 | external | ±10, ±200 | MIL | 16-pin DIP |
| | OPA600VM | 2 | 20 | −100pA | | 400 | 125 | external | ±10, ±200 | MIL | |
| | OPA600UM/883B | 5 | 80 | −100pA | | 400 | 150 | external | ±10, ±200 | MIL | |
| | OPA600UM | 5 | 80 | −100pA | | 400 | 150 | external | ±10, ±200 | MIL | |
| General Purpose Bipolar | 3500R/883B | 5 | 20 | ±30 | 1 | 0.6 | — | internal | ±10, ±10 | MIL | TO-99 |
| | 3500U/883B | 5 | 20[2] | ±30 | 1 | 0.6 | — | internal | ±10, ±10 | MIL | TO-99 |
| Precision Bipolar | 3510VM/883B | 0.12 | 2 | ±25 | 0.25 | 0.5 | — | internal | ±10, ±10 | MIL | TO-99 |
| Low Drift, Low Bias | OPA105WM/883B | 0.250 | 2 | −1pA | 1 | 0.9 | — | internal | ±10, ±10 | MIL | TO-99 |
| | OPA105WM | 0.250 | 2 | −1pA | 1 | 0.9 | — | internal | ±10, ±10 | MIL | TO-99 |
| | OPA105VM/883B | 0.250 | 5 | −1pA | 1 | 0.9 | — | internal | ±10, ±10 | MIL | TO-99 |
| | OPA105VM | 0.250 | 5 | −1pA | 1 | 0.9 | — | internal | ±10, ±10 | MIL | TO-99 |
| | OPA105UM/883B | 0.250 | 15[2] | −1pA | 1 | 0.9 | — | internal | ±10, ±10 | MIL | TO-99 |
| | OPA105UM | 0.250 | 15[2] | −1pA | 1 | 0.9 | — | internal | ±10, ±10 | MIL | TO-99 |
| Ultra Low Bias Current | OPA106WM/883B | 0.250 | 5 | −100fA | 1 | 1.2 | — | internal | ±10, ±5 | MIL | TO-99 |
| | OPA106WM | 0.250 | 5 | −100fA | 1 | 1.2 | — | internal | ±10, ±5 | MIL | TO-99 |
| | OPA106VM/883B | 0.250 | 10 | −150fA | 1 | 1.2 | — | internal | ±10, ±5 | MIL | TO-99 |
| | OPA106VM | 0.250 | 10 | −150fA | 1 | 1.2 | — | internal | ±10, ±5 | MIL | TO-99 |
| | OPA106UM/883B | 0.250 | 20[2] | −300fA | 1 | 1.2 | — | internal | ±10, ±5 | MIL | TO-99 |
| | OPA106UM | 0.250 | 20[2] | −300fA | 1 | 1.2 | — | internal | ±10, ±5 | MIL | TO-99 |
| Low Drift, Low Bias, Low Noise | **OPA111VM/883B** | **0.500** | **10** | **±2pA** | **2** | **1** | — | **internal** | **±10, ±5** | **MIL** | **TO-99** |
| | **OPA111UM** | **0.500** | **10** | **±2pA** | **2** | **1** | — | **Internal** | **±10, ±5** | **MIL** | **TO-99** |
| Power | **OPA501VM/883B** | **5** | **40** | **±20** | **1** | **1.35** | — | **internal** | **±26, ±10A** | **MIL** | **TO-3** |
| | **OPA501VM** | **5** | **40** | **±20** | **1** | **1.35** | — | **internal** | **±26, ±10A** | **MIL** | **TO-3** |
| | **OPA501UM/883B** | **10** | **65** | **±40** | **1** | **1.35** | — | **internal** | **±20, ±10A** | **MIL** | **TO-3** |
| | **OPA501UM** | **10** | **65** | **±40** | **1** | **1.35** | — | **internal** | **±20, ±10A** | **MIL** | **TO-3** |
| | OPA8780VM/883B | 10 | 30 | −0.05 | 5 | 15 | — | internal | ±30, ±60 | MIL | TO-3 |
| | OPA8780VM | 10 | 30 | −0.05 | 5 | 15 | — | internal | ±30, ±60 | MIL | TO-3 |
| | OPA8780UM/883B | 10 | 50 | −0.05 | 5 | 15 | — | internal | ±30, ±60 | MIL | TO-3 |
| | OPA8780UM | 10 | 50 | −0.05 | 5 | 15 | — | internal | ±30, ±60 | MIL | TO-3 |

NOTES: (1) Gain-bandwidth product. (2) −25°C to +85°C.

## INSTRUMENTATION AMPLIFIERS

| Description | Model | Gain Range[1] | Gain Accuracy, G = 100, At 25°C, max (%FS) | Gain Drift, G = 100, typ (ppm/°C) | Non-linearity G = 100 max | Input Parameters: CMR, DC to 60Hz, G = 10, min, 1kΩ Unbal. (dB) | Input Parameters: Offset Voltage vs Temp, G = 1000, max (μV/°C) | Dynamic Response, G = 100, ±3dB BW (kHz) | Temp Range | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| Very High Accuracy | **INA101VG/883B** | **1-1000** | **0.10** | **22** | **0.007** | **96** | **1.75** | **25** | **MIL** | **DIP** |
| | **INA101VG** | **1-1000** | **0.10** | **22** | **0.007** | **96** | **1.75** | **25** | **MIL** | **DIP** |
| | **INA101VM/883B** | **1-1000** | **0.10** | **22** | **0.007** | **96** | **1.75** | **25** | **MIL** | **TO-100** |
| | **INA101VM** | **1-1000** | **0.10** | **22** | **0.007** | **96** | **1.75** | **25** | **MIL** | **TO-100** |
| | INA258WG/883B | 1-1000 | 0.10 | 22 | 0.007 | 96 | 0.5 | 25 | MIL | DIP |
| | INA258WG | 1-1000 | 0.10 | 22 | 0.007 | 96 | 0.5 | 25 | MIL | DIP |
| | INA258VG/883B | 1-1000 | 0.10 | 22 | 0.007 | 96 | 1.0 | 25 | MIL | DIP |
| | INA258VG | 1-1000 | 0.10 | 22 | 0.007 | 96 | 1.0 | 25 | MIL | DIP |
| | INA258UG/883B | 1-1000 | 0.10 | 22 | 0.007 | 96 | 3.0 | 25 | MIL | DIP |
| | INA258UG | 1-1000 | 0.10 | 22 | 0.007 | 96 | 3.0 | 25 | MIL | DIP |
| | INA258WL/883B | 1-1000 | 0.10 | 22 | 0.007 | 96 | 0.5 | 25 | MIL | 20-terminal leadless chip carrier |
| | INA258WL | 1-1000 | 0.10 | 22 | 0.007 | 96 | 0.5 | 25 | MIL | |
| | INA258VL/883B | 1-1000 | 0.10 | 22 | 0.007 | 96 | 1.0 | 25 | MIL | |
| | INA258VL | 1-1000 | 0.10 | 22 | 0.007 | 96 | 1.0 | 25 | MIL | |
| | INA258UL/883B | 1-1000 | 0.10 | 22 | 0.007 | 96 | 3.0 | 25 | MIL | |
| | INA258UL | 1-1000 | 0.10 | 22 | 0.007 | 96 | 3.0 | 25 | MIL | |

NOTE: (1) Set with external resistor.

**For additional details, refer to the Burr-Brown *Product Data Book* and *Supplement*, or contact your nearest Burr-Brown sales office.**

Burr-Brown

# CMD G8880

# Microcircuits

## CMOS Integrated DTMF Transceiver

### Features

- Advanced CMOS technology for low power consumption and increased noise immunity
- Complete DTMF Transmitter/Receiver within a single chip
- Standard 6500/6800 series microprocessor port
- Central office quality and performance
- Adjustable Guard Time
- Automatic Tone Burst mode
- Call Progress mode
- Single +5 volt power supply
- 20-pin DIP or 28-pin PLCC package

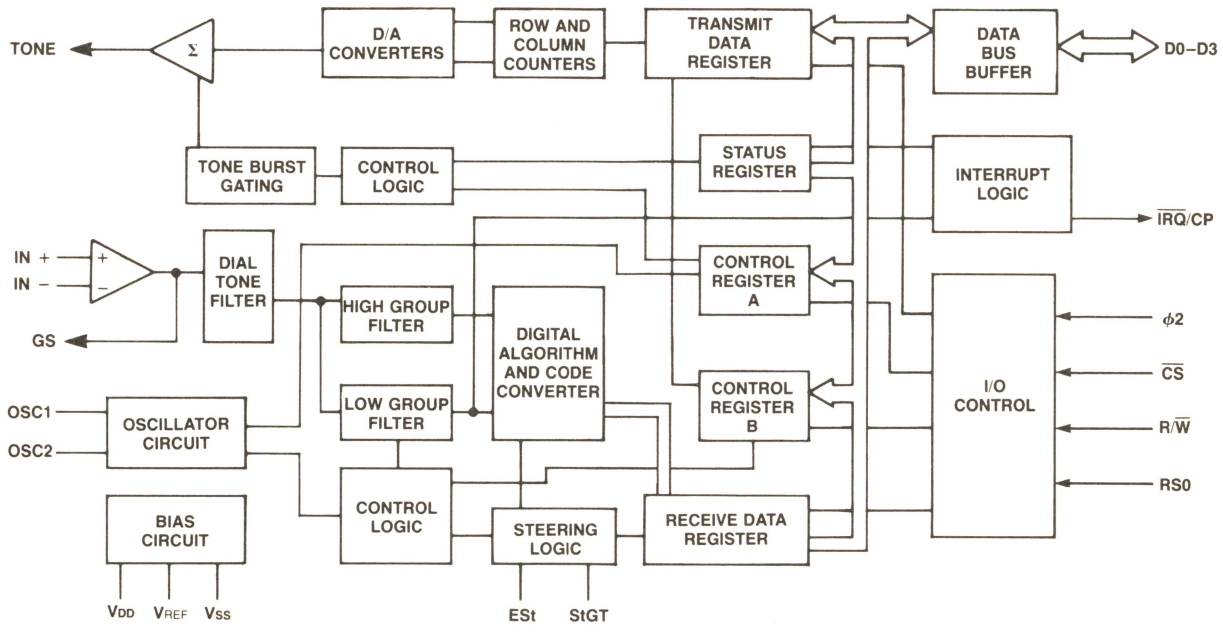
### Applications

- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- PABX systems
- Computer systems

### General Description

The CMD G8880 is a fully integrated DTMF Transceiver, featuring Adjustable Guard Time, Automatic Tone Burst mode, Call Progress mode and a fully compatible 6500/6800 microprocessor interface. The G8880 is manufactured using state-of-the-art Advanced CMOS technology for low power consumption and precise data handling. The G8880 is based on the industry standard G8870 DTMF Receiver, while the transmitter utilizes a switched-capacitor D/A converter for low distortion, highly accurate DTMF signalling. Internal counters provide an Automatic Tone Burst mode which allows tone bursts to be transmitted with precise timing. A Call Progress filter can be selected by an external microprocessor for analyzing Call Progress tones.

### Block Diagram





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California Micro Devices

# CMD G8870

## Microcircuits

## CMOS DTMF Integrated Receiver

### Features

- CMOS technology for low power consumption—35 mW max.
- Full DTMF receiver
- Provides DTMF high and low group filtering
- Adjustable acquisition and release times
- Dial tone suppression
- Integrated bandsplit filter and digital decoder functions
- On-chip differential amplifier, clock oscillator, and latched three-state bus.
- Uses inexpensive 3.58 MHz crystal
- Central office quality and performance
- Single +5 volt power supply
- 18-pin DIP or 20-pin PLCC package

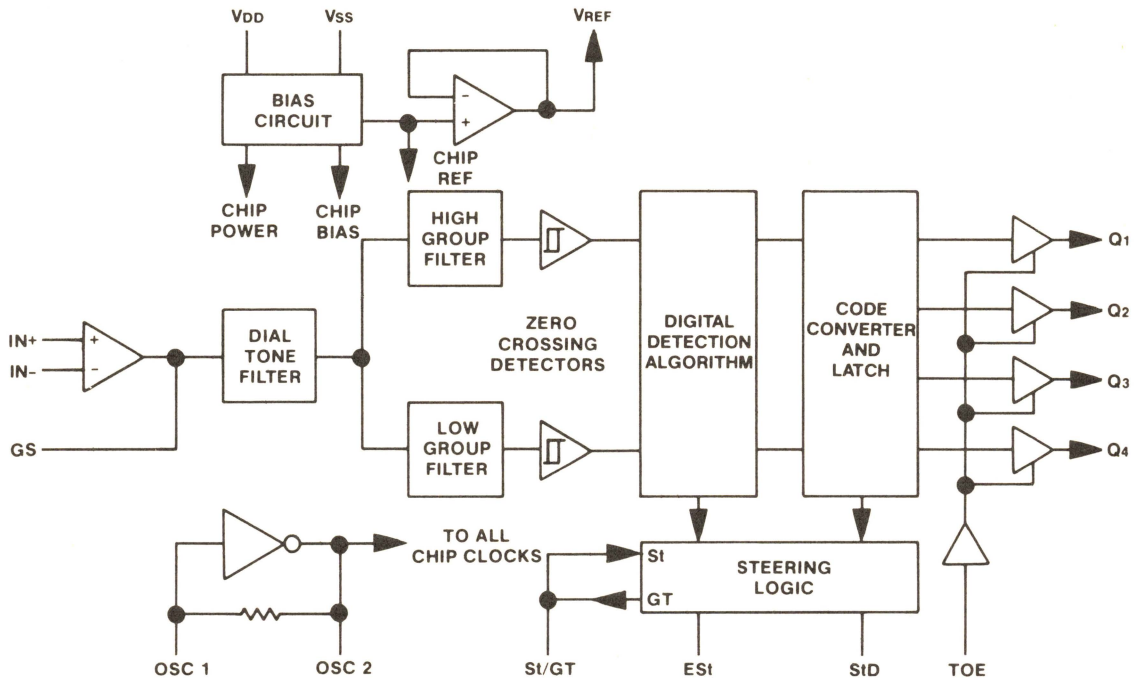
### Applications

- PABX
- Central office
- Key systems
- Mobile radio
- Remote control
- Remote data entry

### General Description

The CMD G8870 provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP or 20-pin PLCC package. The G8870 is manufactured using state-of-the-art CMOS process technology for low power consumption (35 mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The G8870 decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. The G8870 minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal as an external component.

### Block Diagram





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CMD

# G65SC150

## Microcircuits

## CMOS Communications Terminal Unit (Telecommunication Microcomputer)

California Micro Devices

### Features

- Generates signals compatible with switched telephone networks or packet switched data networks
- Provides Dial Pulse (DP), Dual Tone Multi-Frequency (DTMF), and 0-600 baud modem signaling capabilities
- Low power mode (300 μA) enables telephone line-powered operation
- External microprocessor address and data bus facilitates memory and I/O expansion
- On-chip memory: 2K bytes ROM
  64 bytes RAM
- Standard DTMF and modem frequencies can be generated which are accurate to ±1.0% with a 3.58 MHz crystal
- Two sine wave generators
- 6800 and 6500 bus compatibility
- Utilizes G65SC00 microprocessor as CPU
- 27 TTL compatible I/O lines
- Bus expandable to address 65K bytes of external memory
- Single +5 volt power supply
- Available in 68-pin chip carriers

### General Description

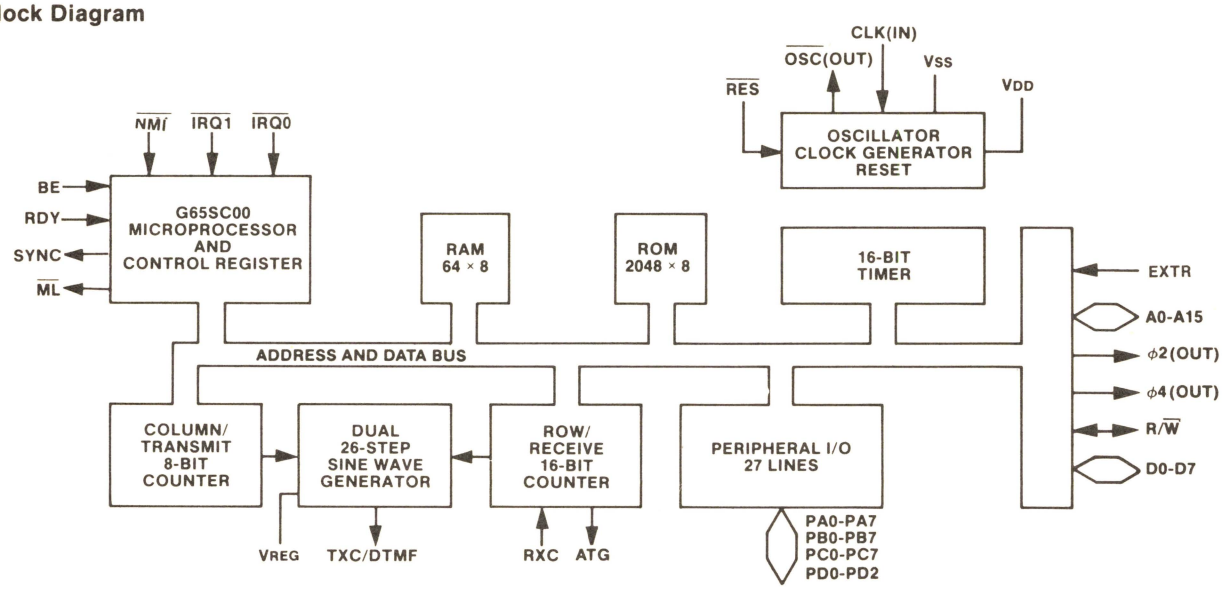
The CMD G65SC150 Communications Terminal Unit (CTU) is a single chip telecommunications microcomputer manufactured using state-of-the-art silicon gate CMOS process technology, which is optimized for telephone line signaling and data transmission applications. A functional block diagram is shown which illustrates the major system functions that are included on the integrated circuit.

The CTU uses the CMD G65SC00 8-bit microprocessor which executes the complete G65SC00 series instruction set. With 2K bytes of ROM and 64 bytes of RAM, the CTU operates as a single-chip microcomputer.

The internal bus interconnects all microcomputer functions. The address and data bus buffers permit expansion of ROM, RAM and memory mapped I/O using the full 65K addressing space of the microprocessor. A peripheral mode is available for use with multiprocessor systems. A test and prototyping mode switches internal ROM addresses to external access. An on-chip oscillator may be driven by an external clock source.

The telecommunications interface circuitry consists of a timer, row/receive counter, column/transmit counter and dual sine wave generators. In addition, 27 general purpose I/O lines can be used for keyboard, telephone Dial Pulse (DP) signaling, phone line control, and other peripheral devices.

### Block Diagram

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# G65SC802
# G65SC816

## Microcircuits

## CMOS 8/16-Bit Microprocessor Family

### Features

- Advanced CMOS design for low power consumption and increased noise immunity
- Emulation mode for total software compatibility with 6502 designs
- Full 16-bit ALU, Accumulator, Stack Pointer, and Index Registers
- Direct Register for "zero page" addressing
- 24 addressing modes (including 13 original 6502 modes)
- Wait for Interrupt (WAI) and Stop the Clock (STP) instructions for reduced power consumption and decreased interrupt latency
- 91 instructions with 255 opcodes
- Co-Processor (COP) instruction and associated vector
- Powerful Block Move instructions

### Features (G65SC802 Only)

- 8-Bit Mode with both software and hardware (pin-to-pin) compatibility with 6502 designs (64 KByte memory space)
- Program selectable 16-bit operation
- Choice of external or on-board clock generation

### Features (G65SC816 Only)

- Full 16-bit operation with 24 address lines for 16 MByte memory
- Program selectable 8-Bit Mode for 6502 coding compatibility.
- Valid Program Address (VPA) and Valid Data Address (VDA) outputs for dual cache and DMA cycle steal implementation
- Vector Pull ($\overline{VP}$) output indicates when interrupt vectors are being fetched. May be used for vectoring/prioritizing interrupts
- Abort interrupt and associated vector for interrupting any instruction without modifying internal registers
- Memory Lock ($\overline{ML}$) for multiprocessor system implementation

### General Description

The G65SC802 and G65SC816 are ADV-CMOS (ADVanced CMOS) 16-bit microprocessors featuring total software compatibility with 8-bit NMOS and CMOS 6500 series microprocessors. The G65SC802 is pin-to-pin compatible with 8-bit 6502 devices currently available, while also providing full 16-bit internal operation. The G65SC816 provides 24 address lines for 16 MByte addressing, while providing both 8-bit and 16-bit operation.

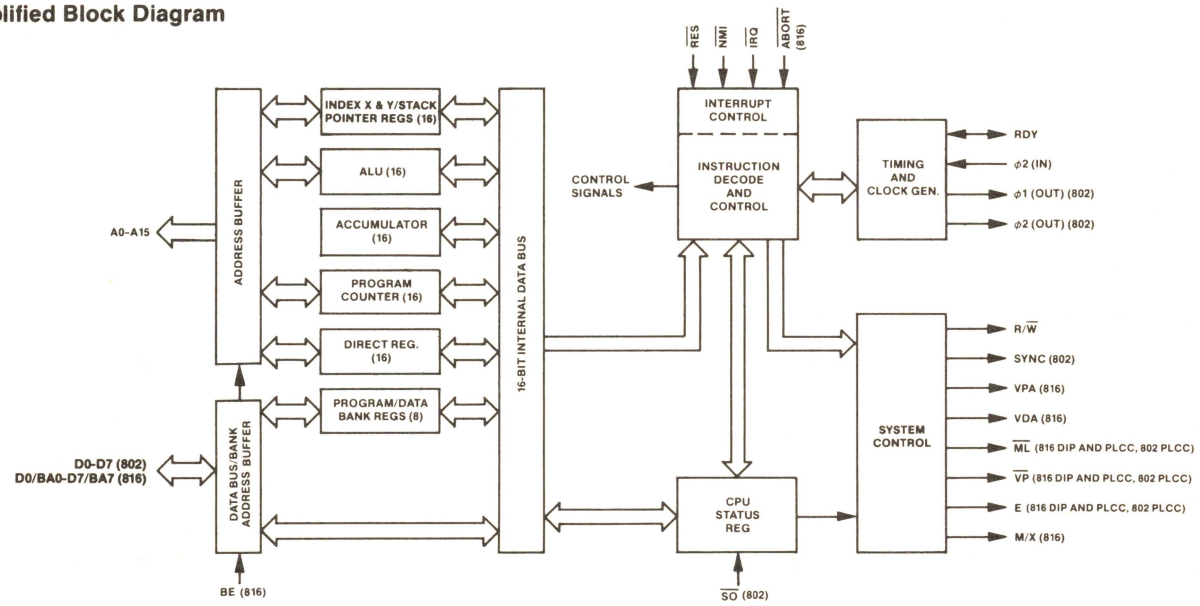
Each microprocessor contains an Emulation (E) mode for emulating 8-bit NMOS and CMOS 6500-Series microprocessors. A software switch determines whether the processor is in the 8-bit emulation mode or in the Native 16-bit mode. This allows existing 8-bit system designs to use the many powerful features of the G65SC802 and G65SC816.

The G65SC802 and G65SC816 provide the system engineer with many powerful features and options. A 16-bit Direct Page Register is provided to augment the Direct Page addressing mode, and there are separate Program Bank Registers for 24-bit memory addressing. Other valuable features include:

- An Abort input which can interrupt the current instruction without modifying internal registers.
- Valid Data Address (VDA) and Valid Program Address (VPA) outputs which facilitate dual cache memory by indicating whether a data or program segment is being accessed.
- Vector modification by simply monitoring the Vector Pull ($\overline{VP}$) output.
- Block Move instructions.

CMD Microcircuits' G65SC802 and G65SC816 microprocessors offer the design engineer a new freedom of design and application, and the many advantages of state-of-the-art ADV-CMOS technology.

### Simplified Block Diagram





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# CMD

# Microcircuits

# G24352
# G24353
# G24354
# G24357

## CMOS Monolithic Serial Interface PCM Codec/Filter Family

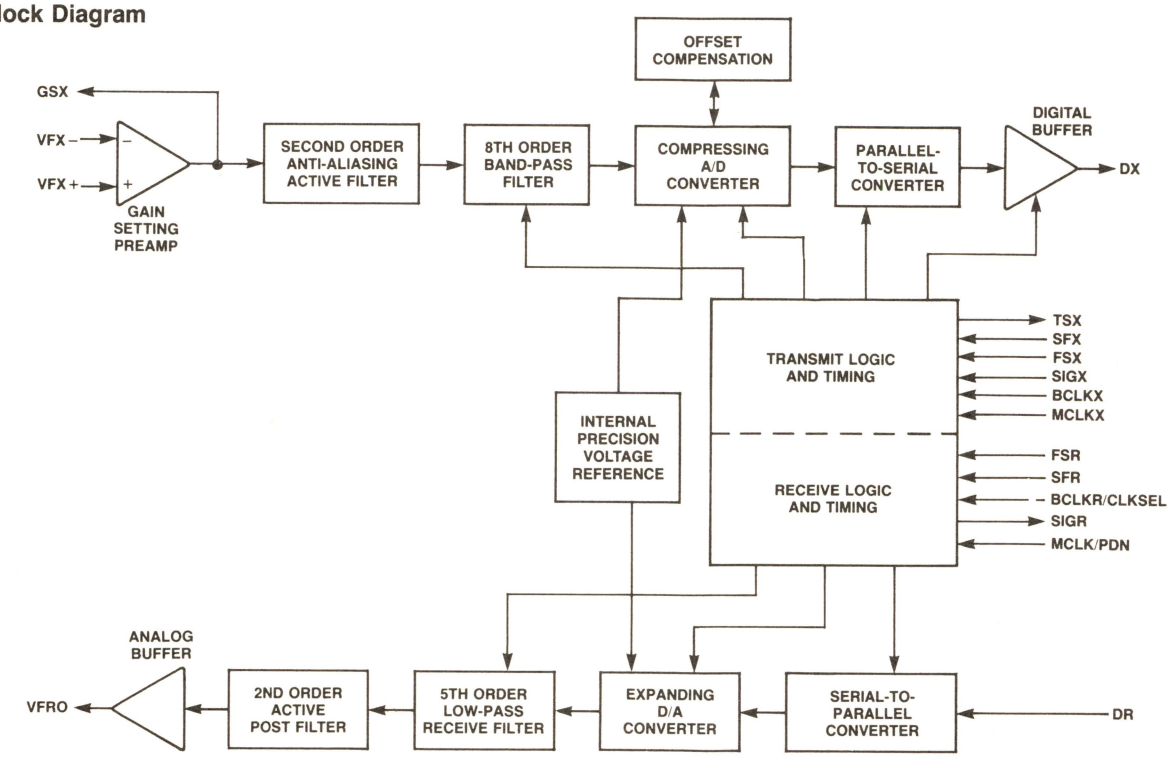
### Features

- Four complete Codec/filtering systems:
  - — G24352 — $\mu$-law with signaling (18-pin version)
  - — G24353 — $\mu$-law with signaling (20-pin version)
  - — G24354 — $\mu$-law without signaling (16-pin version)
  - — G24357 — A-law (16-pin version)
- Low power CMOS design: 60 mW operating (typ), 3 mW standby (typ)
- High-pass and low-pass transmit filtering
- Receive Sin x/x correction
- Resistor programmable gain for transmit section
- Synchronous or asynchronous transmit and receive operation
- Serial I/O interface
- Active RC anti-aliasing and post filters
- Precision internal voltage reference and auto-zero circuits
- Automatic power-down by removing frame Sync's and/or single-pin power-down
- Electrostatic discharge and improved latch-up protection on all inputs
- TTL or CMOS compatible logic
- ± 5V power input

### General Description

CMD Microcircuits' family of $\mu$-law and A-law Codec/Filter circuits feature precision A/D and D/A signal conversion in combination with a serial PCM digital interface. Each device performs voice digitizing and recovery, as well as band limiting and signal restoration as required for companded PCM systems. Within each device, the encode section features an input gain adjust amplifier, active high-frequency RC filter, offset compensation circuitry and a switched-capacitor band-pass filter for rejecting frequencies outside a 200 to 3400 Hz band. Filtered signals are sampled and encoded into the companded $\mu$-law or A-law format. The decode section features an expanding decoder for reconstructing the $\mu$-law or A-law encoded signal, a low-pass filter including Sin x/x response corrections, and a low impedance power amplifier output stage. All devices within the CMD Codec/Filter family meet or exceed AT&T D3/D4 and CCITT specifications, and are manufactured using CMD's state-of-the-art CMOS process technology for increased noise immunity, higher reliability and reduced power consumption.

### Block Diagram





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# CMD G24002

## Microcircuits

## Subscriber Line Interface Circuit (SLIC) — Interface IC

### Features

- Advanced Dielectrically Isolated Bipolar Monolithic technology
- Meets both North American and LSSGR Central Office Transmission and Signaling Standards
- Provides SLIC interface and BORSHT functions
- Longitudinal balance of 59 dB or greater
- Tip Party Mark detection
- Tip/Ring to ground or battery short circuit detection
- Thermal shutdown circuit
- Source/sink current capability (117 mA at Tip and Ring)
- Program-controlled power reduction in Idle mode
- Available in 28-pin DIP or PLCC package

### General Description

CMD Microcircuits' G24002 SLIC Interface IC is a High Voltage Dielectrically Isolated Bipolar Monolithic LSI circuit designed to provide a direct interface to a telephone subscriber loop. The Interface IC is designed to function in combination with the CMD G24010 SLIC Control IC. This two-chip set, when combined with a PCM Codec/Filter, results in a highly versatile solid-state SLIC-based Line Card which is ideally suited for Central Office Switch or PABX applications. The two-chip set provides BORSHT functions which include:

- Floating-polarity battery feed with controlled loop current
- Overvoltage protection (external)
- Ringing
- Supervision/signaling
- 2 to 4 wire hybrid conversion
- System testing
- Microcomputer control logic interface
- Hybrid software selectable networks (one-of-three)

# CMD G24010

## Microcircuits

## Subscriber Line Interface Circuit (SLIC) — Control IC

### Features

- Double-Poly CMOS Monolithic technology
- Meets both North American and LSSGR Central Office Transmission and Signaling Standards
- Provides SLIC control and BORSHT functions
- Performs 2 to 4 wire hybrid conversion with 9:2, loaded and non-loaded networks
- Logic Control Interface for off-chip microcomputer control function
- Interfaces with G24002 SLIC Interface IC and PCM Codec/Filter
- Ring-Trip Detection
- Ground Start Detection
- DC Loop Control
- Loop Sense Detection
- Available in 44-pin PLCC or 40-pin DIP package

### General Description

CMD Microcircuits' G24010 SLIC Control IC is a Double-Poly CMOS Monolithic LSI integrated circuit designed to provide a three-way interface between CMD's G24002 SLIC Interface IC, a PCM Codec/Filter, and external microcomputer control. The G24010 Control IC is designed to function in combination with the CMD G24002 Interface IC. This two-chip set, in combination with a PCM Codec/Filter, results in a highly versatile solid-state SLIC-based Line Card which is ideally suited for Central Office Switch or PABX applications. The combined two-chip set provides BORSHT functions which include:

- Floating-polarity battery feed with controlled loop current
- Overvoltage protection (external)
- Ringing
- Supervision/signaling
- 2 to 4 wire hybrid conversion
- System testing
- Microcomputer control logic interface
- Hybrid software selectable networks (1-of-3)

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# CMD

# G65SCXX Series
# G65SC1XX Series

## Microcircuits

## CMOS G65SCXXX 8-Bit Microprocessor Family

### Features

- CMOS family that is compatible with NMOS 6500 series microprocessors
- Uses single +5 volt power supply
- Low power consumption (4mA @ 1 MHz) allows battery-powered operation
- Enhanced instruction set: 27 additional op codes encompassing eight new instructions enhance software performance compared to existing NMOS 6500 microprocessor instruction set
  —64 microprocessor instructions
  —178 operational codes
  —15 addressing modes
- Choice of 4K, 8K or 65K-byte addressable memory
- 1, 2, 3 or 4 MHz operation
- Choice of external or on-board clock generator operation
- On-board clock generator/oscillator can be driven by an external single-phase clock input, an RC network, or a crystal circuit
- Advanced memory access timing ($\phi$4) on selected versions
- Early address valid allows use with slower memories
- Early write data for dynamic memories
- 8-bit parallel processing
- Decimal and binary arithmetic
- Pipeline architecture
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Available on selected versions, a memory lock output and bus enable input signals simplify multiprocessor designs

### General Description

The G65SCXXX is a totally software-compatible microprocessor family manufactured using the state-of-the-art silicon gate CMOS process. The family consists of two series of devices: one series, designated G65SCXX is pin-to-pin compatible with NMOS versions of the 6500 currently on the market; the other series, designated G65SC1XX includes several enhancements not available with other designs. The family provides the designer with a wide selection of addressable memory ranges, on-board or external clocks, and input interrupt options. All of the microprocessors are software compatible within the group and all are bus compatible with MC6800 products.

As shown in Table I, the family includes 18 microprocessors of which three have on-chip oscillators while the others require an external clock generator. The G65SC02, G65SC102 or G65SC112 clock generator circuit may be driven by an external crystal (Figure 2a), an RC network (Figure 2b) or by an external clock source. The versions of the microprocessor which require an external clock source are generally intended for multiprocessor applications where maximum timing control is necessary. The three family members with on-chip oscillators are intended for high performance, low cost operations where single phase inputs, crystals, or RC inputs provide the time base.

Ten of the microprocessors in the G65SCXX Series are pin-to-pin compatible with the NMOS 6500 microprocessors offered by several other manufacturers. However, the use of the leading-edge CMOS process technology ensures several software or programming enhancements not available to users of the NMOS 6500. The enhancements include two additional addressing modes, an expanded microprocessor instruction set (from 56 to 64 instructions), and expanded operational codes (from 151 to 178). In addition, a series of operational enhancements are provided which materially improve the effective use of the microprocessor. These enhancements are explained in Table V of the section of this data sheet devoted to system software and programming. This series of microprocessors provides the user an architecture and instruction set with which he is basically familiar (6502), the several operational enhancements notwithstanding, plus all of the advantages of leading edge CMOS technology; i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

**TABLE I. G65SCXXX FAMILY MICROPROCESSOR CAPABILITIES**

| ITEM NO. | PART NUMBER | DIP PINS | ADDRESSABLE MEMORY (BYTES) | ON-BOARD CLOCK OSCILLATOR (SEE NOTE) | EXTERNAL CLOCK GENERATOR REQUIRED | ADVANCED MEMORY ACCESS ($\phi$4) | $\overline{IRQ}$ | $\overline{NMI}$ | $\overline{SO}$ | DBE | BE | SYNC | RDY | $\overline{ML}$ | $\overline{RES}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | G65SC02 | 40 | 65K | • | | | • | • | • | | | • | • | | • |
| 2 | G65SC03 | 28 | 4K | | • | | • | • | | | | | | | • |
| 3 | G65SC04 | 28 | 8K | | • | | • | | | | | | | | • |
| 4 | G65SC05 | 28 | 4K | | • | | • | | | | | | • | | • |
| 5 | G65SC06 | 28 | 4K | | • | | • | | | | | | | | • |
| 6 | G65SC07 | 28 | 8K | | • | | | | | | | | • | | • |
| 7 | G65SC12 | 40 | 65K | | • | | • | • | • | • | | • | | | • |
| 8 | G65SC13 | 28 | 4K | | • | | • | • | | | | | | | • |
| 9 | G65SC14 | 28 | 8K | | • | | • | | | | | | | | • |
| 10 | G65SC15 | 28 | 4K | | • | | • | | | | | | • | | • |
| 11 | G65SC102 | 40 | 65K | • | | • | • | • | • | | • | • | • | • | • |
| 12 | G65SC103 | 28 | 4K | | • | • | • | • | | | | | | | • |
| 13 | G65SC104 | 28 | 8K | | • | • | • | | | | | | | | • |
| 14 | G65SC105 | 28 | 4K | | • | • | • | | | | | | • | | • |
| 15 | G65SC106 | 28 | 4K | | • | • | • | | | | | | | | • |
| 16 | G65SC107 | 28 | 8K | | • | • | | | | | | | • | | • |
| 17 | G65SC112 | 40 | 65K | • | | | • | • | • | | • | • | • | • | • |
| 18 | G65SC115 | 28 | 4K | | • | | • | | | | | | • | • | • |

**NOTE:** These devices can operate in any of the following clock generation modes: 1. External crystal 2. External RC network 3. $\phi$0(IN) from external clock source


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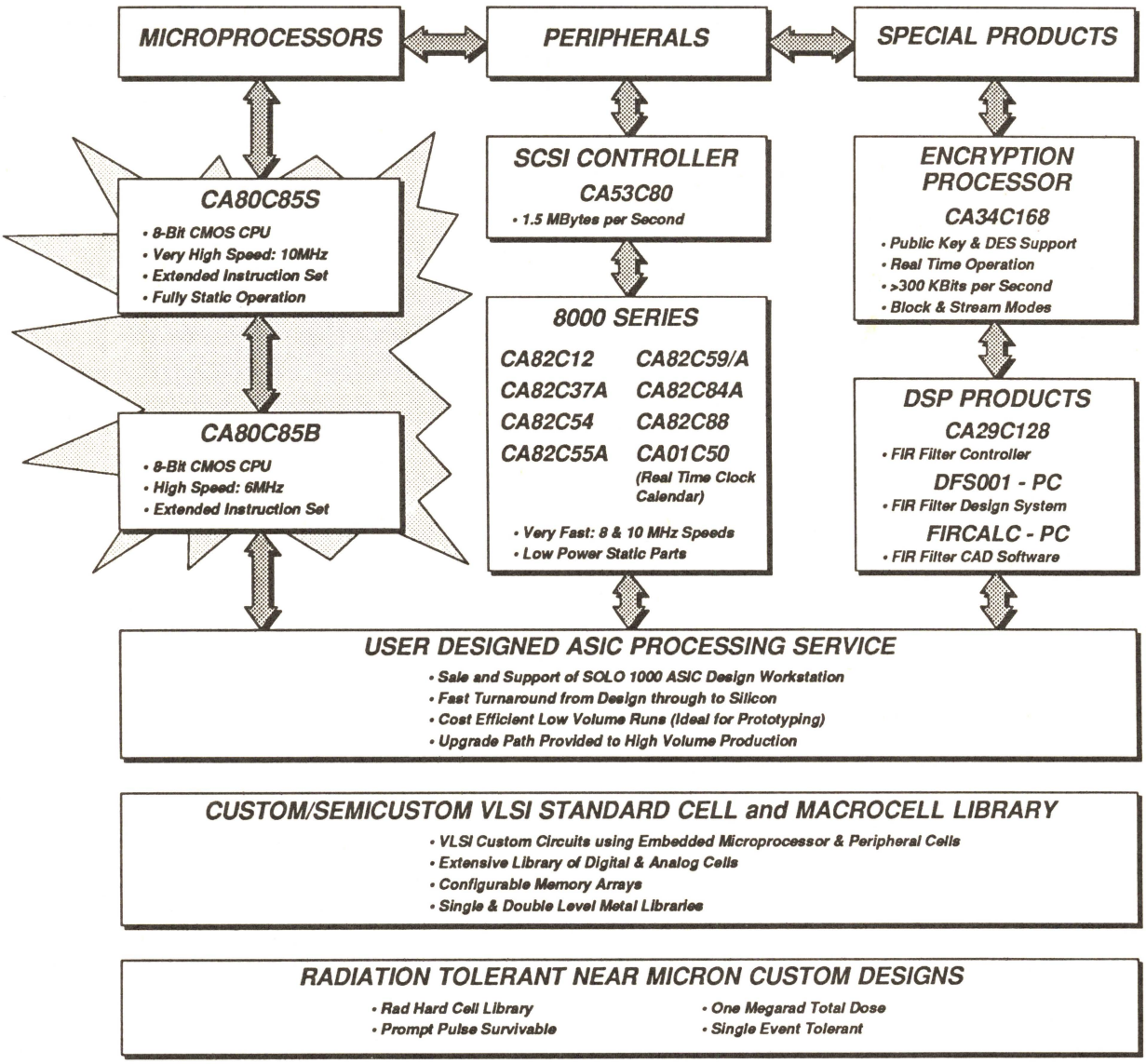
Calmos Systems Inc.

# HIGH SPEED CMOS

## DATA PROCESSING COMPONENTS

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# CTI'S QUICK SELECTION GUIDE FOR MIL-STD-1553.

CTI has long been recognized as a specialist in designing and producing hi-rel microcircuits for the military. We're now a major supplier of standard bus circuits for MIL-STD-1553, with products in use in most major military and space programs (F-18, A-10, LAMPS, and many more). Call or write for details to Circuit Technology Inc., 160 Smith Street, Farmingdale, NY 11735 516/293-8686.

CTI

**Circuit Technology Inc.**

*The military Standard in microelectronics.*

| PG. NO. | RECEIVERS/ TRANSMITTERS | MIL-STD-1553B | MIL-STD-1553A | MAC AIR | SINGLE TRANSCEIVER | DUAL TRANSCEIVER | DRIVER ONLY | RECEIVER ONLY | OPERATES FROM ± 15V | OPERATES FROM ± 12V | REQUIRES + 5V | INVERTED OUTPUT AVAILABLE | BUS CONTROLLER | REMOTE TERMINAL | MONITOR | SINGLE CHANNEL | DUAL REDUNDANT | HYBRID CIRCUIT PACKAGE | LCC PACKAGE(S) | PLUG IN PACKAGE | FLAT PACK AVAILABLE | ENCODE, DECODE PROTOCOL | PROGRAMMABLE | FULL MIL-STD-1553B PROTOCOL | 8 & 16 BIT COMPATIBLE | FIFO/RAM BUFFER | MIL-STD-1750A & µP COMPATIBLE | BUFFERED OUTPUTS | TX STROBE OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | CT1487 M Series | • | • | | • | | | | • | | • | • | | | • | | • | | • | • | | | | | | | | | |
| | CT1487 D Series | • | • | | | • | | | • | | • | • | | | | • | • | | • | • | | | | | | | | | |
| | CT1589 M Series | • | • | | • | | | | | • | • | • | | | • | | • | | • | • | | | | | | | | | |
| | CT1589 D Series | • | • | | | • | | | | • | • | • | | | | • | • | | • | • | | | | | | | | | |
| 5 | CT2077 M | | • | • | | | • | | • | | • | | | | • | | • | | | • | | | | | | | | | |
| | CT3077 M | | • | • | | | • | | | • | • | | | | • | | • | | | • | | | | | | | | | |
| | CT3078 M | • | • | • | | | | • | • | • | • | | | | • | | • | | | • | | | | | | | | | |
| | CT3231 M Series | • | • | | • | | | | • | • | • | | | | • | | • | | • | • | | | | | | | | | |
| | CT3232 M Series | • | • | • | • | | | | • | • | • | | | | • | | • | | • | • | | | | | | | | | |
| | **DATA BIT PROCESSORS** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | CT1820 Series | • | • | | | | | | | | • | | • | • | • | • | | • | | | • | • | • | | • | | | | |
| | CT1775 | • | • | • | • | | | • | • | • | • | | • | • | • | • | | • | | • | • | • | • | | • | | | | |
| | **PROTOCOL PROCESSORS** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | CT1560 | • | | | | | | | | | • | | | • | • | • | | | • | • | | | | • | | | | | |
| | CT1561 | • | | | | | | | | | • | | | • | • | | • | | • | • | | | | • | | | | | |
| | CT1562 | • | | | | | | | | | • | | • | • | • | • | | | • | • | | | | • | | | | | |
| | CT1563 | • | | | | | | | | | • | | • | • | • | | • | | • | • | | | | • | | | | | |
| 6 | CT1602 | • | | | | | | | | | • | | • | • | • | | • | • | | • | • | | | • | | | | • | |
| | CT1606 | • | | | | | | | | | • | | | • | • | • | • | • | | • | | | | • | | | | • | |
| | CT1610 | • | | | | | | | | | • | | • | • | • | • | • | • | | • | • | | | • | | | | | |
| | CT1612 | • | | | | | | | | | • | | • | • | • | • | • | • | | • | • | | • | • | | | | | |
| | CT1615 | • | | | | | | | | | • | | • | • | • | | • | • | | • | | | | • | | | | • | • |
| 7 | CT1617 | • | | • | • | • | | | • | • | • | | • | • | • | • | • | | | | | | | • | | | | • | |
| | **MIL-STD-1553/µP INTERFACE CIRCUITS** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | CT1611 | • | | | | | | | | | • | | • | • | • | • | • | • | | • | • | | • | • | • | • | • | | |
| | CT1800 | • | | | | | | | | | • | | | • | • | • | • | • | | • | • | | • | • | • | • | • | | |
| 7 | CT1801 | • | | | | | | | | | • | | | • | • | • | • | • | | • | • | | • | • | • | • | • | | |

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NEW

# 65CE02 MICROPROCESSOR

PRELIMINARY

***Features***

- **CMOS technology**
- **0–10 Mhz operating speeds**
- **Code compatible with existing 6502/65C02**
- **Instruction set streamlined**
  - —Instructions require fewer cycles
  - —'Dead' cycles removed
  - —Execution times independent of page boundary crossings
- **Executes existing 6502/65C02 code in up to 25% fewer cycles**
- **Stack pointer increased to 16 bits with two modes of operation**
  - —Full 16 bit pointer
  - —Page programmable 8 bit pointer
- **Base page register**
  - —Allows relocation of 'zero' page to any page in memory
- **Additional index register**
  - —Functions similar to the Y index register
- **Enhanced instruction set**
  - —25 new instructions
  - —3 new addressing modes
  - —All 65C02 additions
  - —Z index register commands
  - —New register manipulation commands
  - —Word relative branching (16 bit offset)
  - —Branch to subroutine (word rel)
  - —Indirect and indirect indexed subroutine calls
  - —2's complement
  - —Arithmetic shift right
  - —Increment and decrement word
  - —Arithmetic shift left word
  - —Rotate left word
  - —Subroutine parameter passing via the stack supported
  - —Expandable for customized applications

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***Description***

The Commodore 65CE02 is an enhanced version of the standard 6502, manufactured in CMOS technology for high speed and low power consumption. The 65CE02 is pin for pin compatible with the existing 6502/65C02.

Since the 65CE02 is a true static device, the clock may be stopped in either state, without loss of data and with almost no power dissipation. The instruction set has been expanded to 255 opcodes and streamlined to give up to a 25% improvement in code execution time over a standard 6502/65C02. All branching instructions have been expanded to include a word relative addressing mode which allows conditional branching anywhere within the 64K memory space. A new word relative branch to subroutine has also been added. This new addressing mode aids the programmer in creating re-locatable code modules, resulting in increased software flexibility. Also included is an addressing mode which facilitates parameter passing to subroutines via the stack. Parameters and/or pointers to data arrays can be passed to a subroutine via the stack, and a special return instruction will 'fix' the stack pointer when the subroutine is finished.

The 65CE02 provides the system designer with a high performance, low power microprocessor, while retaining its downward compatibility with the existing family of microprocessor support devices.

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# SPECIAL APPLICATIONS

## 5720 PC MOUSE CONTROLLER CHIP

NEW

The 5720 is a low power CMOS circuit providing complete Mouse interface control for PC applications.

***Features***

- 100% *Microsoft®** software compatible
- Address decoding for:
  - —Serial port—COM1, COM2, disable
  - —Parallel port—LPT1, LPT2, LPT3,disable
  - —Floppy disc controller IC
- Delayed read/write signal generation
- Control for expansion bus data buffers
- Interrupt multiplexing for serial port, parallel port and floppy disc controller
- Single wait state generator
- External device select (disableable)
- Floppy drive controller DRQ delay
- Available in 68 pin PLCC package

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## 6500/1 ONE CHIP MICROCOMPUTER

The 6500/1 is a complete high-performance 8-bit microcomputer on a single chip, and is totally upward/downward software compatible with all members of the 6500 family.

***Features***

- 6502 CPU
- 2048 x 8 mask programmable ROM
- 64 x 8 static RAM
- 16 bit programmable counterlatch with four operating modes:
  - — Interval timer — Event Counter
  - — Pulse Generator — Pulse Width Measurement
- Separate power pin for RAM
- 32 bi-directional TTL compatible I/O lines (4 ports)
- Counter I/O line with asynchronous input mode
- Five Interrupts:
  - — Reset — Two external edge sensitive
  - — Non-maskable — Counter overflow
- 1 to 3 MHz internal clock frequency
- 1 of 3 frequency references
  - — Crystal — Clock — RC

## 6551 ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

The 6551 is an Asychronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems.

***Features***

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths, number of stop bits, and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: odd, even, none, mark, space .
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.
- 1, 2, and 3 MHz operation

*Microsoft is a registered trademark of Microsoft Corporation.


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# SPECIAL APPLICATIONS

## 6582 SOUND INTERFACE DEVICE (SID)

The 6582 Sound Interface Device (SID) is a sound generator chip compatible with the 6500/8500 microprocessor families.

### *Features*

- 3 Tone Oscillators
  Range: 0-4 kHz
- 4 Waveforms per Oscillator
  Triangle, Sawtooth,
  Variable Pulse, Noise
- 3 Amplitude Modulators
  Range: 48 dB
- Random Number/Modulation Generator
- 3 Envelope Generators
  Exponential response
  Attack Rate: 2mS-8S
  Decay Rate: 6mS-24S
  Sustain Level: 0-peak volume
  Release Rate: 6mS-24S
- Oscillator Synchronization
- Ring Modulation
- Programmable Filter
  Cutoff range: 30 Hz-12 kHz
  12 dB/octave Rolloff
  Low pass, Band pass,
  High pass, Notch outputs
  Variable Resonance
- Master Volume Control
- 2 A/D POT Interfaces
- External Audio Input

# STATIC READ ONLY MEMORY

### *Description*

Commodore offers a variety of high performance ROMs with a wide range of access times providing compatibility with most microprocessor systems. The ROMs are TTL compatible, having a single +5 volt power supply and totally static operation.

The 2400 series "Power Down" ROMs offer significantly reduced power consumption while in stand-by mode. Each device has programmable chip select and/or output enable for output bus control and is designed to replace equivalent EPROMs.

### *Available ROMS*

| Device | Organization Words x Bits | Address Access Time (ns) | CE Access Time (ns) | CS/OE Access Time (ns) | Operating Current (Max) | Standby Current (Max) | Process Technology |
|---|---|---|---|---|---|---|---|
| 2332/3 | 4096x8 | 200 | N/A | 75 | 100 mA | N/A | HMOS |
| 2364 | 8192x8 | 250 | N/A | 100 | 100 mA | N/A | HMOS |
| 23128 | 16384x8 | 250 | N/A | 100 | 100 mA | N/A | HMOS |
| 24128 | 16384x8 | 250 | 250 | 100 | 100 mA | 12 mA | HMOS |
| 24256 | 32768x8 | 250 | 250 | 100 | 100 mA | 12 mA | HMOS |
| 24512 | 65536x8 | 250 | 250 | 100 | 100 mA | 12 mA | HMOS |
| 24C128 | 16384x8 | 250 | 250 | 100 | 10 mA | 50 µA | CMOS |
| 24C256 | 32768x8 | 250 | 250 | 100 | 10 mA | 50 µA | CMOS |

### *Packaging*

Available in standard plastic 24/28 pin dual-in-line packages.

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# MICROPROCESSORS

## Description

The 6500/8500 Series family includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors within the group are bus compatible with the M6800 product offering.

The family includes ten microprocessors with on-board clock oscillators and seven microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory.

## Available Microprocessors

| Device | *Clocks | Pins | IRQ | NMI | RDY | Port | Address | AEC | Sync | Speed (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|
| 6502 | O | 40 | X | X | X | — | 64K | — | X | 1,2,3,4 |
| 6503 | O | 28 | X | X | — | — | 4K | — | — | 1,2,3,4 |
| 6504 | O | 28 | X | — | — | — | 8K | — | — | 1,2,3,4 |
| 6505 | O | 28 | X | — | X | — | 4K | — | — | 1,2,3,4 |
| 6506 | O | 28 | X | — | — | — | 4K | — | — | 1,2,3,4 |
| 6507 | O | 28 | — | — | X | — | 8K | — | — | 1,2,3,4 |
| 6508 | E | 40 | X | — | — | 8 | 64K | X | — | 1,2,3 |
| 6509 | E | 40 | X | X | X | ** | 1 MEG | X | X | 1,2,3 |
| 6510 | O,E | 40 | X | X | X | 6,8 | 64K | X | — | 1,2,3,4 |
| 6512 | E | 40 | X | X | X | — | 64K | — | X | 1,2,3,4 |
| 6513 | E | 28 | X | X | — | — | 4K | — | — | 1,2,3,4 |
| 6514 | E | 28 | X | — | — | — | 8K | — | — | 1,2,3,4 |
| 6515 | E | 28 | X | — | X | — | 4K | — | — | 1,2,3,4 |
| 8501 | O | 40 | X | — | X | 7 | 64K | X | — | 1,2,3 |
| 8502 | O | 40 | X | X | X | 7 | 64K | X | — | 1,2,3,4 |
| 8503 | O | 40 | X | — | — | 8 | 64K | X | — | 1,2,3,4 |

*O — On chip clocks, E — External Clocks

**Four extended address pins expand memory capacity to one megabyte.

## Features of the 6500/8500 Family

- Single +5 volt supply
- 56 Instructions
- Decimal and binary arithmetic
- True indexing capability
- 8 bit Bi-directional Data Bus
- Variable length stack
- Programmable stack pointer
- Use with any type or speed memory
- N channel, silicon gate, depletion load technology
- Thirteen addressing modes
- Tri-state address bus, data, bus, and R/W controlled by AEC input.
- Eight bit parallel processing
- Direct memory access capability
- "Ready" input (for single cycle execution)

## Packaging

Available in standard plastic dual-in-line packages.




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# PERIPHERAL INTERFACE DEVICES

## *Description*

Commodore offers a wide assortment of peripheral interface devices compatible with the 6500/8500 microprocessor family. These devices were specifically designed to simplify the implementation of Input/Output control in microprocessor systems. All of the devices are TTL compatible, have a single +5 volt supply, and are based on N-channel depletion load technology. Each device features from 8 to 24 individually programmable I/O lines. Additional functions on selected devices include handshaking capability, control/interrupt input lines, interrupt output, serial I/O, timers, counters, RAM, and ROM.

## *Available Peripheral Devices*

| Device | Pins | 8-bit Ports | IRQ | Hand-shaking (Port) | Control/ Interrupt Input Lines | Darling-ton Drive | Serial I/O | Timers | Timer/ Counters | RAM | ROM | Speed MHz |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6522 | 40 | 2 | X | Read A Write A, B | 4/4 | Port B, CB1, CB2 | X | One 16 bit | One 16 bit | — | — | 1, 2 |
| 6525 | 40 | 3** | X | Read A Write B | 2/5 | — | — | — | — | — | — | *** |
| 6526* | 40 | 2 | X | Read B Write B | 2/1 | — | X | — | Two 16 bit | — | — | 1, 2, 3 |
| 6529 | 20 | 1 | — | — | — | — | — | — | — | — | — | *** |
| 6530 | 40 | 2 | X | — | — | Port A, B | — | One 8 bit | — | 64x8 | 1024x8 | 1, 2 |
| 6532 | 40 | 2 | X | — | — | Port B | — | One 8 bit | — | 128x8 | — | 1, 2 |

* Note: Supports Time of Day Clock function.
** Note: 2 ports if using control/interrupt lines.
*** Note: These devices are not clocked. Speed is determined by access time.

## *Packaging*

Available in standard plastic dual-in-line packages.



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# VIDEO DISPLAY DEVICES

## Description

Commodore's family of Video Controllers offers attractive integration of all video logic necessary for color video graphics and text applications, such as low cost CRT terminals, industrial monitors, control system displays and home video games. Complete logic to implement all format timing, memory interface, attribute control, row buffering and high-speed shifting of pixel data are resident in each device.

The family of VIC II and TED devices provide fixed format display with 5 separate character/bit-map modes of operation. A Raster Compare Interrupt allows the easy mixing of these modes for display of high-res graphics with text. A transparent scheme of using PhO time for fetching video data from memory allows for optimal CPU thruput. The VICs also contain a special type of display image, Movable Image Block (MIB), that once defined, can be moved to any screen position without the inherent character cell constraints.

The programmable 8563/68 features digital RGBI output for very sharp 640V x 400H color video. Direct video memory interface to 64K of DRAM requires no external logic.

## Available Video Devices

| Part No. | Display Format | Display Modes | Video Output | Features | Memory Interface | Pins | Supply |
|---|---|---|---|---|---|---|---|
| **VIC** | | | | | | | |
| 6560 (NTSC)<br>6561 (PALB) | programmable up to 24col/ 25rows 192H x 200V | 2 character modes: Hi-Res Multi-color | 16 color composite | on chip sound system, 2 8-bit A/D converters, interlace/non-interlace, light pen input | access 16K, transparent DMA | 40 | +5 |
| **VIC II** | | | | | | | |
| 6567 (NTSC)<br>6569 (PALB)<br>6572 (PALN)<br>6573 (PALM) | 40col/25row text 320H x 200V bit-map | 3 character modes: Standard Multicolor, Extended color. 2 bit-map modes: Hi-Res Multi-color | 16 color composite | 8 MIB's (sprites), horz and vert scrolling, light pen input, Raster Compare Interrupt | access 16K, interface to multiplexed DRAM, transparent DMA, provides system RAS and CAS | 40 | +5, +12<br>—<br>+5 |
| 8562 (NTSC)<br>8565 (PALB) | | | | | | | |
| **VIC IIE** | | | | | | | |
| 8564 (NTSC)<br>8566 (PALB)<br>8569 (PALN) | same as above | same as above | same as above | above, plus ... Keyboard Control Register, 2 MHz clock, true external DMA and arbitration control | same as above | 48 | +5 |
| **TED** | | | | | | | |
| 8360 (NTSC/ PALB)<br>8365 (PALN)<br>8366 (PALM) | same as above | same as above | 121 color composite | 2 voice sound, 8-bit keyport control, Clk doubling, horz & vert scroll, Raster Compare and 3 timer generated interrupts, hardware cursor, blink and reverse video attributes | access 64K, transparent DMA, provides system RAS, CAS and MUX | 48 | +5 |
| **DVDC** | | | | | | | |
| 8563 | programmable text up to 80 col/25row bitmap 640H x 400V | 3 char. modes: Std., semi-graph, and pixel double width 1 Hi-Res bit-map mode | digital RGBI 16 color or 16 gray-shades | interlace/noninterlace, horz and vert scroll, lightpen input, 80col dbl line buffer, hardware cursor, underline, blink and reverse video, supports 2 character sets of 256 each | access 64K, programmable to interface to either 4164 or 4416 DRAM | 48 | +5 |
| 8568 | | | | above, plus ... Update Ready Interrupt, composite video, and composite sync | | | |
| **CRTC** | | | | | | | |
| 6545-1 | programmable controller | — | — | programmable cursor lightpen input | access 16K, straight binary or row/column | 40 | +5 |

## Packaging

Available in standard plastic Dual-In-Line packages.

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# CMOS Fast Static RAMs

CYPRESS SEMICONDUCTOR

## Features

- **CMOS for optimum speed/power**
- **High speed**
- **Low power**
- **TTL compatible inputs and outputs**
- **5 volt power supply ±10% tolerance both commercial and military**
- **Very broad product line**

## Functional Description

Cypress Static RAMs offer high speed performance with CMOS power savings. A 0.8 micron channel length and lightly doped source and drain regions result in the fastest access times available. TTL conversion circuits provide full TTL compatibility. Latch-up is eliminated by utilizing guard rings and a substrate bias generator. Proprietary input circuitry guarantees electrostatic discharge protection of greater than 2000V.

Cypress RAMs are available in both plastic and ceramic DIP packages at commercial and military temperature ranges.

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ±10% |
| Military | −55°C to +125°C | |

## Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current, into Outputs (Low) ..... 20 mA

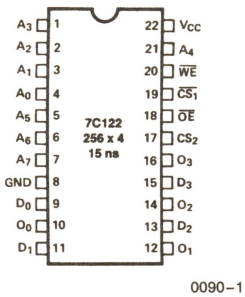
## Electrical Characteristics over the operating range

| Parameters | Description | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage[1] | $V_{CC}$ = Min. | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | −3.0 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | −10 | +10 | μA |

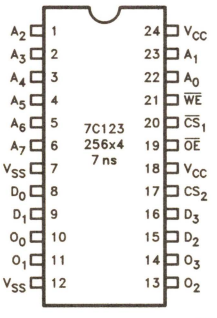
**Note:**

1. CY7C189/90 has a $V_{OL}$ of 0.45V max.

## Pin Configurations




0090-1

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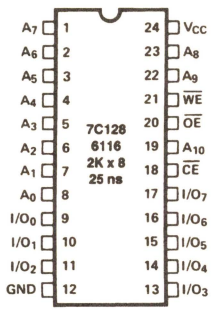


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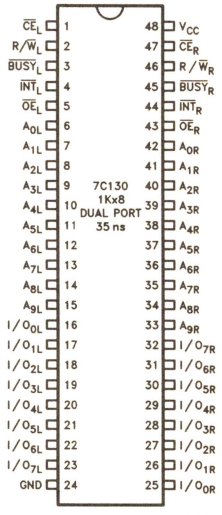


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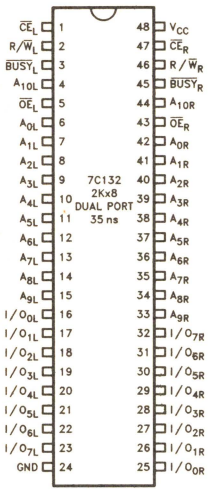
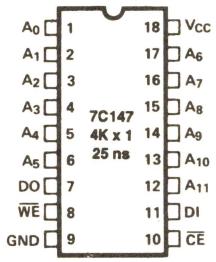
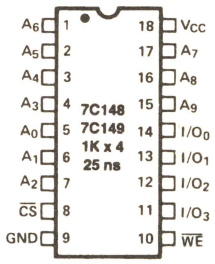
## Pin Configurations (Continued)




0090-5




0090-6

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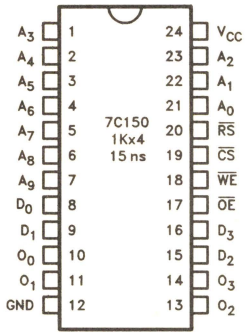


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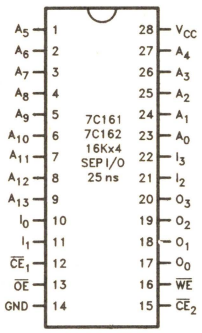


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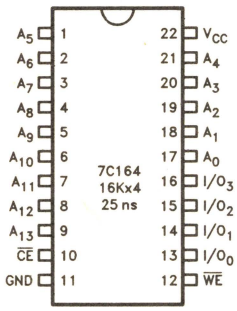


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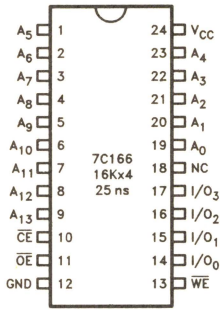


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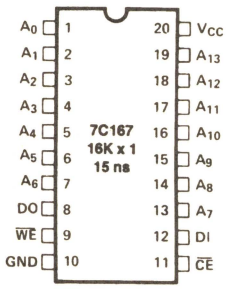


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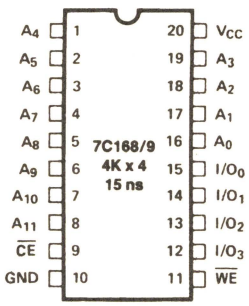


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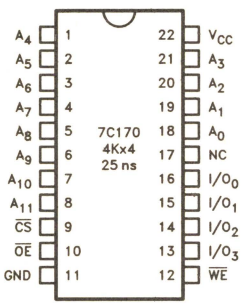


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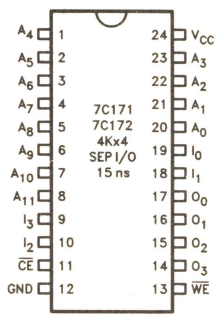


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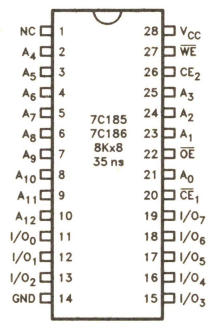


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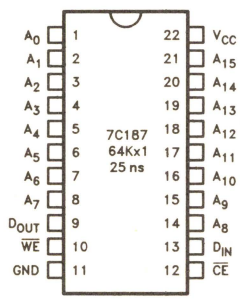


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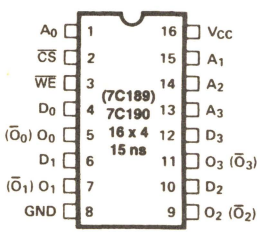


0090-18



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## Selector Guide

**Sorted by decreasing word depth.**

| | | | | | | | | Read Cycle | | | | | | | | Write Cycle | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | PINs | Commercial Power Supply Current | Military Power Supply Current | Commercial Power Down Current | Military Power Down Current | Address Access Time | Chip Select to Data Valid (Max.) | Chip Select Inactive to Output High Z (Max.) | Chip Select Active to Power Up (Min.) | Chip Select Inactive to Power Down (Max.) | Output Enable Active to Data Valid (Max.) | Output Enable Inactive to Output High Z (Max.) | Data Hold from Address Change (Min.) | Address Setup to Write Start (Min.) | Address Hold from Write End (Min.) | Data Setup to Write Start (Min.) | Data Hold from Write End (Min.) | Write Enable Pulse Width (Min.) | Write Enable Active to Output High Z (Max.) | Write Enable Inactive to Low Z (Min.) |
| Part No. | Speed (ns) | Organization | | $I_{CC}$ | $I_{CC}$ | $I_{SB}$ | $I_{SB}$ | $t_{AA}$ | $t_{ACS}$ | $t_{HZCS}$ | $t_{PU}$ | $t_{PD}$ | $t_{DOE}$ | $t_{HZOE}$ | $t_{OHA}$ | $t_{SA}$ | $t_{HA}$ | $t_{SD}$ | $t_{HD}$ | $t_{PWE}$ | $t_{HZWE}$ | $t_{LZWE}$ |
| | | | | mA | mA | mA | mA | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns |
| CY7C187* | 25 | 65,536x1 | 22 | 70 | NA | 20 | NA | 25 | 25 | 15 | 0 | 25 | NA | NA | 3 | 0 | 2 | 20 | 0 | 20 | 15 | 0 |
| | 35 | | | 70 | 70 | 20 | 20 | 35 | 35 | 20 | 0 | 25 | NA | NA | 3 | 0 | 2 | 25 | 0 | 25 | 20 | 0 |
| | 45 | | | 50 | 70 | 20 | 20 | 45 | 45 | 20 | 0 | 30 | NA | NA | 3 | 0 | 2 | 25 | 0 | 25 | 20 | 0 |
| CY7C161* | 25 | 16,384x4 Separate I/O XWR | 28 | 70 | NA | 20 | NA | 25 | 25 | 15 | 0 | 25 | 15 | 15 | 3 | 0 | 2 | 15 | 0 | 15 | NA | NA |
| | 35 | | | 70 | 70 | 20 | 20 | 35 | 35 | 15 | 0 | 25 | 25 | 15 | 3 | 0 | 2 | 20 | 0 | 20 | NA | NA |
| | 45 | | | 50 | 70 | 20 | 20 | 45 | 45 | 15 | 0 | 30 | 30 | 15 | 3 | 0 | 2 | 20 | 0 | 20 | NA | NA |
| CY7C162* | 25 | 16,384x4 Separate I/O | 28 | 70 | NA | 20 | NA | 25 | 25 | 15 | 0 | 25 | 15 | 15 | 3 | 0 | 2 | 15 | 0 | 15 | 10 | 0 |
| | 35 | | | 70 | 70 | 20 | 20 | 35 | 35 | 15 | 0 | 25 | 25 | 15 | 3 | 0 | 2 | 20 | 0 | 20 | 15 | 0 |
| | 45 | | | 50 | 70 | 20 | 20 | 45 | 45 | 15 | 0 | 30 | 30 | 15 | 3 | 0 | 2 | 20 | 0 | 20 | 20 | 0 |
| CY7C164* | 25 | 16,384x4 | 22 | 70 | NA | 20 | NA | 25 | 25 | 15 | 0 | 25 | NA | NA | 3 | 0 | 2 | 10 | 0 | 20 | 10 | 3 |
| | 35 | | | 70 | 70 | 20 | 20 | 35 | 35 | 15 | 0 | 25 | NA | NA | 3 | 0 | 2 | 15 | 0 | 20 | 15 | 3 |
| | 45 | | | 50 | 70 | 20 | 20 | 45 | 45 | 15 | 0 | 30 | NA | NA | 3 | 0 | 2 | 20 | 0 | 35 | 15 | 3 |
| CY7C166* | 25 | 16,384x4 Output Enable | 24 | 70 | NA | 20 | NA | 25 | 25 | 15 | 0 | 25 | 15 | 15 | 3 | 0 | 2 | 10 | 0 | 20 | 10 | 3 |
| | 35 | | | 70 | 70 | 20 | 20 | 35 | 35 | 15 | 0 | 25 | 25 | 15 | 3 | 0 | 2 | 15 | 0 | 20 | 15 | 3 |
| | 45 | | | 50 | 70 | 20 | 20 | 45 | 45 | 15 | 0 | 30 | 30 | 15 | 3 | 0 | 2 | 20 | 0 | 35 | 15 | 3 |
| CY7C167 | 15* | 16,384x1 | 20 | 80 | NA | 20 | NA | 15 | 15 | 12 | 0 | 15 | NA | NA | 3 | 0 | 2 | 10 | 0 | 13 | 12 | 0 |
| | 25L | | | 45 | 60 | 15 | 20 | 25 | 25 | 15 | 0 | 20 | NA | NA | 3 | 0 | 0 | 15 | 0 | 15 | 15 | 0 |
| | 35L | | | 45 | 60 | 15 | 20 | 35 | 35 | 20 | 0 | 25 | NA | NA | 3 | 0 | 0 | 15 | 0 | 20 | 20 | 0 |
| | 45 | | | 50 | 50 | 15 | 20 | 45 | 45 | 25 | 0 | 30 | NA | NA | 3 | 0 | 0 | 15 | 0 | 20 | 20 | 0 |
| CY7C185 CY7C186* | 35 | 8192x8 300/600 mil Pkg | 28 | 100 | NA | 20 | NA | 35 | 35 | 15 | 0 | 20 | 15 | 20 | 3 | 0 | 2 | 15 | 0 | 20 | 15 | 0 |
| | 45 | | | 100 | 100 | 20 | 20 | 45 | 45 | 20 | 0 | 25 | 20 | 25 | 3 | 0 | 2 | 20 | 0 | 25 | 20 | 0 |
| | 55 | | | 80 | 100 | 20 | 20 | 55 | 55 | 20 | 0 | 25 | 25 | 30 | 3 | 0 | 2 | 25 | 0 | 30 | 20 | 0 |
| CY7C168 | 15* | 4096x4 Power Down | 20 | 120 | NA | 20 | NA | 15 | 15 | 12 | 0 | 15 | NA | NA | 3 | 0 | 2 | 7 | 0 | 13 | 6 | 3 |
| | 25L | | | 70 | 90 | 15 | 20 | 25 | 25 | 15 | 0 | 25 | NA | NA | 3 | 0 | 0 | 10 | 0 | 20 | 10 | 6 |
| | 35L | | | 70 | 90 | 15 | 20 | 35 | 35 | 20 | 0 | 25 | NA | NA | 3 | 0 | 0 | 15 | 0 | 30 | 15 | 6 |
| | 45 | | | 70 | 70 | 15 | 20 | 45 | 45 | 25 | 0 | 30 | NA | NA | 3 | 0 | 0 | 15 | 3 | 35 | 20 | 6 |
| CY7C169 | 15* | 4096x4 Fast CE | 20 | 120 | NA | NA | NA | 15 | 12 | 12 | NA | NA | NA | NA | 3 | 0 | 2 | 7 | 0 | 13 | 6 | 3 |
| | 25L | | | 70 | 90 | NA | NA | 25 | 15 | 15 | NA | NA | NA | NA | 3 | 0 | 0 | 10 | 0 | 20 | 10 | 6 |
| | 35L | | | 70 | 90 | NA | NA | 35 | 25 | 20 | NA | NA | NA | NA | 3 | 0 | 0 | 15 | 0 | 30 | 15 | 6 |
| | 40 | | | 70 | 70 | NA | NA | 40 | 25 | 20 | NA | NA | NA | NA | 3 | 0 | 0 | 15 | 3 | 35 | 20 | 6 |
| CY7C170 | 25 | 4096x4 Output Enable | 22 | 90 | NA | NA | NA | 25 | 15 | 15 | NA | NA | 15 | 15 | 3 | 0 | 0 | 10 | 0 | 20 | 10 | 6 |
| | 35 | | | 90 | 120 | NA | NA | 35 | 25 | 20 | NA | NA | 15 | 15 | 3 | 0 | 0 | 15 | 0 | 30 | 15 | 6 |
| | 45 | | | 90 | 120 | NA | NA | 45 | 30 | 25 | NA | NA | 20 | 15 | 3 | 0 | 0 | 15 | 3 | 35 | 20 | 6 |
| CY7C171 | 15* | 4096x4 Separate I/O XWR | 24 | 120 | NA | 20 | NA | 15 | 15 | 12 | 0 | 15 | NA | NA | 3 | 0 | 2 | 7 | 0 | 13 | NA | NA |
| | 25L | | | 70 | 90 | 15 | 20 | 25 | 25 | 15 | 0 | 25 | NA | NA | 3 | 0 | 0 | 10 | 0 | 20 | NA | NA |
| | 35L | | | 70 | 90 | 15 | 20 | 35 | 35 | 20 | 0 | 25 | NA | NA | 3 | 0 | 0 | 15 | 0 | 25 | NA | NA |
| | 45 | | | 70 | 70 | 15 | 20 | 45 | 45 | 20 | 0 | 30 | NA | NA | 3 | 0 | 0 | 15 | 3 | 30 | NA | NA |

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## Selector Guide

**Sorted by decreasing word depth.** (Continued)

| | | | | | | | | Read Cycle | | | | | | | | Write Cycle | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | PINs | Commercial Power Supply Current | Military Power Supply Current | Commercial Power Down Current | Military Power Down Current | Address Access Time | Chip Select to Data Valid (Max.) | Chip Select Inactive to Output High Z (Max.) | Chip Select Active to Power Up (Min.) | Chip Select Inactive to Power Down (Max.) | Output Enable Active to Data Valid (Max.) | Output Enable Inactive to Output High Z (Max.) | Data Hold from Address Change (Min.) | Address Setup to Write Start (Min.) | Address Hold from Write End (Min.) | Data Setup to Write Start (Min.) | Data Hold from Write End (Min.) | Write Enable Pulse Width (Min.) | Write Enable Active to Output High Z (Max.) | Write Enable Inactive to Low Z (Min.) |
| **Part No.** | **Speed (ns)** | **Organization** | | $I_{CC}$ | $I_{CC}$ | $I_{SB}$ | $I_{SB}$ | $t_{AA}$ | $t_{ACS}$ | $t_{HZCS}$ | $t_{PU}$ | $t_{PD}$ | $t_{DOE}$ | $t_{HZOE}$ | $t_{OHA}$ | $t_{SA}$ | $t_{HA}$ | $t_{SD}$ | $t_{HD}$ | $t_{PWE}$ | $t_{HZWE}$ | $t_{LZWE}$ |
| | | | | mA | mA | mA | mA | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns | ns |
| CY7C172 | 15* | 4096x4 Separate I/O | 24 | 120 | NA | 20 | NA | 15 | 15 | 12 | 0 | 15 | NA | NA | 3 | 0 | 2 | 7 | 0 | 13 | 6 | 0 |
| | 25L | | | 70 | 90 | 15 | 20 | 25 | 25 | 15 | 0 | 25 | NA | NA | 3 | 0 | 0 | 10 | 0 | 20 | 10 | 0 |
| | 35L | | | 70 | 90 | 15 | 20 | 35 | 35 | 20 | 0 | 25 | NA | NA | 3 | 0 | 0 | 15 | 0 | 25 | 50 | 0 |
| | 45 | | | 70 | 70 | 15 | 20 | 45 | 45 | 20 | 0 | 30 | NA | NA | 3 | 0 | 0 | 15 | 3 | 30 | 20 | 0 |
| CY7C147 | 25 | 4096x1 | 18 | 90 | NA | 15 | NA | 25 | 25 | 20 | 0 | 20 | NA | NA | 5 | 0 | 0 | 15 | 0 | 15 | 15 | 0 |
| | 35 | | | 80 | 110 | 10 | 10 | 35 | 35 | 30 | 0 | 20 | NA | NA | 5 | 0 | 0 | 20 | 10 | 20 | 20 | 0 |
| | 45 | | | 80 | 110 | 10 | 10 | 45 | 45 | 30 | 0 | 20 | NA | NA | 5 | 0 | 0 | 25 | 10 | 25 | 25 | 0 |
| CY7C132* CY7C142 | 35 | 2048x8 Dual Port | 48 | 120 | NA | 30 | NA | 35 | 35 | 15 | 0 | 20 | 15 | 15 | 5 | 0 | 2 | 15 | 0 | 20 | 15 | 0 |
| | 45 | | | 120 | 150 | 30 | 40 | 45 | 45 | 20 | 0 | 25 | 20 | 20 | 5 | 0 | 2 | 20 | 0 | 20 | 20 | 0 |
| | 55 | | | 120 | 150 | 30 | 40 | 55 | 55 | 25 | 0 | 30 | 25 | 25 | 5 | 0 | 2 | 25 | 0 | 25 | 25 | 0 |
| CY7C128/ CY6116 | 25* | 2048x8 300/600 mil Pkg | 24 | 120 | NA | 20 | NA | 25 | 25 | 15 | 0 | 20 | 15 | 15 | 3 | 0 | 0 | 10 | 0 | 20 | 10 | 0 |
| | 35 | | | 120 | 150 | 20 | 20 | 35 | 35 | 15 | 0 | 20 | 15 | 15 | 5 | 0 | 0 | 15 | 0 | 20 | 15 | 0 |
| | 45 | | | 120 | 130 | 20 | 20 | 45 | 45 | 20 | 0 | 25 | 20 | 15 | 5 | 0 | 0 | 20 | 0 | 20 | 15 | 0 |
| | 55 | | | 90 | 100 | 20 | 20 | 55 | 55 | 20 | 0 | 25 | 25 | 20 | 5 | 0 | 0 | 25 | 0 | 25 | 20 | 0 |
| CY7C130* CY7C140 | 35 | 1024x8 Dual Port | 48 | 120 | NA | 30 | NA | 35 | 35 | 15 | 0 | 20 | 15 | 15 | 5 | 0 | 2 | 15 | 0 | 20 | 15 | 0 |
| | 45 | | | 120 | 150 | 30 | 40 | 45 | 45 | 20 | 0 | 25 | 20 | 20 | 5 | 0 | 2 | 20 | 0 | 20 | 20 | 0 |
| | 55 | | | 120 | 150 | 30 | 40 | 55 | 55 | 25 | 0 | 30 | 25 | 25 | 5 | 0 | 2 | 25 | 0 | 25 | 25 | 0 |
| CY7C148 | 25 | 1024x4 Power Down | 18 | 90 | NA | 15 | NA | 25 | 25 | 15 | 0 | 20 | NA | NA | 0 | 0 | 5 | 12 | 0 | 20 | 8 | 0 |
| | 35 | | | 80 | 110 | 10 | 10 | 35 | 35 | 20 | 0 | 30 | NA | NA | 0 | 0 | 5 | 20 | 0 | 30 | 10 | 0 |
| | 45 | | | 80 | 110 | 10 | 10 | 45 | 45 | 20 | 0 | 30 | NA | NA | 5 | 0 | 5 | 20 | 0 | 35 | 15 | 0 |
| CY7C149 | 25 | 1024x4 Fast CS | 18 | 90 | NA | NA | NA | 25 | 15 | 15 | NA | NA | NA | NA | 0 | 0 | 5 | 12 | 0 | 20 | 8 | 0 |
| | 35 | | | 80 | 110 | NA | NA | 35 | 15 | 20 | NA | NA | NA | NA | 0 | 0 | 5 | 20 | 0 | 30 | 10 | 0 |
| | 45 | | | 80 | 110 | NA | NA | 45 | 20 | 20 | NA | NA | NA | NA | 5 | 0 | 5 | 20 | 0 | 35 | 15 | 0 |
| CY7C150 | 12* | 1024x4 Separate I/O | 24 | 90 | NA | NA | NA | 12 | 10 | 8 | NA | NA | 8 | 8 | 2 | 2 | 2 | 9 | 9 | 9 | 8 | 0 |
| | 15 | | | 90 | NA | NA | NA | 15 | 12 | 11 | NA | NA | 10 | 9 | 2 | 2 | 2 | 11 | 2 | 11 | 12 | 0 |
| | 25 | | | 90 | 100 | NA | NA | 25 | 15 | 20 | NA | NA | 15 | 20 | 2 | 5 | 5 | 15 | 5 | 15 | 20 | 0 |
| | 35 | | | 90 | 100 | NA | NA | 35 | 20 | 25 | NA | NA | 20 | 25 | 2 | 5 | 5 | 20 | 5 | 20 | 25 | 0 |
| CY7C123* | 7 | 256x4 Separate I/O | 24 | 120 | NA | NA | NA | 7 | 7 | 5 | NA | NA | 7 | 5 | NA | 0 | 3 | 5 | 2 | 5 | 5 | 2 |
| | 12 | | | 120 | NA | NA | NA | 12 | 8 | 10 | NA | NA | 8 | 10 | NA | 0 | 3 | 9 | 2 | 9 | 10 | 2 |
| | 15 | | | 120 | 150 | NA | NA | 15 | 10 | 12 | NA | NA | 10 | 12 | NA | 2 | 4 | 11 | 2 | 11 | 12 | 2 |
| CY7C122 | 15 | 256x4 Separate I/O | 22 | 90 | NA | NA | NA | 15 | 8 | 12 | NA | NA | 8 | 12 | NA | 0 | 4 | NA | 2 | 11 | 12 | NA |
| | 25 | | | 60 | 90 | NA | NA | 25 | 15 | 25 | NA | NA | 15 | 20 | NA | 5 | 5 | NA | 5 | 15 | 20 | NA |
| | 35 | | | 60 | 90 | NA | NA | 35 | 25 | 25 | NA | NA | 25 | 30 | NA | 10 | 5 | NA | 5 | 25 | 30 | NA |
| CY7C189 | 15 | 64x4 Separate I/O Inverting Outputs | 16 | 90 | NA | NA | NA | 15 | 12 | 12 | NA | NA | NA | NA | 5 | 0 | 0 | 15 | 0 | 11 | 15 | 12 |
| | 25 | | | 55 | 70 | NA | NA | 25 | 15 | 15 | NA | NA | NA | NA | 5 | 0 | 0 | 20 | 0 | 15 | 20 | 20 |
| CY27LS03 | 65 | | | NA | 38 | NA | NA | 65 | 65 | 35 | NA | NA | NA | NA | NA | 0 | 0 | 55 | 0 | 55 | 35 | NA |
| CY7C190 | 15 | 64x4 Separate I/O | 16 | 90 | NA | NA | NA | 15 | 12 | 12 | NA | NA | NA | NA | 5 | 0 | 0 | 15 | 0 | 11 | 15 | 12 |
| | 25 | | | 55 | 70 | NA | NA | 25 | 15 | 15 | NA | NA | NA | NA | 5 | 0 | 0 | 20 | 0 | 15 | 20 | 20 |

*Preliminary

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# CMOS High Speed PROMs

CYPRESS SEMICONDUCTOR

## Features

- **CMOS for optimum speed/power**
- **High speed (25 ns 7C291, 7C292)**
- **Low power (1/2 Bipolar)**
- **Reprogrammable (7C245, 7C251, 7C254, 7C261, 7C263, 7C264, 7C268, 7C269, 7C271, 7C291, 7C291A, 7C292A and 7C293A)**
- **10% power supply**
- **TTL compatible**
- **100% tested**

## Product Characteristics

Cypress has blended 1.2 micron and floating gate technologies to produce a line of the fastest, lowest power PROMs in the world. Floating gate technology allows reprogrammability by the user and 100% testing at the factory. The 7C245, 7C245A, 7C251, 7C254, 7C261, 7C263, 7C264, 7C268, 7C269, 7C271, 7C291, 7C291A, 7C292A and 7C293A feature optional windows for reprogrammability by the user.

Cypress PROMs are offered in registered, registered diagnostic, and non-registered versions in a variety of packages including 300 mil DIP, LCC and PLCC.

CMOS PROMs offer advantages in reliability such as 2000 volt ESD protection on all pins, 10% power supplies, low power dissipation and latchup protection.

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to 70°C | 5V ± 10% |
| Military | −55°C to +125°C | |

## Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55° to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

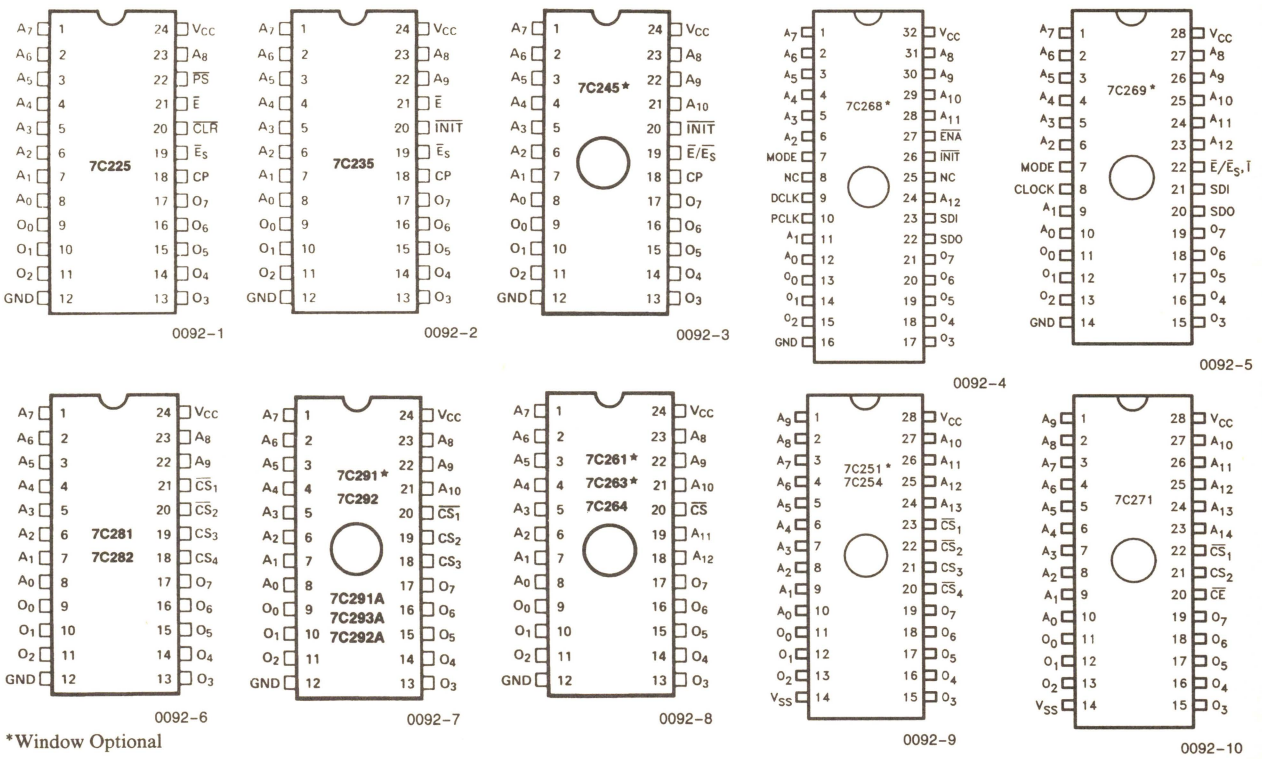
Output Current, into Outputs (Low) ..... 20 mA

DC Program Voltage ..... 14.0V

Static Discharge Voltage ..... >2001V

Latch-up Current ..... >200 mA

## Pin Configurations




*Window Optional

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**October 1987**

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## Electrical Characteristics Over the Operating Range

| Parameters | Description | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $GND \le V_I \le V_{CC}$ | −10 | +10 | μA |

## Selector Guide

**Sorted by decreasing word depth.**

| | | | | | | | | | Registered | | | | | | Non-Registered | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | PINs | Commercial Power Supply Current | Military Power Supply Current | Commercial Power Down Current* | Military Power Down Current* | Address Setup To Clock HIGH (Min.) | Address Hold From Clock HIGH (Min.) | Clock HIGH To Valid Output (Max.) | Clock Pulse Width (Min.) | Active Output From Clock HIGH (Max.) | Inactive Output From Clock HIGH (Max.) | Address To Output Valid (Max.) | Chip Select Inactive To High Z (Max.) | Chip Select Active To Output Valid (Max.) |
| Part No. | Speed (ns) | Organization | | $I_{CC}$ | $I_{CC}$ | $I_{SB}$ | $I_{SB}$ | $t_{SA}$ | $t_{HA}$ | $t_{CO}$ | $t_{PWC}$ | $t_{LZC}$ | $t_{HZC}$ | $t_{TAA}$ | $t_{HCS}$ | $t_{ACS}$ |
| | | | | mA | mA | mA | mA | ns | ns | ns | ns | ns | ns | ns | ns | ns |
| CY7C268† | 40 | 8192x8 Registered Diagnostic | 32/28 | 100 | NA | — | — | 40 | 0 | 20 | 20 | 20 | 20 | — | — | — |
| CY7C269 | 50 | | | 80 | 120 | — | — | 50 | 0 | 25 | 25 | 30 | 30 | — | — | — |
| | 60 | | | 80 | 100 | — | — | 60 | 0 | 30 | 30 | 35 | 35 | — | — | — |
| CY7C245 | 18 | 2048x8 Registered | 24 | 120 | NA | — | — | 18 | 0 | 12 | 12 | 15 | 15 | — | — | — |
| | 20 | | | 130 | NA | — | — | 20 | 0 | 12 | 15 | 15 | 15 | — | — | — |
| | 25 | | | 90 | NA | — | — | 25 | 0 | 12 | 15 | 15 | 15 | — | — | — |
| | 35 | | | 90 | 120 | — | — | 35 | 0 | 20 | 20 | 30 | 30 | — | — | — |
| | 45 | | | 120 | 120 | — | — | 45 | 0 | 25 | 20 | 30 | 30 | — | — | — |
| CY7C245L | 35 | 2048x8 Registered Low Power | 24 | 60 | NA | — | — | 35 | 0 | 20 | 20 | 30 | 30 | — | — | — |
| | 45 | | | 60 | NA | — | — | 45 | 0 | 25 | 20 | 30 | 30 | — | — | — |
| CY7C235 | 30 | 1024x8 Registered | 24 | 90 | NA | — | — | 30 | 0 | 15 | 15 | 20 | 20 | — | — | — |
| | 40 | | | 90 | 120 | — | — | 40 | 0 | 25 | 20 | 25 | 25 | — | — | — |
| CY7C225 | 25 | 512x8 Registered | 24 | 90 | NA | — | — | 25 | 0 | 12 | 10 | 20 | 20 | — | — | — |
| | 30 | | | 90 | 120 | — | — | 30 | 0 | 15 | 15 | 20 | 20 | — | — | — |
| | 35 | | | NA | 120 | — | — | 35 | 0 | 20 | 20 | 25 | 25 | — | — | — |
| | 40 | | | 90 | 120 | — | — | 40 | 0 | 25 | 20 | 30 | 25 | — | — | — |
| CY7C271* | 55 | 32,768x8 Power Down | 28 | 120 | NA | 30 | NA | — | — | — | — | — | — | 55 | 30 | 30 |
| | 65 | | | 120 | 130 | 30 | 35 | — | — | — | — | — | — | 65 | 35 | 35 |
| | 75 | | | NA | 130 | NA | 35 | — | — | — | — | — | — | 75 | 45 | 45 |
| CY7C251* | 45 | 16,384x8 Power Down* | 28 | 100 | NA | 20* | NA* | — | — | — | — | — | — | 45 | 45*/25 | 45*/25 |
| CY7C254† | 55 | | | 100 | 120 | 20* | 30* | — | — | — | — | — | — | 55 | 55*/30 | 55*/30 |
| | 65 | | | 100 | 120 | 20* | 30* | — | — | — | — | — | — | 65 | 65*/35 | 65*/35 |
| CY7C261* | 35 | 8192x8 Power Down* | 24 | 100 | NA | 20* | NA* | — | — | — | — | — | — | 35 | 35*/25 | 35*/20 |
| CY7C263 | 45 | | | 100 | 120 | 20* | 30* | — | — | — | — | — | — | 45 | 45*/30 | 45*/30 |
| CY7C264† | 55 | | | 100 | 120 | 20* | 30* | — | — | — | — | — | — | 55 | 55*/35 | 55*/35 |
| CY7C291 | 20 | 2048x8 Registered Power Down* | 24 | 120 | NA | 20* | NA* | — | — | — | — | — | — | 20 | 22*/15 | 22*/15 |
| | 25 | | | 130 | NA | — | — | — | — | — | — | — | — | 25 | 20 | 20 |
| CY7C292† | 30 | | | NA | 120 | NA* | 30* | — | — | — | — | — | — | 30 | 32*/20 | 32*/20 |
| CY7C293* | 35 | | | 90 | 120 | 20* | 30* | — | — | — | — | — | — | 35 | 35*/25 | 35*/25 |
| | 50 | | | 90 | 120 | 20* | 30* | — | — | — | — | — | — | 50 | 45*/25 | 45*/25 |
| CY7C291L | 35 | 2048x8 Low Power | 24 | 60 | NA | — | — | — | — | — | — | — | — | 35 | 25 | 25 |
| CY7C292L† | 50 | | | 60 | NA | — | — | — | — | — | — | — | — | 50 | 25 | 25 |
| CY7C281 | 30 | 1024x8 | 24 | 100 | NA | — | — | — | — | — | — | — | — | 30 | 20 | 20 |
| CY7C282† | 45 | | | 90 | 120 | — | — | — | — | — | — | — | — | 45 | 25 | 25 |

*Power Down †600 mil

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# CMOS Cascadeable FIFOs

CYPRESS SEMICONDUCTOR

## Features

- **CMOS for optimum speed/power**
- **Dual port RAM cell**
- **High speed: 15, 25, 35 MHz**
- **Fast, 50 ns bubblethrough**
- **Cascadeable**
- **Low power**
- **TTL compatible**
- **10% power supply**

## Functional Description

Cypress First-in First-out memories, FIFOs, combine 1.2 micron CMOS technology with a unique dual port architecture to provide the fastest and lowest power FIFOs available. Unlike traditional FIFOs these devices are designed using dual port memory, read and write pointers, and control logic. The conventional concept of bubble-through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propogate an Output Ready (OR) signal.

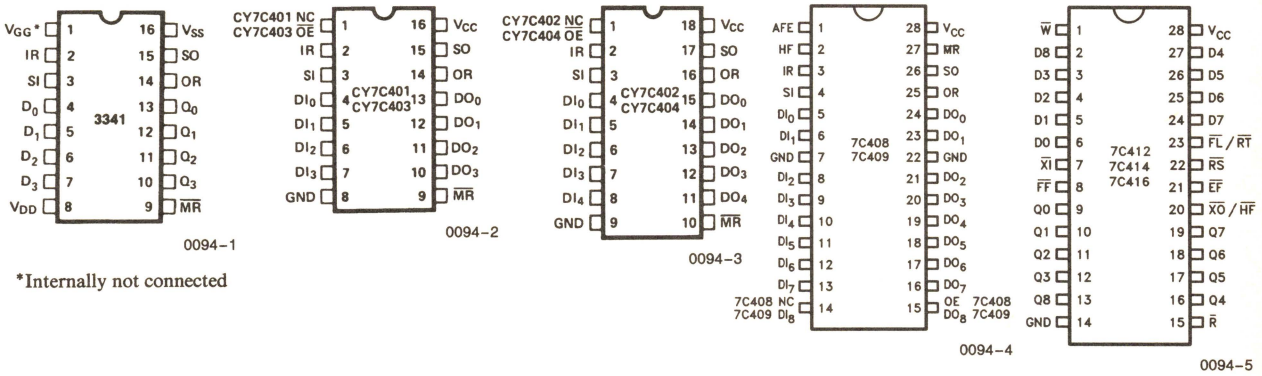
Other features of Cypress FIFOs include: cascadeability, power-on reset, independent asynchronous inputs and outputs, output enable (7C403, 7C404, 7C408), and latchup is prevented by careful layout, guard rings and a substrate bias generator.

## Selection Guide

| Part No. | Description | Temp. Range | Speed (MHz) | $I_{CC}$ (mA) |
|---|---|---|---|---|
| CY3341 | 64 x 4 FIFO Serial Memory | COMM/MIL | 1.2, 2 | 45/65 |
| CY7C401 | Cascadeable 64 x 4 FIFO | Commercial | 5, 10, 15 | 75 |
| | | Military | 10, 15 | 90 |
| CY7C402 | Cascadeable 64 x 5 FIFO | Commercial | 5, 10, 15 | 75 |
| | | Military | 10, 15 | 90 |
| CY7C403 | Cascadeable 64 x 4 FIFO with Output Enable | COMM/MIL | 10, 15, 25 | 75/90 |
| CY7C404 | Cascadeable 64 x 5 FIFO with Output Enable | COMM/MIL | 10, 15, 25 | 75/90 |
| CY7C408 | Cascadeable 64 x 8 FIFO with Output Enable | COMM/MIL | 15, 25, 35 | 100/120 |
| CY7C409 | Cascadeable 64 x 9 FIFO | COMM/MIL | 15, 25, 35 | 100/120 |
| CY7C412 | Cascadeable 512 x 9 FIFO | COMM/MIL | 15, 25, 33 | 80/100 |
| CY7C414 | Cascadeable 1024 x 9 FIFO | COMM/MIL | 15, 25, 33 | 80/100* |
| CY7C416 | Cascadeable 2048 x 9 FIFO | COMM/MIL | 15, 25, 33 | 80/100* |

*$I_{SB}$ = 8/15 mA Commercial/Military

## Pin Configurations

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## Switching Characteristics Over the Operating Range[1]

| Parameters | Description | Test Conditions | 3341 Min. | 3341 Max. | 3341-2 Min. | 3341-2 Max. | 7C401-5 7C402-5 Min. | 7C401-5 7C402-5 Max. | 7C401/2/3/4-10 Min. | 7C401/2/3/4-10 Max. | 7C401/2/3/4-15 Min. | 7C401/2/3/4-15 Max. | 7C403-25[6] 7C404-25[6] Min. | 7C403-25[6] 7C404-25[6] Max. | 7C408-15 7C409-15 Min. | 7C408-15 7C409-15 Max. | 7C408-25 7C409-25 Min. | 7C408-25 7C409-25 Max. | 7C408-35 7C409-35 Min. | 7C408-35 7C409-35 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_O$ | Operating Frequency | Note 2 | | 1.2 | | 2 | | 5 | | 10 | | 15 | | 25 | | 15 | | 25 | | 35 | MHz |
| $t_{PHSI}$ | SI HIGH Time | | 80 | | 80 | | 20 | | 20 | | 20 | | 11 | | 23 | | 11 | | 9 | | ns |
| $t_{PLSI}$ | SI LOW Time | | 80 | | 80 | | 45 | | 30 | | 25 | | 24 | | 25 | | 24 | | 17 | | ns |
| $t_{SSI}$ | Data Setup to SI | Note 3 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HSI}$ | Data Hold from SI | Note 3 | 200 | | 100 | | 60 | | 40 | | 30 | | 20 | | 30 | | 20 | | 10 | | ns |
| $t_{DLIR}$ | Delay, SI HIGH to IR LOW | Note 6 | 20 | 350 | 20 | 160 | | 75 | | 40 | | 35 | | 21/22 | | 35 | | 21 | | 15 | ns |
| $t_{DHIR}$ | Delay, SI LOW to IR HIGH | Note 6 | 20 | 450 | 20 | 200 | | 75 | | 45 | | 40 | | 28/30 | | 40 | | 23 | | 16 | ns |
| $t_{PHSO}$ | SO HIGH Time | | 80 | | 80 | | 20 | | 20 | | 20 | | 11 | | 23 | | 11 | | 9 | | ns |
| $t_{PLSO}$ | SO LOW Time | | 80 | | 80 | | 45 | | 25 | | 25 | | 24 | | 25 | | 24 | | 17 | | ns |
| $t_{OR}$ + $t_{DLOR}$ | Delay, SO HIGH to OR LOW | Note 6 | 20 | 370 | 20 | 160 | | 75 | | 40 | | 35 | | 19/21 | | 35 | | 21 | | 15 | ns |
| $t_{OR}$ – $t_{DHOR}$ | Delay, SO LOW to OR HIGH | Note 6 | 20 | 450 | 20 | 200 | | 80 | | 55 | | 40 | | 34/37 | | 40 | | 23 | | 16 | ns |
| $t_{SOR}$ | Data Setup to OR HIGH | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HSO}$ | Data Hold from SO LOW | | 75 | | 20 | | 5 | | 5 | | 5 | | 5 | | 0 | | 0 | | 0 | | ns |
| $t_{BT}$ | Bubblethrough Time | Note 6 | | 1000 | | 500 | | 200 | 10 | 95 | 10 | 65 | 10 | 50/60 | 10 | 65 | 10 | 60 | 10 | 50 | ns |
| $t_{SIR}$ | Data Setup to IR | Note 4 | | | | | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{HIR}$ | Data Hold from IR | Note 4 | | | | | 30 | | 30 | | 30 | | 20 | | 30 | | 20 | | 20 | | ns |
| $t_{PIR}$ | Input Ready Pulse HIGH | | | | | | 20 | | 20 | | 20 | | 15 | | 23 | | 15 | | 10 | | ns |
| $t_{POR}$ | Output Ready Pulse HIGH | | | | | | 20 | | 20 | | 20 | | 15 | | 23 | | 15 | | 10 | | ns |
| $t_{DHHF}$ | SI LOW to HF HIGH | | | — | | — | | — | | — | | — | | — | | 65 | | 55 | | 45 | ns |
| $t_{DLHF}$ | SO LOW to HF LOW | | | — | | — | | — | | — | | — | | — | | 65 | | 55 | | 45 | ns |
| $t_{DLAFE}$ | SO or SI LOW to AFE LOW | | | — | | — | | — | | — | | — | | — | | 65 | | 55 | | 45 | ns |
| $t_{DHAFE}$ | SO or SI LOW to AFE HIGH | | | — | | — | | — | | — | | — | | — | | 65 | | 55 | | 45 | ns |
| $t_{PMR}$ | $\overline{MR}$ Pulse Width | | 400 | | 200 | | 40 | | 30 | | 25 | | 25 | | 55 | | 45 | | 35 | | ns |
| $t_{DSI}$ | $\overline{MR}$ HIGH to SI HIGH | | 30 | | 30 | | 40 | | 35 | | 25 | | 10 | | 25 | | 10 | | 10 | | ns |
| $t_{DOR}$ | $\overline{MR}$ LOW to OR LOW | | | 400 | | 200 | | 85 | | 40 | | 35 | | 35 | | 55 | | 45 | | 35 | ns |
| $t_{DIR}$ | $\overline{MR}$ LOW to IR HIGH | | | 400 | | 200 | | 85 | | 40 | | 35 | | 35 | | 55 | | 45 | | 35 | ns |
| $t_{LZMR}$ | $\overline{MR}$ LOW to Output LOW | Note 5 | | | | | | 50 | | 40 | | 35 | | 25 | | 55 | | 45 | | 35 | ns |
| $t_{DAE}$ | $\overline{MR}$ LOW to $\overline{AE}$ LOW | | | — | | — | | — | | 35 | | 30 | | 20 | | 55 | | 45 | | 35 | ns |
| $t_{DAF}$ | $\overline{MR}$ LOW to $\overline{AF}$ HIGH | | | — | | — | | — | | 30 | | 25 | | 15 | | 55 | | 45 | | 35 | ns |

**Notes:**

1. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified $I_{OL}/I_{OH}$ and 30 pF load capacitance, as in *Figure 1.*
2. $I/f_O > t_{PHSI} + t_{DHIR}$, $I/f_O > t_{PHSO} + t_{DHOR}$.
3. $t_{SSI}$ and $t_{HSI}$ apply when memory is not full.
4. $t_{SIR}$ and $t_{HIR}$ apply when memory is full, SI is HIGH and minimum bubblethrough ($t_{BT}$) conditions exist.
5. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.
6. Commercial/Military.

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CYPRESS SEMICONDUCTOR

## Features

- **High speed**
- **Low power**
- **10% power supply**
- **Available in DIP, LCC, PLCC, PGA**

## Product Characteristics

Cypress offers the low power alternative for Bit-Slice and DSP applications. 1.2 micron CMOS technology provides products that are faster or as fast as their bipolar equivalents at one-half to one-tenth the power.

These products are available in a variety of packages including DIP, LCC, PLCC, SOIC, and Pin Grid Array. Reliability advantages include ESD protection on all pins, latch-up protection via a substrate bias generator and layout techniques, and low power dissipation.

These products are the:

| | |
|---|---|
| CY7C510 | 16 x 16 Multiplier-Accumulator |
| CY7C516 | 16 x 16 Multiplier |
| CY7C517 | 16 x 16 Multiplier |
| CY7C901 | 4-Bit Slice ALU |
| CY7C909 | Microprogram Sequencer |
| CY7C910 | Microprogram Controller |
| CY7C911 | Microprogram Sequencer |
| CY7C9101 | 16-Bit Slice ALU |

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ±10% |
| Military | −55°C to +125°C | |

## Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

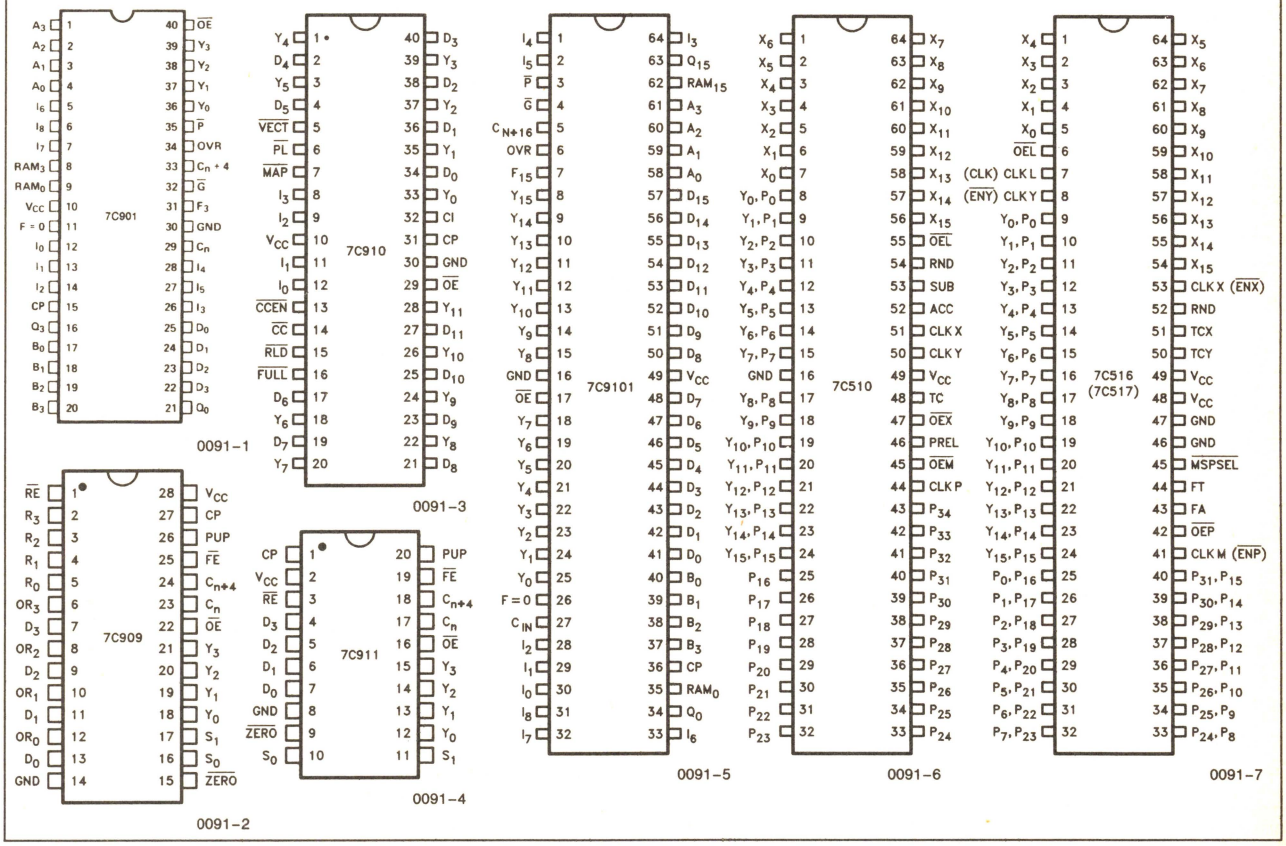
Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

## Pin Configurations

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## Electrical Characteristics over the operating range

| Product | Parameters | Description | Test Conditions | | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| ALL | $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | | 2.4 | | V |
| | $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. | | | 0.4 | V |
| | $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ | V |
| | $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| | $I_{IX}$ | Input Leakage Current | $GND \le V_I \le V_{CC}$ | | −10 | +10 | μA |
| 7C510 7C516 7C517 | $I_{CC}$ | Supply Current | $V_{IH} \ge 3.85V$, $V_{IL} \le 0.4V$ | Commercial | | 20 | mA |
| | | | | Military | | 25 | |
| | $I_{CC}$ | Supply Current | $V_{CC}$ = Max., $f_O$ = 10 MHz | Commercial | | 100 | mA |
| | | | | Military | | 110 | |
| 7C901 | $I_{CC}$ | Supply Current | $V_{IH} \ge V_{CC} - 1.2V$, $V_{IL} \le 0.4V$, $f_O$ = 10 MHz | Commercial | | 26.5 | mA |
| | | | | Military | | 31 | |
| | $I_{CC}$ | Supply Current | $V_{CC}$ = Max. | Commercial | | 70 | mA |
| | | | | Military | | 90 | |
| 7C909 7C911 | $I_{CC}$ | Supply Current | $V_{IH} \ge 3.0V$, $V_{IL} \le 0.4V$, $V_{CC}$ = Max. | Commercial | | 35 | mA |
| | | | | Military | | 35 | |
| | $I_{CC}$ | Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA | Commercial | | 55 | mA |
| | | | | Military | | 55 | |
| 7C910 | $I_{CC}$ | Supply Current | $V_{IH} \ge 3.85V$, $V_{IL} \le 0.4V$ | Commercial | | 35 | mA |
| | | | | Military | | 50 | |
| | $I_{CC}$ | Supply Current | $V_{CC}$ = Max. | Commercial | | 70 | mA |
| | | | | Military | | 90 | |
| 7C9101 | $I_{CC}$ | Supply Current (Quiescent) | $V_{IH} \ge 3.85V$, $V_{IL} \le 0.4V$, $\overline{OE}$ = High | Commercial | | 25 | mA |
| | | | | Military | | 30 | |
| | $I_{CC}$ | Supply Current | $V_{CC}$ = Max., $f_O$ = 10 MHz, $\overline{OE}$ = High | Commercial | | 60 | mA |
| | | | | Military | | 85 | |

**Note:**
1. All supply current specifications are at $V_{CC}$ = Max.

## Selector Guide

| Product | Description | Temp. Range | Speed Grades | Units |
|---|---|---|---|---|
| 7C510 | Multiply-Accumulate Time | Commercial | 45, 55, 65, 75 | ns |
| | | Military | 55, 65, 75 | |
| 7C516 | Clocked Multiply Time | Commercial | 38, 45, 55, 65, 75 | ns |
| | | Military | 42, 55, 65, 75 | |
| 7C517 | Clocked Multiply Time | Commercial | 38, 45, 55, 65, 75 | ns |
| | | Military | 42, 55, 65, 75 | |
| 7C901 | Read-Modify-Write Cycle Time | Commercial | 23, 31 | ns |
| | | Military | 27, 32 | |
| 7C909 | Clock to Output Cycle Time | Commercial | 30, 40 | ns |
| | | Military | 30, 40 | |
| 7C910 | Clock Period I = 14 | Commercial | 40, 50, 93 | ns |
| | | Military | 46, 51, 99 | |
| 7C911 | Clock to Output Cycle Time | Commercial | 30, 40 | ns |
| | | Military | 30, 40 | |
| 7C9101 | Read-Modify-Write Cycle Time | Commercial | 30, 40 | ns |
| | | Military | 35, 45 | |

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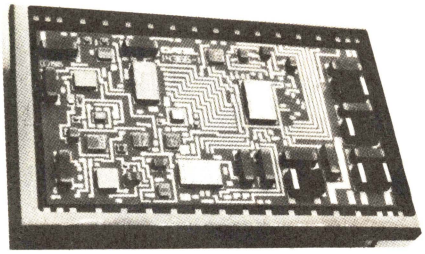
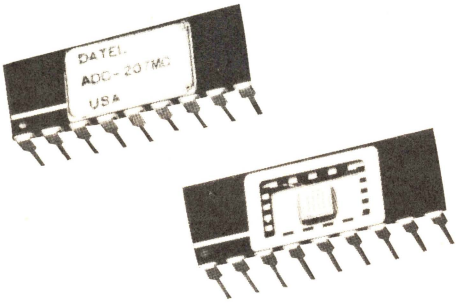
# New Products from DATEL



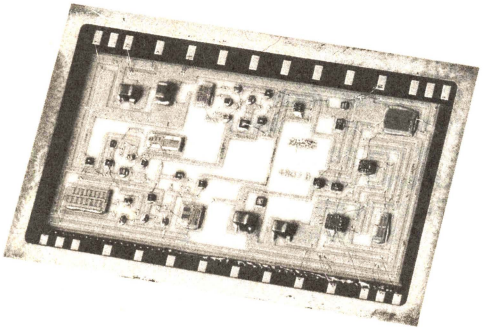
## ADC-500
**High-Speed, Low Power, 12-Bit A/D Converter**

- 500 nSec. conversion time
- 12-Bit accuracy
- 1.7 Watts power dissipation
- −55°C to +125°C available
- Small, 32-pin DIP



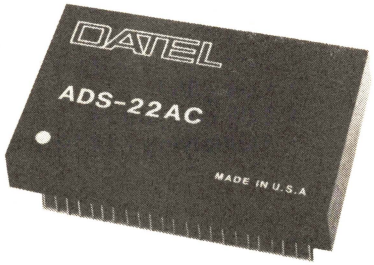

## ADC-207
**High-Speed, 7-Bit, Low Power Flash A/D Converter**

- 20 MHz Conversion rate
- 7-Bit accuracy
- Fully specified
- −55°C to +125°C available
- 1.25 Micron CMOS monolithic process



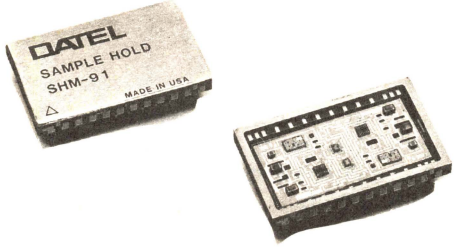
## SHM-45
**High-Speed, Precision Sample/Hold Amplifier**

- Ideally suited for ADC-500/505 applications
- 200 nSec. maximum acquisition time
- 0.01% Accuracy
- Operates at different gain settings




## ADS-21AC/-22AC
**12-Bit Sampling A/D Converters**

- 1.3 MHz (ADS-21AC) or 1.0 MHz (ADS-22AC) throughput rate
- 12-Bit accuracy
- S/H included
- Single 46-pin DIP




## SHM-91
**Dual, Precision Sample/Hold Amplifier**

- 2 μSec. acquisition time
- 12- and 14-Bit applications
- Multiplexed inputs and outputs
- −55°C to +125°C available

Datel

**DATEL, INC.**, 11 CABOT BOULEVARD, MANSFIELD, MA 02048 • TEL. (617) 339-3000 / TWX 710-346-1953 / TLX 951340 / FAX (617) 339-6356

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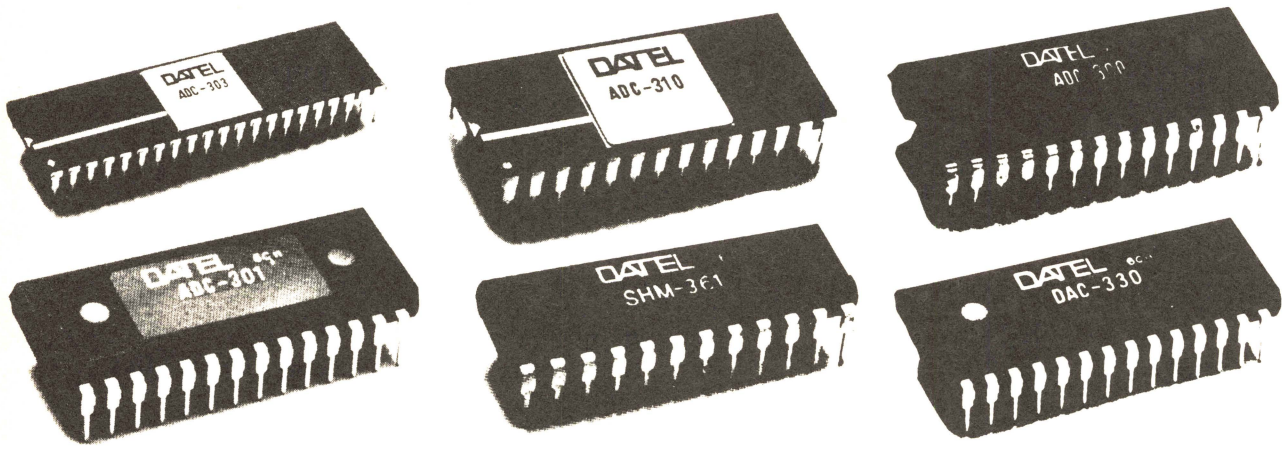
# New *Video-Speed* Devices from DATEL




## APPLICATIONS

- HIGH SPEED DATA ACQUISITION
- RADAR PULSE ANALYSIS
- TV VIDEO ENCODING
- HIGH ENERGY PHYSICS
- TRANSIENT ANALYSIS
- MEDICAL ELECTRONICS
- FLUID FLOW ANALYSIS
- SONAR SYSTEMS

## FEATURES

### ADC-300
- 8 Bits at 20 MHz
- 700 mW power dissipation
- ±½ LSB linearity
- Buffered outputs
- Single supply operation
- ECL-compatible
- Input bandwidth 5.5 MHz

### ADC-301
- 8-Bit resolution
- Non-linearity ±½ LSB
- Conversion rate 30 MHz
- 15 MHz bandwidth
- 35 pF Input capacitance
- Power dissipation 420 mW

### ADC-302
- 8-Bit resolution
- Non-linearity ±½ LSB
- Conversion rate 50 MHz
- 25 MHz bandwidth
- 35 pF Input capacitance
- Power dissipation 550 mW

### ADC-303
- 8 Bits resolution
- Speed up to 100 MHz guaranteed
- ±½ LSB linearity
- Input bandwidth 40 MHz
- Output latch and buffer
- Low input capacitance, 35 pF typical
- Low power
- ECL-compatible

### ADC-310
- 10-Bit resolution
- 20 MHz conversion rate
- Very low power 360 mW
- Buffered output
- ECL-compatible
- Input bandwidth 10 MHz

### DAC-330
- 10-Bit resolution
- Conversion rate 160 MHz
- Low power
- Single −5V supply
- Low glitch
- ECL-compatible
- Multiplying - 14 MHz bandwidth

### SHM-40
Video Speed Sample/Hold Amplifier
- 40 nSec. acquisition time
- 0.1% Non-linearity
- 40 MHz bandwidth
- −55°C to +125°C available

### SHM-360, -361
- 8 nsec. and 1 nsec. acquisition time
- Sampling frequency 18 MHz and 35 MHz
- Input amplifier bandwidth 25 MHz and 55 MHz
- Linearity 0.08%
- Low power

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# HIGH-RELIABILITY SCREENING FOR MILITARY APPLICATIONS

DATEL is committed to meeting the demanding requirements of military and aerospace applications. Toward that commitment, DATEL has pursued and received full Certification to MIL-STD-1772 for its hybrid manufacturing facility.

With this MIL-STD-1772 Certification, DATEL can now offer several levels of high-reliability screening:

1. DATEL'S STANDARD -QL PROGRAM
   (see chart below)
2. MIL-STD-883 CLASS B COMPLIANT DEVICES
   (Consult the factory for further information concerning products which are fully compliant with MIL-STD-883)

## DATEL'S QL PROGRAM

| TEST | METHOD | PURPOSE |
|---|---|---|
| Internal Visual (PRECAP) | Method 2017 | Eliminates devices with potential for failure under mechanical, electrical or thermal stress |
| Stabilization Bake | Method 1008. Test Condition C. 24 hrs at 150°C | Eliminates device failure due to storage at elevated temperatures |
| Temperature Cycling | Method 1010, test condition C, −65°C to 150°C | Determines resistance of device to sudden exposure to extreme temperature changes. Removes potential failures due to thermal stress on bonds, etc. |
| Constant Acceleration | Method 2001, test condition A, Y AXIS, 5 kg | Eliminates potential failures due to structural or mechanical weaknesses not detected in shock or vibration tests. |
| Burn-in Test | Method 1015, test condition B, 160 hrs at +125°C | Stresses devices at temperature in order to eliminate infant mortality failures. |
| PDA 10% | Static Tests performed at +25°C | Percent defective allowable — Rejects lots with static test failures greater than 10% |
| Final Electrical Tests | Performed at +25°C and at max. & min. operating temperatures | Verifies that device still meets specified data sheet parameters. |
| Seal Fine and Gross | Method 1014, test condition A (fine). $5 \times 10^{-7}$ cc/sec test condition C (gross) | Insures hermeticity of device package. Eliminates degradation due to absorption of water vapor or other contaminants. |
| External Visual | Method 2009 | Insures that materials, design, construction, marking, and workmanship conform with applicable procurement documentation. |

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# HYBRID HIGH RELIABILITY PRODUCTS

DATEL is a recognized industry leader in the design and manufacture of thin and thick-film hybrid data conversion products.

The following list briefly summarizes DATEL's "QL" hybrid products.

## ANALOG-TO-DIGITAL CONVERTERS

| MODEL NO. | RESOLUTION | CONVERSION TIME | LINEARITY |
|---|---|---|---|
| ADC-HC12BMM-QL | 12 bits | 300 μsec. | ± ½ LSB |
| ADC-HS12BMM-QL | 12 bits | 9 μsec. | ± ½ LSB |
| ADC-HX12BMM-QL | 12 bits | 20 μsec. | ± ½ LSB |
| ADC-HZ12BMM-QL | 12 bits | 8 μsec. | ± ½ LSB |
| ADC-505BMM-QL | 12 bits | 500 nsec. | 0.0125% ± ½ LSB |
| ADC-810MM-QL | 12 bits | 2 μsec. | ± 1 LSB |
| ADC-811MM-QL | 12 bits | 3 μsec. | ± 1 LSB |
| ADC-815MM-QL | 8 bits | 700 nsec. | ± ½ LSB |
| ADC-508MM-QL | 12 bits | | 0.0125% ± ½ LSB |
| ADC-816MM-QL | 10 bits | 800 nsec. | ± ½ LSB |
| ADC-817MM-QL | 12 bits | 2 μsec. | ± 1 LSB |
| ADC-825MM-QL | 8 bits | 1 μsec. | ± ½ LSB |
| ADC-826MM-QL | 10 bits | 1.4 μsec. | ± ½ LSB |
| ADC-827MM-QL | 12 bits | 3 μsec. | ± 1 LSB |
| ADC-5101H-QL | 8 bits | 900 nsec. | ± ½ LSB |
| ADC-5211H-QL | 12 bits | 13 μsec. | ± ½ LSB |
| ADC-5212H-QL | 12 bits | 13 μsec. | ± ½ LSB |
| ADC-5214H-QL | 12 bits | 13 μsec. | ± ½ LSB |
| ADC-5215H-QL | 12 bits | 13 μsec. | ± ½ LSB |
| ADC-5216H-QL | 12 bits | 13 μsec. | ± ½ LSB |
| ADC-520MM-QL | 12 bits | 800 nsec. | ± ½ LSB |
| ADC-521MM-QL | 12 bits | 800 nsec. | ± ½ LSB |
| ADC-515MM-QL | 10 bits | 700 nsec. | ± ½ LSB |

## DIGITAL-TO-ANALOG CONVERTERS

| MODEL NO. | RESOLUTION | OUTPUT SETTLING TIME | LINEARITY |
|---|---|---|---|
| DAC-HF8BMM-QL | 8 bits | 25 nsec. | ± ½ LSB |
| DAC-HF10BMM-QL | 10 bits | 25 nsec. | ± ½ LSB |
| DAC-HF12BMM-QL | 12 bits | 50 nsec. | ± ½ LSB |
| DAC-HK12BMM-QL | 12 bits | 3 μsec. | ± ½ LSB |
| DAC-HP16BMM-QL | 16 bits | 15 μsec. | ± 2 LSB |
| DAC-HZ12BMM-QL | 12 bits | 3 μsec. | ± ½ LSB |

## SAMPLE-HOLD AMPLIFIERS

| MODEL NO. | ACCURACY | ACQUISITION TIME | HOLD MODE DROOP |
|---|---|---|---|
| SHM-6MM-QL | 0.01% | 1 μsec. | 10 μV/μsec. |
| SHM-9MM-QL | 0.01% | 6 μsec. | 0.2 mv/ms |
| SHM-HUMM-QL | 0.10% | 25 nsec. | 50 μV/μsec. |
| SHM-4860MM-QL | 0.01% | 200 nsec. | 0.5 μV/μsec. |
| SHM-40MM-QL | 0.1% | 40 nsec. | 100 μV/μsec. |
| SHM-45MM-QL | 0.01% | 200 nsec. | 0.5 μV/μsec. |
| SHM-91MM-QL | 0.003% | 2 μsec. | 5.0 μV/μsec. |

## OPERATIONAL AMPLIFIERS

| MODEL NO. | INPUT OFFSET VOLTAGE | GAIN BANDWIDTH | OUTPUT |
|---|---|---|---|
| AM-500MM-QL | 3 mV | 130 MHz | ± 10V at 50 mA |
| AM-1435MM-QL | 5 mV | 1000 MHz | ± 7V at 14 mA |

## PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIERS

| MODEL NO. | GAIN RANGE | SETTLING TIME | OUTPUT |
|---|---|---|---|
| AM-551MM-QL | 1 to 1000 | 2 μsec. | ± 11V at ± 5 mA |

## DATA ACQUISITION SUBSYSTEMS

| MODEL NO. | RESOLUTION | INPUT CHANNELS | THROUGHPUT RATE |
|---|---|---|---|
| HDAS-8MM-QL | 12 bits | 8 Differential | 50 kHz |
| HDAS-16MM-QL | 12 bits | 16-Single Ended | 50 kHz |

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# ANALOG TO DIGITAL CONVERTERS

## Less than 8 Bit Resolution

| Model Number | Conversion Time | Linearity | Temp Range * | Power Dissipation | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| ADC-207 | 50 ns | 0.39% | C | 385 mV max | 18 pin DIP | yes | CMOS flash converter |

## 8 Bit Resolution

| Model Number | Conversion Time | Linearity | Temp Range * | Power Dissipation | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| ADC-EK8B | 1.8 ms | 0.195% | C | 25 mW | 24 pin DIP | | Integrating ADC |
| ADC-ET8BC | 1.8 ms | 0.195% | C | 10 mW | 24 pin DIP | | Three State Output |
| ADC-830C | 100 μs | 0.195% | C | 10 mW | 20 pin DIP | | Ratiometric, CMOS |
| ADC-847 | 9 μs | 0.195% | C | 125 mW | 18 pin DIP | | Three State Output |
| ADC-881 | 1.5 μs | 0.016% | C | 4.5 W | 3″ × 5″ MOD | | 14 bit linear |
| ADC-825 | 1.0 μs | 0.195% | C,M | 1.25 W max | 24 pin DIP | yes | |
| ADC-5101 | 900 ns | 0.195% | C,M | 1.2 W max | 24 pin DIP | yes | |
| ADC-815 | 700 ns | 0.195% | C,M | 1.25 W max | 24 pin DIP | yes | |
| ADC-300 | 50 ns | 0.195% | C | 700 mW | 28 pin DIP | | 20 MHz, ECL |
| ADC-301 | 33 ns | 0.195% | C | 420 mW | 28 pin DIP | | 30 MHz, ECL |
| ADC-302 | 20 ns | 0.195% | C | 550 mW | 28 pin DIP | | 50 MHz, ECL |
| ADC-303 | 10 ns | 0.195% | C | 1.2 W | 42 pin DIP | | 100 MHz, ECL |
| ADC-208 | 40 ns | 0.39% | C,M | 500 mW | 24 pin DIP | yes | CMDS Flash Converter |
| ADC-304 | 50 ns | 0.39% | C | 360 mW | 28 pin DIP | | TTL Compatible |
| ADC-B300 | 62.5 ns | 0.39% | C | 8.1 W | Eurocard | | Complete Sampling A/D |
| ADC-B301 | 25 ns | 0.39% | C | 6 W | Eurocard | | Complete Sampling A/D |
| ADC-B302 | 17 ns | 0.39% | C | 7.6 W | Eurocard | | Complete Sampling A/D |
| ADC-B303 | 10 ns | 0.39% | C | 3.9 W | Eurocard | | Complete Sampling A/D |
| ADC-B304 | 50 ns | 0.39% | C | 4 W | Eurocard | | Complete Sampling A/D |

## 10 Bit Resolution

| Model Number | Conversion Time | Linearity | Temp Range * | Power Dissipation | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| ADC-EK12D | 12 ms | 0.05% | C,I,M | 20 mW | 24 pin DIP | | Integrating |
| ADC-EK10B | 6 ms | 0.05% | C | 20 mW | 24 pin DIP | | Integrating |
| ADC-ET10BC | 6 ms | 0.05% | C | 20 mW | 24 pin DIP | | Integrating |
| ADC-856 | 10 μs | 0.05% | C,M | 500 mW | 28 pin DIP | | Tracking ADC |
| ADC-816 | 800 ns | 0.05% | C,M | 1.7 W | 32 pin DIP | yes | Fast Hybrid |
| ADC-310 | 50 ns | 0.17% | C | 360 mW | 28 pin DIP | | Ultra fast monolithic |
| ADS-115 | 1 μs | 0.05% | C,M | 2.1 W | 32 pin DIP | yes | Sampling A/D |
| ADS-116 | 1 μs | 0.05% | C,M | 2.1 W | 32 pin DIP | yes | Sampling A/D |
| ADC-510 | 450 ns | 0.05% | C | 1.6 W | 32 pin DIP | yes | Two-Pass A/D |
| ADC-515 | 650 ns | 0.05% | C,M | 1.6 W | 32 pin DIP | yes | Two-Pass A/D |
| ADC-B310 | 50 ns | 0.17% | C | 6.5 W | Eurocard | | Complete Sampling A/D |

## 12 Bit Resolution

| Model Number | Conversion Time | Linearity | Temp Range * | Power Dissipation | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| ADC-7109 | 33 ms | 0.024% | C | 20 mW | 40 pin DIP | | Integrating Ind Std |
| ADC-EK12B | 24 ms | 0.012% | C | 20 mW | 24 pin DIP | | Integrating |
| ADC-ET12B | 24 ms | 0.012% | I,M | 20 mW | 24 pin DIP | | Integrating |
| ADC-HC12B | 300 μs | 0.012% | C,M | 112 mW | 32 pin DIP | yes | Low Power CMOS ADC |
| ADC-574A | 25 μs | 0.012% | C | 720 mW | 28 pin DIP | | μProcessor Compatible |
| ADC-HX12B | 20 μs | 0.012% | C,M | 1.1 W | 32 pin DIP | yes | Low Cost |
| ADC-5211 | 13 μs | 0.012% | C,M | 1 W | 24 pin DIP | yes | Adjustment free |
| ADC-5212 | 13 μs | 0.012% | C,M | 1 W | 24 pin DIP | yes | Adjustment free |
| ADC-5214 | 13 μs | 0.012% | C,M | 1 W | 24 pin DIP | yes | Adjustment free |
| ADC-5215 | 13 μs | 0.012% | C,M | 1 W | 24 pin DIP | yes | Adjustment free |
| ADC-5216 | 13 μs | 0.012% | C,M | 1 W | 24 pin DIP | yes | Adjustment free |
| ADC-HS12B | 9 μs | 0.012% | C,M | 1.1 W | 32 pin DIP | yes | Includes T/H |
| ADC-HZ12B | 8 μs | 0.012% | C,M | 1.1 W | 32 pin DIP | yes | Fast Low cost ADC |
| ADC-811 | 3 μs | 0.024% | C,M | 2.8 W | 32 pin DIP | yes | AC85/87 pinout |
| ADC-827 | 3 μs | 0.024% | C,M | 2.2 W | 32 pin DIP | yes | Buffered |
| ADC-810 | 2 μs | 0.024% | C,M | 2.8 W | 32 pin DIP | yes | ADC85/87 pinout |
| ADC-817 | 2 μs | 0.024% | C,M | 2.2 W | 32 pin DIP | yes | Buffered |
| ADC-505 | 550 ns | 0.012% ± ½ LSB | C,M | 1.5 W | 32 pin DIP | yes | Two pass A/D |
| ADC-868 | 500 ns | 0.012% | C | 8.6 W | 4″ × 6″ MOD | | Three state output |
| ADC-500 | 500 ns | 0.012% ± ½ LSB | C | 1.5 W | 32 pin DIP | yes | Two pass A/D |
| ADC-508 | 700 ns | 0.012% | C,M | 1.6 W | 32 pin DIP | yes | Two pass A/D |
| ADC-520 | 800 ns | 0.012% | C,M | 1.6 W | 32 pin DIP | yes | Two pass A/D |
| ADC-521 | 800 ns | 0.012% | C,M | 1.6 W | 32 pin DIP | yes | Two pass A/D |
| ADS-21 | 770 ns | 0.012% ± ½ LSB | C | 2.4 W | 46 pin DIP | | Sampling A/D |
| ADS-22 | 1 μs | 0.012% ± ½ LSB | C | 2.4 W | 46 pin DIP | | Sampling A/D |
| ADS-105 | 1.3 μs | 0.012% ± ½ LSB | C,M | 2.1 W | 32 pin DIP | | Sampling A/D |
| ADS-106 | 1.3 μs | 0.012% ± ½ LSB | C,M | 2.1 W | 32 pin DIP | | Sampling A/D |
| ADS-125 | 1.6 μs | 0.012% | C,M | 2.1 W | 32 pin DIP | | Sampling A/D |

## 15 Bit Plus Sign Resolution

| Model Number | Conversion Time | Linearity | Temp Range * | Power Dissipation | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| ADC-800 | 400 ms | 0.003% | C | 20 mW | 40 pin DIP | | Integrating, CMOS |

*C = Commercial 0° to + 70°C I = Industrial – 25° to + 85°C M = Military/Extended – 55° to + 125°C.

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# DIGITAL TO ANALOG CONVERTERS

## Less than 8 Bit Resolution

| Model Number | Settling Time | Linearity | Temp Range* | Analog Output | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| DAC-0405MR | 4 ns | 3.125% | I | 0 to −1.0V | 24 pin DIP | | Composite Video DAC |
| DAC-0605MR | 6 ns | 0.78% | I | 0 to −1.0V | 24 pin DIP | | Composite Video DAC |

## 8 Bit Resolution

| Model Number | Settling Time | Linearity | Temp Range* | Analog Output | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| DAC-UP8B | 2.0 μs | 0.195% | C, M | ±5, 0 to 10V | 22 pin DIP | | With Input Latches |
| DAC-608C | 1.0 μs | 0.195% | C | Vref/15K | 20 pin DIP | | Latched CMOS MDAC |
| DAC-IC8B | 300 ns | 0.195% | C, M | 0 to −2mA | 16 pin DIP | | Low Cost |
| DAC-7523 | 200 ns | 0.1% | C | Vref/20K | 16 pin DIP | | CMOS MDAC |
| DAC-08B | 150 ns | 0.195% | C, M | 0 to −2mA | 16 pin DIP | | High speed, compliance |
| DAC-HF8B | 25 ns | 0.195% | C, M | 0 to 5mA, ±2.5mA | 24 pin DIP | yes | Ultra fast |
| DAC-0805 | 8 ns | 0.195% | I | 0 to −1.0V | 24 pin DIP | | Composite Video DAC |
| DAC-8308 | 7.5 ns | 0.195% | C | 0 to −1.054V | 2″ x 3″ MOD | | Composite Video DAC |
| DAC-8318 | 7.5 ns | 0.195% | C | 0 to −1 V | 2″ x 3″ MOD | | Composite Video DAC |

## 10 Bit Resolution

| Model Number | Settling Time | Linearity | Temp Range* | Analog Output | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| DAC-HA12D | 5.0 μs | 0.05% | C, M | ±Vref/10K | 18 pin DIP | | 3 digit Multiplying |
| DAC-UP10BC | 5.0 μs | 0.05% | C | 0 to 10V, ±5V | 24 pin DIP | | Input Register |
| DAC-HA10B | 1.3 μs | 0.05% | C, M | ±Vref/10K | 16 pin DIP | | CMOS Multiplying DAC |
| DAC-7533 | 800 ns | 0.1% | C | Vref/20K | 16 pin DIP | | CMOS MDAC |
| DAC-610C | 500 ns | 0.05% | C | Vref/15K | 20 pin DIP | | Latched CMOS MDAC |
| DAC-IC10BC | 250 ns | 0.1% | C | 0 to −2mA | 16 pin DIP | | Low Cost |
| DAC-IC10B | 250 ns | 0.05% | C, M | 0 to −2mA | 16 pin DIP | | Low Cost |
| DAC-330 | 4.7 ns | 0.1% | I | 0 to −1V | 28 pin DIP | | Buffered, Vout Video DAC |
| DAC-HF10B | 50 μs | 0.1% | C,M | 0 to 5mA, ± 2.5mA | 24 pin DIP | yes | Ultra fast |

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## 12 Bit Resolution

| Model Number | Settling Time | Linearity | Temp Range* | Analog Output | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| DAC-HA12B | 5.0 μs | 0.012% | C, M | ±Vref/10k | 18 pin DIP | | CMOS Multiplying DAC |
| DAC-7134J | 3.0 μs | 0.012% | C | Vref/Rin | 28 pin DIP | | MDAC w/PROM correction |
| DAC-HZ12B | 3.0 μs | 0.012% | C, M | 5 Voltage Ranges | 24 pin DIP | yes | Complete, Low Cost |
| DAC-HK12B | 3.0 μs | 0.012% | C, M | 5 Voltage Ranges | 24 pin DIP | yes | Latched, Fast, Binary |
| DAC-HK12B-2 | 3.0 μs | 0.012% | C, M | 5 Voltage Ranges | 24 pin DIP | yes | Latched, Fast, 2's Comp |
| DAC-7541 | 1.0 μs | 0.012% | C | Vref/20K | 28 pin DIP | | CMOS MDAC |
| DAC-612C | 1.0 μs | 0.012% | I | Vref/15K | 24 pin DIP | | Latched CMOS MDAC |
| DAC-DG12B | 600 ns | 0.012% | C | 5 Voltage Ranges | 4″ x 2″ MOD | | Deglitched |
| DAC-562 | 400 ns | 0.012% | C, M | 0 to −2, ±1mA | 24 pin DIP | | Monolithic 12 bit DAC |
| DAC-HF12B | 50 ns | 0.024% | C, M | 0 to 5mA, ±2.5mA | 24 pin DIP | yes | Ultra fast |

## Greater than 12 Bit Resolution

| Model Number | Settling Time | Linearity | Temp Range* | Analog Output | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|
| DAC-HP16B | 15 μs | 0.003% | C, I, M | 0 to 10V, ±5V | 24 pin DIP | yes | Complete DAC |
| DAC-7134L | 3.0 μs | 0.006% | C | Vref/Rin | 28 pin DIP | | MDAC w/PROM correction |
| DAC-7134K | 3.0 μs | 0.003% | C | Vref/Rin | 28 pin DIP | | MDAC w/PROM correction |

* C = Commercial 0° to +70°C  I = Industrial −25° to +85°C  M = Military/Extended −55° to +125°C.

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## SAMPLE-HOLD AMPLIFIERS

| Model Number | Acquisition Time | Accuracy | Droop Rate | Temp Range* | Input Range | Package | MIL-STD-883 | Description |
|---|---|---|---|---|---|---|---|---|
| SHM-9M | 6.0 μs | 0.01% | 0.2μV/μs | C, M | ±11.5V | 16 pin DIP | yes | Low cost, fast |
| SHM-LM-2 | 6.0 μs | 0.01% | 0.2μV/μs | C | ±10V | TO-99 Can | | Low cost, ext cap |
| SHM-IC-1 | 5.0 μs | 0.01% | 50μV/μs | C, M | ±10V | 14 pin DIP | | Low cost, ext cap |
| SHM-91M | 2.0 μs | 0.003% | 5μV/μs | C, M | ±10V | 24 pin DIP | yes | Precision dual T/H |
| SHM-6M | 1.0 μs | 0.02% | 10μV/μs | C, M | ±10V | 32 pin DIP | yes | High speed |
| SHM-20C | 1.0 μs | 0.01% | 0.08μV/μs | C | ±10V | 14 pin DIP | | Internal hold cap |
| SHM-5 | 350 ns | 0.01% | 20μV/μs | C | ±10V | 2″ x 2″ MOD | | Alternate source |
| SHM-45M | 200 ns | 0.01% | 0.5μV/μs | C, M | ±5, 10, 20V | 24 pin DIP | yes | High Speed |
| SHM-4860 | 200 ns | 0.01% | 0.5μV/μs | C, M | ±10.25V | 24 pin DIP | yes | 16 MHz bandwidth |
| SHM-40M | 40 ns | 0.1% | 100μV/μs | C, M | ±2.5V | 24 pin DIP | yes | Video T/H |
| SHM-7M | 40 ns | 0.1% | 100μV/μs | C, | ±5, 2.5V | 24 pin DIP | | Dual outputs |
| SHM-HU | 25 ns | 0.1% | 50μV/μs | C, M | ±2.5V | 24 pin DIP | yes | Ultra fast |
| SHM-361 | 20 ns | 0.15% | 10mV/μs | >C | ±3V | 24 pin DIP | | Video monolithic |
| SHM-360 | 11 ns | 0.15% | 10mV/μs | >C | ±3V | 24 pin DIP | | Video monolithic |

## ANALOG MULTIPLEXERS

| Model Number | Channels | Settling Time | Access Time | $R_{on}$ | ABS Max Input | Temp Range* | Package | Description |
|---|---|---|---|---|---|---|---|---|
| MVD-409 | 4 Diff | 2.8 μs | 350 ns | 250 ohm | ±17V | C, M | 16 pin DIP | Dielectrically Isolated |
| MXD-409 | 4 Diff | 3.0 μs | 500 ns | 1.5K | ±35V | C, M | 16 pin DIP | Overvoltage Protection |
| MX-818 | 4 Diff/8 S.E. | 800 ns | 125 ns | 750 ohm | ±17V | C, M | 18 pin DIP | High Speed |
| MV-808 | 8 S.E. | 2.8 μs | 350 ns | 250 ohm | ±17V | C, M | 16 pin DIP | Low cost |
| MX-808 | 8 S.E. | 3.0 μs | 500 ns | 1.5K | ±35V | C, M | 16 pin DIP | Overvoltage Protection |
| MVD-807 | 8 Diff | 2.4 μs | 300 ns | 270 ohm | ±17V | C, M | 28 pin DIP | Dielectrically Isolated |
| MXD-807 | 8 Diff | 3.0 μs | 500 ns | 1.5K | ±35V | C, M | 28 pin DIP | Overvoltage Protection |
| MX-1616 | 8 Diff/16 S.E. | 800 ns | 150 ns | 750 ohm | ±17V | C, M | 28 pin DIP | Dielectrically Isolated |
| MV-1606 | 16 S.E. | 2.4 μs | 300 ns | 270 ohm | ±17V | C, M | 28 pin DIP | Dielectrically Isolated |
| MX-1606 | 16 S.E. | 3.0 μs | 500 ns | 1.5K | ±35V | C, M | 28 pin DIP | Overvoltage Protection |

## OPERATIONAL AMPLIFIERS

| Model Number | Input offset | Gain BW | Slew Rate | Settling Time | Output | Temp Range* | Package | Description |
|---|---|---|---|---|---|---|---|---|
| AM-1435 | 5 mV | 1000 MHz | 300V/μs | 70ns/0.01% | 7V/14mA | C, I, M | 14 pin DIP | Ultra fast settling |
| AM-500 | 3 mV | 100 MHz | 1000V/μs | 200ns/0.01% | 10V/50mA | C, I, M | 14 pin DIP | Ultra fast inverting |
| AM-462-1 | 3 mV | 100 MHz | 35V/μs | 1.0μs/0.1% | 10V/10mA | C, M | 14 pin DIP | Wideband |
| AM-462-2 | 3 mV | 100 MHz | 35V/μs | 1.0μs/0.1% | 10V/10mA | C, M | 8 pin TO-99 | Wideband |
| AM-452-2 | 5 mV | 20 MHz | 120V/μs | 200ns/0.1% | 10V/10mA | C, M | 8 pin TO-99 | Wideband fast settling |
| AM-450-2 | 4 mV | 12 MHz | 30V/μs | 300ns/0.1% | 10V/10mA | C, M | 8 pin TO-99 | Wideband fast settling |
| AM-460-2 | 3 mV | 12 MHz | 7V/μs | 1.5μs/0.1% | 10V/10mA | C, M | 8 pin TO-99 | Wideband fast settling |
| AM-453-2 | 4 mV | 10 MHz | 13V/μs | | 12V/20mA | C, M | 8 pin TO-99 | Low noise wideband |
| AM-427-1 | 25 μV (B grade) | 5 MHz | 1.7V/μs | | 11V/18mA | C, M | 8 pin DIP | Instrumentation Grade |
| AM-427-2 | 25 μV (B grade) | 5 MHz | 1.7V/μs | | 11V/18mA | C, M | 8 pin TO-99 | Instrumentation Grade |
| AM-464-2 | 6 mV | 4 MHz | 5V/μs | | 35V/10mA | C, M | 8 pin TO-99 | High Output Voltage |
| AM-430 | 25 μV (B grade) | 2.5 MHz | 0.5V/μs | 11μs/0.1% | 10V/25mA | C, M | 8 pin TO-99 | Low drift (0.6μV/C) |
| AM-7650-1 | 5 μV | 2.0 MHz | 2.5V/μs | | 4.7V | C | 14 pin DIP | Chopper Stabilized |
| AM-7650-2 | 5 μV | 2.0 MHz | 2.5V/μs | | 4.7V | C | 8 pin TO-99 | Chopper Stabilized |

## DIGITALLY PROGRAMMABLE INSTRUMENTATION AMPLIFIERS

| Model No. | Gain Range | Settling Time | Output | Temp Range* |
|---|---|---|---|---|
| AM-542MC | 1 to 1024 | 150 μs | ±10.5V to 5 mA | C |
| AM-543MC | 1 to 128 | 6 μs | ±11V to 1 mA | C |

## PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIERS

| Model No. | Gain Range | Settling Time | Output | Temp Range* |
|---|---|---|---|---|
| AM-551MC | 1 to 1000 | 2 μs | ±11V to 5 mA | C |

## DATA ACQUISITION SUBSYSTEMS

| Model No. | Resolution | Input Channels | Throughout Rate | Temp Range* |
|---|---|---|---|---|
| DAS-952R | 8 bits | 16 Single-Ended | 17 kHZ | I |
| HDAS-8M | 12 bits | 8 Differential | 50 kHZ | C, M |
| HDAS-16M | 12 bits | 16 Single-Ended | 50 kHZ | C, M |

## VOLTAGE TO FREQUENCY CONVERTERS

| Model No. | Linearity | Output Range | Gain Tempco | Temp Range* |
|---|---|---|---|---|
| VFQ-1C | 0.05% | 10 kHz to 100 kHz | 40 ppm °C | C |
| VFQ-1R | 0.05% | 10 kHz to 100 kHz | 40 ppm °C | I |

## ACTIVE FILTERS

| Model No. | Frequency Range | $F_O$ Accuracy | Q Range | Temp Range* |
|---|---|---|---|---|
| FLT-U2 | 0.01 Hz to 200 kHZ | ±5% | 0.1 to 1000 | C |

## MONOLITHIC VOLTAGE CONVERTER

| Model No. | Input Voltage Range | Input Current | Output Voltage Range | Temp Range* |
|---|---|---|---|---|
| VI-7660 | +1.5V to +10.0V | 500 μA | −1.5V to −10.0V | C |

* C = Commercial 0° to +70°C I = Industrial −25° to +85°C M = Military/Extended −55° to +125°C.

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## MONOLITHICS - DIP / LCC

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT $I_{CC1}$ (mA) | TYPICAL DC CURRENT $I_{SB1}$ (mA) | TYPICAL DC CURRENT $I_{CCDR}$ ($\mu$A) | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| DPS9167/-G | 16K× 1 | 35 | 30 | 1 | 50 | 1.000×0.300×0.200 | 20-PIN DIP/20-PAD LCC |
| DPS9168/-G | 4K× 4 | 25 | 30 | 1 | 50 | 1.000×0.300×0.200 | 20-PIN DIP/20-PAD LCC |
| DPS9116/-G | 2K× 8 | 35 | 30 | 1 | 50 | 1.200×0.600×0.200 | 24-PIN DIP/32-PAD LCC |
| DPS9287/-G | 64K× 1 | 25 | 45 | 1 | 100 | 1.100×0.300×0.200 | 22-PIN DIP/22-PAD LCC |
| DPS9264/-G | 8K× 8 | 35 | 30 | 1 | 50 | 1.400×0.600×0.200 | 28-PIN DIP/32-PAD LCC |
| DPS9788/-G | 16K× 4 | 25 | 45 | 1 | 100 | 1.100×0.300×0.200 | 22-PIN DIP/22-PAD LCC |
| DPS92256/-G | 32K× 8 | 100 | 40 | 1 | 50 | 1.400×0.600×0.200 | 28-PIN DIP/32-PAD LCC |
| DPS8181/-G | 256K× 1 | 45 | 45 | 1 | 200 | 1.200×0.400×0.200 | 24-PIN DIP/24-PAD LCC |
| DPS8186/-G | 64K× 4 | 55 | 60 | 2 | 200 | 1.400×0.600×0.200 | 28-PIN DIP/32-PAD LCC |
| DPS921024* | 128K× 8 | 100 | 50 | 1 | 70 | 1.600×0.600×0.200 | 32-PIN DIP/32-PAD LCC |
| DPD91256/-G | 256K× 1 | 100 | 60 | 1 | 400 | 0.800×0.300×0.200 | 16-PIN DIP/16-PAD LCC |
| DPD91644/-G | 64K× 4 | 100 | 60 | 1 | 400 | 0.900×0.300×0.200 | 18-PIN DIP/18-PAD LCC |
| DPD9001/-G | 1MB× 1 | 100 | 60 | 1 | 400 | 0.900×0.300×0.200 | 18-PIN DIP/18-PAD LCC |
| DPD92564/-G | 256K× 4 | 100 | 60 | 1 | 400 | 0.900×0.300×0.200 | 18-PIN DIP/18-PAD LCC |
| DPV27C256/-G | 32K× 8 | 120 | 60 | 1 | 100 | 1.400×0.600×0.200 | 28-PIN DIP/32-PAD LCC |
| DPV27C512/-G | 64K× 8 | 120 | 60 | 1 | 100 | 1.400×0.600×0.200 | 28-PIN DIP/32-PAD LCC |
| DPV27C1024A/-G | 128K× 8 | 120 | 60 | 1 | 100 | 1.400×0.600×0.200 | 32-PIN DIP/32-PAD LCC |
| DPV27C1024B/-G | 64K×16 | 120 | 60 | 1 | 100 | 2.000×0.600×0.200 | 40-PIN DIP/44-PAD LCC |
| DPE2864/-G | 8K× 8 | 120 | 45 | 1 | N/A | 1.400×0.600×0.200 | 28-PIN DIP/32-PAD LCC |
| DPE28256/-G | 32K× 8 | 120 | 50 | 1 | N/A | 1.400×0.600×0.200 | 28-PIN DIP/32-PAD LCC |

DPS = SRAM DPD = DRAM DPV = EPROM DPE = EEPROM

# SRAMS

## 16K×1 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT $I_{CC1}$ (mA) | TYPICAL DC CURRENT $I_{SB1}$ (mA) | TYPICAL DC CURRENT $I_{CCDR}$ ($\mu$A) | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| DPS8132* | 32K× 1 | 20 | 32 | 0.2 | 8 | 1.100×0.300×0.150 | 22-PIN DIP |
| DPS81C64* | 64K× 1 | 20 | 35 | 0.4 | 16 | 2.600×0.300×0.200 | 26-PIN SIP |
| DPS166167 | 256K× 1 | 20 | 45 | 1.6 | 64 | 1.980×0.900×0.240 | 40-PIN DIP |
| DPS166167 | 128K× 2 | 20 | 75 | 1.6 | 64 | 1.980×0.900×0.240 | 40-PIN DIP |
| DPS7M464 | 16K× 4 | 20 | 120 | 0.4 | 16 | 1.100×0.400×0.240 | 22-PIN DIP |
| DPS8M464 | 16K× 4 | 20 | 120 | 0.4 | 16 | 1.100×0.400×0.240 | 22-PIN DIP |
| DPS16X4 | 16K× 4 | 20 | 120 | 0.4 | 16 | 2.800×0.400×0.200 | 28-PIN SIP |
| DPS257 | 64K× 4 | 20 | 135 | 1.6 | 64 | 1.980×0.900×0.240 | 40-PIN DIP |
| DPS16X5 | 16K× 5 | 20 | 150 | 0.5 | 20 | 2.800×0.400×0.200 | 28-PIN SIP |
| DPS257 | 32K× 8 | 20 | 270 | 1.6 | 64 | 1.980×0.900×0.240 | 40-PIN DIP |
| DPS129 | 16K× 8 | 20 | 180 | 0.8 | 32 | 3.600×0.420×0.200 | 36-PIN SIP |
| DPS288 | 32K× 9 | 20 | 270 | 1.0 | 64 | 2.500×0.900×0.240 | 50-PIN DIP |
| DPS257 | 16K×16 | 20 | 480 | 5.0 | 64 | 1.980×0.900×0.240 | 40-PIN DIP |
| DPS288 | 16K×18 | 20 | 540 | 1.0 | 64 | 2.500×0.900×0.240 | 50-PIN DIP |

## 4K×4 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT $I_{CC1}$ (mA) | TYPICAL DC CURRENT $I_{SB1}$ (mA) | TYPICAL DC CURRENT $I_{CCDR}$ ($\mu$A) | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| DPS84H08 | 8K× 4 | 25 | 45 | 0.4 | 32 | 1.100×0.300×0.120 | 22-PIN DIP |
| DPS88H04 | 4K× 8 | 25 | 90 | 0.1 | 32 | 1.200×0.300×0.120 | 24-PIN DIP |
| DPS88H08 | 8K× 8 | 25 | 180 | 1.2 | 48 | 1.400×0.600×0.160 | 28-PIN DIP |
| DPS88H16 | 16K× 8 | 25 | 190 | 2.4 | 96 | 1.400×0.600×0.240 | 28-PIN DIP |
| DPS4X16 | 4K×16 | 25 | 160 | 1.0 | 32 | 2.000×0.350×0.180 | 36-PIN ZIP |
| DPS4H16* | 4K×16 | 25 | 160 | 1.0 | 32 | 2.000×0.300×0.180 | 36-PIN SIP |
| DPS266* | 16K×16 | 25 | 80 | 5.0 | 64 | 1.980×0.900×0.240 | 40-PIN DIP |
| DP4X32* | 4K×32 | 25 | 320 | 5.0 | 64 | 2.800×0.400×0.240 | 56-PIN SIP |




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## 2K×8 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPS8808* | 8K× 8 | 35 | 65 | 0.01 | 48 | 1.400×0.600×0.240 | 28-PIN DIP |
| DPS2X16* | 2K×16 | 35 | 40 | 0.01 | 16 | 2.000×0.600×0.150 | 40-PIN DIP |
| DPS2X32* | 2K×32 | 35 | 140 | 0.11 | 16 | 2.000×0.600×0.150 | 56-PIN DIP |

## 64K×1 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPS8256 | 256K× 1 | 25 | 35 | 0.4 | 16 | 3.000×0.400×0.200 | 30-PIN SIP |
| DP5122* | 1MB× 1 | 25 | 45 | 1.6 | 64 | 2.200×0.900×0.240 | 44-PIN DIP |
| DP5122* | 512K× 2 | 25 | 75 | 1.6 | 64 | 2.200×0.900×0.240 | 44-PIN DIP |
| DP86M44* | 64K× 4 | 25 | 120 | 0.4 | 16 | 1.200×0.400×0.240 | 24-PIN DIP |
| DPS8644 | 64K× 4 | 25 | 120 | 0.4 | 16 | 3.000×0.400×0.200 | 30-PIN SIP |
| DPS8645 | 64K× 4 | 25 | 120 | 0.4 | 16 | 2.800×0.400×0.200 | 28-PIN SIP |
| DPS1024 | 256K× 4 | 25 | 135 | 1.6 | 64 | 2.150×0.900×0.240 | 42-PIN DIP |
| DPS1026 | 256K× 4 | 25 | 135 | 1.6 | 64 | 2.150×0.900×0.240 | 40-PIN DIP |
| DPS1027 | 256K× 4 | 25 | 135 | 1.6 | 64 | 2.150×0.900×0.240 | 40-PIN DIP |
| DPS320 | 64K× 5 | 25 | 150 | 0.5 | 20 | 4.000×0.420×0.200 | 40-PIN SIP |
| DPS384 | 64K× 6 | 25 | 180 | 0.6 | 24 | 4.000×0.420×0.200 | 40-PIN SIP |
| DPS8524* | 64K× 8 | 25 | 240 | 0.8 | 32 | 4.000×0.400×0.240 | 40-PIN SIP |
| DPS8589* | 64K× 9 | 25 | 270 | 0.9 | 36 | 4.000×0.400×0.240 | 40-PIN SIP |
| DPS1152 | 128K× 9 | 25 | 270 | 1.0 | 64 | 2.500×0.900×0.240 | 50-PIN DIP |
| DPS1024 | 128K× 8 | 25 | 240 | 1.6 | 64 | 2.100×0.900×0.240 | 42-PIN DIP |
| DPS1025 | 128K× 8 | 25 | 240 | 1.6 | 64 | 2.100×0.900×0.240 | 40-PIN DIP |
| DPS1026 | 128K× 8 | 25 | 240 | 1.6 | 64 | 2.100×0.900×0.240 | 40-PIN DIP |
| DPS1027 | 128K× 8 | 25 | 240 | 1.6 | 64 | 2.100×0.900×0.240 | 40-PIN DIP |
| DP6410* | 64K×10 | 25 | 320 | 1.0 | 40 | 1.800×0.900×0.240 | 36-PIN DIP |
| DP6412* | 64K×12 | 25 | 360 | 1.2 | 48 | 1.800×0.900×0.240 | 36-PIN DIP |
| DPS1024 | 64K×16 | 25 | 480 | 5.0 | 64 | 2.100×0.900×0.240 | 42-PIN DIP |
| DPS1025 | 64K×16 | 25 | 480 | 5.0 | 64 | 2.100×0.900×0.240 | 40-PIN DIP |
| DPS1026 | 64K×16 | 25 | 480 | 5.0 | 64 | 2.100×0.900×0.240 | 40-PIN DIP |
| DPS1027 | 64K×16 | 25 | 480 | 5.0 | 64 | 2.100×0.900×0.240 | 40-PIN DIP |
| DPS1152 | 64K×18 | 25 | 540 | 1.0 | 64 | 2.500×0.900×0.240 | 50-PIN DIP |

## 8K×8 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPS8M628 | 8K×16 | 45 | 40 | 0.10 | 16 | 2.000×0.600×0.240 | 40-PIN DIP |
| DPS8M656 | 16K×16 | 45 | 44 | 0.20 | 32 | 2.000×0.600×0.240 | 40-PIN DIP |
| DPS41129 | 16K× 8 | 45 | 20 | 0.05 | 16 | 1.400×0.600×0.240 | 28-PIN DIP |
| DPS41193 | 24K× 8 | 45 | 22 | 0.08 | 24 | 1.400×0.600×0.240 | 28-PIN DIP |
| DPS41257 | 32K× 8 | 45 | 24 | 0.10 | 32 | 1.400×0.600×0.240 | 28-PIN DIP |
| DPS1124 | 128K× 8 | 45 | 30 | 1.60 | 64 | 2.800×1.400×0.240 | 56-PIN DIP |
| DPS1224 | 128K× 8 | 45 | 30 | 1.60 | 64 | 2.400×1.400×0.240 | 48-PIN DIP |
| DPS91288 | 128K× 8 | 45 | 30 | 1.00 | 120 | 3.400×1.200×0.240 | 68-PIN DIP |
| DPS1124 | 64K×16 | 45 | 30 | 5.00 | 64 | 2.800×1.400×0.240 | 56-PIN DIP |

## 16K×4 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPS32H8* | 32K× 8 | 25 | 160 | 2.0 | 80 | 1.400×0.600×0.240 | 28-PIN DIP |
| DPS16X16 | 16K×16 | 25 | 120 | 4 | 64 | 2.400×0.600×0.240 | 38-PIN DSIP |
| DPS16X17 | 16K×16 | 25 | 120 | 4 | 64 | 2.400×0.600×0.240 | 36-PIN DSIP |
| DPS3216* | 32K×16 | 25 | 130 | 10.0 | 128 | 2.400×0.600×0.240 | 44-PIN DIP |



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## 64K×4 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPS5124 | 512K× 4 | 55 | 50 | 10 | 2 | 2.695×0.600×0.270 | 54-PIN DIP |
| DPS5124 | 262K× 8 | 55 | 100 | 10 | 2 | 2.695×0.600×0.270 | 54-PIN DIP |
| DPS5125* | 512K× 8 | 55 | 50 | 10 | 2 | 1.500×1.500×0.270 | 64-PIN PGA |
| DPS5125* | 262K× 8 | 55 | 100 | 10 | 2 | 1.500×1.500×0.270 | 54-PIN PGA |
| DPS6432 | 256K× 8 | 55 | 100 | 10 | 2 | 2.995×0.600×0.270 | 60-PIN DIP |
| DPS6432 | 128K×16 | 55 | 200 | 10 | 2 | 2.995×0.600×0.270 | 60-PIN DIP |
| DPS6432 | 64K×32 | 55 | 400 | 10 | 2 | 2.995×0.600×0.270 | 60-PIN DIP |
| DPS12832* | 128K×32 | 55 | 200 | 10 | 2 | 1.600×1.600×0.270 | 60-PIN PGA |

## 32K×8 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPS4648 | 64K× 8 | 70 | 32 | 0.2 | 8 | 1.600×0.600×0.120 | 32-PIN DIP |
| DPS4968 | 96K× 8 | 70 | 35 | 0.3 | 12 | 1.600×0.600×0.120 | 32-PIN DIP |
| DPS41288 | 128K× 8 | 70 | 30 | 1.6 | 64 | 1.600×0.600×0.120 | 32-PIN DIP |
| DPS42568* | 256K× 8 | 70 | 40 | 1.6 | 64 | 3.200×0.600×0.240 | 64-PIN SIP |
| DPS45128 | 512K× 8 | 70 | 40 | 5.0 | 80 | 2.400×1.400×0.240 | 48-PIN DIP |
| DPS42568* | 128K×16 | 70 | 60 | 1.6 | 64 | 3.200×0.600×0.240 | 64-PIN SIP |
| DPS8M612 | 32K×16 | 45 | 64 | 0.2 | 16 | 2.000×0.600×0.220 | 40-PIN DIP |
| DPS8M624 | 64K×16 | 45 | 68 | 0.4 | 32 | 2.000×0.600×0.220 | 40-PIN DIP |
| DPS96122 | 512K× 8 | 70 | 40 | 5.0 | 160 | 3.400×1.200×0.240 | 68-PIN DIP |
| DPS45129* | 256K×16 | 70 | 80 | 5.0 | 80 | 2.800×1.400×0.240 | 56-PIN DIP |
| DPS6433 | 128K×16 | 55 | 200 | 10.0 | 2 | 3.000×0.600×0.270 | 60-PIN DIP |
| DPS6433 | 64K×32 | 55 | 400 | 10.0 | 2 | 3.000×0.600×0.270 | 60-PIN DIP |

## 256K×1 SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPS1024M1* | 1024K× 1 | 35 | 35 | 0.4 | 16 | 1.600×0.450×0.240 | 32-PIN DIP |
| DPS10241* | 1024K× 1 | 35 | 35 | 0.4 | 16 | 1.600×0.400×0.200 | 32-PIN DIP |
| DPS20482* | 4MB× 1 | 35 | 45 | 1.6 | 64 | 2.200×0.900×0.240 | 44-PIN DIP |
| DPS20482* | 2MB× 2 | 35 | 75 | 1.6 | 64 | 2.200×0.900×0.240 | 44-PIN DIP |
| DPS256M4* | 256K× 4 | 35 | 120 | 0.4 | 16 | 1.600×0.400×0.240 | 32-PIN DIP |
| DPS2564* | 256K× 4 | 35 | 120 | 0.4 | 16 | 3.200×0.400×0.200 | 32-PIN SIP |
| DPS25616* | 1MB× 4 | 35 | 135 | 1.6 | 64 | 2.200×0.900×0.240 | 44-PIN DIP |
| DPS2566* | 256K× 6 | 35 | 180 | 0.6 | 24 | 4.400×0.420×0.200 | 44-PIN DIP |
| DPS2568* | 256K× 8 | 35 | 240 | 0.8 | 32 | 4.400×0.400×0.240 | 44-PIN DIP |
| DPS25616* | 512K× 8 | 35 | 240 | 1.6 | 64 | 2.200×0.900×0.240 | 44-PIN DIP |
| DPS2569* | 256K× 9 | 35 | 270 | 0.9 | 36 | 4.400×0.400×0.240 | 44-PIN DIP |
| DPS25618* | 512K× 9 | 35 | 270 | 1.0 | 64 | 2.500×0.900×0.240 | 54-PIN DIP |
| DPS25612* | 256K×12 | 35 | 360 | 1.2 | 48 | 4.400×0.900×0.240 | 40-PIN DIP |
| DPS25616* | 256K×16 | 35 | 480 | 5.0 | 64 | 2.200×0.900×0.240 | 44-PIN DIP |
| DPS25618* | 256K×18 | 35 | 540 | 1.0 | 64 | 2.500×0.900×0.240 | 54-PIN DIP |

# NOVRAMS

## 512K×4 NOVRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPN18 | 1K×8 | 250 | 310 | 220 | N/A | 1.400×0.600×0.150 | 28-PIN DIP |
| DPN28 | 2K×8 | 250 | 530 | 440 | N/A | 1.400×0.600×0.240 | 28-PIN DIP |
| DPN88 | 8K×8 | 250 | 970 | 880 | N/A | 2.400×1.400×0.240 | 48-PIN DIP |





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## 64K×1 DRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPD4256 | 256K×1 | 100 | 36 | 2 | 400 | 2.200×0.300×0.140 | 22-PIN SIP |
| DPD4464 | 64K×4 | 100 | 144 | 8 | 1600 | 2.200×0.300×0.140 | 22-PIN SIP |
| DPD4848 | 64K×8 | 100 | 288 | 16 | 2400 | 3.000×0.625×0.150 | 30-PIN SIP |
| DPD4849 | 64K×9 | 100 | 324 | 18 | 3600 | 3.000×0.625×0.150 | 30-PIN SIP |

## 256K×1 DRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPD411M | 1MB×1 | 60 | 42 | 8 | N/A | 2.400×0.300×0.140 | 22-PIN SIP |
| DPD5124 | 512K×4 | 60 | 144 | 16 | N/A | 2.400×0.400×0.240 | 24-PIN SIP |
| DPD44256 | 256K×4 | 60 | 144 | 8 | N/A | 2.400×0.300×0.140 | 22-PIN SIP |
| DPD45256 | 256K×5 | 60 | 180 | 10 | N/A | 2.600×0.300×0.140 | 26-PIN SIP |
| DPD42568 | 256K×8 | 60 | 288 | 16 | N/A | 3.000×0.625×0.150 | 30-PIN SIP |
| DPD45269 | 256K×9 | 60 | 324 | 18 | N/A | 3.000×0.625×0.150 | 30-PIN SIP |
| DPD42568LL | 256K×8 | 60 | 288 | 16 | N/A | 3.000×0.625×0.150 | 30-PIN SIP |
| DPD42569LL | 256K×9 | 60 | 324 | 18 | N/A | 3.000×0.625×0.150 | 30-PIN SIP |
| DPD42568LP | 256K×8 | 60 | 288 | 16 | N/A | 3.000×0.425×0.150 | 30-PIN SIP |
| DPD42569LP | 256K×9 | 60 | 324 | 18 | N/A | 3.000×0.425×0.150 | 30-PIN SIP |

## 1MB×1 DRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPD414M* | 4MB×1 | 80 | 50 | 8 | N/A | 1.500×0.500×0.240 | 30-PIN SIP |
| DPD441M* | 1MB×4 | 80 | 200 | 8 | N/A | 1.500×0.500×0.240 | 30-PIN SIP |
| DPD4M8* | 4MB×8 | 80 | 400 | 64 | N/A | 3.000×1.200×0.240 | 60-PIN DIP |
| DPD1M8* | 1MB×8 | 80 | 400 | 16 | N/A | 3.200×0.725×0.240 | 30-PIN SIP |
| DP1M9* | 1MB×9 | 80 | 415 | 20 | N/A | 3.200×0.725×0.240 | 30-PIN SIP |

## 256K×4 DRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPD51240* | 512K×40 | 80 | 500 | 40 | N/A | 3.000×0.700×0.275 | 60-PIN DIP |

# VIDEO RAMS

## 64K×1 VIDEO RAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPO10V24 | 64K×16 | 100 | 640 | 160 | N/A | 2.600×0.900×0.240 | 52-PIN DIP |

## 64K×4 VIDEO RAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPO2564* | 256K×4 | 40 | 80 | 6 | 1600 | 2.600×0.900×0.240 | 52-PIN SIP |
| DPO5124* | 512K×4 | 40 | 100 | 24 | 6400 | 3.400×0.900×0.240 | 76-PIN SIP |
| DPO3848* | 384K×8 | 40 | 100 | 24 | 6400 | 2.900×0.500×0.800 | 56-PIN DIP |

## 8K×8 EEPROM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPE41129 | 16K× 8 | 60 | 48 | 6 | N/A | 1.400×0.600×0.240 | 28-PIN DIP |
| DPE40128 | 16K× 8 | 60 | 48 | 6 | N/A | 1.400×0.600×0.240 | 28-PIN DIP |
| DPE41193 | 24K× 8 | 60 | 51 | 9 | N/A | 1.400×0.600×0.240 | 28-PIN DIP |
| DPE40192 | 24K× 8 | 60 | 51 | 9 | N/A | 1.400×0.600×0.240 | 28-PIN DIP |
| DPE40256 | 32K× 8 | 60 | 54 | 12 | N/A | 1.400×0.600×0.240 | 28-PIN DIP |
| DPE41257 | 32K× 8 | 60 | 54 | 12 | N/A | 1.400×0.600×0.240 | 28-PIN DIP |
| DPE1224 | 128K× 8 | 60 | 90 | 48 | N/A | 2.400×1.400×0.240 | 48-PIN DIP |
| DPE1124 | 128K× 8 | 60 | 90 | 48 | N/A | 2.800×1.400×0.240 | 56-PIN DIP |
| DPE8M628 | 8K×16 | 60 | 96 | 12 | N/A | 2.000×0.600×0.240 | 40-PIN DIP |
| DPE8M656 | 16K×16 | 60 | 96 | 12 | N/A | 2.000×0.600×0.240 | 40-PIN DIP |

## 32K×8 EEPROM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPE4648 | 64K× 8 | 150 | 48 | 6 | N/A | 1.600×0.600×0.120 | 32-PIN DIP |
| DPE4968 | 96K× 8 | 150 | 51 | 9 | N/A | 1.600×0.600×0.120 | 32-PIN DIP |
| DPE41288 | 128K× 8 | 150 | 54 | 12 | N/A | 1.600×0.600×0.120 | 32-PIN DIP |
| DPE45128 | 512K× 8 | 150 | 90 | 48 | N/A | 2.400×1.400×0.240 | 48-PIN DIP |
| DPE45129* | 512K× 8 | 150 | 90 | 48 | N/A | 2.800×1.400×0.240 | 56-PIN DIP |
| DPE42568* | 256K× 8 | 150 | 40 | 2 | N/A | 3.200×0.600×0.240 | 64-PIN SIP |
| DPE42568* | 128K×16 | 150 | 60 | 2 | N/A | 3.200×0.600×0.240 | 64-PIN SIP |
| DPE45129* | 256K×16 | 150 | 135 | 48 | N/A | 2.800×1.400×0.240 | 56-PIN DIP |
| DPE8M624 | 64K×16 | 150 | 110 | 12 | N/A | 2.000×0.600×0.275 | 40-PIN DIP |
| DPE8M612 | 32K×16 | 150 | 108 | 12 | N/A | 2.000×0.600×0.275 | 40-PIN DIP |

# EPROMS

## 8K×8, 32K×8, 64K×8, 128K×8 and 64K×16 EPROM BASED MODULES

| PART NUMBER | ORGANIZATION | ELEMENT | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|---|
| | | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ (μA) | | |
| DPV8X16* | 8K×16 | 8K× 8 | 150 | 60 | 2 | 2 | 2.000×0.600×0.240 | 40-PIN DIP |
| DPV8X24* | 8K×24 | 8K× 8 | 150 | 90 | 3 | 3 | 2.400×0.600×0.240 | 48-PIN DIP |
| DPV8X32* | 8K×32 | 8K× 8 | 150 | 120 | 4 | 4 | 2.800×0.600×0.240 | 56-PIN DIP |
| DPV32X16* | 32K×16 | 32K× 8 | 150 | 60 | 2 | 2 | 2.000×0.600×0.240 | 40-PIN DIP |
| DPV32X24* | 32K×24 | 32K× 8 | 150 | 90 | 3 | 3 | 2.400×0.600×0.240 | 48-PIN DIP |
| DPV32X32* | 32K×32 | 32K× 8 | 150 | 120 | 4 | 4 | 2.800×0.600×0.240 | 56-PIN DIP |
| DPV128X16 | 128K×16 | 32K× 8 | 150 | 70 | 8 | 8 | 2.800×1.500×0.240 | 56-PIN DIP |
| DPV64X24* | 64K×24 | 64K× 8 | 150 | 90 | 3 | 3 | 2.400×0.600×0.240 | 48-PIN DIP |
| DPV64X32* | 64K×32 | 64K× 8 | 150 | 120 | 4 | 4 | 2.800×0.600×0.240 | 56-PIN DIP |
| DPV512X8* | 512K× 8 | 64K× 8 | 150 | 40 | 8 | 8 | 2.800×1.500×0.240 | 56-PIN DIP |
| DPV128X16B* | 128K×16 | 128K× 8 | 150 | 60 | 2 | 2 | 2.400×0.600×0.240 | 48-PIN DIP |
| DPV128X24B* | 128K×24 | 128K× 8 | 150 | 90 | 3 | 3 | 2.800×0.600×0.240 | 56-PIN DIP |
| DPV128X32* | 128K×32 | 128K× 8 | 150 | 120 | 4 | 4 | 3.200×0.600×0.240 | 64-PIN DIP |
| DPV1048X8* | 1048K× 8 | 128K× 8 | 150 | 45 | 8 | 8 | 2.200×1.300×0.240 | 44-PIN DIP |
| DPV512X16B* | 512K×16 | 128K× 8 | 150 | 70 | 8 | 8 | 2.600×1.500×0.240 | 48-PIN DIP |
| DPV256X32* | 256K×32 | 128K× 8 | 150 | 140 | 8 | 8 | 3.200×1.500×0.240 | 64-PIN DIP |
| DPV64X32B* | 64K×32 | 64K×16 | 150 | 60 | 4 | 8 | 3.200×1.500×0.240 | 64-PIN DIP |
| DPV128X32B* | 128K×32 | 64K×16 | 150 | 120 | 8 | 16 | 3.200×1.500×0.240 | 64-PIN DIP |
| DPV256X32B* | 256K×32 | 64K×16 | 150 | 140 | 16 | 32 | 3.200×1.500×0.240 | 64-PIN DIP |





When contacting suppliers, say you saw it in IC MASTER

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## VERSAPAC SRAM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ ($\mu$A) | | |
| DPS4X8V | 4K× 8 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS8X8V | 8K× 8 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS16X8V | 16K× 8 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS32X8V | 32K× 8 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS128X8V | 128K× 8 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS256X8V | 256K× 8 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS512X8V | 512K× 8 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS4X16V | 4K×16 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS8X16V | 8K×16 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS16X16V | 16K×16 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS32X16V | 32K×16 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS64X16V | 64K×16 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS128X16V | 128K×16 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS4X24V | 4K×24 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS16X24V | 16K×24 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS32X24V | 32K×24 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS64X24V | 64K×24 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS128X24V | 128K×24 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS4X32V | 4K×32 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS16X32V | 16K×32 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS32X32V | 32K×32 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS64X32V | 64K×32 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPS128X32V | 128K×32 | 35 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |

## VERSPAC EEPROM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ ($\mu$A) | | |
| DPE8X8V | 8K× 8 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE16X8V | 16K× 8 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE32X8V | 32K× 8 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE128X8V | 128K× 8 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE256X8V | 256K× 8 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE512X8V | 512K× 8 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE8X16V | 8K×16 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE16X16V | 16K×16 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE32X16V | 32K×16 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE64X16V | 64K×16 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE128X16V | 128K×16 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE8X24V | 8K×24 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE16X24V | 16K×24 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE32X24V | 32K×24 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE64X24V | 64K×24 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE128X24V | 128K×24 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE8X32V | 8K×32 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE16X32V | 16K×32 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE32X32V | 32K×32 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE64X32V | 64K×32 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |
| DPE128X32V | 128K×32 | 70 | TBD | TBD | N/A | 1.090×1.090×0.240 | 66-PIN PGA |

## VERSAPAC EPROM BASED MODULES

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | DIMENSIONS (INCHES) | PACKAGE |
|---|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ ($\mu$A) | | |
| DPV16X8V | 16K× 8 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV32X8V | 32K× 8 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV128X8V | 128K× 8 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV256X8V | 256K× 8 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV512X8V | 512K× 8 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV8X16V | 8K×16 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV16X16V | 16K×16 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV32X16V | 32K×16 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV64X16V | 64K×16 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV128X16V | 128K×16 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV2X24V | 2K×24 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV4X24V | 4K×24 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV8X24V | 8K×24 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV16X24V | 16K×24 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV32X24V | 32K×24 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV64X24V | 64K×24 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV128X24V | 128K×24 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV2X32V | 2K×32 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV4X32V | 4K×32 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV8X32V | 8K×32 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV16X32V | 16K×32 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV32X32V | 32K×32 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV64X32V | 64K×32 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |
| DPV128X32V | 128K×32 | 70 | TBD | TBD | TBD | 1.090×1.090×0.240 | 66-PIN PGA |

# DUAL-PORTED RAMS

## DUAL PORTED RAM MODULES - Advance Information

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | PACKAGE |
|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ ($\mu$A) | |
| DPP2X8 | 2K× 8 | 35 | TBD | TBD | TBD | 58-PIN DIP |
| DPP4X8 | 4K× 8 | 35 | TBD | TBD | TBD | 58-PIN DIP |
| DPP8X8 | 8K× 8 | 35 | TBD | TBD | TBD | 58-PIN DIP |
| DPP16X8 | 16K× 8 | 35 | TBD | TBD | TBD | 58-PIN DIP |
| DPP32X8 | 32K× 8 | 35 | TBD | TBD | TBD | 58-PIN DIP |
| DPP128X8 | 128K× 8 | 35 | TBD | TBD | TBD | 58-PIN DIP |
| DPP2X16 | 2K×16 | 35 | TBD | TBD | TBD | 64-PIN DIP |
| DPP4X16 | 4K×16 | 35 | TBD | TBD | TBD | 64-PIN DIP |
| DPP8X16 | 8K×16 | 35 | TBD | TBD | TBD | 64-PIN DIP |
| DPP16X16 | 16K×16 | 35 | TBD | TBD | TBD | 64-PIN DIP |
| DPP32X16 | 32K×16 | 35 | TBD | TBD | TBD | 64-PIN DIP |
| DPP64X16 | 64K×16 | 35 | TBD | TBD | TBD | 64-PIN DIP |
| DPP2X32 | 2K×32 | 35 | TBD | TBD | TBD | 84-PIN DIP |
| DPP4X32 | 4K×32 | 35 | TBD | TBD | TBD | 84-PIN DIP |
| DPP8X32 | 8K×32 | 35 | TBD | TBD | TBD | 84-PIN DIP |
| DPP16X32 | 16K×32 | 35 | TBD | TBD | TBD | 84-PIN DIP |
| DPP32X32 | 32K×32 | 35 | TBD | TBD | TBD | 84-PIN DIP |
| DPP64X32 | 64K×32 | 35 | TBD | TBD | TBD | 84-PIN DIP |



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## FLASH EEPROM MODULES - Advance Information

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | PACKAGE |
|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ ($\mu$A) | |
| DPZ8M628 | 8K×16 | 170 | TBD | TBD | N/A | 40-PIN DIP |
| DPZ8M656 | 16K×16 | 170 | TBD | TBD | N/A | 40-PIN DIP |
| DPZ8M624 | 64K×16 | 170 | TBD | TBD | N/A | 40-PIN DIP |
| DPZ8M612 | 32K×16 | 170 | TBD | TBD | N/A | 40-PIN DIP |
| DPZ48C512 | 64K× 8 | 170 | TBD | TBD | N/A | 32-PIN DIP |
| DPZ48C1024 | 128K× 8 | 170 | TBD | TBD | N/A | 32-PIN DIP |
| DPZ48C2048 | 256K× 8 | 170 | TBD | TBD | N/A | 32-PIN DIP |
| DPZ48C4096 | 512K× 8 | 170 | TBD | TBD | N/A | 32-PIN DIP |
| DPZ20488 | 2048K× 8 | 170 | TBD | TBD | N/A | 48-PIN DIP |

## FIFO MODULES

## FIFO MODULES - Advance Information

| PART NUMBER | ORGANIZATION | SPEED (ns) | TYPICAL DC CURRENT | | | PACKAGE |
|---|---|---|---|---|---|---|
| | | | $I_{CC1}$ (mA) | $I_{SB1}$ (mA) | $I_{CCDR}$ ($\mu$A) | |
| DPF2X9 | 2K× 9 | 35 | TBD | TBD | N/A | 28-PIN PGA |
| DPF4X9 | 4K× 9 | 35 | TBD | TBD | N/A | 28-PIN PGA |
| DPF8X9 | 8K× 9 | 35 | TBD | TBD | N/A | 28-PIN PGA |
| DPF16X9 | 16K× 9 | 35 | TBD | TBD | N/A | 28-PIN PGA |
| DPF32X9 | 32K× 9 | 35 | TBD | TBD | N/A | 28-PIN PGA |
| DPF128X9 | 128K× 9 | 35 | TBD | TBD | N/A | 28-PIN PGA |
| DPF2X18 | 2K×18 | 35 | TBD | TBD | N/A | 40-PIN PGA |
| DPF4X18 | 4K×18 | 35 | TBD | TBD | N/A | 40-PIN PGA |
| DPF8X18 | 8K×18 | 35 | TBD | TBD | N/A | 40-PIN PGA |
| DPF16X18 | 16K×18 | 35 | TBD | TBD | N/A | 40-PIN PGA |
| DPF32X18 | 32K×18 | 35 | TBD | TBD | N/A | 40-PIN PGA |
| DPF64X18 | 64K×18 | 35 | TBD | TBD | N/A | 60-PIN PGA |
| DPF2X36 | 2K×36 | 35 | TBD | TBD | N/A | 60-PIN PGA |
| DPF4X36 | 4K×36 | 35 | TBD | TBD | N/A | 60-PIN PGA |
| DPF8X36 | 8K×36 | 35 | TBD | TBD | N/A | 60-PIN PGA |
| DPF16X36 | 16K×36 | 35 | TBD | TBD | N/A | 60-PIN PGA |
| DPF32X36 | 32K×36 | 35 | TBD | TBD | N/A | 60-PIN PGA |
| DPF64X36 | 64K×36 | 35 | TBD | TBD | N/A | 60-PIN PGA |



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# Basic Theory of Operation
## Digital Synthesis Fundamentals

To learn about and understand Direct Digital Synthesis techniques, it is easiest to return to the very fundamentals of oscillation. Any oscillator generates a repetitive waveform, conceptualized by continuous travel around a circle. Each point on this circle, often referred to as the phase circle, corresponds to a particular point on the output waveform. Output signal accuracy depends on the precision with which this linear phase travel is performed. Typically the output waveform is sinusoid, but it does not have to be.

The heart of a digital oscillator is a circuit that corresponds to linear motion around the phase circle: the phase accumulator. The digital phase circle is divided into a specific number of points; one point for each number the accumulator can represent. For an N bit wide phase accumulator there are 2^N states and, therefore, 2^N separate points on the phase circle. Resolution increases very rapidly with more bits; eight bits provides 256 points a little more than one degree apart, twenty bits provides over one million points, and thirty two bits provide over four BILLION individual points. Travel around the digital phase circle is quite precise, as each point is uniquely identified to a single phase accumulator state. The input number to the phase accumulator (**M**) represents the 'jump size', or how many points on the circle to skip when going to the next one. This jump occurs each time a clocking pulse is received from the timebase. Dividing this phase change by the timebase period gives the digital oscillator's rate of change of phase: frequency. In the digital oscillator then, the output frequency (**fout**) is dependent on three parameters; the actual frequency of the timebase oscillator (**fclk**), the length of the phase accumulator (**N**), and the tuning input number (**M**), related by **equation (1)**. Each of these can easily be tightly controlled, so the digital oscillator exhibits outstanding performance in frequency stability, accuracy, resolution, and agility.

$$fout = \frac{fclk}{2^N} * M \qquad (1)$$

Following the phase accumulator is the Waveform Map, which tells the digital oscillator what the output wave shape is to be. In the waveform map the value of the desired output waveform is stored for each phase value. The digital oscillator imposes no restrictions on wave shape. Any number can be stored for each phase position, so sinewaves are simply a particularly popular application.

After the waveform map, enough is known to do the conversion from digital numbers to analog voltage. This analog conversion completes the basic digital oscillator, and accuracy is essential to maintain signal quality. Each value from the waveform map is a number of finite precision. To obtain the maximum performance from the digital oscillator these converted voltages must closely resemble what the continuous time waveform would ideally be.

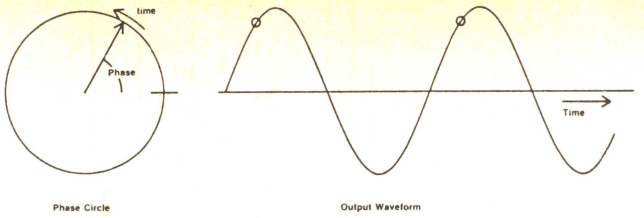



Figure 1 **Circular Oscillator Model**

| N | Number of Points |
|---|---|
| 8 | 256 |
| 12 | 4096 |
| 16 | 65536 |
| 20 | 1,048,576 |
| 24 | 16,777,216 |
| 28 | 268,435,456 |
| 32 | 4,294,967,296 |

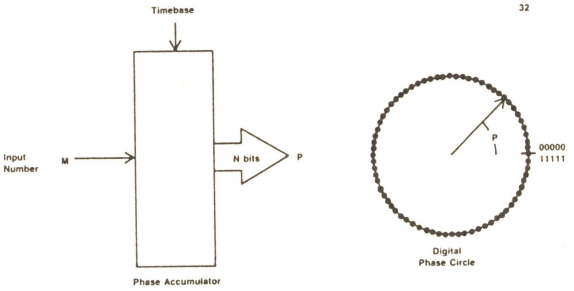



Figure 2 **Phase Accumulator Oscillator**

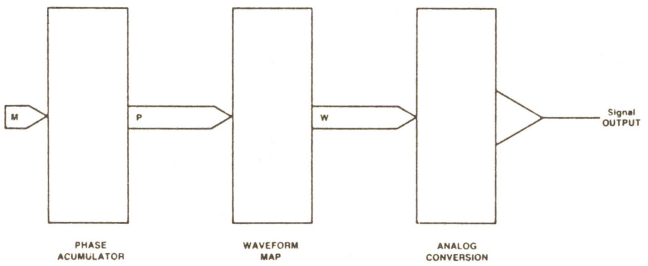



Figure 4 **Basic Digital Oscillator**

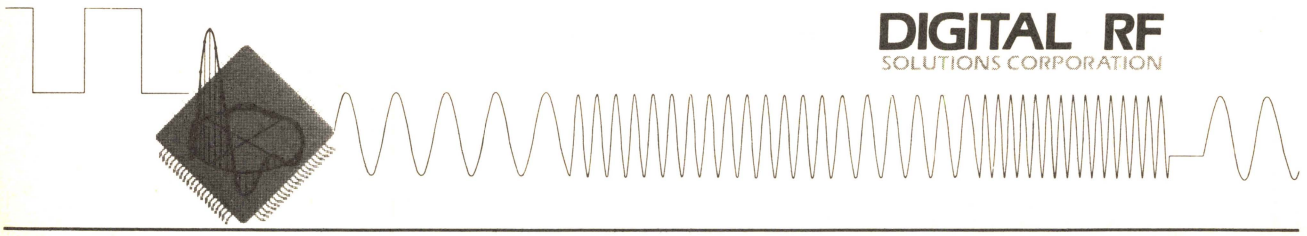
Direct Digital Synthesizer (DDS)
Number Controlled Oscillator (NCO)

To examine tuning linearity of the digital oscillator refer to **equation(1)**. With both the timebase frequency and phase accumulator length fixed, their ratio is constant, and this tuning equation takes on the form of a straight line through the origin. From this several conclusions are immediately drawn:

1) The digital oscillator tunes linearly over its entire range.
2) DC is within the tuning range, since M can be set to zero.
3) Tuning sensitivity is set by the timebase frequency and phase accumulator length.
4) Frequency accuracy will match the accuracy of the tuning input number M.
5) Frequency stability will match that of the timebase, when the tuning input number M is constant.

When a frequency change is performed, the phase accumulator simply continues on from its current phase value at the new rate. Frequency changes therefore occur very rapidly and in a phase continuous manner.

Since it works with numbers, the digital oscillator is a sampled data system and is subject to the Nyquist criteria for proper waveform reconstruction. In particular, the maximum output frequency is half of the timebase frequency, since at least two samples are needed to accurately reconstruct a sinusoid. If a non-sinusoidal waveform is being generated, the limit may well be much lower.



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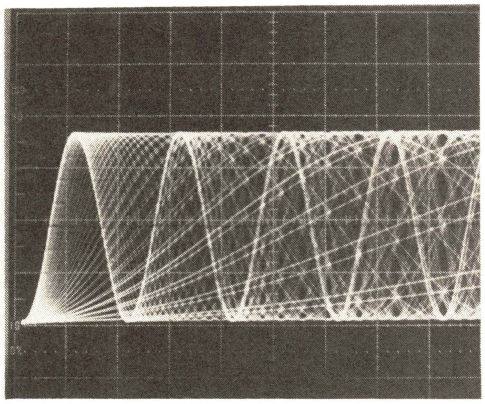
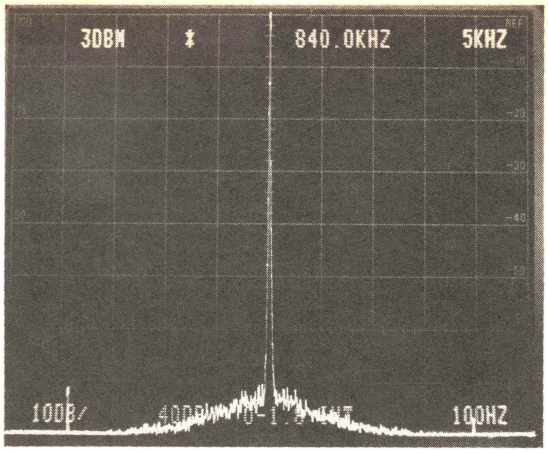
# Applications Ideas

## Signal Generator

Of primary importance to modern RF communications systems is residual noise in oscillators. This measure of short term (nanoseconds to about onesecond) instability directly affects the overall system signal to noise ratio and can severely limit dynamic range. Digital oscillators inherit both their short term and long term stabilities from the timebase used. Timebase oscillators, being single frequency devices, are designed to provide minimal drift and residual noise characteristics. As a result, digital oscillators also possess these qualities.

Optimization to particular applications is easily accomplished by using the most appropriate input tuning mode and waveform map. Any questions regarding particular applications and optimization strategy may be discussed with **Digital RF Solutions** at **(408) 727-5995** or outside California (800)782-NCMO.






## Sweep Oscillator

A sweep oscillator has a variable frequency with time, usually linear upor linear down. With two ways to control the frequency of the **NCMO** a sweep oscillator is readily achieved. For a base frequency sweep oscillator, the sweep start frequency is set through the tuning inputs. Linear sweep requires the simple connection of a digital counter to the modulation port. The number on the modulation port is directly added to the tuning information to set the actual operating frequency of the **NCMO**. To build a centered sweep oscillator, the modulation port needs to be connected up slightly differently. The **MSB** of the sweep counter is inverted and connected to all higher order input bits. The **NCMO** interprets this assigned arithmetic, producing lower frequencies when the **MSB** is zero (inverter output is high) and higher frequencies when the **MSB** changes state.

Fancier sweep strategies can be effected with further complexity in the drive circuitry, including very complex frequency hopping driven by computer. NOTE: SPURIOUS RESPONSES CAN BE MINIMIZED OR ELIMINATED BY SYNCHRONIZING THE FREQUENCY CHANGE COMMANDS WITH THE NCMO TIMEBASE. Additional minimization of sideband energy can be achieved by synchronizing frequency change commands with **PA-COUT** (Phase Accumulator Carry OUTput). This causes frequency (phase slope) changes to occur at signal peaks, where signal slope is zero.

## Amplitude Modulation

Amplitude modulation (**AM**) of the digital oscillator is achieved with theinclusion of the **DRFS-2400 Digital Amplitude Modulator** (**DAM**). Since amplitude is a property of the specific waveform used, it must be controlled following the waveform map.

Fully signed modulation allows generation of both suppressed carrier and full carrier signals. Use of the sign bit (**MSB**) produces phase reversals in the carrier, which nulls the carrier whenever the modulating waveform is symmetrical. Double sideband - suppressed carrier (**DSB-SC**) **AM** is the result.

To maintain carrier in the signal, carrier phase reversals must not be produced. Typically the **MSB** is set to 0 (grounded), eliminating a phase shift in the **DAM**. Double sideband (**DSB**) **AM** with **full carrier - standard AM** results.

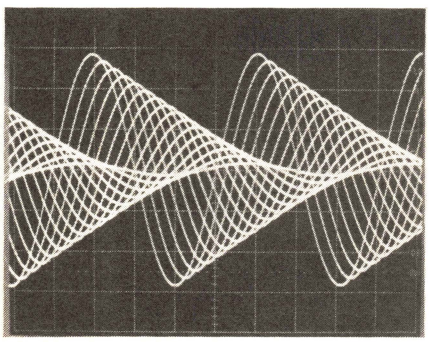
## Polar Data Modulation PDM(tm)

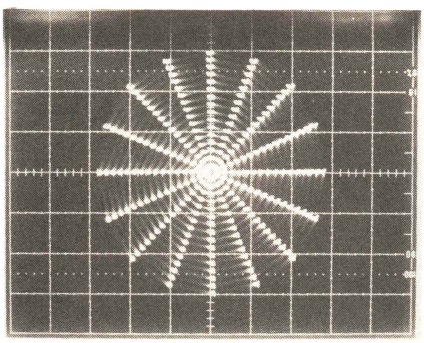
With direct, digital control of the **NCMO** signal output, the designer can independently specify any desired amplitude and phase shift. Independent control of amplitude and phase is equivalent to the polar definition of a vector.Therefore the combination of phase and amplitude modulation of the **NCMO** constitutes vector modulation, also known as **Polar Data Modulation** (**PDM** tm).

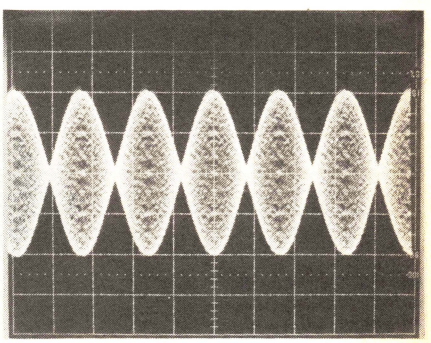
Any signalling constellation can be described in polar, as well as rectangular coordinates. Storing the constellation in a memory, which produces the desired amplitude and phase information for each data combination, is all that is needed for construction of a **Vector Modulated Oscillator** (**VMO** tm).

The **DRFS-2250 NCMO** is directly capable of 12 bits (4096 points) of phase shift, with 12 bits (4096 levels) of amplitude modulation. These provide 4096* 4096 = 16,777,216 separate vectors available for defining the signal constellation - more than enough to support current systems, in addition to those in the foreseeable future.

By storing not just the desired constellation points (in polar form), but also the desired tran sition between each, a very tightly controlled signal spectrum can be realized. Shaping of each tran sition is independent, and set in the time domain. Such capability frees the signal designer from shapes restricted by filter responses, and allows transition types to be independently optimized in various parts of any signalling constellation. Direct control of signalling transitions within a constellation is referred to as **Signal Transition Mapping** (**STM**).







## PIN DESCRIPTIONS

| Pin 84 PLCC | Pin F-80 | Name Comments | Description |
|---|---|---|---|
| 73 | 1 | VDD | (+5VDC) |
| 75 | 2 | T21 | Tuning word bit 21 (parallel mode) |
| 76 | 3 | T20 | Tuning word bit 20 (parallel mode) |
| 77 | 4 | OB/T19 | Optical Encoder line B (count mode)<br>Tuning word bit 19 (parallel mode) |
| 78 | 5 | OA/T18 | Optical Encoder line A (count mode)<br>Tuning word bit 18 (parallel mode) |
| 79 | 6 | R2/T17 | Optical Encoder count Rate control bit 2<br>Tuning word bit 17 (parallel mode) |
| 80 | 7 | R1/T16 | Optical Encoder count Rate control bit 1<br>Tuning word bit 16 (parallel mode) |
| 81 | 8 | R0/T15 | Optical Encoder count Rate control bit 0<br>Tuning word bit 15 (parallel mode) |
| 82 | 9 | T14 | Tuning word bit 14 (parallel mode) |
| 83 | 10 | T13 | Tuning word bit 13 (parallel mode) |
| 84 | 11 | T12 | Tuning word bit 12 (parallel mode) |
| 1 | 12 | VSS | Ground (0VDC) |
| 2 | 13 | T11 | Tuning word bit 11 (parallel mode) |
| 3 | 14 | RD/T10 | Data bus ReaD pulse (active low)<br>Tuning word bit 10 (parallel mode) |
| 4 | 15 | A1/T9 | Bus data word Address bit 1<br>Tuning word bit 9 (parallel mode) |
| 5 | 16 | A0/T8 | Bus data word Address bit 0<br>Tuning word bit 8 (parallel mode) |
| 6 | 17 | B7/T7 | Data Bus bit 7 (bus mode)<br>Tuning word bit 7 (parallel mode) |
| 7 | 18 | B6/T6 | Data Bus bit 6 (bus mode)<br>Tuning word bit 6 (parallel mode) |
| 7 | 19 | B5/T5 | Data Bus bit 5 (bus mode)<br>Tuning word bit 5 (parallel mode) |
| 9 | 20 | B4/T4 | Data Bus bit 4 (bus mode)<br>Tuning word bit 4 (parallel mode) |
| 10 | 21 | B3/T3 | Data Bus bit 3 (bus mode)<br>Tuning word bit 3 (parallel mode) |
| 11 | 22 | B2/T2 | Data Bus bit 2 (bus mode)<br>Tuning word bit 2 (parallel mode) |
| 13 | 23 | B1/T1 | Data Bus bit 1 (bus mode)<br>Tuning word bit 1 (parallel mode) |
| 14 | 24 | B0/T0 | Data Bus bit 0 (bus mode)<br>Tuning word bit 0 (parallel mode) |
| 15 | 25 | VSS | Ground (0VDC) |
| 16 | 26 | P0 | Phase output word bit 0 |
| 17 | 27 | P1 | Phase output word bit 1 |
| 18 | 28 | P2 | Phase output word bit 2 |
| 19 | 29 | P3 | Phase output word bit 3 |
| 20 | 30 | P4 | Phase output word bit 4 |
| 21 | 31 | P5 | Phase output word bit 5 |
| 22 | 32 | P6 | Phase output word bit 6 |
| 23 | 33 | P7 | Phase output word bit 7 |
| 24 | 34 | P8 | Phase output word bit 8 |
| 25 | 35 | P9 | Phase output word bit 9 |
| 26 | 36 | P10 | Phase output word bit 10 |
| 27 | 37 | P11 | Phase output word bit 11 |
| 28 | 38 | UP/UD | Phase count Up and Down (high level)<br>Phase count UP only (low level) |
| 29 | 39 | TEST | output TEST pin<br>show upper 12 bits (high level / open)<br>show lower 12 bits (low level) |
| 30 | 40 | VDD | (+5VDC) |
| 31 | 41 | VDD | (+5VDC) |
| 33 | 42 | MOD0 | Modulation word bit 0 |
| 34 | 43 | MOD1 | Modulation word bit 1 |
| 35 | 44 | MOD2 | Modulation word bit 2 |
| 36 | 45 | MOD3 | Modulation word bit 3 |
| 37 | 46 | MOD4 | Modulation word bit 4 |
| 38 | 47 | MOD5 | Modulation word bit 5 |
| 39 | 48 | MOD6 | Modulation word bit 6 |
| 40 | 49 | MOD7 | Modulation word bit 7 |
| 41 | 50 | MOD8 | Modulation word bit 8 |
| 42 | 51 | MOD9 | Modulation word bit 9 |
| 43 | 52 | MOD10 | Modulation word bit 10 |
| 44 | 53 | MOD11 | Modulation word bit 11 |
| 45 | 54 | MOD12 | Modulation word bit 12 |
| 46 | 55 | MOD13 | Modulation word bit 13 |
| 47 | 56 | MOD14 | Modulation word bit 14 |
| 48 | 57 | MOD15 | Modulation word bit 15 |

## PIN DESCRIPTIONS

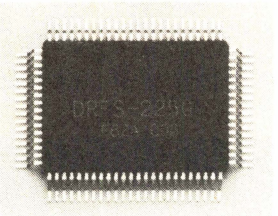
| Pin 84 PLCC | Pin F-80 | Name Comments | Description |
|---|---|---|---|
| 49 | 58 | MOD16 | Modulation word bit 16 |
| 50 | 59 | MOD17 | Modulation word bit 17 |
| 51 | 60 | MOD18 | Modulation word bit 18 |
| 52 | 61 | MOD19 | Modulation word bit 19 |
| 53 | 62 | MOD20 | Modulation word bit 20 |
| 55 | 63 | MOD21 | Modulation word bit 21 |
| 56 | 64 | MOD22 | Modulation word bit 22 |
| 57 | 65 | VSS | Ground (0VDC) |
| 58 | 66 | MOD23 | Modulation word bit 23 |
| 59 | 67 | PA-COUT | Phase Accumulator cascade Carry OUT |
| 60 | 68 | CLKOUT | clock oscillator feedback (crystal mode)<br>CLocK CMOS OUTput |
| 61 | 69 | CLKIN | CLocK oscillator INput (crystal mode)<br>CMOS timebase input (driven / synchronous mode) |
| 62 | 70 | FM-COUT | Frequency Modulation cascade Carry OUT |
| 63 | 71 | FM/PM | modulation select –<br>Frequency Modulation (high level / open)<br>Phase Modulation (low level) |
| 64 | 72 | TC-COUT | Tuning serial Counter cascade Carry OUT |
| 65 | 73 | SERCNT | tuning SERial CouNTer mode select (active low)<br>SERCNT overrides PR/BUS |
| 66 | 74 | TC-CIN | Tuning serial Counter cascade Carry IN |
| 67 | 75 | FM-CIN | Frequency Modulation cascade Carry IN |
| 68 | 76 | PR/BUS | input mode select –<br>PaRallel mode, all 24 bits direct (high level)<br>BUS mode, 8 bits wide – 3 registers (low level) |
| 69 | 77 | PA-CIN | Phase Accumulator cascade Carry IN |
| 70 | 78 | T23 | Tuning word bit 23 (parallel mode) |
| 71 | 79 | T22 | Tuning word bit 22 (parallel mode) |
| 72 | 80 | RESET | NCMO RESET pin forces the phase accumulator to all ones (1111 1111 1111), asynchronous of the clock Active LOW, level sensitive |

## Ordering Information

| Package Type | Clock Speed | Operating Temperature | Part number |
|---|---|---|---|
| 80 pin Flatpack | 15 MHz | 0C to 70C | DRFS-2250-15FC |
| | 20 MHz | " | DRFS-2250-20FC |
| | 25 MHz | " | DRFS-2250-25FC |
| 84 PLCC | 15 MHz | 0C to 70C | DRFS-2250-15JC |
| | 20 MHz | " | DRFS-2250-20JC |
| | 25 MHz | " | DRFS-2250-25JC |
| | 15 MHz | -20C to 85C | DRFS-2250-15JI |
| | 20 MHz | " | DRFS-2250-20JI |
| | 25 MHz | " | DRFS-2250-25JI |

For full military temperature rated components, consult the factory for detailed information.

The Digital RF Solutions Corporation is continuously improving and expanding its product lines. DRFS reserves the right to improve product specifications without notice to provide its customers with the highest value and quality products possible.



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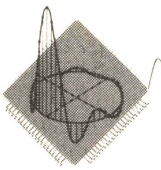

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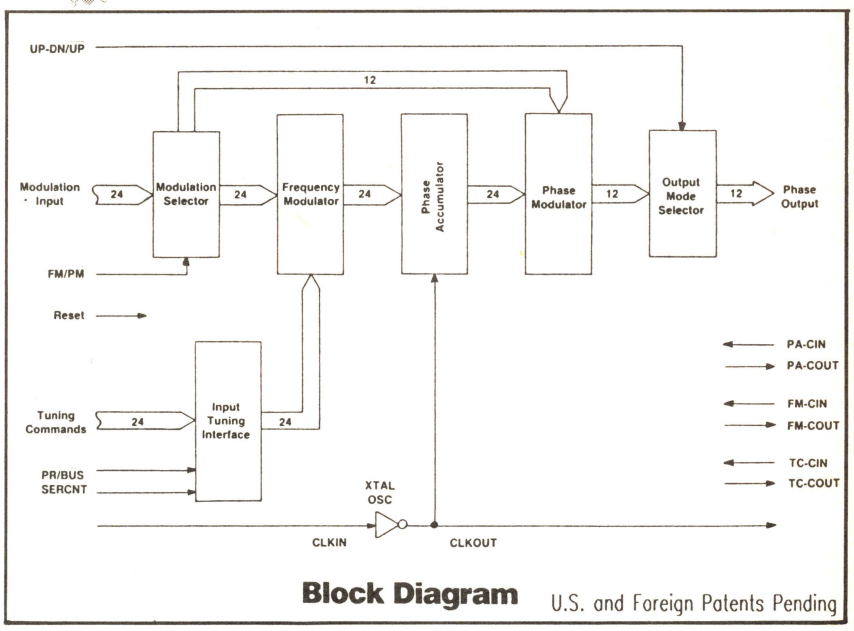
# DRFS-2250

## NCMO – Number Controlled Modulated Oscillator

### FEATURES

- 12 bit phase output resolution
- Angle modulation
  - frequency
  - phase
- Modulation bandwidth includes DC
- High clock frequency: to 25 MHz
- Sinusoid synthesis from DC to 12.5 MHz
- Extremely rapid frequency changes: two clock periods (100 nanoseconds with a 20 MHz clock)
- Cascadable for nano-Hertz resolution
- Short and long term stability matches the timebase tone
- Three tuning input modes:
  - parallel
  - bus
  - serial
- Completely general output waveform
- Internal pull-ups on all inputs
- CMOS technology for low power consumption
- Surface mount packaging




**Block Diagram** U.S. and Foreign Patents Pending

## GENERAL DESCRIPTION

The DRFS-2250 NCMO provides a new basic oscillator technology. Using digital techniques, the Number Controlled Modulated Oscillator (NCMO) provides the RF communications industry with a cost-effective, low noise signal source which simultaneously features high stability, fine resolution and rapid switchability. Two NCMO devices can be cascaded for nano-Hertz frequency resolution. Frequency modulation can be effected over the entire tuning range, including cascading over multiple devices. Phase modulation resolution exceeds 0.1 degree. For symmetrical output waveforms, the phase output is configurable to count up during half the period and then count down to return to zero.

Input interface circuitry is included to simplify application in the three basic tuning modes: 24 bit direct parallel, 8 bit bus, and quadrature clocked serial (used in many encoders).

## AC Characteristics

VDD = 5.00VDC, unless otherwise stated

| Parameter | Symbol | DRFS 2250-15 MIN | TYP | MAX | DRFS 2250-20 MIN | MAX | DRFS 2250-25 MIN | MAX | Units |
|---|---|---|---|---|---|---|---|---|---|
| Clock Frequency | Fclk | 15 | 18 | | 20 | | 25 | | MHz |
| Output Transitions: | | | | | | | | | |
| Rise Time | tr | | | 10 | | 10 | | 10 | ns(1) |
| Fall Time | tf | | | 10 | | 10 | | 10 | |
| Input Timing (Bus Mode): | | | | | | | | | |
| Setup Time | tsu | 10 | | | 10 | | 10 | | ns |
| Read Pulsewidth | PW | 25 | | | 25 | | 25 | | ns |

## DC Characteristics

| Parameter | Symbol | MIN | TYP | MAX | Units | Conditions |
|---|---|---|---|---|---|---|
| Static Current | IQ | – | – | 10 | uA | VIN = VDD or VSS<br>IOH = IOL = 0 |
| Input Leakage | IL | -1 | – | 1 | uA | VDD = 5.25V<br>VIH = VDD<br>VIL = VSS |
| Input High Voltage | | | | | | |
| CLKIN | | 3.5 | – | – | V | |
| All other inputs | VIH | 2.2 | – | – | | VDD = 5.25V |
| Input Low Voltage | | | | | | |
| CLKIN | | – | – | 1.0 | V | |
| All other inputs | VIL | – | – | 0.6 | | VDD = 4.75V |
| Input Pull-up Resistance | Rpu | 55 | – | 1000 | Kohm | VDD = 5.0V |
| Output Voltages: | | | | | | |
| High Level | VOH | VDD 0.4 | – | | V | VDD = 4.75V<br>IOH = -2mA |

## Absolute Maximum Ratings

| Parameter | Symbol | Limits | Units |
|---|---|---|---|
| Power Supply Voltage | VDD | VSS-0.3 to 7.0 | Volts |
| Input Voltage | VIN | VSS-0.3 to VDD + 0.3 | Volts |
| Output Voltage | VOUT | VSS-0.3 to VDD + 0.3 | Volts |
| Output Curren | IOUT | +/-10 | mA |
| Power Dissipation | PD | 300 | mW |
| Storage Degrees | Tstg | -55 to +125 | degrees C |

## Recommended Operating Conditions

Note: VSS = 0V VDD =5.0V

| Parameter | Symbol | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|
| Power Supply Voltage | VDD | 4.75 | 5.00 | 5.25 | Volts |
| Input Voltage | VIN | VSS | | VDD | Volts |
| Operating Temperature: | Topr | | | | |
| Commercial Grade (C) | | 0 | | +70 | degrees C |
| Industrial Grade (I) | | -20 | | +85 | degrees C |

## ESD Caution

The DRFS-2250 NCMO is a static sensitive device. All inputs are protected, however it is recommended that all handling of these parts follow approved static-free procedures. Unused devices should be stored in a conductive environment.



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# Analog Signal Processing Integrated Circuits

| | | Pkg Pins | Max Input Signal Frequency (KHz) | Max Ext. Clk (MHz) | Description |
|---|---|---|---|---|---|
| Analog/Audio Delay Lines | RD5106A | 8 | 170 | 1 | 256-sample analog/audio delay with driver and S/H output. Delay from 512 sec to 1 sec. |
| | RD5107A | 8 | 170 | 1 | 512-sample analog/audio delay with driver and S/H output. Delay from 1.02 msec to 2 sec. |
| | RD5108A | 8 | 170 | 1 | 1024-sample analog/audio delay with driver and S/H output. Delay from 2.05 msec to 4 sec. |
| General Purpose Filters (Switched Capacitor) | RM5604A | 16 | 350 | 1.4 | Triple 1/3 octave bandpass filter |
| | RM5605A | 16 | 350 | 1.4 | Double 1/2 octave bandpass filter |
| | RM5606A | 16 | 350 | 1.4 | Single 1 octave bandpass filter |
| | RF5609A | 8 | 625 | 2.5 | 7th order elliptical lowpass |
| | RF5611A | 8 | 625 | 2.5 | 5th order Chebychev highpass |
| | RF5612A | 8 | 625 | 2.5 | 4th order Notch |
| | RF5613A | 8 | 625 | 2.5 | 7th order linear phase lowpass |
| | RF5614A | 8 | 250 | 1 | 6th order single 1/3 octave bandpass |
| | RF5615A | 8 | 250 | 1 | 6th order single 1/2 octave bandpass |
| | RF5616A | 8 | 250 | 1 | 6th order single 1 octave bandpass |
| | RF6651 | 24 | 56/28/56 | 3.58 | C-message/1010 Hz notch/program weighting combo |
| Modem Filters (Switched Capacitor) | RM5630A | 16 | 125 | 1 | Bell 103 compatible, 300 baud, full duplex. |
| | RM 5631A | 16 | 125 | 1 | CCITT V.21 compatible, 200/300 baud, full duplex. |
| | RM5632A | 24 | 38.4 | .1536 | Bell 212A/CCITT V.22, 1200 bps, full duplex. |
| | RM5635A | 16 | 38.4 | .1536 | CCITT V.22 bis compatible, 2400 bps, full duplex. |
| | RM5636B | 22 | 28.8 | 3.6864 | Bell 201/CCITT V.26 compatible, 2400 bps filter combo. |
| | RM5637A | 22 | 28.8 | 3.6864 | Bell 208/CCITT V.27 compatible, 4800 bps filter combo. |
| | RM5638A | 16 | 3.- -8.8 | 3.6864 | Bell 209/CCITT V.29 compatible, 9600 bps filter combo. Contains a receiver bandpass filter, a fixed compromise delay equalizer filter, and a transmit lowpass filter. |
| Universal Active Filters (Switched Capacitor) | RU5620A | 18 | 312 | 1.25 | One 2nd order, corner frequency and Q digital-programmable. |
| | RU5621A | 14 | 375 | .75 | Two 2nd order sections, resistor-programmable. |
| | RU5622A | 20 | 375 | .75 | Four 2nd order sections, resistor-programmable. |
| Transversal Filters /Special Signal Processing | RT5601AA | 22 | 1000 | 2 | Non-windowed, quad-chirped 512-point DFT. |
| | RT5601AB | 22 | 1000 | 2 | Hanning-windowed quad-chirped 512-point DFT. |
| | RT5601BB | 22 | 5000 | 10 | Buried-channel windowed 512-point DFT. |
| | RT5602AA | 16 | 500 | 4 | 64-stage lowpass transversal filter. |
| | RT5602AC | 16 | 500 | 4 | 64-stage bandpass transversal filter. |
| | RT5602AG | 16 | 500 | 4 | Hanning-windowed sine chirp (64 stages). |
| | RT5602AH | 16 | 500 | 4 | Hanning-windowed cosine chirp (64 stages). |

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

| Device | Features | Applications | Part No. | Temp. | Pins/Pkge. |
|---|---|---|---|---|---|
| **EL2003** | **VIDEO LINE DRIVER** | | | | |
| | • 1200 V/µs Slew Rate | Op Amp Booster | EL2003CH | I | 8 TO-99 |
| | • 100 MHz BW | Coax Cable Driver | EL2003CJ | I | 8 CDIP |
| | • Short Circuit Protected | Capacitive Load Buffer | EL2003CN | I | 8 PDIP |
| | | | EL2003H | M | 8 TO-99 |
| | | | EL2003J | M | 8 CDIP |
| | | | EL2003H-8 | M | 8 TO-99 |
| | | | EL2003J-8 | M | 8 CDIP |
| **EL2004** | **350 MHz FET BUFFER** | | | | |
| | • 2500 V/µs Slew Rate | ATE Pin Driver | EL2004CG | I | 12 TO-8 |
| | • ±5 V to ±15 V Supplies | Video Line Driver | EL2004CL | I | 52 LCC |
| | • 250 mA Peak Output | Instrumentation Buffer | EL2004G | M | 12 TO-8 |
| | | | EL2004G/883 | M | 12 TO-8 |
| | | | EL2004L | M | 52 LCC |
| | | | EL2004L/883 | M | 52 LCC |
| **EL2005** | **HIGH ACCURACY BUFFER** | | | | |
| | • 140 MHz BW | A/D Converter Buffer | EL2005CG | I | 12 TO-8 |
| | • 50 pA Input Current | Nuclear Instruments | EL2005G | M | 12 TO-8 |
| | • 2 mV Input Offset | Sample/Hold Amplifiers | EL2005G/883 | M | 12 TO-8 |
| **EL2006** | **PRECISION HIGH SPEED FET AMPLIFIER** | | | | |
| | • High Gain - 86 dB | High Speed Integrators | EL2006CG | I | 12 TO-8 |
| | • 250 MHz Gain BW | Pulse Amplifiers | EL2006CL | I | 52 LCC |
| | • Low Offset Voltage Drift | Video Amplifiers | EL2006G | M | 12 TO-8 |
| | | | EL2006G/883 | M | 12 TO-8 |
| | | | EL2006L | M | 52 LCC |
| | | | EL2006L/883 | M | 52 LCC |
| **EL2007** | **PRECISION SERVO DRIVER** | | | | |
| | • Single Supply Operation | Disc Drive Voice Coil Driver | EL2007- 2CD | C | 24 DIP |
| | • Class "B" and "D" | Robotics Servo Driver | | | |
| | • High Efficiency | Gyro Platform Driver | | | |
| | • Low Output SAT-1.5 V @ 2 A | | | | |
| **EP2015** | **350 MHz QUAD PNP** | | | | |
| | • 1 mV $\Delta V_{be}$ | Current Sources | EP2015ACJ | C | 14 CDIP |
| | • 5 % $\Delta h_{fe}$ | Current Mirrors | EP2015ACN | C | 14 PDIP |
| | • 150 min $h_{fe}$ | Log Amps | EP2015AJ | M | 14 CDIP |
| | | Multipliers | EP2015AJ-8 | M | 14 CDIP |
| | | | EP2015CJ | C | 14 CDIP |
| | | | EP2015CN | C | 14 PDIP |
| | | | EP2015J | M | 14 CDIP |
| | | | EP2015J-8 | M | 14 CDIP |
| **EN2016** | **300 MHz QUAD NPN** | | | | |
| | • 1 mV $\Delta V_{be}$ | Current Sources | EN2016ACJ | C | 14 CDIP |
| | • 5 % $\Delta h_{fe}$ | Current Mirrors | EN2016ACN | C | 14 PDIP |
| | • 150 min $h_{fe}$ | Log Amps | EN2016AJ | M | 14 CDIP |
| | | Multipliers | EN2016AJ-8 | M | 14 CDIP |
| | | | EN2016CJ | C | 14 CDIP |
| | | | EN2016CN | C | 14 PDIP |
| | | | EN2016J | M | 14 CDIP |
| | | | EN2016J-8 | M | 14 CDIP |
| **EL2017** | **SERVO CONTROLLER** | | | | |
| | • Complete Servo Loop | Voice Coil Drivers | EL2017CJ | C | 20 CDIP |
| | • Class "B" and "D" | Remote Camera Positioning | EL2017CN | C | 20 PDIP |
| | • Single Supply | Missile Servo Controls | EL2017J | M | 20 CDIP |
| | | | EL2017J/883 | M | 20 CDIP |
| **EL2018** | **FAST HIGH VOLTAGE COMPARATOR W/LATCH** | | | | |
| | • 20 ns tpd | ATE Pin Receivers | EL2018CH | I | 8 TO-99 |
| ✯ | • 20 V differential | A/D Converters | EL2018CJ | I | 8 CDIP |
| | • 20k Gain | Zero Crossing Detectors | EL2018CN | I | 8 PDIP |
| | • 3 State TTL Output | Window Comparators | EL2018H | M | 8 TO-99 |
| | | | EL2018H-8 | M | 8 TO-99 |
| | | | EL2018J | M | 8 CDIP |
| | | | EL2018J-8 | M | 8 CDIP |

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

| Device | Features | Applications | Part No. | Temp. | Pins/Pkge. |
|---|---|---|---|---|---|
| **EL2019** | **FAST HIGH VOLTAGE COMPARATOR W/MASTER SLAVE FLIP FLOP** | | | | |
| ✯ | • 15 ns tpd | ATE Pin Receivers | EL2019CH | I | 8 TO-99 |
| | • 20 V differential | A/D Converters | EL2019CJ | I | 8 CDIP |
| | • Infinite Gain | Zero Crossing Detectors | EL2019CN | I | 8 PDIP |
| | • 3 State TTL Output | Window Comparators | EL2019H | M | 8 TO-99 |
| | | | EL2019H-8 | M | 8 TO-99 |
| | | | EL2019J | M | 8 CDIP |
| | | | EL2019J-8 | M | 8 CDIP |
| **EL2020** | **50 MHz CURRENT MODE FEEDBACK AMPLIFIER** | | | | |
| | • 50 MHz BW | Video Gain Block | EL2020CJ | I | 8 CDIP |
| | • 500 V/µs Slew Rate | Coax Cable Driver | EL2020CN | I | 8 PDIP |
| | • 50 ns 1% Settling | I to V Converter | EL2020J | M | 8 CDIP |
| | • 33 mA Output | Radar Systems | EL2020J-8 | M | 8 CDIP |
| **EL2022** | **165 MHz CURRENT MODE FEEDBACK AMPLIFIER** | | | | |
| | • 165 MHz BW | Video Gain Block | EL2022CG | I | 12 TO-8 |
| ✯ | • 3000 V/µs Slew Rate | A/D Converters | EL2022G | M | 12 TO-8 |
| | • 22 ns 0.1% Settling | DAC Output Amp | EL2022G/883 | M | 12 TO-8 |
| | • 100 mA Output | Radar | | | |
| **EL2033** | **VIDEO LINE DRIVER** | | | | |
| | • 1200 V/µs Slew Rate | Op Amp Booster | EL2033CJ | I | 8 CDIP |
| | • 100 MHz BW | Coax Cable Driver | EL2033CN | I | 8 PDIP |
| | • Replaces 5002, 5033 | Capacitive Load Buffer | EL2033J | M | 8 CDIP |
| | • Short Circuit Protected | | EL2033J-8 | M | 8 CDIP |
| **EL2039** | **VERY HIGH SLEW, WIDE BAND OP AMP** | | | | |
| | • 600 MHz Gain BW | Pulse Amps | EL2039CJ | C | 14 CDIP |
| ✯ | • 600 V/µs Slew Rate | Sample and Holds | EL2039CN | C | 14 PDIP |
| | • 15k Gain | RF Oscillators | EL2039J | M | 14 CDIP |
| | • 13 mA Supply Current | | EL2039J/883 | M | 14 CDIP |
| | | | EL2039L/883 | M | 20 LCC |
| **EL2040** | **WIDE BAND, FAST SETTLING OP AMP** | | | | |
| | • 400 MHz Gain BW | Pulse Amps | EL2040CJ | C | 14 CDIP |
| ✯ | • 400 V/µs Slew Rate | Sample and Holds | EL2040CN | C | 14 PDIP |
| | • 200 ns Settling | RF Oscillators | EL2040J | M | 14 CDIP |
| | • 13 mA Supply Current | | EL2040J/883 | M | 14 CDIP |
| | | | EL2040L/883 | M | 20 LCC |
| **EL2041** | **WIDE BAND, FAST SETTLING OP AMP** | | | | |
| | • 40 MHz BW | Pulse Amps | EL2041CG | C | 12 TO-8 |
| | • 200 V/µs Slew Rate | Sample and Holds | EL2041CJ | C | 14 CDIP |
| | • 90 ns Settling | RF Oscillators | EL2041G | M | 12 TO-8 |
| | • Unity Gain Stable | | EL2041G/883 | M | 12 TO-8 |
| | • 13 mA Supply Current | | EL2041J | M | 14 CDIP |
| | | | EL2041J/883 | M | 14 CDIP |
| **EL2190/2195** | **WIDE BAND, FAST SETTLING OP AMP** | | | | |
| | • 150 MHz Gain BW | Pulse Amps | EL2195CG | C | 12 TO-8 |
| ✯ | • 200 V/µs Slew Rate | Sample and Holds | EL2195CJ | C | 14 CDIP |
| | • 70 ns Settling | RF Oscillators | EL2190G | M | 12 TO-8 |
| | • 13 mA Supply Current | | EL2190G/883 | M | 12 TO-8 |
| | | | EL2190J | M | 14 CDIP |
| | | | EL2190J/883 | M | 14 CDIP |
| | | | EL2190L/883 | M | 20 LCC |
| **ELH0002** | **100 mA CURRENT BUFFER** | | | | |
| | • 400 mA Pulsed Output | Solenoid Driver | 7801301XC (DESC) | M | 8 TO-5 |
| | • 30 MHz BW | Video Buffer | ELH0002CH | I | 8 TO-5 |
| | • 200 V/µs Slew Rate | Cable Driver | ELH0002H | M | 8 TO-5 |
| | | | ELH0002H/883 | M | 8 TO-5 |

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| Device | Features | Applications | Part No. | Temp. | Pins/Pkge. |
|---|---|---|---|---|---|
| **ELH0021** | **1A POWER OP AMP** | | | | |
| | • High Output- 1.2A | DC Servo Driver | 8508801YX (DESC) | M | 8 TO-3 |
| | • 20 kHz FP BW | ATE | ELH0021CK | I | 8 TO-3 |
| | • ±12 V Output Swing | | ELH0021K | M | 8 TO-3 |
| | | | ELH0021K/883 | M | 8 TO-3 |
| **ELH0032** | **HIGH SPEED FET OP AMP** | | | | |
| | • 70 MHz BW | Video Amplifiers | 8001301ZX (DESC) | M | 12 TO-8 |
| | • 5 mV Offset Voltage | Image Processing | ELH0032CG | I | 12 TO-8 |
| | • High Input Impedance | Flash A/D Driver | ELH0032G | M | 12 TO-8 |
| | | | ELH0032G/883 | M | 12 TO-8 |
| **ELH0033** | **HIGH SPEED FET BUFFER** | | | | |
| | • 100 mA Output Drive | Fast Line Driver | 8001401ZX (DESC) | M | 12 TO-8 |
| | • 100 MHz BW | High Speed S/H | ELH0033CG | I | 12 TO-8 |
| | • 1500 V/µs Slew Rate | Flash A/D Driver | ELH0033G | M | 12 TO-8 |
| | | | ELH0033G/8 | M | 12 TO-8 |
| **ELH0041** | **200 mA POWER AMP** | | | | |
| | • High Gain - 106 dB | Programmable Power Supplies | | | |
| | • Low Offset Voltage-1 mV | Servo Amp | 8508701ZX (DESC) | M | 12 TO-8 |
| | | | ELH0041CG | I | 12 TO-8 |
| | | | ELH0041G | M | 12 TO-8 |
| | | | ELH0041G/883 | M | 12 TO-8 |
| **ELH0101/0101A** | **2A POWER OP AMP** | | | | |
| | • 5A Peak Output Current | Precision Servos | 8508901YX (DESC) | M | 8 TO-3 |
| | • 0.008% THD | ATE | 8508902YX (DESC) | M | 8 TO-3 |
| | • 10 V/µs Slew Rate | | ELH0101ACK | I | 8 TO-3 |
| | | | ELH0101AK | M | 8 TO-3 |
| | | | ELH0101AK/883 | M | 8 TO-3 |
| | | | ELH0101CK | I | 8 TO-3 |
| | | | ELH0101K | M | 8 TO-3 |
| | | | ELH0101K/883 | M | 8 TO-3 |
| **EDH0006** | **CURRENT DRIVER** | | | | |
| | • 10V to 45V Supply | Solenoid Drivers | EDH0006CH | I | 10 TO-100 |
| | • 1.6 mA Standby Current | Lamp Drivers | EDH0006H | M | 10 TO-100 |
| | • 1.5A Peak Pulse Current | Relay Drivers | EDH0006H/883 | M | 10 TO-100 |
| **EDH0008** | **HIGH VOLTAGE, HIGH CURRENT DRIVER** | | | | |
| | • 10V to 45V Supply | Solenoid Drivers | EDH0006CH | I | 10 TO-100 |
| | • 1.6 mA Standby Current | Stepper Motor Drive | EDH0006H | M | 10 TO-100 |
| | • 3A Peak Pulse Current | Squib Actuators | EDH0006H/883 | M | 10 TO-100 |
| **EHA2500/02/05** | **PRECISION HIGH SLEW RATE OP AMPS** | | | | |
| | • 30 V/µs Slew Rate | Signal Generators | EHA2-2500-2 | M | 8 TO-99 |
| | • Internally Compensated | Pulse Amplifiers | EHA2-2500-8 | M | 8 TO-99 |
| | • 12 MHz Gain BW | Wide Band Filters | EHA7-2500-2 | M | 8 CDIP |
| | | | EHA7-2500-8 | M | 8 CDIP |
| | | | EHA2-2502-2 | M | 8 TO-99 |
| | | | EHA2-2502-8 | M | 8 TO-99 |
| | | | EHA7-2502-2 | M | 8 CDIP |
| | | | EHA7-2502-8 | M | 8 CDIP |
| | | | EHA2-2505-5 | C | 8 TO-99 |
| | | | EHA3-2505-5 | C | 8 PDIP |
| | | | EHA7-2505-5 | C | 8 CDIP |
| **EHA2510/12/15** | **HIGH SLEW RATE OP AMPS** | | | | |
| | • 60 V/µs Slew Rate | DAC Output Buffer | EHA2-2510-2 | M | 8 TO-99 |
| | • Internally Compensated | Video Amplifier | EHA2-2510-8 | M | 8 TO-99 |
| | • 100 MΩ Input Impedance | ATE Composite AMP | EHA7-2510-2 | M | 8 CDIP |
| | | | EHA7-2510-8 | M | 8 CDIP |
| | | | EHA2-2512-2 | M | 8 TO-99 |
| | | | EHA2-2512-8 | M | 8 TO-99 |
| | | | EHA7-2512-2 | M | 8 CDIP |
| | | | EHA7-2512-8 | M | 8 CDIP |
| | | | EHA2-2515-5 | C | 8 TO-99 |
| | | | EHA3-2515-5 | C | 8 PDIP |
| | | | EHA7-2515-5 | C | 8 CDIP |

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| Device | Features | Applications | Part No. | Temp. | Pins/Pkge. |
|---|---|---|---|---|---|
| **EHA2520/22/25 UNCOMPENSATED HIGH SLEW RATE OP AMPS** | | | | | |
| | • 120 V/μs Slew Rate | High Speed Integrator | EHA2-2520-2 | M | 8 TO-99 |
| | • 2 MHz Power Bandwidth | Video Buffer | EHA2-2520-8 | M | 8 TO-99 |
| | • 20 MHz Gain BW | R.F. Amplifier | EHA4-2520-8 | M | 20 LCC |
| | | | EHA7-2520-2 | M | 8 CDIP |
| | | | EHA7-2520-8 | M | 8 CDIP |
| | | | EHA2-2522-2 | M | 8 TO-99 |
| | | | EHA2-2522-8 | M | 8 TO-99 |
| | | | EHA7-2522-2 | M | 8 CDIP |
| | | | EHA7-2522-8 | M | 8 CDIP |
| | | | EHA2-2525-5 | C | 8 TO-99 |
| | | | EHA3-2525-5 | C | 8 PDIP |
| | | | EHA7-2525-5 | C | 8 CDIP |
| **EHA2539 VERY HIGH SLEW, WIDE BAND OP AMP** | | | | | |
| | • 600 MHz Gain BW | Pulse Amps | EHA1-2539-2 | M | 14 CDIP |
| ✯ | • 600 V/μs Slew Rate | Sample and Holds | EHA1-2539-4 | I | 14 CDIP |
| | • 15k Gain | RF Oscillators | EHA1-2539-5 | C | 14 CDIP |
| | | | EHA1-2539-8 | M | 14 CDIP |
| | | | EHA3-2539-5 | C | 14 PDIP |
| | | | EHA4-2539-8 | M | 20 LCC |
| **EHA2540 WIDE BAND, FAST SETTLING OP AMP** | | | | | |
| | • 400 MHz Gain BW | Pulse Amps | EHA1-2540-2 | M | 14 CDIP |
| ✯ | • 400 V/μs Slew Rate | Sample and Holds | EHA1-2540-4 | I | 14 CDIP |
| | • 200 ns Settling | RF Oscillators | EHA1-2540-5 | C | 14 CDIP |
| | | | EHA1-2540-8 | M | 14 CDIP |
| | | | EHA3-2540-5 | C | 14 PDIP |
| | | | EHA4-2540-8 | M | 20 LCC |
| **EHA2600/02/05 WIDE BANDWIDTH, HIGH IMPEDANCE OP AMP** | | | | | |
| | • 12 MHz BW | Precision Comparator | EHA2-2600-2 | M | 8 TO-99 |
| | • 1 nA Input Bias Current | Pulse Amplifier | EHA2-2600-8 | M | 8 TO-99 |
| | • 500 μV Input Offset | Video Amplifier | EHA7-2600-2 | M | 8 CDIP |
| | | | EHA7-2600-8 | M | 8 CDIP |
| | | | EHA2-2602-2 | M | 8 TO-99 |
| | | | EHA2-2602-8 | M | 8 TO-99 |
| | | | EHA7-2602-2 | M | 8 CDIP |
| | | | EHA7-2602-8 | M | 8 CDIP |
| | | | EHA2-2605-5 | C | 8 TO-99 |
| | | | EHA3-2605-5 | C | 8 PDIP |
| | | | EHA7-2605-5 | C | 8 CDIP |
| **EHA2620/22/25 WIDE BANDWIDTH, UNCOMPENSATED OP AMPS** | | | | | |
| | • 100 MHz Gain BW | High Speed S/H | EHA2-2620-2 | M | 8 TO-99 |
| | • 1 nA Input Bias Current | High "Q" Filters | EHA2-2620-8 | M | 8 TO-99 |
| | • 500 μV Input Offset | | EHA4-2620-8 | M | 20 LCC |
| | | | EHA7-2620-2 | M | 8 CDIP |
| | | | EHA7-2620-8 | M | 8 CDIP |
| | | | EHA2-2622-2 | M | 8 TO-99 |
| | | | EHA2-2622-8 | M | 8 TO-99 |
| | | | EHA7-2622-2 | M | 8 CDIP |
| | | | EHA7-2622-8 | M | 8 CDIP |
| | | | EHA2-2625-5 | C | 8 TO-99 |
| | | | EHA3-2625-5 | C | 8 PDIP |
| | | | EHA7-2625-5 | C | 8 CDIP |
| **EHA5190/5195 WIDE BAND, FAST SETTLING OP AMP** | | | | | |
| | • 150 MHz Gain BW | Pulse Amps | EHA1-5190-2 | M | 14 CDIP |
| ✯ | • 200 V/μs Slew Rate | Sample and Holds | EHA1-5190-8 | M | 14 CDIP |
| | • 70 ns Settling | RF Oscillators | EHA2-5190-2 | M | 12 TO-8 |
| | | | EHA2-5190-8 | M | 12 TO-8 |
| | | | EHA4-5190-8 | M | 20 LCC |
| | | | EHA1-5195-5 | C | 14 CDIP |
| | | | EHA2-5195-5 | C | 12 TO-8 |


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M= –55°C to +125°C  I= –25°C to +85°C  C=0°C to +75°C

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# EL2003/EL2003C

## 100 MHz Video Line Driver

### Features

- Differential Gain 0.1%
- Differential Phase 0.1°
- 100 mA continuous output current guaranteed
- Short circuit protected
- Wide bandwidth—100 MHz
- High slew rate—1200 V/μs
- High input impedance—2 MΩ
- Low quiescent current drain
- Pin compatible with LH0002CN and LH0002H

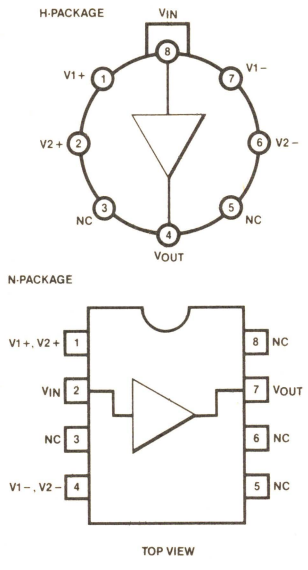
### Applications

- Co-ax cable driver
- Flash converter driver
- Video DAC buffer
- Op amp booster

### Ordering Information

| Part No. | Temp. Range | Package |
|---|---|---|
| EL2003CN | −25°C to +85°C | P-DIP |
| EL2003CN/E+ | −25°C to +85°C | P-DIP |
| EL2003CH | −25°C to +85°C | TO–99 |
| EL2003CH/E+ | −25°C to +85°C | TO–99 |
| EL2003H | −55°C to +125°C | TO–99 |
| EL2003H-8 | −55°C to +125°C | TO–99 |

### Connection Diagrams




### General Description

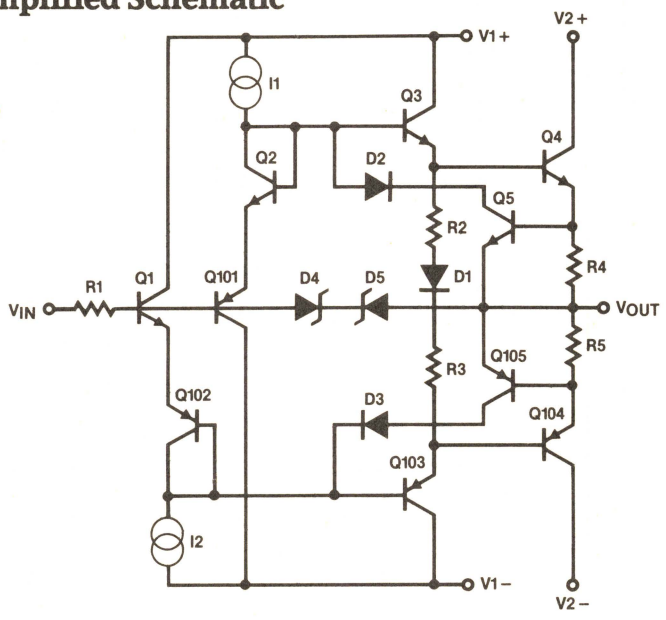
The EL2003 is a general purpose monolithic unity gain buffer featuring 100 MHz, −3 dB bandwidth and 4 ns small signal rise time. This buffer is capable of delivering a ±100 mA current to a resistive load and is oscillation free into capacitive loads. In addition, the EL2003 has internal output short circuit current limiting which will protect the device under both a DC fault condition and AC operation with reactive loads. The extremely fast slew rate of 1200 V/μs, wide bandwidth, and high output drive make the EL2003 an ideal choice for closed loop buffer applications with wide band op amps. These same characteristics and excellent DC performance make the EL2003 an excellent choice for open loop applications such as driving coaxial and twisted pair cables.

The EL2003 is constructed using Elantec's proprietary dielectric isolation process that produces PNP and NPN transistors with essentially identical AC and DC characteristics.

The EL2003 is specified for operation over the −55°C to +125°C military temperature range and is available in the 8-lead TO–99 hermetic package. The EL2003C is specified for operation over the −25°C to +85°C temperature range and is available in both TO–99 and 8-lead plastic mini-DIP.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*

### Simplified Schematic

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# EP2015/2015A
## *Fast Quad PNP Array*

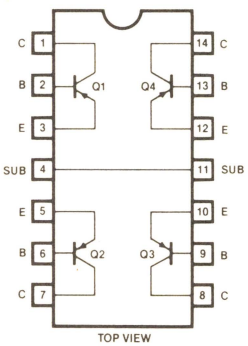
## Features
- Four Independent Fast PNP's
- 350 MHz $f_t$
- Tight $V_{be}$ Matching—1 mV
- Tight $H_{fe}$ Matching—5%
- One Chip Construction With Dielectric Isolation
- Excellent Thermal Tracking
- High $H_{fe}$—150 Minimum
- 40 Volt Minimum $BV_{ceo}$
- Each Transistor Similar to 2N3906
- Pin Compatible With TPQ3906 and MPQ3906

## Applications
- Current Sources
- Current Mirrors
- Log Amplifiers
- Multipliers

## Ordering Information

| Part No. | Temp. Range | Pkg. | Outline# |
|---|---|---|---|
| EP2015CN | 25°C | P-DIP | MDP0012 |
| EP2015ACN | -25 to +85°C | P-DIP | MDP0012 |
| EP2015CJ | 25°C | Cerdip | MDP0014 |
| EP2015ACJ | -25 to +85°C | Cerdip | MDP0014 |
| EP2015J | -55 to +125°C | Cerdip | MDP0014 |
| EP2015AJ | -55 to +125°C | Cerdip | MDP0014 |
| EP2015J-8 | -55 to +125°C | Cerdip | MDP0014 |
| EP2015AJ-8 | -55 to +125°C | Cerdip | MDP0014 |

## Connection Diagram



TOP VIEW

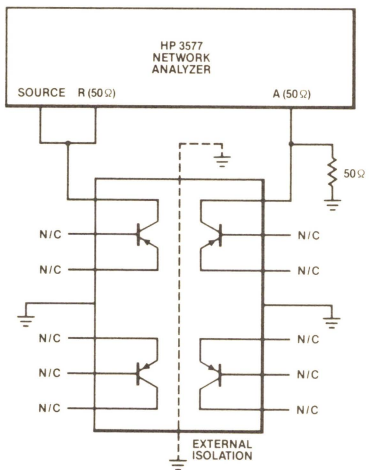
## General Description

The EP2015 family are quad monolithic vertical PNP transistor arrays which offer excellent parametric matching and high speed performance. The 350 MHz $f_t$ provides A.C. performance similar to 2N3906 class devices. Manufactured on Elantec's Dielectric Isolation process, these transistors are electrically isolated from each other by a layer of oxide. The resulting low collector to substrate capacitance allows very high speed performance with minimal crosstalk. In addition, complete D.C. isolation is achieved. Substrate biasing is not required for normal operation, however for optimum high speed performance the substrate should be grounded. One-chip construction insures excellent parameter matching and tracking over temperature.

The low cost EP2015C is specified at 25°C. The EP2015AC is more tightly specified and guaranteed over the commercial temperature range of -25°C to +85°C. The EP2015 and the more stringently specified EP2015A are tested over the full military temperature range of -55°C to +125°C. The EP2015C and EP2015AC are available in either 14 pin plastic dual-in-line or ceramic dual-in-line packages. The EP2015 and EP2015A are available in a 14 pin ceramic dual-in-line package. The EP2015 is also available in chip form for hybrid applications. Its large bonding pads provide for easy automated manufacturing.

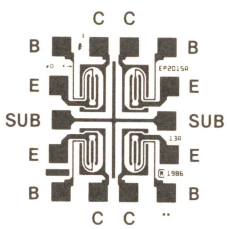
For information on a complementary NPN transistor array, see Elantec's EN2016 family data sheet.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*



**Isolation Characteristics Test Circuit**

## Die Layout



DIE SIZE: 38 x 45 MILS

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# EN2016/EN2016A

## *Fast Quad NPN Array*

## Features

- Four Independent Fast NPN's
- 350 MHz $f_t$
- Tight $V_{be}$ Matching—1 mV
- Tight $H_{fe}$ Matching—5%
- One Chip Construction With Dielectric Isolation
- Excellent Thermal Tracking
- High $H_{fe}$—150 Minimum
- 40 Volt Minimum $BV_{ceo}$
- Each Transistor Similar to 2N3904
- Pin Compatible With TPQ3904 and MPQ3904

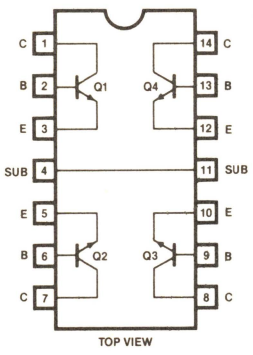
## Applications

- Current Sources
- Current Mirrors
- Log Amplifiers
- Multipliers

## Ordering Information

| Part No. | Temp. Range | Pkg. | Outline# |
|---|---|---|---|
| EN2016CN | 25°C | P-DIP | MDP0012 |
| EN2016ACN | −25 to +85°C | P-DIP | MDP0012 |
| EN2016CJ | 25°C | Cerdip | MDP0014 |
| EN2016ACJ | −25 to +85°C | Cerdip | MDP0014 |
| EN2016J | −55 to +125°C | Cerdip | MDP0014 |
| EN2016AJ | −55 to +125°C | Cerdip | MDP0014 |
| EN2016J-8 | −55 to +125°C | Cerdip | MDP0014 |
| EN2016AJ-8 | −55 to +125°C | Cerdip | MDP0014 |

## Connection Diagram



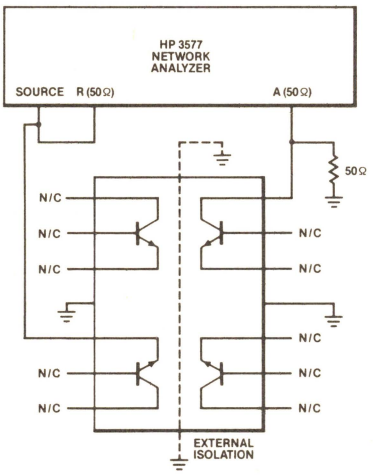

## General Description

The EN2016 family are quad monolithic vertical NPN transistor arrays which offer excellent parametric matching and high speed performance. The 350 MHz $f_t$ provides A.C. performance similar to 2N3904 class devices. Manufactured on Elantec's Dielectric Isolation process, these transistors are electrically isolated from each other by a layer of oxide. The resulting low collector to substrate capacitance allows very high speed performance with minimal crosstalk. In addition, complete D.C. isolation is achieved. Substrate biasing is not required for normal operation, however for optimum high speed performance the substrate should be grounded. One-chip construction insures excellent parameter matching and tracking over temperature.

The low cost EN2016C is specified at 25°C. The EN2016AC is more tightly specified and guaranteed over the commercial temperature range of −25°C to +85°C. The EN2016 and the more stringently specified EN2016A are tested over the full military temperature range of −55°C to +125°C. The EN2016C and EN2016AC are available in either 14 pin plastic dual-in-line or ceramic dual-in-line packages. The EN2016 and EN2016A are available in a 14 pin ceramic dual-in-line package. The EN2016 is also available in chip form for hybrid applications. Its large bonding pads provide for easy automated manufacturing.

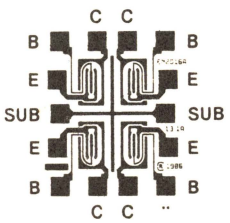
For information on a complementary PNP transistor array, see Elantec's EP2015 family data sheet.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*




**Isolation Characteristics Test Circuit**

## Die Layout




DIE SIZE: 38 × 45 MILS

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# EL2018/EL2018C

*Fast, High Voltage Comparator with Transparent Latch*

## Features

- Fast response time – 20 ns
- Wide input differential voltage range — 24 V on ±15 V supplies
- Precision input stage – $V_{os}$ = 1 mV
- Low input bias current – $I_B$ = 100 nA
- Low input offset current – $I_{os}$ = 30 nA
- ±4.5 V to ±18 V supplies
- 3 State TTL and CMOS compatible output
- No supply current glitch during switching
- High voltage gain – 40 V/mV
- 50% power reduction in shutdown mode
- Input and latch remain active in shutdown mode
- P/N compatible with industry standard comparators

## Applications

- Analog to digital converters
- ATE pin receiver
- Precision crystal oscillators
- Zero crossing detector
- Window detector
- Pulse width modulation generator
- "Go/no-go" detector

## General Description

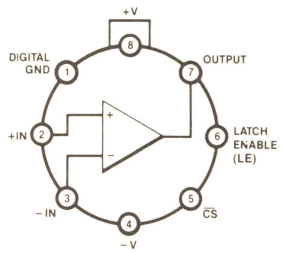
The EL2018 represents a quantum leap forward in comparator speed, accuracy and functionality. Manufactured with Elantec's proprietary Dielectric Isolation (DI) process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures the part maintains speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and latch remain active.

The EL2018 is available in 8 pin Cerdip, 8 pin plastic DIP, and 8 pin metal can packages.

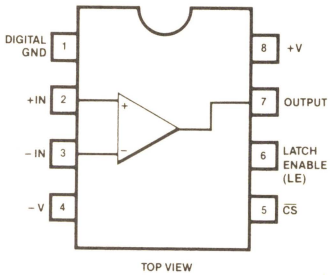
Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see: *Elantec's Military Processing-Monolithic Products.*

## Connection Diagrams

**To-99 Metal Can**




**8-Pin CerDIP**
**8-Pin Plastic DIP**




## Ordering Information

| Part No. | Temp. Range | Package | Outline# |
|---|---|---|---|
| EL2018CH | –25°C to +85°C | TO-99 | MDP 0004 |
| EL2018CH/E+ | –25°C to +85°C | TO-99 | MDP 0004 |
| EL2018CJ | –25°C to +85°C | Cerdip | MDP 0010 |
| EL2018CJ/E+ | –25°C to +85°C | Cerdip | MDP 0010 |
| EL2018CN | –25°C to +85°C | P-DIP | MDP 0006 |
| EL2018CN/E+ | –25°C to +85°C | P-DIP | MDP 0006 |
| EL2018H | –55°C to +125°C | TO-99 | MDP 0004 |
| EL2018H-8 | –55°C to +125°C | TO-99 | MDP 0004 |
| EL2018J | –55°C to +125°C | Cerdip | MDP 0010 |
| EL2018J-8 | –55°C to +125°C | Cerdip | MDP 0010 |

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# EL2019/EL2019C

*Fast, High Voltage Comparator with Master Slave Flip-Flop*

## Features

- Comparator cannot oscillate
- Fast response – 5 ns data to clock setup, 20 ns clock to output
- Wide input differential voltage range – 24 V on ±15 V supplies
- Wide input common mode voltage range – ±12 V
- Precision input stage – $V_{os}$ = 1.5 mV
- Low input bias current – 100 nA
- Low input offset current – 30 nA
- ±4.5 V to ±18 Volt supplies
- 3 State TTL compatible output
- No supply current glitch during switching
- 103 dB voltage gain (Low input uncertainty ≈ 30 μV)
- 50% power reduction in shutdown mode
- Input and flip-flop remain active in shutdown mode

## Applications

- Analog to digital converters
- ATE pin receiver
- Zero crossing detector
- Window detector
- "Go/no-go" detector

## Ordering Information

| Part No. | Temp. Range | Package | Outline# |
|---|---|---|---|
| EL2019CH | –25°C to +85°C | TO-99 | MDP 0004 |
| EL2019CH/E+ | –25°C to +85°C | TO-99 | MDP 0004 |
| EL2019CJ | –25°C to +85°C | Cerdip | MDP 0010 |
| EL2019CJ/E+ | –25°C to +85°C | Cerdip | MDP 0010 |
| EL2019CN | –25°C to +85°C | P-DIP | MDP 0006 |
| EL2019CN/E+ | –25°C to +85°C | P-DIP | MDP 0006 |
| EL2019H | –55°C to +125°C | TO-99 | MDP 0004 |
| EL2019H-8 | –55°C to +125°C | TO-99 | MDP 0004 |
| EL2019J | –55°C to +125°C | Cerdip | MDP 0010 |
| EL2019J-8 | –55°C to +125°C | Cerdip | MDP 0010 |

## General Description

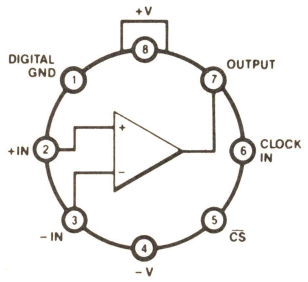
The EL2019 offers a new feature previously unavailable in a comparator before — a master/slave edge triggered flip-flop. The comparator output will only change output state after a positive going clock edge is applied. Thus the output can't feed back to the input and cause oscillation. Manufactured with Elantec's proprietary Dielectric Isolation (DI) process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate current glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and master slave flip-flop remain active.

The EL2019 is available in 8-pin Cerdip, 8-pin plastic DIP, and 8-pin metal can packages.

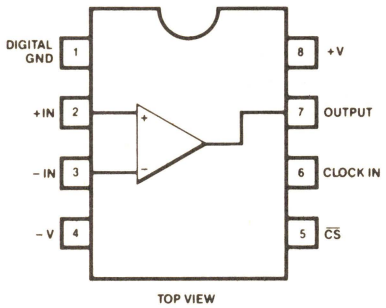
Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see *Elantec's Military Processing-Monolithic Products.*

## Connection Diagrams

**To-99 Metal Can**




**8-Pin CerDIP**
**8-Pin Plastic DIP**




TOP VIEW

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# EL2020/EL2020C

## *50 MHz Current Feedback Amplifier*

### Features

- Slew rate 500 V/$\mu$s
- $\pm$33 mA output current
- Drives $\pm$2.4 Volts into 75 $\Omega$
- Differential phase $<0.1°$
- Differential gain $<0.1\%$
- Vsupply $\pm$5 Volts to $\pm$18 Volts
- Output short circuit protected
- Uses current mode feedback
- 1% settling time of 50 ns for 10 volt step
- Low cost
- 9 mA supply current
- 8 pin mini-dip

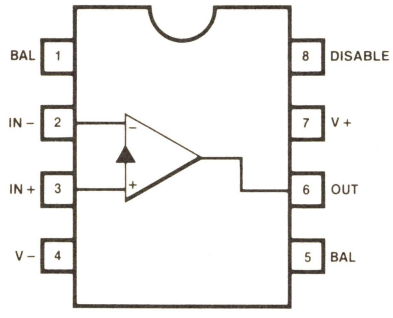
### Applications

- Video gain block
- Residue amplifier
- Radar systems
- Current to voltage converter
- Coax cable driver with gain of 2

### Ordering Information

| Part No. | Temp. Range | Pkg | Outline# |
|---|---|---|---|
| EL2020CN | −25°C to +85°C | 8 pin P-DIP | MDP0006 |
| EL2020CN/E+ | −25°C to +85°C | 8 pin P-DIP | MDP0006 |
| EL2020CJ | −25°C to +85°C | 8 pin Cerdip | MDP0010 |
| EL2020CJ/E+ | −25°C to +85°C | 8 pin Cerdip | MDP0010 |
| EL2020J | −55°C to +125°C | 8 pin Cerdip | MDP0010 |
| EL2020J-8 | −55°C to +125°C | 8 pin Cerdip | MDP0010 |

### Connection Diagram




### General Description

The EL2020 is a fast settling, wide bandwidth amplifier optimized for gains of between −10 and +10. Built using the Elantec monolithic dielectric isolation process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain then a conventional voltage feedback operational amplifier.

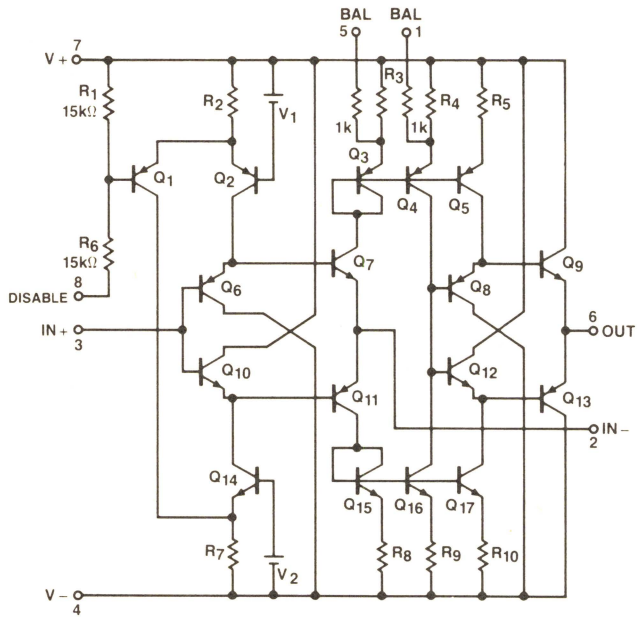
The EL2020 will drive two double terminated 75Ω coax cables to video levels with low distortion. Since it is a closed loop device, the EL2020 provides better gain accuracy and lower distortion than an open loop buffer. The device includes output short circuit protection, and input offset adjust capability.

The bandwidth and slew rate of the EL2020 are relatively independent of the closed loop gain taken. The 50 MHz bandwidth at unity gain only reduces to 30 MHz at a gain of 10. The EL2020 may be used in most applications where a conventional op amp is used, with a big improvement in speed power product.

The EL2020 is available in both 8 pin Plastic DIP and 8 pin Cerdip.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see: *Elantec's Military Processing-Monolithic Products.*

### Equivalent Circuit




Note: The information contained in this data sheet has been carefully checked and is believed to be accurate when published; however this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation.

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# General Purpose Filters

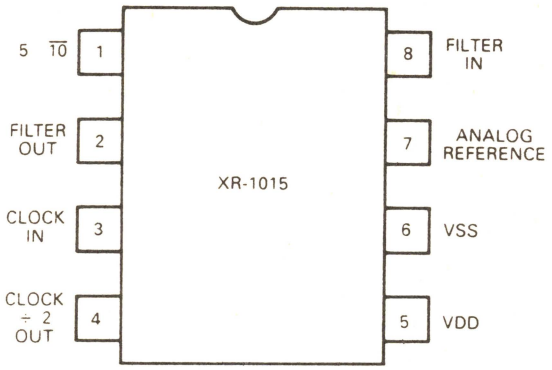
## XR-1015/1016 SEVENTH ORDER ELLIPTIC LOW PASS FILTERS

The XR-1015 and XR-1016 are seven pole and six zero elliptic low pass switched capacitor filters. The position of the passband of the filter is set by the frequency of the clock which allows for easy adjustment. The use of switched capacitor filters reduces the amount of variation in the filter response that occurs with discrete use of capacitors, inductors and resistors. The XR-1015 and XR-1016 also provide synchronized sampled inputs and outputs that allows the device to be cascaded without the need of an additional sample and-hold. The XR-1015 and XR-1016 are produced with a 3 um polysilicon gate dual metal CMOS process for low power dissipation.

The XR-1015 is an eight pin device that can operate from ±2.5 VDC to ±5 VDC. The device can also be biased so that it can be operated with a single +5 to +10 VDC supply. The clock to corner ratio of the XR-1015 is fixed at 100:1.

The XR-1016 is a 14 pin device which provides two uncommitted operational amplifiers for use as a reconstruction filter, anti-aliasing filters or for additional pre-filter gain. The XR-1016 has the ability to change the clock to corner ratio from 100:1 to 50:1.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Greater than 70 dB Stopband Rejection
Operation at +5 VDC (at 250 kHz $f_{CLOCK}$)
Precise Filter Positioning
Low Power Consumption
No External Components Required for Filter

### APPLICATIONS

General Purpose Filtering
Anti-alias Filters (for analog-to-digital converters)
Reconstruction Filters (for digital-to-analog converters)
Band Limiting of Voice for Linear Predictive Coding
Digital Signal Processing Front End
Filtering of Voice for Music for Special Effects (echo, phasing, etc.)

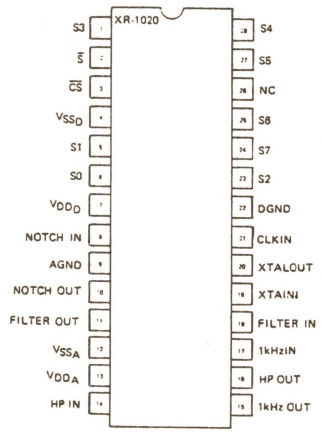
### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-1015CN | Ceramic | 0°C to 70°C |
| XR-1015CP | Plastic | 0°C to 70°C |
| XR-1016CN | Ceramic | 0°C to 70°C |
| XR-1016CP | Plastic | 0°C to 70°C |

## XR-1020 DATA COMMUNICATION INSTRUMENTATION FILTER

The XR-1020 is a data communication/telecommunication instrumentation filter. This device provides ten of the filters used to characterize communication links for both IEEE/Bell and CCITT standards. The filters provided are: C-message Weighting, C-Notch (1010 Hz Notch), Psophometric (CCITT Equivalent of C-Message Weighted), CCITT Psophometric Notch (825 Hz), Program Weighting, 3 kHz Flat, 15 kHz Flat, 1 kHz Band Pass (phase jitter measurements), 50 kilobit (low pass filter portion only), and Peak-to-Average Ratio Band Pass Filter (P/AR).

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Ten Filters Provided in One 28 Pin Dual In Line (DIP) Package
Microprocessor Bus Interface
Low Noise
Power Down Mode for Battery Operation
3.579 MHz Clock Operation with On-chip Oscillator
Separate Notch Filter Output
Separate 1 kHz Band Pass (Phase Jitter Measurements) Filter Output
TTL/CMOS Compatible Digital Inputs
On-chip Output Smoothing Filters

### APPLICATIONS

Telephone Impairment Measurement Sets (TIMS)
C-message Weighted Meters
Telecommunication Test Instruments
Audio Test Systems
General Instrumentation Purposes
C-message Weighted Meters,-

### APPLICATIONS

Telephone Impairment Measurement Sets (TIMS)
C-message Weighted Meters
Telecommunication Test Instruments
Audio Test Systems
General Instrumentation Purposes

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-1020N | Ceramic | 0°C to 70°C |
| XR-1020P | Plastic | 0°C to 70°C |
| XR-1020CN | Ceramic | 0°C to 70°C |
| XR-1020CP | Plastic | 0°C to 70°C |

Exar Corp./Exel

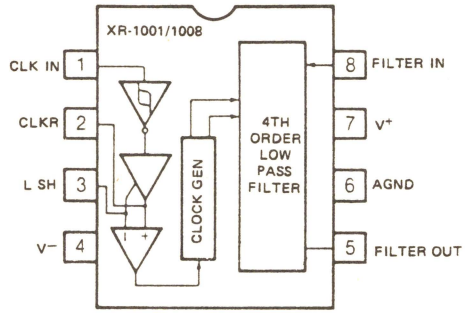
# Switched Capacitor Filters

## XR-1001/1002/1003/1004/1005/1006/1007/1008 FOURTH ORDER SWITCHED CAPACITOR LOW PASS FILTERS

Each of these devices in the series is a fourth order switched capacitor low pass filter providing 24 dB/octave of roll-off outside of the pass band. Within this series, Butterworth, Bessel or Chebyshev (0.5 or 0.1 dB of ripple) filter responses can be optained. Also, each filter response is available in either a 50:1 or 100:1 clock-to-corner ratio device for added flexibility. All devices have the same pin out (8 pin dual-in-line), so one can easily be substituted for the other, depending on the application.

Switched capacitor filters provide the ability to tune the corner frequency of the filter response with the adjustment of the input clock. The XR-1001/1008 can also be used in a stand alone mode, where an external resistor and capacitor will set the input clock frequency. For additional precision, an external crystal can be used to set the corner frequency.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Single 5 Volt Operation
Low Power Consumption
Precise Filter Positioning
Stand Alone Mode with RC or Crystal
Low Noise – Typically –72 dBm
Corner Frequency Adjustable to 40 kHz

### APPLICATIONS

Mechanical Processes
Telecommunications
Instrumentation
Anti-alias Filters
Reconstruction Filters
Digital Signal Processing
Musical Effects

### ORDERING INFORMATION

| Part Number | Response/Ripple | $f_{clock}/f_{corner}$ |
|---|---|---|
| XR-1001CP/CN | Butterworth | 100:1 |
| XR-1002CP/CN | Butterworth | 50:1 |
| XR-1003CP/CN | Bessel | 100:1 |
| XR-1004CP/CN | Bessel | 50:1 |
| XR-1005CP/CN | Chebyshev (0.1dB) | 100:1 |
| XR-1006CP/CN | Chebyshev (0.1dB) | 50:1 |
| XR-1007CP/CN | Chebyshev (0.5dB) | 100:1 |
| XR-1008CP/CN | Chebyshev (0.5dB) | 50:1 |

Note: CN = Ceramic, CP = Plastic, Operating Temperature Range is 0°C to 70°C.

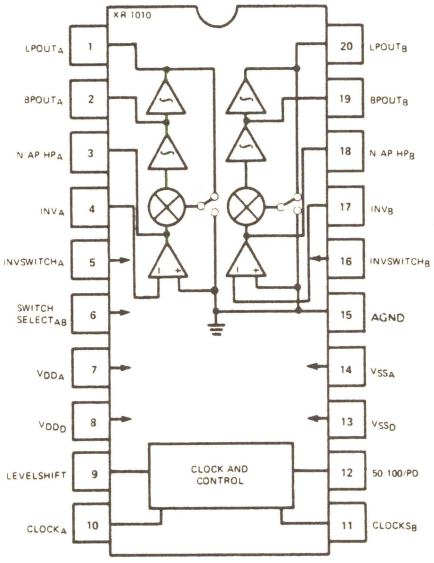
## XR-1010 SECOND ORDER SWITCHED CAPACITOR FILTER

The XR-1010 is a fully adjustable dual second order switched capacitor filter. With the intermediate nodes of the switched capacitor filter brought out, many different filter functions can be obtained. One half of the XR-1010 is composed of an operational amplifier, and two switched capacitor integrators. With the use of external resistors, to adjust the amplitude of the feedback, notch, band pass, all pass, low pass and high pass filter functions can be obtained.

By cascading the two halves of the XR-1010, a fourth order filter can be obtained. With the use of additional XR-1010, higher order filters can be obtained.

The XR-1010 is fabricated in polysilicon gate 3-micron CMOS. With this single +5 VDC operation (at 250 kHz) and low power consumption can be obtained.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Easy to Use: Simple resisitor divider equations for filter Q
No External Capacitors Needed to Set Corner Frequency
Cascadable to Obtain Higher Order Filter Functions
Pin-for-Pin Compatible with National Semiconductor MF-10

### APPLICATIONS

Low Pass, High Pass, Band Pass, Notch & All Pass Filters
Group Delay Compensation Filtering
Modem Filters (CCITT V.21, V.23, V.26)
Band Separation for Analog Front End
Linear Phase Filtering (All Pole Filtering)
Loop Filter for Phase-Lock Loops

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-1010N | Ceramic | -40°C to +85°C |
| XR-1010P | Plastic | -40°C to +85°C |
| XR-1010CN | Ceramic | 0°C to +70°C |
| XR-1010CP | Plastic | 0°C to +70°C |

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# Modem Circuits

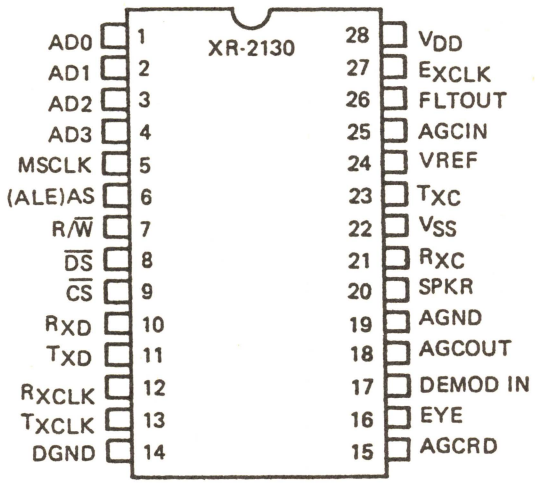
## XR-2130 SINGLE CHIP BELL 212A/V.22 MODEM

The XR-2130 is a single chip modem which supplies the complete Bell 212A or CCITT V.22 function. The XR-2130 is designed to interface directly to the XR-2131 modem controller to form a complete smart modem, such as a Hayes compatible type.

The XR-2130 supplies the modulation and demodulation for 1200 BPS DPSK (212A/V.22) and 300 BPS FSK (212A). For 1200 BPS operation, advanced circuit techniques are utilized such as digital echo modulation for precise transmit carrier spectrum shaping and coherent Costas Loop type demodulator for excellent BER vs. S/N performance. The XR-2130 is also very feature intensive, supporting virtually all the "smart modem" functions. These include call progress monitoring (CPM), DTMF dialing, and both analog and digital test facilities (ALB and DLB).

Fabricated in silicon gate CMOS, the XR-2130 offers low power operation from ±5 volt power supplies. The XR-2130 is available in a 28 pin plastic or ceramic DIP, or a range of surface mount packages.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Bell 212A/CCITT V.22 Operation
1200 BPS DPSK/300 BPS FSK
Universal Microcontroller Interface
Costas Loop Coherent PSK Demodulator
Call Progress Monitoring
ALB and DLB Test Modes
DTMF Dialing
Voice Output Port
Hayes Type Software Available (XR-2131 Modem Controller)
Low Power CMOS
Eye Pattern Output (Quality)

### APPLICATIONS

Stand Alone, Internal, Smart Modems
Hayes Compatible Modem
Bell 212A, CCITT V.22 Type Modems

### ORDERING INFORMATION

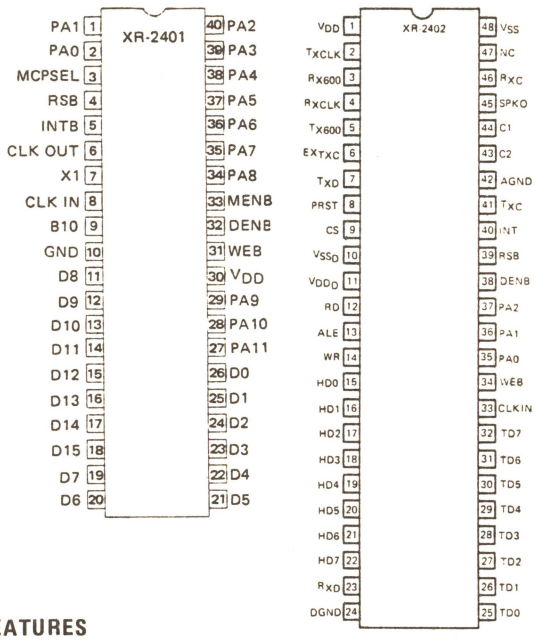
| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-2130CN | Ceramic | 0°C to 70°C |
| XR-2130CP | Plastic | 0°C to 70°C |

## XR-2400 V.22 bis MODEM CHIP SET

The XR-2400 Chip Set is designed to provide the complete modem function for V.22 bis (2400 BPS) type modems. The chip set consists of the XR-2401 DSP Modem Signal Processor and the XR-2402 DSP Interface. The XR-2400 set also provides Bell 212A (1200/300 BPS) and CCITT V.22 (1200 BPS) modes for a Bell/ CCITT compatible system.

The XR-2401 is the heart of the system. It is a digital signal processor (DSP) based chip providing 300 BPS FSK, 1200 BPS DPSK, and 2400 BPS QAM modulation and demodulation for the system. Other functions included are scrambler/descrambler, adaptive equalizer, carrier detection, and DTMF tone generator.The XR-2402 provides the interface functions for the XR-2401, such as A/D and D/A converters for getting into and out of the DSP chip. Also provided are band splitting filters (SCF type), programmable gain amplifier (PGA), asynchronous to synchronous and synchronous to asynchronous conversion, and guard tone generation for CCITT applications.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

2400 BPS (QAM), 1200 BPS (DPSK), 300 BPS (FSK) Operation
V.22 bis, V.22, 212A, 103 Compatible
DSP Based (XR-2401)
Bus Structured Control
No Adjustments
DTMF Dialing
Low Power CMOS - XR-2401 5 V, XR-2402 ±5 V
Adaptive Equalization
Asynchronous/Synchronous Operation
550 Hz/1800 Hz Guard Generation
Automatic Call Progress Monitoring

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-2401CP | Plastic | 0°C to 70°C |
| XR-2401CN | Ceramic | 0°C to 70°C |
| XR-2402CP | Plastic | 0°C to 70°C |

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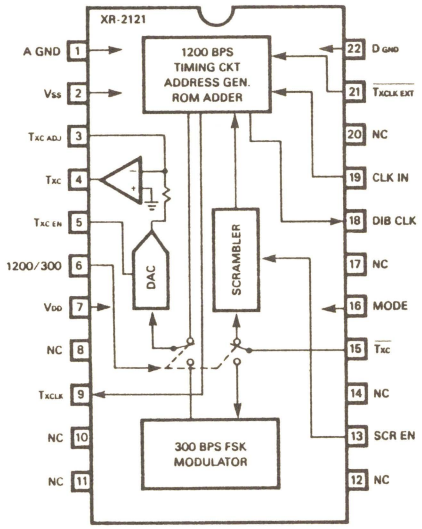
# Modem Circuits

## XR-2121 BELL 212A TYPE MODULATOR

The XR-2121 is designed to provide the complete modulator function for a Bell 212A type modem. The circuit accepts a synchronous serial data stream and generates either a 300 BPS frequency shift keyed (FSK) or a 1200 BPS differential phase shift keyed (DPSK) carrier signal. An on-board digital-to-analog converter provides a synthesized sine wave output. Also provided on the transmitted carrier output is an inverting amplifier with external feedback resistor to provide a carrier amplitude adjust.

A 1200 Hz transmit clock output is provided for 1200 BPS operation, although the XR-2121 will also accept an external transmit clock. For test or other purposes, a 600 Hz baud clock output is also supplied.

### FUNCTIONAL BLOCK DIAGRAM

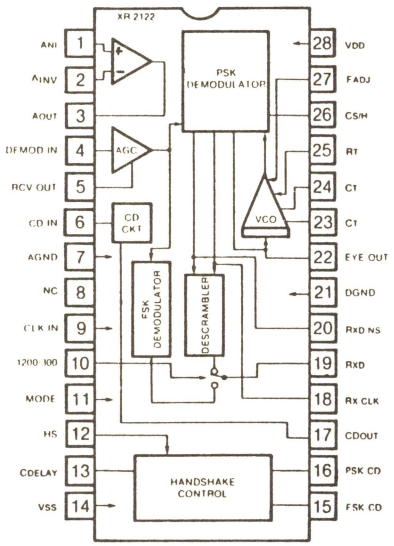



## XR-2122 BELL 212A TYPE DEMODULATOR

The XR-2122 is designed to perform the complete Bell 212A type modem demodulator function. Both 1200 BPS differential phase shift keyed (DPSK) and 300 BPS frequency shift keyed carrier demodulation is performed by the XR-2122. The 1200 BPS portion utilizes coherent demodulation, while the 300 BPS uses phase-locked loop techniques. For 1200 BPS operation, an internal 17 bit descrambler provides the descrambled output with the nondescrambled output also available.

Automatic speed selection is performed by a handshake circuit. Carrier detect outputs are supplied for FSK data, PSK data, and conventional energy detection.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Bell 212A Compatible/CCITT V.22 Adaptable
1200 BPS DPSK
300 BPS FSK
Digital Modulation Techniques for DPSK
External Transmit Clock Input
600 Hz Dibit Clock Output
Complete Scrambler Function with Disable Input
Transmit Carrier Level Adjust
1.8432 MHz Clock
±5 Volt Operation

### APPLICATIONS

CCITT V.22 Type Demodulator
Bell 212A Type Demodulator
Bell 103 Type Demodulator

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-2121CN | Ceramic | 0°C to 70°C |
| XR-2121CP | Plastic | 0°C to 70°C |

### FEATURES

Bell 212A Compatible/CCITT V.22 Adaptable
1200 BPS DPSK Coherent Demodulation
300 BPS FSK Demodulation
Eye Diagram Output
Internal 17 Bit Descrambler
Non-descrambled Demodulation Output Available
FSK, PSK and Energy-type Carrier Detect Outputs
Automatic Speed Selection
Non-committed Op Amp for Input AGC Amplifier
AGC Input Circuit for Wide Dynamic Range

### APPLICATIONS

Bell 212A Type Demodulator
Bell 103 Type Demodulator

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-2122CN | Ceramic | 0°C to 70°C |
| XR-2122CP | Plastic | 0°C to 70°C |

All devices are also available in Surface Mount Packages. Consult factory for complete information.

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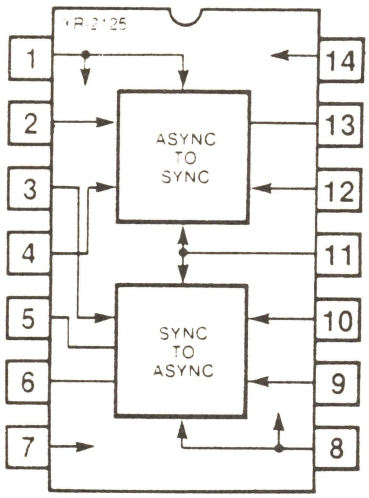
# Modem Circuits

## XR-2125 DATA BUFFER

The XR-2125 is a logic circuit designed to perform the data buffer function for Bell 212A type modem systems. Both asynchronous to synchronous and synchronous to asynchronous coversion are performed at nominal data rates of 1200 bits per second. The XR-2125 is selectable for character lengths of 9 or 10 bits. Separate enable/disable inputs are supplied for async to sync and sync to async converter sections. These inputs allow the same data lines to be used for asynchronous or synchronous operation.

### FUNCTIONAL BLOCK DIAGRAM




### NEW BUFFER PRODUCTS – Contact EXAR for Details

XR-2124 Universal Data Buffer
XR-2135 Bell/CCITT Data Buffer

### FEATURES

Bell 212A Compatible
Asynchronous to Synchronous Conversion
Synchronous to Asynchronous Conversion
Independent Disable Input for Receiver & Transmitter Sections
1.8432 MHz Clock
Break Signal Automatic Extension for Transmitter
1200 BPS +1%, -2.5% Operation
Single 5 Volt Operation

### APPLICATIONS

Bell 212A Data Buffer

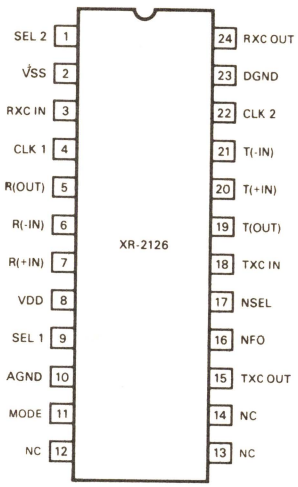
### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-2125CN | Ceramic | 0°C to 70°C |
| XR-2125CP | Plastic | 0°C to 70°C |

## XR-2126/2127/2128/2129 Bell 212A CCITT V.22 MODEM FILTERS

The XR-2126/2127/2128/2129 modem filters are monolithic CMOS switched capacitor filters designed for use in full duplex 1200 BPS modems. They meet all the filtering functions of the Bell 212A and CCITT V.22 modem specifications. They include the low band (centered at 1200 Hz) and high band (centered at 2400 Hz) filters with full channel compromise equalization and output smoothing filters for both bands.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Bell 212A/CCITT V.22 Compatible Transmit and Receive Filters with Full Channel Compromise Equalization
Selectable V.22 Notch Filters Included (550 Hz/1800 Hz)
Built-in Call Progress Mode/Enhanced Call Progress Mode
Analog Loop Back Capability (XR-2127/8/9)
Phone Line Status Monitor Capability (Bypass Mode)
Additional Equalization for Worst Case Line (3002, C0)Conditions
On-chip Transmit and Receive Output Smoothing Filters
Two Uncommitted Operational Amplifiers
Choice of Clock Frequencies:
153.6 KHz or 1.2288 MHz/2.4576 MHz on XR-2126, XR-2127, XR-2128
1.8432 MHz Crystal with On-chip Clock Oscillator on XR-2129
TTL/CMOS Compatible Digital Inputs

### APPLICATIONS

Bell 212A Modem Filtering
CCITT V.22 / V.22 bis Modem Filtering
Bell 103 Modem Filtering
Other Modem Filter Applications

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-2126/7/8/9CN/CP | Ceramic/Plastic | 0°C to 70°C |

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# Disk Drive Circuits

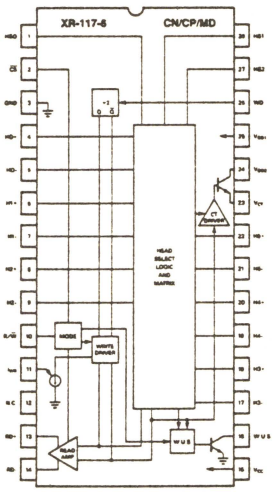
## XR-117 HARD DISK READ/WRITE

The XR-117 is a high speed head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-117 is compatible with 3½" to 14" single and multiple platter drives, and features high bandwidth, large dynamic range, and low noise. Several packaging options extend usefulness to applications requiring two, four, or six center-tapped read/write heads; multiple devices are easily cascaded for drives with more heads.

The XR-117R includes internal damping resistors, facilitating use in circuits requiring minimum external complexity and mass.

The XR-117, manufactured with a high speed bipolar process, operates on +5 V and +12 V.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Complete Head Interfacing Functions, Read and Write
High Bandwidth and Dynamic Range
Low Noise
Available in Two, Four, and Six Head Versions
Easily Cascaded for Larger Systems
Power Monitor with Automatic Disable
TTL Compatible Inputs

### APPLICATIONS

Single or Multiple Platter Hard Disk Drives

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-1172CP | 18 Pin Plastic | 0°C to 70°C |
| XR-117-4CP | 22 Pin Plastic | 0°C to 70°C |
| XR-117-6CP | 28 Pin Plastic | 0°C to 70°C |
| XR-117-xCN | Ceramic | 0°C to 70°C |
| XR-117-xCQ* | Surface Mount Quad | 0°C to 70°C |
| XR-117-xMD* | Surface Mount | 0°C to 70°C |
| XR-117-6CJ | 28 Pin PLCC | 0°C to 70°C |
| XR-117R-xCP | Plastic | 0°C to 70°C |
| XR-117R-xCQ* | Surface Mount Quad | 0°C to 70°C |
| XR-117R-xMD* | Surface Mount | 0°C to 70°C |
| XR-117R-6CJ | 28 Pin PLCC | 0°C to 70°C |

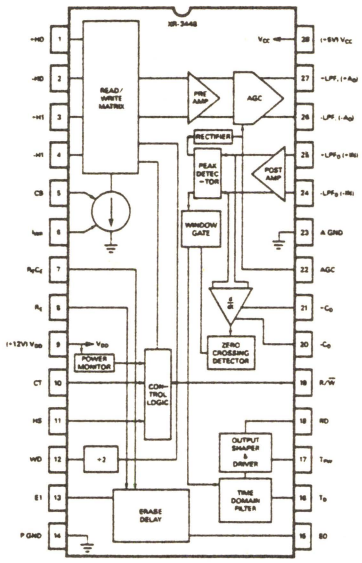
* = contact factory for availability
x = 2, 4 or 6, depending on number of heads required

## XR-3448 FLOPPY DISK READ/WRITE

The XR-3448 Floppy Disk Read/Write is a single 28 Pin monolithic solution for double-sided floppy disk drives. The device is compatible with 8", 5¼", and 3½" drives, providing all read and write functions and offering improved performance over industry standard dual chip sets, with lower external parts count. Schmitt trigger inputs and separate analog and power grounds aid noise and cross-talk immunity. Both pre and post amplifiers, plus an AGC, allow reliable operation with input signals ranging from 0.5 mV to 25mV.

The XR-3448 is available in standard or small outline 28 Pin packages. Control, write inputs, and read outputs are TTL compatible. The device operates from +12 V and +5 V supplies. The pinout is specially designed for similarity to the SSI-570 Read/Write, and in many applications, the XR-3448 acts as an improved version of that device.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

All Read/Write Functions on a Single Chip
Schmitt Trigger Inputs for Noise Immunity
TTL Compatible
Power Up and Low Voltage Inhibit
Low Peak Shift — No Trimming Necessary
On Board AGC
Wide Read Dynamic Range
Low External Parts Count
All Delays RC Programmable
Separate Power and Signal Ground
Tunnel or Straddle Erase Compatibility

### APPLICATIONS

Single or Dual Head Floppy Disk Drive Systems

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-3448CP | Plastic | 0°C to +70°C |
| XR-3448CN | Ceramic | 0°C to +70°C |
| XR-3448MD | Small Outline | 0°C to +70°C |

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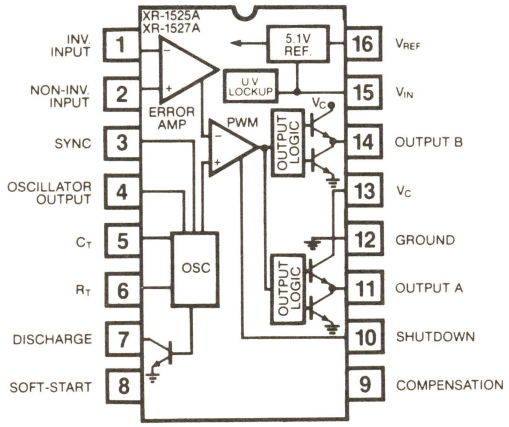
# PWM Regulators

## XR-1525A/2525A/3525A
## XR-1527A/2527A/3527A
## PULSE-WIDTH MODULATING REGULATORS

The XR-1525A/1527A are a series of monolithic integrated circuits that contain all of the control circuitry necessary for a pulse-width modulating regulator. Included are the voltage reference, error amplifier, oscillator, pulse-width modulator, under-voltage lockout, soft-start circuitry, and output drivers.

The on-chip + 5.1-volt reference is trimmed to ± 1% initial accuracy. Dead-time is adjustable with a single external resistor. The XR-1525A series gives a LOW output for an OFF state, while the XR-1527A series gives a HIGH output for an OFF state.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

8- to 35-Volt Operation
Adjustable Dead-Time Control
Internal Soft-Start
Latching PWM to Prevent Double Pulsing
Dual Source/Sink Output Driver Capable of +200 mA

### APPLICATIONS

Pulse-Width Modulation
Switching Regulators
Power Control Systems
Industrial Controls

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-1525/27AM | Ceramic | -55°C to +125°C |
| XR-2525/27AN | Ceramic | -25°C to +85°C |
| XR-2525/27AC | Plastic | -25°C to +85°C |
| XR-3525/27AN | Ceramic | 0°C to +70°C |
| XR-3525/27AC | Plastic | 0°C to +70°C |

**XR-494 PULSE-WIDTH MODULATING REGULATOR**
**XR-495 PULSE-WIDTH MODULATING REGULATOR**
**XR-1524/2524/3524 PULSE-WIDTH MODULATING REGULATORS**
**XR-1543/2543/3543 POWER SUPPLY OUTPUT SUPERVISORY CIRCUITS**

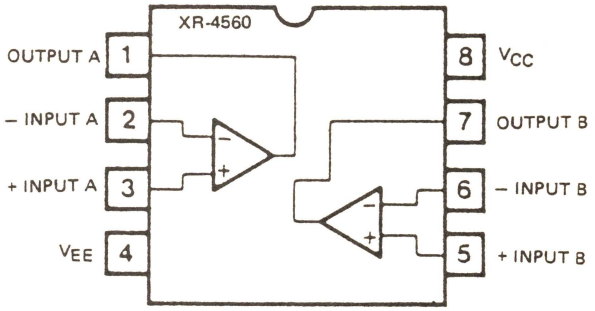
# Op Amplifiers

## XR-4560 DUAL LOW NOISE OPERATIONAL AMPLIFIER

The XR-4560 is a dual low noise, wide bandwidth operational amplifier ideal for active filter applications. The device is similar to the XR-1458/4558, with greatly enhanced slew rate, bandwidth, and guaranteed noise characteristics.

Pin for pin compatibility allows direct substitution for industry standard dual op amps where the low noise and wide bandwidth of the XR-4560 is imperative.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

High Gain, Low Input Noise
Internally Compensated
Wide Small Signal Bandwidth
Interchangeable with General Purpose 4560-type Op Amps

### APPLICATIONS

High Gain, Low Noise Amplifier
High Performance Active Filter
Small Signal Amplifier
Servo Control System
Telephone Channel Amplifier

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-4560CP | Plastic | 0°C to 70°C |
| XR-4560CN | Ceramic | 0°C to 70°C |
| XR-4560 | SO-8 | 0°C to 70°C |

**XR-082/083 DUAL BIPOLAR JFET OP AMP**
**XR-084 QUAD BIPOLAR JFET OP AMP**
**XR-3403/3503 QUAD OP AMP**
**XR-4136 QUAD OP AMP**
**XR-4558 DUAL OP AMP**
**XR-4741 QUAD OP AMP**
**XR-5532/5533A DUAL LOW NOISE OP AMP**
**XR-5534/5534A DUAL LOW NOISE OP AMP**

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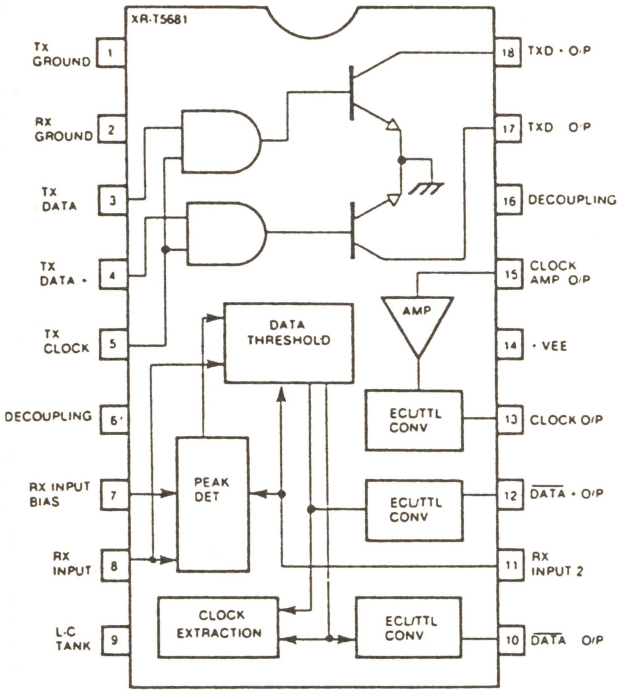
# T1 Trunk Interface Circuits

## XR-T5681 PCM TRANSCEIVER CHIP

The XR-T5681 is a PCM transceiver chip. It consists of both transmit and receive circuitry in a CERDIP 18 pin package. The transceiver is designed for short line application (<−10 dB) such as in digital muliplexed interfacing and digital PBX environments. The maximum frequency of operation is 3 MBits/s so it covers T1, T148C, and Europe's 2.048 MBit/s PCM system. The device is designed to operate over the temperature range of 0°C to +70°C.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Single +5.0 V Supply
Receiver Can Accept Either Balanced or Unbalanced Inputs
TTL Compatible Interface
Transmitter and Receiver in One Package

### APPLICATIONS

T1, T143C, and 2.048 MBits/s PCM Line Interface
CPI
DMI

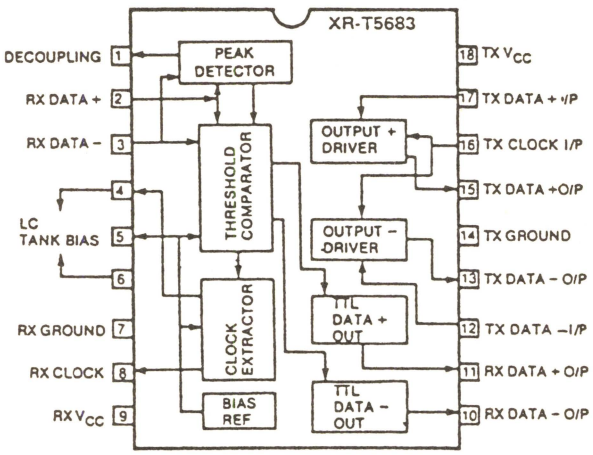
### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-T5681 | Ceramic | 0°C to 70°C |

## XR-T5683 PCM LINE INTERFACE CHIP

The XR-T5683 is a PCM line interface chip. It consists of both transmit and receive circuitry in a DIL 18 pin package. The maximum bit rate the chip can handle is 8.448 M Bits/s and the signal level to the receiver can be attenuated by −10 dB cable loss at half the bit rate. Total current consumption is between 27-46 mA at +5.0 V.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Single +5.0 V Supply
Receiver Input Can Be Either Balanced or Unbalanced
Up to 8.448 MBits/s Operation in Both
$T_X$ and $R_X$ Directions
TTL Compatible Interface

### APPLICATIONS

T1, T148C, T2, 2048 & 8448 KBits/s
PCM Line Interface
CPI
DMI

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-T5683 | Ceramic | -40°C to +85°C |

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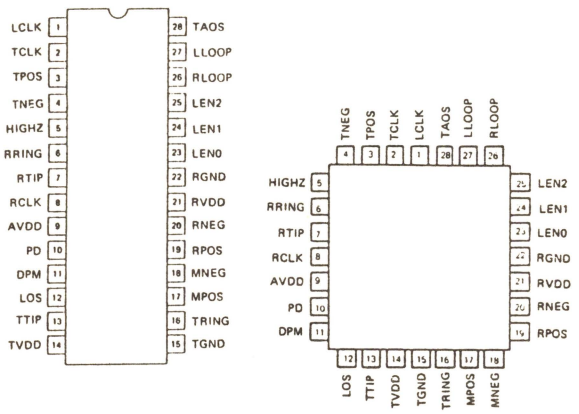
# T1 Interface Circuits

## XR-T5684 CMOS T1 TRUNK INTERFACE (ADVANCED INFORMATION)

The XR-T5684 is a PCM line transceiver IC. It consists of both transmit and receive circuitry in a 28 pin package. The transceiver is designed for short loop application (<-6 dB) such as digital office environments. It can operate at 1.544 Mbits/s as well as 2.048 Mbits/s for U.S. and European PCM systems. The device is designed to operate over the temperature range of -40°C to 85°C.

### FUNCTIONAL BLOCK DIAGRAM




XR-T5684

### FEATURES

Single +5 Volt Supply
Receiver Can Accept Either Balanced or Unbalanced Inputs
TTL Compatible Interface
Transmitter and Receiver in One Package
No L-C Tuning Required
CMOS Digital Technology

High Jitter Tolerance
Meets Bell Pub 62411 (October 1986) and Pub 43802 Requirements, and CCITT G.703 Requirements
Built-in Line Equalization for up to 650 Feet of Cable

### APPLICATIONS

T1, PCM Line Interface
CEPT, PCM Line Interface
CPI
DMI

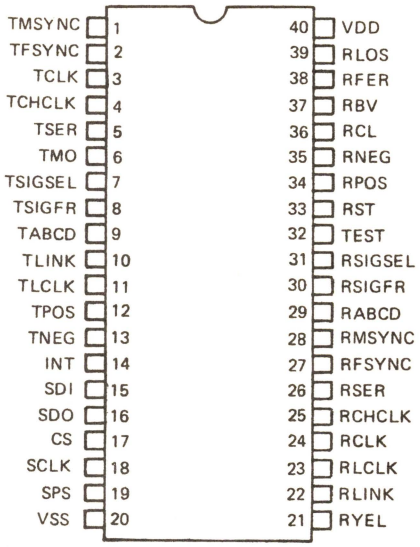
### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-T5684CN | Ceramic DIP | -40°C to 85°C |
| XR-T5684CP | Plastic DIP | 0°C to 70°C |
| XR-T5684CJ | PLCC | 0°C to 70°C |

## XR-T5690 SERIAL T1 TRANSCEIVER (ADVANCED INFORMATION)

The XR-T5690 is a monolithic CMOS IC designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing 12 frame/super frame applications. The 193E framing mode supports the extended super frame format (24 frames/super frame). Clear channel capability is provided by selection of appropriate zero suppression and signaling mode.

### FUNCTIONAL BLOCK DIAGRAM




XR-T5690

### FEATURES

Single +5 Volt Supply
Low Power CMOS Digital Technology
Single Chip DS1 Rate Transceiver
Supports 12 Frame/Super Frame and 24 Frame/Super Frame
B8ZS , B7 Stuffing and Transparent Zero Suppresion Modes
No Host Processor for Hardware Mode
Supports Host Processor for Serial Data Transmission
Selectable 0,2,4,16 State Robbed Bit Signaling Mode
Allows Mix of "CLEAR" and "NON CLEAR" DS0 Channels on Same DS1 Link
Alarm Generation and Detection
Receive Error Detection and Counting for Transmission Performance Monitoring

### APPLICATIONS

Digital MUXs
Channel Banks

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-T5690CP | Plastic DIP | 0°C to 70°C |
| XR-T5690CJ | PLCC | 0°C to 70°C |

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EXAR

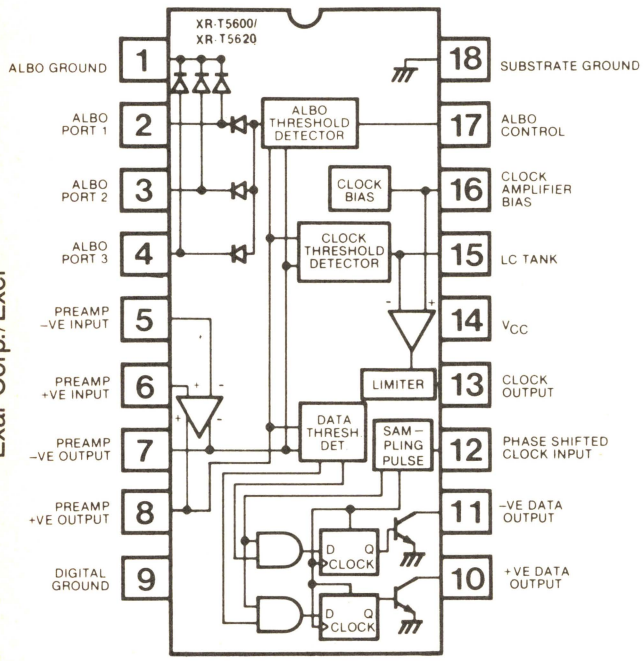
# Repeater Chips

## XR-T5600/T5620
## T1, T148C and 2 MBit/s PCM LINE REPEATER

The XR-T5600/T5620 is a bipolar monolithic repeater IC designed for PCM carrier systems operating at 1.544 M bit/s (T1), 2 M bit/s, or 2.37 M bit/s (T148C). It provides all of the active circuits required for one side of a PCM repeater.

A crystal filter clock extraction version of XR-T5600/ T5620 is available as XR-T5700/T5720.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

Single 5.1 V Power Supply
Less than 10 ns Sampling Pulse over the Operating Range
Triple Matched ALBO Ports
2 M Bit/s Capability

### APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
European 2 M Bit/s PCM Repeater
T1C PCM Repeater (require external preamplifier)

### ORDERING INFORMATION

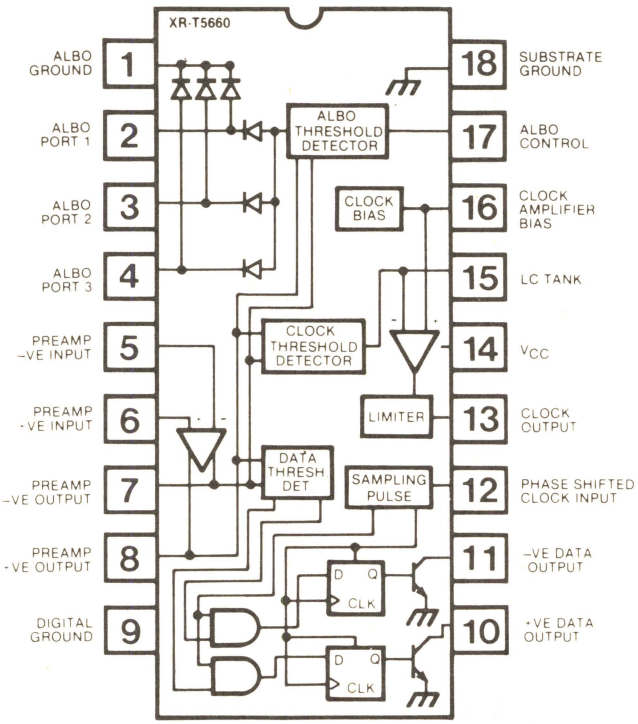
| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-T5600 | Plastic | -40°C to 85°C |
| XR-T5620 | Ceramic or Plastic | -40°C to 85°C |

## XR-T5650 PCM LINE RECEIVER AND CLOCK RECOVERY CIRCUIT

The XR-5650 is a monolithic bipolar IC designed for PCM type line receiver applications operating at T1. T148C, T1C and 2 M bit/s data rates. It provides all the active circuitry required to perform automatic line build out (ALBO), threshold detection, positive and negative data and clock recovery.

Clock recover using a crystal filter instead of an LC tank circuit is also available as XR-T5750.

### FUNCTIONAL BLOCK DIAGRAM




### FEATURES

On Chip Positive and Negative Data, Clock Recovery
Less than 10 ns Sampling Pulse over the Operating Range
Double Matched ALBO Ports
Single 5.1 V Power Supply
2 M Bit/s Capability

### APPLICATION

T1 PCM Line Receiver
T148C Line Receiver
T1C PCM Line Receiver (requires external amplifier)
General Purpose Bipolar Line Receiver
HDB3 Line Receiver
B8ZS Line Receiver

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-T5650 | Ceramic | -40°C to +85°C |

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# Local Area Network Circuits

## XR-T82515/T82C516 STARLAN TRANSCEIVER CHIP SET

The transceiver chip set XR-T82515 and XR-T82C516 is intended for interfacing between the transmission line and the LAN controller. It operates at 1 Mbit/sec and supports Carrier Sense Multiple Access with Collision Detect (CSMA/ CD) as specified in the IEEE 802.3, 1Base5 Standard Specification.

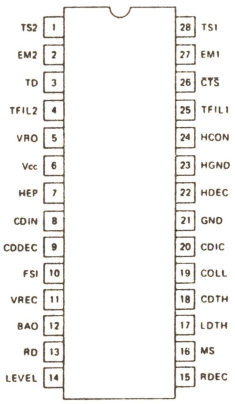
It is designed to operate in two environments:

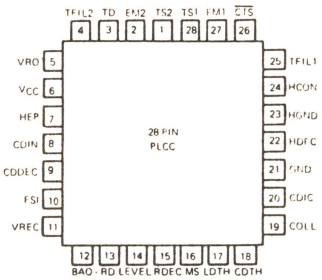
1. Coaxial Bus topology based on 75 ohm CATV cable (4000' cable length) or twised pair (24 AWG) bus configuration (1600' cable length).

2. Twisted pair Star topology systems (24 AWG/one transmit pair and one receive pair for up to 2400' cable length).

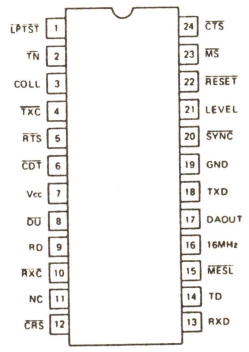
This is a low cost network implementation based on twisted pair wiring available in office buildings. The transceiver is compatible with the Intel 82586 or 82588 LAN communication controllers.

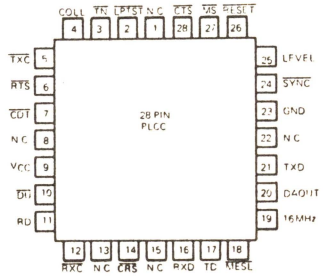
## FUNCTIONAL BLOCK DIAGRAM




XR-T82515




XR-T82C516

## FEATURES

100% Compatible with IEEE 802.3 StarLAN Specification
Based on Carrier Sense Multiple Access with Collision
Supports 48 Nodes Downstream in a Bus Configuration
Adaptive Hybrid Operation for Bus and Multipoint
Extension Topologies
Interfaces with Intel's 82586 or 82588 Communication Controllers
Supports 14 dB Attenuation in Bus and 20 dB in Star Configuration
Level and Logic Based Collision Detection
Built-in Jabber Function to Detect Faulty Transmitters
Manchester Encoding and Decoding
Detects Manchester Code Violation
External Slew Rate Control
Low Power Consumption When in Idle Mode

## APPLICATIONS

Synchronous and Asynchronous Communication Servers
File Servers
Remote Site Gateways
StarLAN Repeaters
Print Servers
Voice - Data PBX

## ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-T82515CP | Plastic | 0°C to 70°C |
| XR-T82515CJ | PLCC | 0°C to 70°C |
| XR-T82C516CP | Plastic | 0°C to 70°C |
| XR-T82C516CJ | PLCC | 0°C to 70°C |

Exar Corp./Exel

# Dual Channel UART

## XR-68C681/88C681 CMOS DUAL CHANNEL UART (DUART)

The EXAR Dual Univeral Asynchronous Receiver and Transmitter (DUART) is a data communications device that provides two fully independent full duplex asynchronous communications channels in a single package. The DUART is designed for use in micrprocessor based systems and may be used in a polled or interrupt driven environment.

Two basic versions of the DUART are available, each optimized for use with various microprocessor families: XR-88C681 for 8080/85, 8086/88, Z80, Z8000, 68xx and 65xx family based systems, and the XR-68C681 for 68000 family based systems. A programmable mode of the XR-88C681 version provides an interrupt daisy chain capability for use in Z80 and Z8000 based systems. However, the bus interfaces are general enough to allow interfacing with other microprocessors and microcontrollers. The XR-88C681 and XR-68C681 are enhanced versions of the Signetics, Motorola 2681 and 68681 respectively, and are pin and function compatible with those devices.

The DUART is fabricated using advanced two-layer metal high density CMOS process to provide high performance and low power consumption and is packaged in a 40 pin DIP. The XR-88C861 is also available in a 28 pin DIP.

## FEATURES

Full Duplex, Dual Channel, Asynchronous Receiver & Transmitter
Quadruple-Buffered Receiver, Dual-Buffered Transmitter
Stop Bits Programmable in 1/16-bit Increments
Internal Bit Rate Generator with 23 Bit Rates
Independent Bit Rate Selection for Each
  Receiver and Transmitter
Maximum Bit Rate: 1x Clock - 1 Mb/Sec, 16x Clock - 125Kb/Sec
Normal, Autoecho, Local Loopback, and Remote Loopback Modes
Multi-Function 16-Bit Counter/Timer
Interrupt Output with Eight Maskable Interrupting Cond.
Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
Up to 15 I/O Pins (Depending on Package and Version)
Change of State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine-Bit Mode
On-Chip Oscillator for Crystal
Standby Mode to Reduce Operating Power
Advanced CMOS Low Power Technology

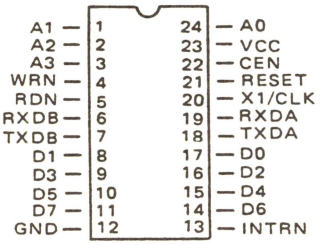
## ORDERING INFORMATION

XR-88C681XX/40, XR-88C681XX/28 and XR-68C681XX are offered in the following packages:

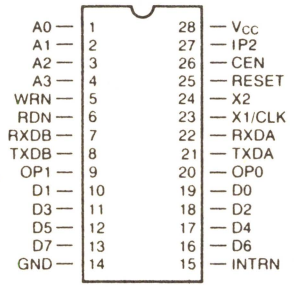
| XX=Suffix | Package | Operating Temperature |
|---|---|---|
| CN | Ceramic | 0°C to +70°C |
| N | Ceramic | -40°C to +85°C |
| M | Ceramic | -55°C to +125°C |
| L | Ceramic LCC | -40°C to +85°C |
| ML | Ceramic LCC | -55°C to +125°C |
| CP | Plastic | 0°C to 70°C |
| P | Plastic | -40°C to 85°C |
| CJ | PLCC | 0°C to 70°C |
| J | PLCC | -40°C to 85°C |

Contact factory for additional information.

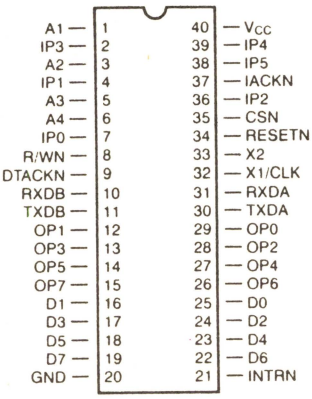
## FUNCTIONAL BLOCK DIAGRAM



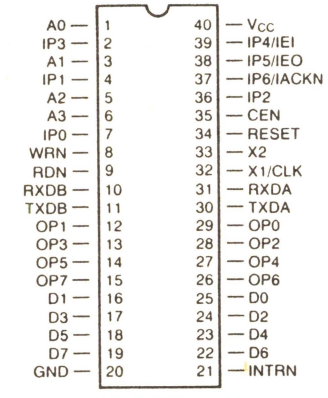

XR-88C681/24




XR-88C681/28




XR-68C681/40




XR-88C681/40

Exar Corp./Exel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# Quad Channel UART

## XR-82C684 CMOS QUAD CHANNEL UART (QUART)

The EXAR Quad Universal Asynchronous Receiver and Transmitter (QUART) is a data communications device that provides four fully independent full duplex asynchronous communications channels in a single package. The QUART is designed for use in microprocessor-based systems and may be used in a polled or interrupt driven environment.

The XR-82C684 offers a single IC solution for various microprocessor families by tying the SEL pin to VDD or VSS.

The QUART is fabricated using an advanced two-layer metal high density EPI/CMOS process to provide high performance and low power consumption, and is packaged in 68/44 pin PLCC and 64/40 pin DIP.

## FEATURES

Full Duplex, Four Independent Channels, Asynchronous Receiver and Transmitter
Quadruple Buffer Receiver and Transmitter
Programmable Stop Bits in 1/16 Bit Increments
Pin Selectable for Various Microprocessors
Four Independent Internal Bit Rate Generators With More Than 23 Bit Rates
Independent Bit Rate Selection for Each Transmitter and Receiver
External Clock Maximum Bit Rates:
1 x Clock = 1 Mbits/s
16 x Clock = 1 Mbits/s
Normal, Auto Echo, Local Loopback and Remote Loopback Modes
Two Multi-function 16 Bit Counter/Timer
Interrupt Output with Sixteen Maskable Interrupt Conditions
Prioritized Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
Sixteen General Purpose Outputs
Sixteen General Purpose Inputs with Eight Change-of-State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine Bit Mode
On-Chip Oscillator for Crystal
Stand-by Mode to Reduce Operation Power

## APPLICATIONS

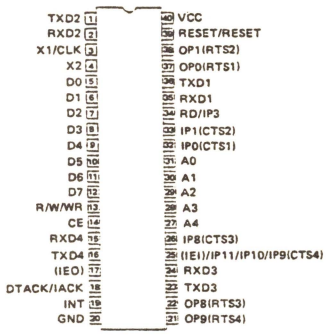
Multi-frame Computers
Workstations
CAD Systems

## ORDERING INFORMATION

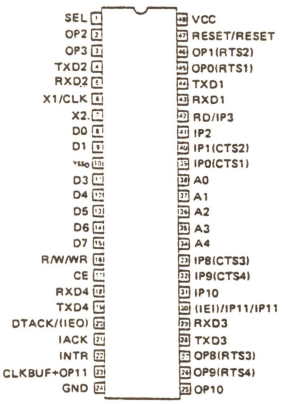
| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-82C684CP/XX* | DIP | 0°C to +70°C |
| XR-82C684CJ/XX | PLCC | 0°C to +70°C |

*Note: XX designates the pin count.
Contact the factory for information on industrial and military temperature ranges and 883C grade parts.

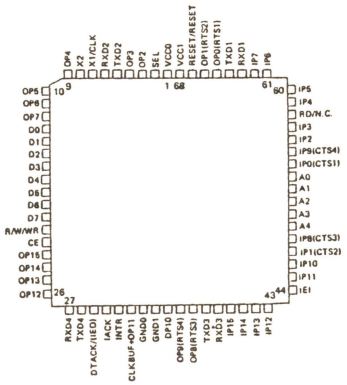
## FUNCTIONAL BLOCK DIAGRAM



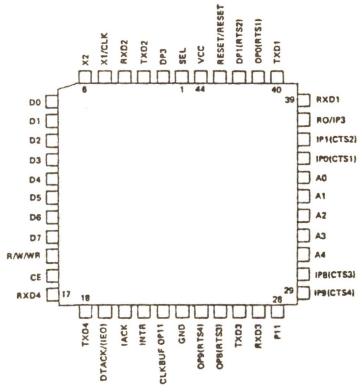

XR-82C684 40 pin DIP




XR-82C684 48 pin DIP




XR-82C684 68 pin PLCC




XR-82C684 44 pin PLCC

Exar Corp./Exel

FUJITSU

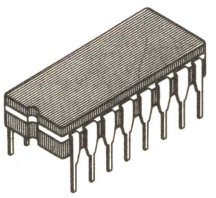
# ULTRA HIGH SPEED ECL ICs

## MB 810A/MB 811A MB 813A/MB 814A

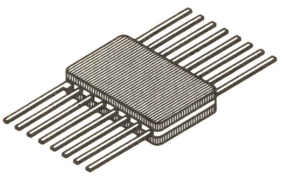
March 1987
Edition 1.0

### ULTRA HIGH SPEED ECL FAMILY

The Fujitsu MB 810A series is an ultra high speed logic designed for high speed digital systems. The MB 810A series is suitable not only for a high speed transmission equipment, a radio installation, a high speed logic treatment equipment, a high performance measuring instrument but for high speed gate array peripherals. The inputs/outputs level and power supply voltage are compatible with ECL 10 kH series. The MB 810A series devices are housed in 16-pin mini-flat packages and 16-pin dual-in-line packages.



CERAMIC PACKAGE
DIP-16C-C01



CERAMIC PACKAGE
FPT-16C-C01

- Ultra high speed:
  Propagation delay time – 400 ps/gate typ.
- ECL Interface level:
  10 kH ECL compatible inputs and outputs
- Output rising/falling time – 350 ps typ.
- Max. clock frequency: 1.5 GHz typ.
- Emitter Follower Output: Wired OR capability, 50 Ω line drivability
- Stable bias circuit for the changeable power supply voltage

### ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply ($V_{CCS}$ = $V_{CCF}$ = 0) | $V_{EE}$ | –7.0 to 0 | V |
| Input Voltage ($V_{CCS}$ = $V_{CCF}$ = 0) | $V_{IN}$ | –3.0 to 0 | V |
| Output Current | $I_{OUT}$ | –50 to 0 | mA |
| Operating Ambient Temperature | $T_A$ | –30 to +125 | °C |
| Storage Temperature | $T_{STG}$ | –55 to +150 | °C |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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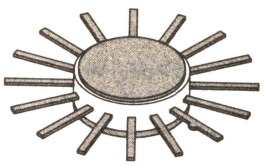
# ULTRA HIGH SPEED ECL ICs

**MB 881/MB 882**
**MB 883/MB 884**

September 1986
Edition 1.0

## ULTRA HIGH SPEED ECL FAMILY

The Fujitsu MB 880 series is a family of ultra high speed ECL integrated circuits. It is useful for Giga-bits fiber communication systems, and electrical measuring instruments. The inputs/outputs interface and power voltage are compatible with ECL 10K series. The MB 880 series devices are packaged in the compact circular ceramic flat packages that are convenient for mounting a high speed and high density printed circuit board.



**CERAMIC PACKAGE**
**FPT-16C-A01**

- Ultra High Speed:
  Propagation delay time — 150 ps/gate typ.
- ECL Interface Level:
  10K ECL compatible inputs and outputs

**Input/Output Characteristic**

| Parameter | Temperature Coefficient | $V_{EE}$ Coefficient |
|---|---|---|
| $V_{OH}$ | 1.6 mV/°C typ. | 20 mV/V typ. |
| $V_{OL}$ | 0.4 mV/°C typ. | 250 mV/V typ. |
| Input threshold voltage | 1.1 mV/°C typ. | 140 mV/V typ. |

- Single Power Supply:
  -5.2 V for $V_{EE}$, -2.0 V for output load terminations
- Emitter Follower Output:
  Wired OR capability, 50 Ω line drivability
- Compact Circular Flat Package:
  Low thermal resistance (10°C/W typ.(junction to case)), high density mounting capability
- 2 Pins for 1 Input:
  Having 2 pins for each input makes it easy to design the signal patterns on the printed circuit board.

**ABSOLUTE MAXIMUM RATINGS** ($V_{CC}$ = 0 V)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | $V_{EE}$ | -7.0 to 0 | V |
| Input Voltage | $V_I$ | -5.5 to 0 | V |
| Output Current | $I_{OUT}$ | 50 | mA |
| Case Temperature | $T_C$ | -30 to 125 | °C |
| Storage Temperature | $T_{STG}$ | -55 to 150 | °C |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

Fujitsu Microelectronics

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# ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

**MBM 10474A-5**
**MBM 10474A-7**

June 1987
Edition 1.0

## 4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The MBM 10474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as U-Fox (U-groove isolation with thick field oxide) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

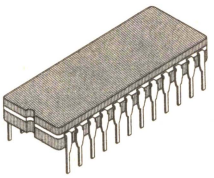
Operation for the MBM 10474A is specified over a temperature range of from 0° to 75°C ($T_A$ for DIP, $T_C$ for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 5 ns max. (MBM 10474A-5)
  7 ns max. (MBM 10474A-7)
- Chip select access time: 3 ns max. (MBM 10474A-5)
  5 ns max. (MBM 10474A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.33 mW/bit typ. (MBM 10474A-5)
  0.24 mW/bit typ. (MBM 10474A-7)
- DOPOS and U-Fox processing
- Pin compatible with the F10474

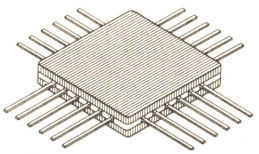
### ABSOLUTE MAXIMUM RATINGS (See NOTE)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| $V_{EE}$ Pin Potential to Ground Pin | $V_{EE}$ | +0.5 to -7.0 | V |
| Input Voltage | $V_{IN}$ | +0.5 to $V_{EE}$ | V |
| Output Current (DC, Output High) | $I_{OUT}$ | -30 | mA |
| Temperature under Bias | $T_A$ for DIP | -55 to +125 | °C |
| | $T_C$ for Flat Package and LCC | -55 to +125 | |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.



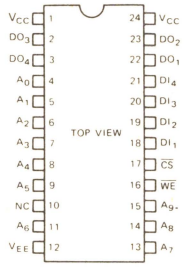
**CERAMIC PACKAGE**
**DIP-24C-C05**



**CERAMIC PACKAGE**
**FPT-24C-C02**

LCC-24C-F02: See page 10

**PIN ASSIGNMENT**




$V_{CC}$ grounded

LCC PAD CONFIGURATION : See page 10

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

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# ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMOLY

## MBM 10484A-10

March 1987
Edition 1.0

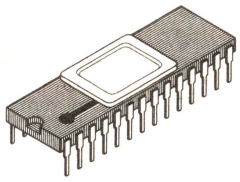
### 16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

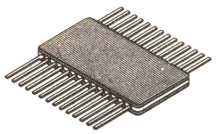
The MBM 10484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high hields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10484A is specified over a temperature range of from 0°C to 75°C ($T_A$ for DIP $T_C$ for Flat Package and LCC). It also features 28-pin ceramic DIP, Flat package, or LCC and is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 10 ns max.
- Chip select access time: 5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.07 mW/bit typ.
- DOPOS and IOP-II processing



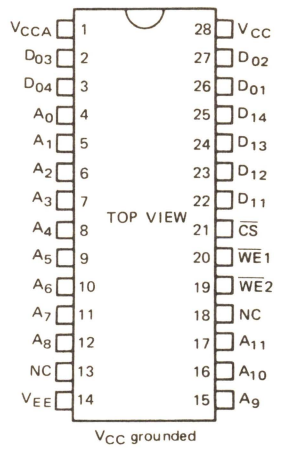
**CERAMIC PACKAGE**
**DIP-28C-A06**



**CERAMIC PACKAGE**
**FPT-28C-C03**

LCC-28C-F01 : See Page 10
LCC-28C-F02 : See Page 11

**PIN ASSIGNMENT**




See Page 10
LCC PAD CONFIGURATION: See Page 11

### ABSOLUTE MAXIMUM RATINGS (See NOTE)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| $V_{EE}$ Pin Potential to Ground Pin | $V_{EE}$ | +0.5 to -7.0 | V |
| Input Voltage | $V_{IN}$ | +0.5 to $V_{EE}$ | V |
| Output Current (DC, Output High) | $I_{OUT}$ | -30 | mA |
| Temperature under Bias | $T_A$ for DIP | -55 to +125 | °C |
| | $T_C$ for Flat Package and LCC | -55 to +125 | |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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# ECL 65536-BIT BIPOLAR RANDOM ACCESS MEMORY

**MBM100490-15**
**MBM100490-25**

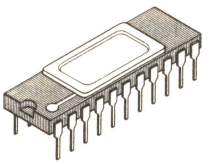
July 1987
Edtion 1.0

## 65536-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

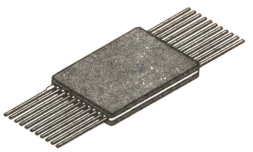
The Fujitsu MBM 100490 is fully decoded 65536-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on-chip voltage temperature compensation for improved noise margin.

The MBM 100490 offers extremely small cell and chip size, realized through the use of Fujitsu's patened IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 100490 is specified over a temperature range of from 0°C to 85°C ($T_C$). It also features 22 pin Ceremic DIP or Flat Package. It is fully compatible with industry-standard 100K-series ECL familes.



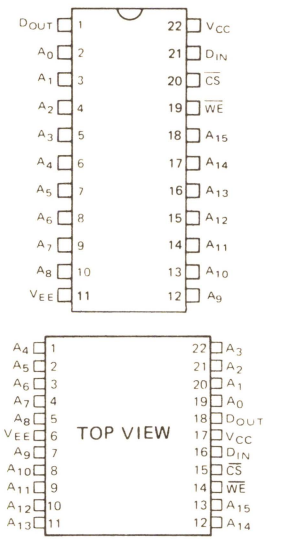
**CERAMIC PACKAGE**
**DIP-22C-A02**



**CERAMIC PACKAGE**
**FPT-22C-C01**

- 65536 words x 1 bit organization
- On-chip voltage temperature compensation for improved noise margin.
- Fully compatible with industry-standard 100K-series ECL families.
- Address access time: 15 ns max. (MBM 100490-15)
  25 ns max. (MBM 100490-25)
- Chip select access time: 10 ns max. (MBM 100490-15)
  15 ns max. (MBM 100490-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.017 mW/bit typ. (MBM 100490-15)
  0.012 mW/bit typ. (MBM 100490-25)
- IOP-II

**PIN ASSIGNMENT**




*$V_{CC}$ grounded

LCC PAD CONFIGURATION : SeePage 10

**ABSOLUTE MAXIMUM RATINGS (See NOTE)**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| $V_{EE}$ Pin Potential to Ground Pin | $V_{EE}$ | +0.5 to −7.0 | V |
| Input Voltage | $V_{IN}$ | +0.5 to $V_{EE}$ | V |
| Output Current (DC, Output High) | $I_{OUT}$ | −30 | mA |
| Temperature under Bias | $T_C$ | −55 to +125 | °C |
| Storage Temperature | $T_{STG}$ | −65 to +150 | °C |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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# CMOS UV ERASABLE 262144-BIT READ ONLY MEMORY

**MBM 27C256H-10**
**MBM 27C256H-12**

June 1986
Edition 1.0

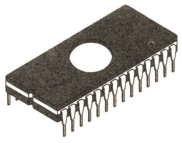
## CMOS 262144 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

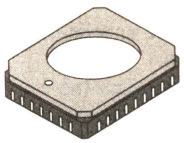
The Fujitsu MBM 27C256H is a 262,144 bits high speed CMOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM 27C256H. The transparent lid allows the user to expose the device to ultra violet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C256H is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



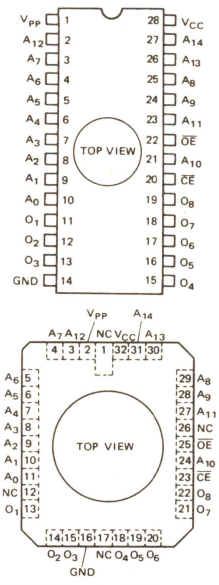
**CERAMIC PACKAGE**
**DIP-28C-C01**



**CERAMIC PACKAGE**
**LCC-32C-F01**

- CMOS power consumption
  Standby: 550 μW max.
  Active: 330 mW max.
- 32,768 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ algorithm
- Programming voltage: 12.5V
- No clocks required (fully static operation)
- Fast access time:
  100 ns max. (MBM 27C256H-10)
  120 ns max. (MBM 27C256H-12)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Single +5V supply, ±10% tolerance
- Standard 28-pin ceramic
  DIP: Suffix-Z
- Standard 32-pad ceramic
  LCC: Suffix-TV

### PIN ASSIGNMENT




### ABSOLUTE MAXIMUM RATINGS (see NOTE)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Temperature under Bias | $T_{BIAS}$ | -25 to +85 | °C |
| Storage Temperature | $T_{STG}$ | -65 to +125 | °C |
| All Inputs/Outputs Voltage with respect to GND | $V_{IN}$, $V_{OUT}$ | -0.6 to $+V_{CC}$ + 0.6 | V |
| Voltage on $A_9$ with respect to GND | $V_{A9}$ | -0.6 to +13.5 | V |
| $V_{PP}$ Voltage with respect to GND | $V_{PP}$ | -0.6 to +13.5 | V |
| Supply Voltage with repsect to GND | $V_{CC}$ | -0.6 to +7 | V |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Quick Pro™ is a trademark of FUJITSU LIMITED

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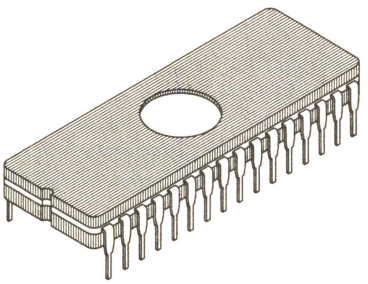
# CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

**MBM 27C1001-20**
**MBM 27C1001-25**

March 1987
Edition 1.0

## CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

PRELIMINARY



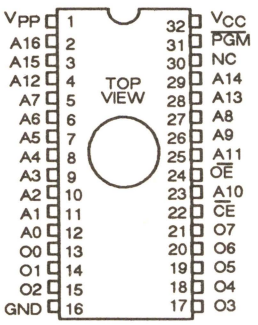
CERAMIC PACKAGE
DIP-32C-C01

The Fujitsu MBM 27C1001 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The device contains 1,048,576 programmable or reprogrammable bits organized in a 131,072-byte/8-bit format. The MBM 27C1001 is housed in a 32-pin DIP with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15-to-21 minutes. A new bit pattern can then be written into memory.

The MBM 27C1001 EPROM is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM 27C1001 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

- 131,072-byte/8-bit organization with on-chip decoding
- Single-byte or four-byte programming capability with Quick Pro™ algorithm
- Static operation (no clocks required)
- Upward compatible with 256K/512K EPROMS
- Fast access time:
  MBM 27C1001-20 = 200 ns (max)
  MBM 27C1001-25 = 250 nx (max)
- Easy and simple memory expansion via @pin
- Three-state output for wired-OR capability
- TTL-compatible inputs/outputs
- Single =5V (+10%) power supply with low current drain:
  Active operation = 30 mA (max)
  Standby operation = 0.1 mA (max)
- Programming voltage: +12.5V
- JEDEC-approved pin assignments
- 32-pin CERDIP

### PIN ASSIGNMENT




### ABSOLUTE MAXIMUM RATINGS (see NOTE)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage with respect to ground | $V_{CC}$ | -0.6 to + 7.0 | V |
| Programming Voltage with respect to ground | $V_{PP}$ | -0.6 to + 14.0 | V |
| Input/Output Voltage (except for $A_9$ with respect to ground) | $V_{IN\ 1}$ | -0.6 to $V_{CC}$ + 0.6 | V |
| Programming Voltage with respect to ground | $V_{IN\ 2}$ | -0.6 to + 13.5 | V |
| Temperature under Bias | $T_{BIAS}$ | -25 to + 85 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 to + 125 | °C |

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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# CMOS 1048576-BIT FAST PAGE DYNAMIC RAM

**MB81C1000-10**
**MB81C1000-12**
**MB81C1000-15**

July 1987
Edition 3.0

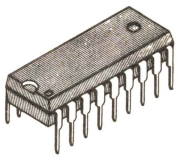
## CMOS 1,048,576 x 1 BIT FAST PAGE DYNAMIC RAM

The Fujitsu MB 81C1000 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB 81C1000 has been designed for mainframe memories, buffer memories, and video image memories requiring highspeed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very lower power dissipation.

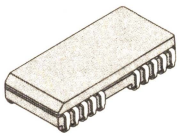
Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB 81C1000 high $\alpha$-ray soft error immunity and long refresh time.

Since the CMOS circuits are used for peripheral circuits, low power dissipation and high speed operation are realized.

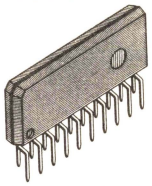
The CMOS standby current is about one-tenth that of the conventional NMOS DRAM, so large capacity memory systems such as semiconductor disks with less power and battery backup becomes possible, i.e., low standby current makes the RAM applicable as non-volatile memories. RAM not requiring large cooling mechanisms are also ideal for equipment which need to work quietly.



**PLASTIC PACKAGE**
**DIP-18P-M04**



**PLASTIC PACKAGE**
**LCC-26P-M01**

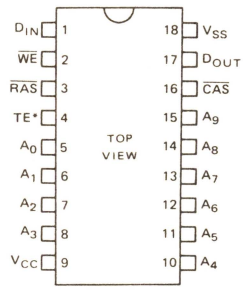


**PLASTIC PACKAGE**
**ZIP-20P-M02**

**DIP-18C-A01: See Page 17**
**LCC-26C-A01: See Page 18**

- 1,048,576 x 1 CMOS DRAM, 18-pin DIP, 26-pin SOJ, and 20-pin ZIP
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- Row Access Time ($t_{RAC}$),
  100 ns max. (MB 81C1000-10)
  120 ns max. (MB 81C1000-12)
  150 ns max. (MB 81C1000-15)
- Random Cycle Time ($t_{RC}$),
  180 ns min. (MB 81C1000-10)
  210 ns min. (MB 81C1000-12)
  260 ns min. (MB 81C1000-15)
- Column Access Time ($t_{CAC}$),
  30 ns max. (MB 81C1000-10)
  35 ns max. (MB 81C1000-12)
  40 ns max. (MB 81C1000-15)
- Fast Page Mode Cycle Time ($t_{PC}$),
  60 ns min. (MB 81C1000-10)
  70 ns min. (MB 81C1000-12)
  80 ns min. (MB 81C1000-15)
- Single 5V±10% Supply
- Low Power Dissipation
  330 mW max. (MB 81C1000-10)
  275 mW max. (MB 81C1000-12)
  220 mW max. (MB 81C1000-15)
  11 mW max. (TTL level input)
  5.5 mW max. (CMOS level input)
- 512 refresh cycles every 8.2 ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Early Write and Delayed Write
- Fast Page Mode Read-Modify-Write capability.
- Common I/O capability by using early write

### PIN ASSIGNMENT




*: Test Enable (will be available)

**Pin Assignment**
**For SOJ: See Page 15/18**

**Pin Assignment**
**For ZIP: See Page 16**

### ABSOLUTE MAXIMUM RATINS (See NOTE)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | | $V_{IN}$, $V_{OUT}$ | -1 to +7 | V |
| Voltage on $V_{CC}$ Relative to $V_{SS}$ | | $V_{CC}$ | -1 to +7 | V |
| Storage Temperature | Ceramic | $T_{STG}$ | -55 to +150 | °C |
| | Plastic | | -55 to +125 | |
| Power Dissipation | | $P_D$ | 1.0 | W |
| Short Circuit Output Current | | — | 50 | mA |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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# CMOS 262,144-BIT STATIC RANDOM ACCESS MEMORY

**MB 81C81-45**
**MB 81C81-55**

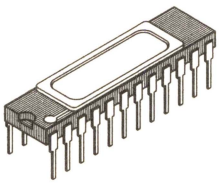
April 1987
Edition 1.0

## 262,144 WORDS × 1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

The Fujitsu MB81C81 is 262,144 words × 1 bit static random access memory fabricated with a CMOS technology.
Since MB81C81 consists of NMOS cells and CMOS peripherals, it is packaged in 300mil DIP and reached low power dissipation such as 550mW (55ns version).
It uses fully static circuitry and therefore requires no clocks or refreshing to operate.
The MB81C81 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.
MB81C81 is compatible with TTL logic families in all respects; input, output and a single +5V supply.

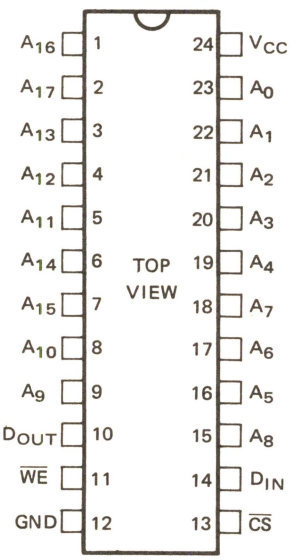
- Organization: 262,144 words × 1 bit
- Static operation: No clocks or refresh required
- Fast access time: 45ns max. (MB81C81-45)
  55ns max. (MB81C81-55)
- Low Power Consumption: Operating 660mW max. (MB81C81-45)
  550mW max. (MB81C81-55)
  Standby 83mW max. (CMOS level)
  165mW max. (TTL level)
- Single +5V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 24-pin DIP (300mil width) (Suffix: C)

PRELIMINARY



**CERAMIC PACKAGE**
**DIP-24C-A08**

**PIN ASSIGNMENT**




**ABSOLUTE MAXIMUM RATINGS (See NOTE)**

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | −0.5 to +7 | V |
| Input Voltage on any pin with respect to GND | | $V_{IN}$ | −3.5* to +7 | V |
| Output Voltage on any pin with respect to GND | | $V_{OUT}$ | −0.5 to +7 | V |
| Output Current | | $I_{OUT}$ | ±20 | mA |
| Power Dissipation | | $P_D$ | 1.0 | W |
| Temperature Under Bias | | $T_{BIAS}$ | −10 to +85 | °C |
| Storage Temperature | Ceramic | $T_{STG}$ | −65 to +150 | °C |

*DC: Min.=−0.5V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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# CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

**MB 84256-10/10L/10LL**
**MB 84256-12/12L/12LL**
**MB 84256-15/15L/15LL**

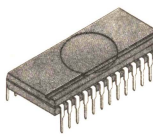
August 1986
Edition 2.0

## 256K-BIT (32,768 x 8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

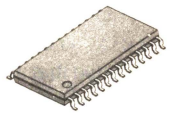
The Fujitsu MB 84256 is a 32,768-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronouse circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volts power supply is required.

The MB 84256 is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

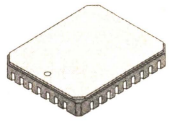
- Organization: 32,768 x 8 bits
- Fast access time: 100 ns max. (MB 84256-10/10L/10LL)
  120 ns max. (MB 84256-12/12L/12LL)
  150 ns max. (MB 84256-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state outputs
- Single +5V power supply, ±10% tolerance
- Low power standby:
  CMOS level: 5.5 mW max. (MB 84256-10/12/15)
  0.55 mW max. (MB 84256-10L/10LL/12L/12LL/15L/15LL)
  TTL level: 16.5 mW max. (MB 84256-10/10L/10LL/12/12L/12LL/15/15L/15LL)
- Data retention: 2.0V
- Standard 28-pin DIP (600 mil) (Suffix: -P)
- Standard 28-pin Bend-type Plastic Flat Package (450 mil) (Suffix: -PF)
- Standard 32-pad LCC (Suffix: -CV)



PLASTIC PACKAGE
DIP-28P-M02

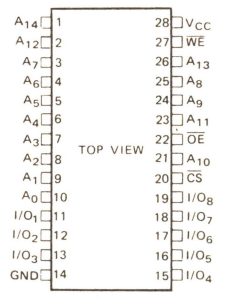


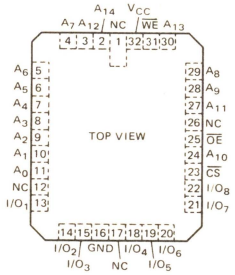
PLASTIC PACKAGE
FPT-28P-M02



CERAMIC PACKAGE
LCC-32C-A02

### PIN ASSIGNMENT




### ABSOLUTE MAXIMUM RATINGS (see NOTE)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | −0.5 to +7.0 | V |
| Input Voltage | | $V_{IN}$ | −0.5 to $V_{CC}$+0.5 | V |
| Output Voltage | | $V_{OUT}$ | −0.5 to $V_{CC}$+0.5 | V |
| Temperature Under Bias | | $T_{BIAS}$ | −10 to +85 | °C |
| Storage Temperature Range | CERAMIC | $T_{STG}$ | −65 to +150 | °C |
| | PLASTIC | | −40 to +125 | |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fujitsu Microelectronics

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# SCSI PROTOCOL CONTROLLER

# MB87030

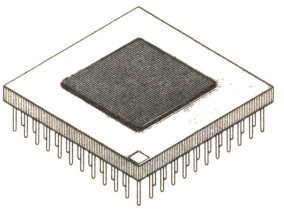
April 1986
Edition 1.0

## DESCRIPTION

The MB87030 SCSI Protocol Controller (SPC) is a CMOS LSI circuit specifically designed to control a Small Computer Systems Interface (SCSI). The SPC can serve as either an Initiator or Target for the SCSI; thus, it can be used as an I/O controller or as a host adapter. To use the device in the most effective manner, it is recommended that the user be thoroughly familiar with the SCSI protocol. For detailed information in these areas, the user should request the "Users Guide for MB87030 SCSI" from the nearest Sales Office of Fujitsu.

The SPC is designed to control all SCSI interface signals and virtually all interface control procedures. Used as an 8- or 16-bit peripheral, the device provides high-level control for almost all SCSI configurations.

To achieve optimum performance and interface flexiblity, the SPC contains an 8-byte First In First Out (FIFO) data buffer register and a 24-bit transfer byte counter. Independent data busses for the CPU and the DMA controller plus separate input/output pins for all control signals greatly reduces the possiblity of a "busy" condition. Data transfers can be executed in either the synchronous or asynchronous mode with a maximum offset of 8-bytes.



PGA-88C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

## FEATURES

- Independent data transfer bus for CPU and DMA controller
- Full support for SCSI control
- Serves as either *Initiator* or *Target* device
- Synchronous mode transfer with a programmable offset of up to eight bytes
- In synchronous mode, data transfer speed programmable at four rates
- Data transfer rates of up to 4 megabytes per second
- Eight-byte data buffer register
- 24-bit transfer byte counter
- Compatible with single-ended and/or differential alternative for SCSI
- Single +5V supply
- Low power dissipation
- TTL-compatible I/O
- 88-Pin Ceramic Repeated Quad-In-Line Package

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# ETHERNET DATA LINK CONTROLLER

**MB 8795B**

April 1987
Edition 1.0

## ETHERNET DATA LINK CONTROLLER

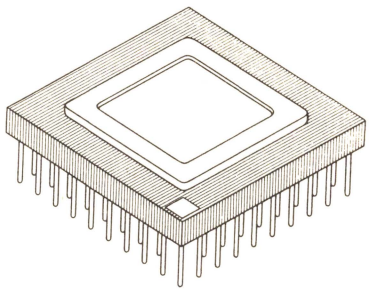
The Fujitsu MB 8795B Ethernet Data Link Controller (EDLC), manufactured with Fujitsu's Advanced CMOS Technology, is designed for Ethernet™ Local Area Network Systems and to be used with Fujitsu's MB 502A Ethernet Encoder/Decoder (EED).

The MB 8795B EDLC provides the user with a low power implementation of the Data Link Layer of the Ethernet Blue Book Specification. High throughput is possible via the separate data ports, while low cost implementations are also possible by tying the ports together.

The host system communicates with the MB 8795B EDLC using the command and status registers accessed through the control port. Functions provided include complete transmit and receive control, and interrupt masking.

- Implementing Ethernet Blue Book Specification
- Function to generate and remove preamble and CRC
- Conversion between serial and parallel data
- Four modes of address recognition:

  Accept no packet, Physical Address/Multicast-group Address/Broadcast Address, Physical Address/Multicast Address, Accept all packets
- Random exponential backoff to recover from collisions
- Three separate data ports providing flexible interface: Transmit, Receive, Control Ports
- Optional parity check on transmit byte stream
- Odd parity generated for receive byte stream
- Low power, advanced silicon gate CMOS Technology
- Space Saving 64-pin pin grid array package



**Ceramic Package**
**PGA-64C-A02**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

### ABSOLUTE MAXIMUM RATINGS (SEE NOTES)

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Supply Voltage | $V_{CC}$ | GND - 0.3* | 7.0 | V |
| Input and Output Voltage | $V_I$, $V_{OUT}$ | GND - 0.3* | $V_{CC}$ + 0.3* | V |
| Storage Temperature | $T_{STG}$ | -55 | 150 | °C |
| Operating Temperature | $T_{OP}$ | 0 | 70 | °C |

NOTES 1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. *0.3 V is for stable state. For transit state, 0.5 V is allowed (20 to 30 nsec).

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FUJITSU

# ETHERNET ENCODER / DECODER

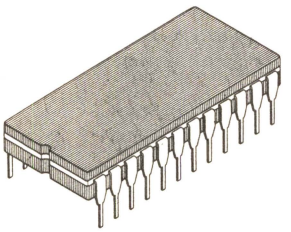
# MB 502A

October 1983
Edition 2.0

## ETHERNET ENCODER/DECODER

The Fujitsu MB 502A is an Ethernet* Encoder/Decoder designed to meet all the requirements of the Ethernet Blue Book specification and fabricated with high-speed ECL and Schottky TTL technology.

The encoder converts serial binary data into complementary Manchester code. The decoder converts Manchester code into binary data and synchronous clock signals. The decoding method is a digital phase locked loop with dual bandwidth which allows both fast lock-on and a small amount of jitter. Typical acquisition is eight bits or better. A key feature of the decoder design is its capability to recover distorted input signals. The MB 502A is packaged in a 24-pin ceramic standard DIP.

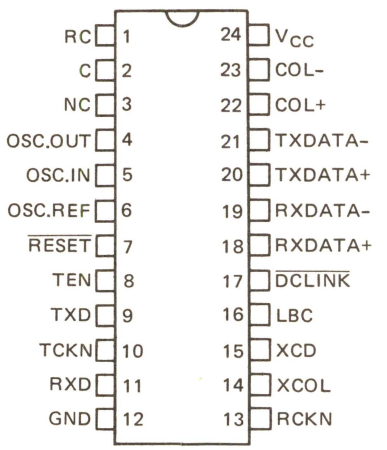


CERAMIC PACKAGE
DIP-24C-C01

## FEATURES

- Full Ethernet compatibility
- Manchester encode and decode
- Level conversion: transceiver level to/from TTL level
- Carrier detection
- Large distortion recovery: ±20 ns
- Dual bandwidth phase locked loop: allows fast acquisition
- Loopback "CONFIDENCE" test feature
- Built-in clock generator
- Small external parts count: all passive external components
- High-speed ECL and Schottky TTL technology
- Single power supply: +5V
- Low power dissipation: 750mW typ.
- 24-pin standard Dual In-line Ceramic Package

PIN ASSIGNMENT

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# MB88303
## NMOS Television Display Controller

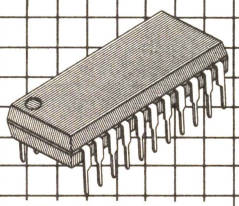
### Description

The Fujitsu MB88303 NMOS Television Display Controller (TVDC) is an interface LSI that displays 180 alphanumeric characters (20 characters x 9 lines) in white on a TV screen. The characters overlay the picture on the TV screen.

While designed to operate in conjunction with the Fujitsu MB8840/8850 and MB88400/88500 single-chip 4-bit microcomputers, the MB88303 TVDC can also be interfaced to a wide range of 4- and 8-bit microprocessors.

The MB88303 allows simple interface to almost any TV display (raster scan CRT with horizontal and vertical scanning) regardless of interlace or non-interlace scan.

The MB88303 is fabricated with N-channel silicon-gate E/D MOS process, and packaged in a 22-pin plastic DIP. Also, it is powered by a single +5V power supply, and operates over a temperature range of -30°C to +70°C.



**Plastic Package**
**DIP-22P-M02**

### Features

- **Character display controller available for NTSC, PAL and SECAN TV sets**
- **20 character x 9-line screen format (Max. 180 characters/screen)**
- **5x7-dot matrix character format (1-dot horizontal and 2-dot vertical spacings)**
- **64-character set**
- **Programmable character size: 4 widths and 4 heights**
- **Programmable display start position: 57 horizontal and 64 vertical positions**
- **Programmable character blinking control**
- **Automatic inter-dot filling function for improved smoothness**
- **Black-level background output for improved clarity**
- **180 x 7-bit display data RAM**
- **406 x 5-bit character generator ROM**
- **Four control registers**
- **3-bit general-purpose open-drain latched output**
- **On-chip clock generator for external RC-network**
- **Single +5V power supply**
- **Wide operating temperature range: -30° C to +70° C**
- **N-channel silicon-gate E/D MOS process**
- **22-pin plastic DIP**



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# Advanced CMOS Logic (ACL)



RCA's new Advanced High-Speed CMOS Logic (ACL) product represents the second generation of high-speed CMOS logic that began with the introduction of high-speed CMOS in 1982. Designated the CD74AC and CD74ACT families, these devices match Fairchild's bipolar FAST™ devices in speed, performance and logic/type output drive, but at CMOS power levels.

Featuring < 3-ns gate propagation delays, ACL is the fastest CMOS logic yet available. (By contrast, the standard propagation delay for CMOS logic is 95 ns, and for high-speed CMOS logic, 9 ns.) ACL can operate at more than 150 MHz. Output drive capability is 24 mA, compared with 6 mA for HC/HCT. This capability enables ACL to drive transmission lines, yet still generate the voltages necessary to operate the receiving logic devices safely.

Benefits of the ACL family compared to other logic families include:

- Lower power dissipation
- Balanced propagation delay
- Superior input characteristics
  Larger noise immunity and noise margin
  Input switching voltage stability with temperature variation
  Lower input current
- Improved output source current with better balance
- Wider operating supply voltage range
- Wider commercial-product operating-temperature range
- Lower 3-state output leakage current (high-Z mode)
- Improved reliability in general, and particularly in surface-mount (small-outline) packages
- Rail-to-rail output voltage swing

## ACL Family Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | -0.5 to 6.0V |
| DC Input Diode Current ($I_{IK}$) $V_I < 0$ | ± 20 mA |
| DC Input Voltage ($V_I$) | -0.5 to $V_{CC}$ +0.5V |
| DC Output Diode Current ($I_{OK}$), $V_O < 0$ | ± 50 mA |
| DC Output Voltage ($V_O$) | -0.5 to $V_{CC}$ +0.5V |
| DC Output Source or Sink ($I_O$) | ± 50 mA |
| Current, Per Output Pin | |
| DC $V_{CC}$ or Ground Current ($I_{CC}$ or $I_{gnd}$) | ± 100 mA* |

*(For up to 4 outputs per device: add +25 mA for each additional output.)

## Recommended Operating Conditions for ACL Family

| | | | |
|---|---|---|---|
| Supply Voltage* (life test voltage = 5.5V) | $V_{CC}$ | 1.5 to 5.5 | V |
| Input Voltage | $V_I$ | 0 to $V_{CC}$ | V |
| Output Voltage | $V_O$ | 0 to $V_{CC}$ | V |
| Operating Temperature Range 74AC | $T_A$ | -40 to +125 | °C |
| Input Rise and Fall Times, $t_r$, $t_f$ | 1.5V | 0 to 250 | ns |
| | 3.0V | 0 to 250 | |
| | 5.5V | 0 to 100 | |

*Unless otherwise specified.

## ACL Family DC Specifications

| Characteristic | $V_{CC}$ (V) | Test Conditions | Temperature (°C) +25° C Min. | +25° C Max. | -40 to +85°C Min. | -40 to +85°C Max. | -55 to +125°C Min. | -55 to +125°C Max. | |
|---|---|---|---|---|---|---|---|---|---|
| High Level Input Voltage, $V_{IH}$ | 1.5 | | 1.2 | — | 1.2 | — | 1.2 | — | V |
| | 3.0 | | 2.10 | — | 2.10 | — | 2.10 | — | |
| | 5.5 | | 3.85 | — | 3.85 | — | 3.85 | — | |
| Low Level Input Voltage, $V_{IL}$ | 1.5 | | — | 0.3 | — | 0.3 | — | 0.3 | |
| | 3.0 | | — | 0.9 | — | 0.9 | — | 0.9 | |
| | 5.5 | | — | 1.65 | — | 1.65 | — | 1.65 | |
| High Level Output Voltage, $V_{OH}$ | 1.5 | $V_I = V_{IH}$ or $V_{IL}$ -50 μA | 1.40 | — | 1.40 | — | 1.40 | — | V |
| | 3.0 | -50μA | 2.90 | — | 2.90 | — | 2.90 | — | |
| | 4.5 | -50 μA | 4.40 | — | 4.40 | — | 4.40 | — | |
| | 3.0 | -4 mA | 2.58 | — | 2.48 | — | 2.40 | — | |
| | 4.5 | -24 mA | 3.94 | — | 3.80 | — | 3.70 | — | |
| Low Level Output Voltage, $V_{OL}$ | 1.5 | $V_I = V_{IH}$ or $V_{IL}$ 50 μA | — | 0.10 | — | 0.10 | — | 0.10 | V |
| | 3.0 | 50 μA | — | 0.10 | — | 0.10 | — | 0.10 | |
| | 4.5 | 50 μA | — | 0.10 | — | 0.10 | — | 0.10 | |
| | 3.0 | 12 mA | — | 0.36 | — | 0.44 | — | 0.50 | |
| | 4.5 | 24 mA | — | 0.36 | — | 0.44 | — | 0.50 | |
| Input Leakage Current, $I_L$* | 5.5 | $V_I = V_{CC}$ or Gnd | — | 0.1 | — | ±1 | — | ±1 | μA |
| 3-State Output Current, $I_{OZ}$ | 5.5 | $V_I = V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or Gnd | — | 0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply • Current, $I_{CC}$† Δ | 5.5 | $V_I = V_{CC}$ or Gnd | — | 4 | — | 40 | — | 80 | μA |
| | 5.5 | $I_O = 0$ | — | 8 | — | 80 | — | 160 | |

*For I/O pins, use $I_{OZ}$. †Refer to objective specifications. • SSI/FF Δ MSI


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# Product Selection Guide

| Type | Function/Description | Classification |
|---|---|---|
| **CD74** | **NAND/NOR Gates** | |
| AC/ACT00 | Quad 2-Input NAND Gate | SSI |
| AC/ACT02 | Quad 2-Input NOR Gate | SSI |
| AC/ACT10 | Triple 3-Input NAND Gate | SSI |
| AC/ACT20 | Dual 4-Input NAND Gate | SSI |
| | **AND/OR/EXCLUSIVE-OR Gates** | |
| AC/ACT08 | Quad 2-Input AND Gate | SSI |
| AC/ACT32 | Quad 2-Input OR Gate | SSI |
| AC/ACT86 | Quad 2-Input EXCLUSIVE-OR Gate | SSI |
| | **Inverters/Buffers/Bus Drivers** | |
| AC/ACT04 | Hex Inverter/Buffer | SSI |
| AC/ACT05 | Hex Inverter/Buffer with Open-Drain Outputs | SSI |
| AC/ACT240 | Octal Buffer/Line Driver; 3-State; Inverting | MSI |
| AC/ACT241 | Octal Buffer/Line Driver; 3-State | MSI |
| AC/ACT244 | Octal Buffer/Line Driver; 3-State | MSI |
| AC/ACT540 | Octal Buffer/Line Driver; 3-State; Inverting | MSI |
| AC/ACT541 | Octal Buffer/Line Driver; 3-State | MSI |
| | **Flip-Flops** | |
| AC/ACT74 | Dual D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger | FF |
| AC/ACT109 | Dual $J\overline{K}$ Flip-Flop with Set and Reset; Positive-Edge Trigger | FF |
| AC/ACT112 | Dual JK Flip-Flop with Set and Reset; Negative-Edge Trigger | FF |
| AC/ACT174 | Hex D-Type Flip-Flop with Reset; Positive-Edge Trigger | MSI |
| AC/ACT175 | Quad D-Type Flip-Flop with Reset; Positive-Edge Trigger | MSI |
| AC/ACT273 | Octal D-Type Flip-Flop with Reset; Positive-Edge Trigger | MSI |
| AC/ACT374 | Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State | MSI |
| AC/ACT534 | Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting | MSI |
| AC/ACT564 | Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting | MSI |
| AC/ACT574 | Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State | MSI |
| | **Shift/FIFO Buffer/Multiport Registers** | |
| AC/ACT164 | 8-Bit Serial-In/Parallel-Out Shift Register | MSI |
| AC/ACT299 | 8-Bit Universal Shift/Storage Register; 3-State; Asynchronous Reset | MSI |
| AC/ACT323 | 8-Bit Universal Shift/Storage Register; 3-State; Synchronous Reset | MSI |
| AC/ACT7201 | 512 x 9-Bit Parallel FIFO | MSI |
| AC/ACT7202 | 1024 x 9-Bit Parallel FIFO | MSI |
| | **Arithmetic Circuits** | |
| AC/ACT280 | 9-Bit Odd/Even Parity Generator/Checker | MSI |
| AC/ACT283 | 4-Bit Full Adder with Fast Carry | MSI |
| | **Counters** | |
| AC/ACT161 | Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset | MSI |
| AC/ACT163 | Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset | MSI |
| AC/ACT191 | Presettable Synchronous 4-Bit Binary Up/Down Counter | MSI |
| AC/ACT193 | Presettable Synchronous 4-Bit Binary Up/Down Counter with Reset | MSI |
| AC/ACT7060 | 14-Stage Binary Ripple Counter with Oscillator | MSI |
| | **Digital Multiplexers/Demultiplexers** | |
| AC/ACT138 | 3-to-8-Line Decoder/Demultiplexer; Inverting | MSI |
| AC/ACT139 | Dual 2-to-4-Line Decoder/Demultiplexer | MSI |
| AC/ACT151 | 8-Input Multiplexer | MSI |
| AC/ACT153 | Dual 4-Input Multiplexer | MSI |
| AC/ACT157 | Quad 2-Input Multiplexer | MSI |
| AC/ACT158 | Quad 2-Input Multiplexer; Inverting | MSI |
| AC/ACT238 | 3-to-8-Line Decoder/Demultiplexer | MSI |
| AC/ACT251 | 8-Input Multiplexer; 3-State | MSI |
| AC/ACT253 | Dual 4-Input Multiplexer; 3-State | MSI |
| AC/ACT257 | Quad 2-Input Multiplexer; 3-State; Non-Inverting Outputs | MSI |
| AC/ACT258 | Quad 2-Input Multiplexer; 3-State; Inverting Outputs | MSI |
| | **Decoders/Encoders** | |
| AC/ACT138 | 3-to-8-Line Decoder/Demultiplexer; Inverting | MSI |
| AC/ACT139 | Dual 2-to-4-Line Decoder/Demultiplexer | MSI |
| AC/ACT238 | 3-to-8-Line Decoder/Demultiplexer | MSI |

*GE/RCA Products*



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# Product Selection Guide

| Type | Function/Description | Classification |
|---|---|---|
| **CD74** | **Bus Transceivers** | |
| AC/ACT245 | Octal-Bus Transceiver; 3-State | MSI |
| AC/ACT623 | Octal-Bus Transceiver; 3-State | MSI |
| AC/ACT646 | Octal-Bus Transceiver/Register; 3-State | MSI |
| AC/ACT647 | Octal-Bus Transceiver/Register with Open Drain | MSI |
| AC/ACT648 | Octal-Bus Transceiver/Register; 3-State; Inverting | MSI |
| AC/ACT649 | Octal-Bus Transceiver/Register with Open Drain; Inverting | MSI |
| AC/ACT651 | Octal-Bus Transceiver/Register; 3-State; Inverting | MSI |
| AC/ACT652 | Octal-Bus Transceiver/Register; 3-State | MSI |
| AC/ACT653 | Octal-Bus Transceiver/Register; Open-Drain (A Side); 3-State (B Side); Inverting | MSI |
| AC/ACT654 | Octal-Bus Transceiver/Register; Open-Drain (A Side 3-State (B-Side) | MSI |
| AC/ACT7623 | Octal-Bus Transceiver; 3-State (B Side); Open-Drain (A Side) | MSI |
| | **Schmitt Trigger** | |
| AC/ACT14 | Hex Inverting Schmitt Trigger | SSI |
| | **Latches** | |
| AC/ACT373 | Octal Transparent Latch; 3-State | MSI |
| AC/ACT533 | Octal Transparent Latch; 3-State; Inverting | MSI |
| AC/ACT563 | Octal Transparent Latch; 3-State; Inverting | MSI |
| AC/ACT573 | Octal Transparent Latch; 3-State | MSI |

# High-Speed CMOS Digital Integrated Circuits

The RCA series of high-speed CMOS logic integrated circuits include an extensive line of products that are pin compatible with many existing bipolar 54/74 LSTTL and CMOS 4000 series of digital logic types.

These IC's provide high-speed CMOS replacements for the most popular LSTTL devices in existing designs and also offer low-power all-CMOS designs for new digital systems.

The high-speed CMOS product line consists of CD54/74HC-series types, which feature CMOS input voltage level compatiblity and CD54/74HCT-series types, which are input voltage level compatible with LSTTL devices.

The high-speed CMOS line also includes a limited number of single-stage, unbuffered inverter types (CD54/74HCU-series) for added versatility in oscillator and amplifier applications.

This comprehensive line of high speed digital integrated circuits meet, in all respects, the industry-standard specifications established by JEDEC.

**Variety of logic functions provided by QMOS products.**

| Device Function | Number of Types |
|---|---|
| Inverters/Buffers/Bus Drivers | 14 |
| Flip-Flop/Latches | 28 |
| Bus Transceivers | 22 |
| Registers | 10 |
| Counters | 10 |
| Decoders/Encoders | 6 |
| Digital Multiplexers/ Demultiplexers | 22 |
| Schmitt Triggers | 2 |
| Arithmetic Circuits | 4 |
| Gates | 14 |

**Family Features**

- *Functionally and pin compatible with industry 54 and 74 LSTTL-series and CD4000B-series types.*
- *CMOS outputs for maximum noise margins.*
- *Fan-out (over temperature):*
  *Standard Outputs - 10 LSTTL loads*
  *Bus-Driver Outputs - 15 LSTTL loads*
- *Wide operating temperature range:*
  *CD74HC/HCT/HCU: -40 to +85°C*
  *CD54HC/HCT/HCU: -55 to +125°C*
- *Balanced propagation and transition times.*
- *Significant power reduction compared to LSTTL logic.*
- *Alternate source - Philips/Signetics*

NOTE: Each function is available in both an HCT and HC version.

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltage referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR $-0.5 V < V_O V_{CC} + 0.5$ V):
STANDARD OUTPUT ..... ±25 mA
BUS DRIVER OUTPUT ..... ±35 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$):
STANDARD OUTPUT ..... ±50 mA
BUS DRIVER OUTPUT ..... ±70 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +100°C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE F) ..... Derate linearly at 8 mW/°C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +150°C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

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# High-Speed CMOS Digital Integrated Circuits

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| Type | Function/Description | Classification | No. of Pins |
|---|---|---|---|
| | **NAND/NOR GATES** | | |
| HC/HCT00 | Quad 2-Input NAND Gate | SSI | 14 |
| HC/HCT02 | Quad 2-Input NOR Gate | SSI | 14 |
| HC/HCT03 | Quad 2-Input NAND Gate with Open Drain | SSI | 14 |
| HC/HCT10 | Triple 3-Input NAND Gate | SSI | 14 |
| HC/HCT20 | Dual 4-Input NAND Gate | SSI | 14 |
| HC/HCT27 | Triple 3-Input NOR Gate | SSI | 14 |
| HC/HCT30 | 8-Input NAND Gate | SSI | 14 |
| HC/HCT4002 | Dual 4-Input NOR Gate | SSI | 14 |
| | **AND/OR/EXCLUSIVE-OR Gates** | | |
| HC/HCT08 | Quad 2-Input AND Gate | SSI | 14 |
| HC/HCT11 | Triple 3-Input AND Gate | SSI | 14 |
| HC/HCT21 | Dual 4-Input AND Gate | SSI | 14 |
| HC/HCT32 | Quad 2-Input OR Gate | SSI | 14 |
| HC/HCT86 | Quad 2-Input EXCLUSIVE-OR Gate | SSI | 14 |
| HC/HCT4075 | Triple 3-Input OR Gate | SSI | 14 |
| HC7266 | Quad Exclusive NOR | SSI | 14 |
| | **Inverters/Buffers/Bus Drivers** | | |
| HC/HCT04 | Hex Inverter | SSI | 14 |
| HCU04 | Hex Inverter (Unbuffered) | SSI | 14 |
| HC/HCT125 | Quad 3-State Buffer | MSI | 14 |
| HC/HCT126 | Quad 3-State Buffer | MSI | 14 |
| HC/HCT240* | Octal Buffer/Line Driver; 3-State; Inverting | MSI | 20 |
| HC/HCT241* | Octal Buffer/Line Driver; 3-State | MSI | 20 |
| HC/HCT244* | Octal Buffer/Line Driver; 3-State | MSI | 20 |
| HC/HCT365* | Hex Buffer/Line Driver; 3-State | MSI | 16 |
| HC/HCT366* | Hex Buffer/Line Driver; 3-State Inverting | MSI | 16 |
| HC/HCT367* | Hex Buffer/Line Driver; 3-State | MSI | 16 |
| HC/HCT368* | Hex Buffer/Line Driver; 3-State; Inverting | MSI | 16 |
| HC/HCT540* | Octal Buffer/Line Driver; 3-State; Inverting | MSI | 20 |
| HC/HCT541* | Octal Buffer/Line Driver; 3-State | MSI | 20 |
| HC4049 | Hex Inverting HIGH-to-LOW Level Shifter | SSI | 16 |
| HC4050 | Hex HIGH-to-LOW Level Shifter | SSI | 16 |
| | **Flip-Flops/Latches/Registers** | | |
| HC/HCT73 | Dual JK FLip-Flop with Reset; Negative-Edge Trigger | FF | 14 |
| HC/HCT74 | Dual D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger | FF | 14 |
| HC/HCT107 | Dual JK Flip-Flop with Reset; Negative-Edge Trigger | FF | 14 |
| HC/HCT109 | Dual JK Flip-Flop with Set and Reset; Positive-Edge Trigger | FF | 16 |
| HC/HCT112 | Dual JK Flip-Flop with Set and Reset; Positive-Edge Trigger; 3-State | FF | 16 |
| HC/HCT173* | Quad D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger; 3-State | MSI | 16 |
| HC/HCT174 | Hex D-Type Flip-Flop with Reset; Positive-Edge Trigger | MSI | 16 |
| HC/HCT175 | Quad D-Type Flip-Flop with Reset; Positive-Edge Trigger | MSI | 16 |
| HC/HCT273 | Octal D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger | MSI | 20 |
| HC/HCT374* | Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State | MSI | 20 |
| HC/HCT377 | Octal D-Type Flip-Flop with Data Enable; Positive-Edge Trigger | MSI | 20 |
| HC/HCT534* | Octal D-Type Flip-Flop; Positive Edge Trigger; 3-State; Inverting | MSI | 20 |
| HC/HCT564* | Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting | MSI | 20 |
| HC/HCT574* | Octal D-Type Flip-Flop; Positive-Edge; 3-State | MSI | 20 |
| | **Shift/FIFO Buffer/Multiport Registers** | | |
| HC/HCT164 | 8-Bit Serial-In/Parallel-Out Shift Register | MSI | 14 |
| HC/HCT165 | 8-Bit Parallel-In/Serial-Out Shift Register | MSI | 16 |
| HC/HCT166 | 8-Bit Parallel/Serial-In Serial-Out Shift Register | MSI | 16 |
| HC/HCT194 | 4-Bit Bidirectional Universal Shift Register | MSI | 16 |
| HC/HCT195 | 4-Bit Parallel Access Shift Register | MSI | 16 |
| HC/HCT299* | 8-Bit Universal Shift Register; 3-State | MSI | 20 |
| HC/HCT597 | 8-Bit Shift Register with Input Latch | MSI | 16 |
| HC/HCT670 | 4 x 4 Register File; 3-State | MSI | 16 |
| HC/HCT4015 | Dual 4-Bit Serial-In/Parallel-Out Shift Register | MSI | 16 |
| HC/HCT4094 | 8-Stage Shift-and-Store Bus Register | MSI | 16 |
| HC/HCT40104* | 4-Bit Bidirectional Universal Shift Register; 3-State | MSI | 16 |
| HC/HCT40105 | 4 Bits x 16 Words FIFO Register | MSI | 16 |
| HC/HCT7030 | 4 Bits x 64 Words FIFO Register; 3-State | MSI | 28 |
| | **Analog Switches** | | |
| HC/HCT4016 | Quad Bilateral Switch | SSI | 14 |
| HC/HCT4066 | Quad Bilateral Switch | SSI | 14 |
| HC/HCT4316 | Quad Analog Switch | MSI | 16 |
| | **Bus Transceivers** | | |
| HC/HCT242* | Quad Bus Transceiver; 3-State; Inverting | MSI | 14 |
| HC/HCT243* | Quad Bus Transceiver; 3-State | MSI | 14 |
| HC/HCT245* | Octal Bus Transceiver; 3-State | MSI | 20 |
| HC/HCT640* | Octal Bus Transceiver; 3-State Inverting | MSI | 20 |
| HC/HCT643* | Octal Bus Transceiver; 3-State True/Inverting | MSI | 20 |
| HC/HCT646* | Octal Bus Transceiver; 3-State | MSI | 24 |
| HC/HCT648* | Octal Bus Transceiver; 3-State; Inverting | MSI | 24 |
| HC/HCT7038 | 9-Bit Bus Transceiver with Latch | MSI | 24 |
| | **Schmitt Triggers** | | |
| HC/HCT14 | Hex Inverting Schmitt Trigger | SSI | 14 |
| HC/HCT132 | Quad 2-Input NAND Schmitt Trigger | SSI | 14 |

*Types with a bus driver output stage.

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# High-Speed CMOS Digital Integrated Circuits

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| Type | Function/Description | Classification | No. of Pins |
|---|---|---|---|
| | **Arithmetic Circuits** | | |
| HC/HCT85 | 4-Bit Magnitude Comparator | MSI | 16 |
| HC/HCT181 | ALU | MSI | 24 |
| HC/HCT182 | Carry Generator | MSI | 16 |
| HC/HCT280 | 9-Bit Odd/Even Parity Generator/Checker | MSI | 14 |
| HC/HCT283 | 4-Bit Full Adder With Fast Carry | MSI | 16 |
| HC/HCT583 | Adder | MSI | 16 |
| HC/HCT688 | 8-Bit Magnitude Comparator | MSI | 20 |
| | **Counters** | | |
| HC/HCT93 | 4-Bit Binary Ripple Counter | MSI | 14 |
| HC/HCT160 | Presettable Synchronous BCD Decade Counter; Asynchronous Reset | MSI | 16 |
| HC/HCT161 | Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset | MSI | 16 |
| HC/HCT162 | Presettable Synchronous BCD Decade Counter, Synchronous Reset | MSI | 16 |
| HC/HCT163 | Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset | MSI | 16 |
| HC/HCT190 | Presettable Synchronous BCD Decade Up/Down Counter | MSI | 16 |
| HC/HCT191 | Presettable Synchronous 4-Bit Binary Up/Down Counter | MSI | 16 |
| HC/HCT192 | Presettable Synchronous BCD Decade Up/Down Counter | MSI | 16 |
| HC/HCT193 | Presettable Synchronous 4-Bit Binary Up/Down Counter | MSI | 16 |
| HC/HCT390 | Dual Decade Ripple Counter | MSI | 16 |
| HC/HCT393 | Dual 4-Bit Binary Ripple Counter | MSI | 14 |
| HC/HCT4017 | Johnson Decade Counter with 10 Decoded Outputs | MSI | 16 |
| HC/HCT4020 | 14-Stage Binary Ripple Counter | MSI | 16 |
| HC/HCT4024 | 7-Stage Binary Ripple Counter | MSI | 16 |
| HC/HCT4040 | 12-Stage Binary Ripple Counter | MSI | 16 |
| HC/HCT4059 | Programmable Divide by "N" Counter | MSI | 24 |
| HC/HCT4060 | 14-Stage Binary Ripple Counter with Oscillator | MSI | 16 |
| HC/HCT4510 | Presettable Synchronous 4-Bit BCD Up/Down Counter | MSI | 16 |
| HC/HCT4516 | Presettable Synchronous 4-Bit Binary Up/Down Counter | MSI | 16 |
| HC/HCT4518 | Dual Synchronous BCD Counter | MSI | 16 |
| HC/HCT4520 | Dual 4-Bit Synchronous Binary Counter | MSI | 16 |
| HC/HCT40102 | 8-Bit Synchronous BCD Down Counter | MSI | 16 |
| HC/HCT40103 | 8-Bit Binary Down Counter | MSI | 16 |
| | **Analog and Digital Multiplexers/Demultiplexers** | | |
| HC/HCT151 | 8-Input Multiplexer | MSI | 16 |
| HC/HCT153 | Dual 4-Input Multiplexer | MSI | 16 |
| HC/HCT157 | Quad 2-Input Multiplexer | MSI | 16 |
| HC/HCT158 | Quad 2-Input Multiplexer; Inverting | MSI | 16 |
| HC/HCT251 | 8-Input Multiplexer; 3-State | MSI | 16 |
| HC/HCT253 | Dual 4-Input Multiplexer; 3-State | MSI | 16 |
| HC/HCT257* | Quad 2-Input Multiplexer; 3-State | MSI | 16 |
| HC/HCT258 | Quad 2-Line to 4-Line Data Selector | MSI | 16 |
| HC/HCT354* | 8-Input Multiplexer/Register; 3-State | MSI | 20 |
| HC/HCT356 | 8-Input Multiplexer/Register; 3-State | MSI | 20 |
| HC/HCT4051 | 8-Channel Analog Multiplexer/Demultiplexer | MSI | 16 |
| HC/HCT4052 | Dual 4-Channel Analog Multiplexer/Demultiplexer | MSI | 16 |
| HC/HCT4053 | Triple 2-Channel Analog Multiplexer/Demultiplexer | MSI | 16 |
| HC/HCT4067 | 16-Channel Analog Multiplexer/Demultiplexer | MSI | 18 |
| HC/HCT4351 | Analog Multiplexer with Latch | MSI | 20 |
| HC/HCT4352 | Analog Multiplexer with Latch | MSI | 20 |
| HC/HCT4353 | Analog Multiplexer with Latch | MSI | 20 |
| | **Decoders/Encoders** | | |
| HC/HCT42 | BCD to Decimal Decoder (1-of-10) | MSI | 16 |
| HC/HCT137 | 3-to-8 Line Decoder with Latch | MSI | 16 |
| HC/HCT138 | 3-to-8 Line Decoder/Demultiplexer; Inverting | MSI | 16 |
| HC/HCT139 | Dual 2-to-4 Line Decoder/Demultiplexer | MSI | 16 |
| HC/HCT147 | 10-to-4-Line Priority Encoder | MSI | 16 |
| HC/HCT154 | 4-to-16-Line Decoder/Demultiplexer | MSI | 24 |
| HC/HCT237 | 3-to-8-Line Decoder | MSI | 16 |
| HC/HCT238 | 3-to-8-Line Decoder/Demultiplexer | MSI | 16 |
| HC/HCT4511 | BCD-to-7-Segment Latch/Decoder/Driver | MSI | 16 |
| HC/HCT4514 | 4-to-16-Line Decoder/Demultiplexer with Input Latches | MSI | 24 |
| HC/HCT4515 | 4-to-16-Line Decoder/Demultiplexer with Input Latches | MSI | 24 |
| HC/HCT4543 | BCD-to-7-Segment Latch/Decoder/Driver for LCDs | MSI | 16 |
| | **Latches** | | |
| HC/HCT75 | Dual 2-Bit Bistable Transparent Latch | FF | 16 |
| HC/HCT259 | 8-Bit Addressable Latch | MSI | 16 |
| HC/HCT373* | Octal Transparent Latch; 3-State | MSI | 20 |
| HC/CHT533* | Octal Transparent Latch; 3-State; Inverting | MSI | 20 |
| HC/HCT563* | Octal Transparent Latch; 3-State; Inverting | MSI | 20 |
| HC/HCT573* | Octal Transparent Latch; 3-State | MSI | 20 |
| | **One-Shot Multivibrators** | | |
| HC/HCT123 | Dual Retriggerable Monostable Multivibrator with Reset | MSI | 16 |
| HC/HCT221 | Dual Monostable Multivibrator with Reset | MSI | 16 |
| HC/HCT423 | Dual Retriggerable Monostable Multivibrator with Reset | MSI | 16 |
| HC/HCT4538 | Dual Retriggerable Precision Monostable Multivibrator | MSI | 16 |
| | **Phase-Locked Loops (PLL)** | | |
| HC/HCT297 | Digital Phase-Locked Loop Filter | MSI | 16 |
| HC/HCT4046A | Phase-Locked Loop with VCO | MSI | 16 |
| HC/HCT7046A | Phase-Locked Loop with In-Lock Detection | MSI | 16 |

*Types with a bus driver output stage.

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# CMOS Digital Logic Integrated Circuits (CD4000-Series)

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The RCA CMOS product line covers a broad range of SSI, MSI, and LSI functions from simple gates to complex counters, registers, and arithmetic circuits, and includes both standard circuit types for commercial and industrial applications and high-reliability slash (/) series types for aerospace, military, and critical industrial applications.

Following its tradition of leadership in CMOS, RCA offers a comprehensive line of high-voltage ("B"-series) CMOS digital integrated circuits which meet, in all respects, the industry standard specifications established by JEDEC.

## CMOS Gates

| Function | Type No. | No. of Pins |
|---|---|---|
| **Gates** | | |
| **NOR/NAND** | | |
| Dual 4-input NOR | CD4002B | 14 |
| | CD4002UB | 14 |
| Dual 4-input NAND | CD4012B | 14 |
| | CD4012UB | 14 |
| Triple 3-input NOR | CD4025B | 14 |
| | CD4025UB | 14 |
| Triple 3-input NAND | CD4023B | 14 |
| | CD4023UB | 14 |
| Quad 2-input NOR | CD4001B | 14 |
| | CD4001UB | 14 |
| | CD4001A | 14 |
| Quad 2-input NAND | CD4011B | 14 |
| | CD4011UB | 14 |
| | CD4011A | 14 |
| 8-input NOR/OR | CD4078B | 14 |
| 8-input NAND/AND | CD4068B | 14 |
| Dual 3-input NOR plus inverter | CD4000B | 14 |
| | CD4000UB | 14 |
| Dual 2-input NAND buffer/driver | CD40107B | 8, 14 |
| **OR/AND** | | |
| Dual 4-input OR | CD4072B | 14 |
| Dual 4-input AND | CD4082B | 14 |
| Triple 3-input OR | CD4075B | 14 |
| Triple 3-input AND | CD4073B | 14 |
| Quad 2-input OR | CD4071B | 14 |
| Quad 2-input AND | CD4081B | 14 |
| **Buffers and Inverters** | | |
| Dual complementary pair plus inverter | CD4007UB | 14 |
| | CD4007A | 14 |
| Hex inverter | CD4069UB | 14 |
| Hex inverter/buffer (3-state) | CD4502B | 16 |
| Hex inverter (3-state non-inverting) | CD4503B | 16 |
| Hex buffer/converter (inverting) | CD4009UB | 16 |
| | CD4009A | 16 |
| Hex buffer/converter (inverting) | CD4049UB | 16 |
| | CD4049A | 16 |
| Hex buffer/converter (non-inverting) | CD4010B | 16 |
| | CD4010A | 16 |
| Hex buffer/converter (non-inverting) | CD4050B | 16 |
| Quad true/complement buffer | CD4041UB | 14 |
| Dual 2-input NAND buffer/driver | CD40107B | 8, 14 |
| **Multi-function/AOI** | | |
| Quad exclusive-OR | CD4030B | 14 |

| Function | Type No. | No. of Pins |
|---|---|---|
| **Multi-function/AOI (cont'd.)** | | |
| Quad exclusive-OR | CD4070B | 14 |
| Quad exclusive-NOR | CD4077B | 14 |
| Quad AND/OR Select | CD4019B | 16 |
| Dual 2-wide, 2-input AND/OR invert (AOI) | CD4085B | 14 |
| Expandable 4-wide, 2-input AND/OR invert (AOI) | CD4086B | 14 |
| Multifunctional expandable 8-input (3-state output) | CD4048B | 16 |
| **Decoders/Encoders** | | |
| BCD-to-decimal decoder | CD4028B | 16 |
| 8-input priority encoder | CD4532B | 16 |
| 10-line to 4-line BCD priority encoder | CD40147B | 16 |
| 4-bit latch/4-to-16 line decoder (outputs high) | CD4514B | 24 |
| 4-bit latch/4-to-16 line decoder (outputs low) | CD4515B | 24 |
| Dual 1-of-4 decoder/demultiplexer (outputs high) | CD4555B | 16 |
| Dual 1-of-4 decoder/demultiplexer (outputs low) | CD4556B | 16 |
| **Schmitt Trigger** | | |
| Quad 2-input NAND | CD4093B | 14 |
| Hex | CD40106B | 14 |
| **Interface** | | |
| Quad low-to-high voltage | CD40109B | 16 |
| Hex high-to-low voltage (inverting) | CD4009UB | 16 |
| | CD4009A | 16 |
| | CD4049UB | 16 |
| | CD4049A | 16 |
| Hex high-to-low voltage (non-inverting) | CD4010B | 16 |
| | CD4010A | 16 |
| | CD4050B | 16 |
| Dual 2-input NAND buffer/driver | CD40107B | 8, 14 |
| 8-bit bidirectional CMOS-to-TTL level converter | CD40115* | 22 |
| 8-bit bidirectional CMOS-to-TTL level converter | CD40116* | 22 |
| Programmable dual 4-bit terminator | CD40117B* | 14 |

*Indicates types designed for special applications.





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# CMOS Digital Logic Integrated Circuits (CD4000-Series)

GE Solid State

## CMOS Multivibrators

- *CD4047 for monostable (one-shot) or astable (free-running) operation*
- *CD4098 for retriggerable/resettable one-shot operation*

Flip-flops

- *Clock rates from 12 to 16 MHz (typical)*
- *CD4013, CD4027 with set/reset capability*
- *CD4095, CD4096 with gated input*
- *CD40174 with 6 identical "D"-type units having independent data inputs*
- *CD4076 with 3-stage outputs*

Latches

- *Propagation delay times from 50 to 75 ns (typ.)*
- *CD4508 has 2 independent 4-bit latches, each with an individual master reset*
- *CD4099 is suitable for a wide variety of functions*

| Function | Type No. | No. of Pins |
|---|---|---|
| **Multivibrators** | | |
| Monostable/astable | CD4047B | 14 |
| | CD4047A | 14 |
| Dual monostable | CD4098B | 16 |
| Dual precision monostable | CD4538B | 16 |
| **Flip-Flops** | | |
| Dual "D" with set/reset capability | CD4013B | 14 |
| | CD4013A | 14 |
| Dual "J-K" with set/reset capability | CD4027B | 16 |
| | CD4027A | 16 |
| Gated "J-K" (non-inverting) | CD4095B | 14 |
| Gated "J-K" (inverting and non-inverting) | CD4096B | 14 |
| Hex "D" | CD40174B | 16 |
| 4-bit "D" with 3-state outputs | CD4076B | 14 |
| Quad "D" | CD40175B | 16 |
| **Latches** | | |
| Quad clocked "D" | CD4042B | 16 |
| Quad NOR R/S (3-state outputs) | CD4043B | 16 |
| Quad NAND R/S (3-state outputs) | CD4044B | 16 |
| Dual 4-bit | CD4508B | 24 |
| 8-bit addressable | CD4099B | 16 |
| | CD4724B | 16 |

## CMOS Registers

Shift registers

- *Clock rates from 5 to 16 MHz (typical)*
- *Bidirectional types, types with recirculating capability, LIFO or FIFO capability, standard TTL drive capability*

Storage Registers

- *CD4099 serial input/parallel output type can perform a variety of functions*
- *CD4076 is a "D" type flip-flop with 3-state outputs*

FIFO Buffer Register

- *3-state outputs*
- *Expandable in either direction*
- *Independent asynchronous inputs and outputs*

| Function | Type No. | No. of Pins |
|---|---|---|
| **Registers** | | |
| **Shift Registers-Static** | | |
| Dual 4-stage with serial input/parallel output | CD4015B | 16 |
| 18-stage | CD4006B | 14 |
| 64-stage | CD4031B | 16 |
| Dual 64-bit | CD4517B | 16 |
| 8-stage with synchronous parallel or serial input/serial output | CD4014B | 16 |
| 8-stage with asynchronous parallel input or synchronous serial input/serial output | CD4021B | 16 |
| 4-stage parallel-in/parallel-out with J-K input and true/complement output | CD4035B | 16 |
| 4-bit universal bidirectional with 3-stage outputs | CD40104B | 16 |
| 4-bit universal bidirectional with asynchronous master reset | CD40194B | 16 |
| 6-stage bidirectional parallel or serial input/parallel output | CD4034B | 24 |
| 32-bit left/right | CD40100B | 16 |
| 8-stage shift-and-store bus | CD4094B | 16 |
| **Shift Registers-Dynamic** | | |
| 200-stage | CD4062A | 12 |
| **Storage Registers** | | |
| 8-bit addressable latch | CD4099B | 16 |
| | CD4724B | 16 |
| 4-bit "D"-type with 3-state outputs | CD4076B | 16 |
| 4 X 4 Multiport | CD40108B | 24 |
| 4 X 4 Multiport | CD40208B | 24 |
| **FIFO Buffer Registers** | | |
| 4 bit x 16 word | CD40105B | 16 |

## CMOS Counters

- *Max. input pulse frequencies from 3.6 to 10 MHz*
- *Fully static operation*
- *Programmable types*
  *CD40160, CD40161 with asynchronous clear input*
- *CD40162, CD40163 with synchronous clear input*
- *CD4059 synchronous programmable divide-by-"N"*
  *CD4018 fixed or programmable*

| Function | Type No. | No. of Pins |
|---|---|---|
| **Counters** | | |
| **Binary Ripple** | | |
| 7-stage | CD4024B | 14 |
| | CD4024A | 14 |
| 12-stage | CD4040B | 16 |
| 14-stage | CD4020B | 16 |
| | CD4020A | 16 |
| 14-stage counter/divider and oscillator | CD4060B | 16 |
| | CD4060A | 16 |
| **Timers** | | |
| 21-stage | CD4045B | 14 |
| Programmable | CD4536B | 16 |
| | CD4541B | 14 |

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# CMOS Digital Logic Integrated Circuits (CD4000-Series)

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| Function | Type No. | No. of Pins |
|---|---|---|
| **Counters (cont'd.)** | | |
| **Synchronous** | | |
| Decade counter/divider plus 10 decoded decimal outputs | CD4017B | 16 |
| | CD4017A | 16 |
| Divide-by-8 counter/divider with 8 decimal outputs | CD4022B | 16 |
| Presettable divide-by-"N" counter, fixed or programmable | CD4018B | 16 |
| | CD4018A | |
| Programmable-divide-by-"N" counter | CD4059A | 24 |
| Presettable up/down counter, binary or BCD-decade | CD4029B | 16 |
| | CD4029A | 16 |
| Presettable 4-bit BCD up/down counter | CD4510B | 16 |
| Presettable 4-bit binary up/down counter | CD4516B | 16 |
| Presettable 2-decade BCD down counter | CD40102B | 16 |
| Presettable 8-bit binary down counter | CD40103B | 16 |
| Presettable 4-bit BCD up/down counter | CD40192B | 16 |
| Presettable 4-bit binary up/down counter | CD40193B | 16 |
| Dual BCD up counter | CD4518B | 16 |
| Dual binary up counter | CD4520B | 16 |
| Decade counter/asynchronous clear | CD40160B | 16 |
| Binary counter/asynchronous clear | CD40161B | 16 |
| Decade counter/synchronous clear | CD40162B | 16 |
| Binary counter/synchronous clear | CD40163B | 16 |

## CMOS Display Drivers

- *CD4026B, CD4033B have counter and 7-segment decoder in one package; easily interfaced with 7-segment display types*
- *CD40110B has separate clock up and clock down lines; allows one line to be clocked regardless of the state of the other line*
- *CD4054B, CD4055B, CD4056B provide level-shifting functions on chip; have equivalent ac output drive, for liquid-crystal displays, no external capacitor required*
- *CD4511B has high output-sourcing capability, up to 25 mA; also lamp-test and blanking capability.*

| Function | Type No. | No. of Pins |
|---|---|---|
| **Display Drivers With Counter** | | |
| Decade counter/divider with 7-segment display outputs and display enable | CD4026B | 16 |
| Decade counter/divider with 7-segment display outputs and ripple blanking | CD4033B | 16 |
| Up/Down Counter-Latch-Decoder-Driver | CD40110B | 16 |
| **For Liquid-Crystal-Display Drive** | | |
| 4-segment display driver | CD4054B | 16 |
| BCD-to-7-segment decoder/driver with "display-frequency" output | CD4055B | 16 |
| BCD-to-7-segment decoder/driver with strobed-latch function | CD4056B | 16 |
| | CD4543B | 16 |

| Function | Type No. | No. of Pins |
|---|---|---|
| **For Liquid-Crystal-Display Drive (cont'd.)** | | |
| 4-digit decoder/driver with hexidecimal display | CD7211 | 40 |
| 4-digit decoder/driver with decimal display | CD7211A | 40 |
| 4-digit decoder/driver with hexidecimal display | CD7211M | 40 |
| 4-digit decoder/driver with decimal display | CD7211AM | 40 |
| **For Light-Emitting-Diode Drive** | | |
| BCD-to-7-segment latch decoder/driver | CD4511B | 16 |

## CMOS Multiplexers

- *CD4051B, CD4052B, CD4053B, CD4067B, CD4097B have very low quiescent dissipation (0.2 μW typ. at $V_{DD}$ =10V) under all digital control input and supply conditions*
- *CD4051B, CD4052B, CD4053B have a wide range of digital and analog signal levels: 3 to 20V digital, 20 Vp-p analog*
- *CD4067B, CD4097B have binary address decoding on chip*
- *CD4555B, CD4556B have 2 select inputs (A and B), an Enable input (E), and 4 mutually exclusive outputs for each decoder*
- *CD40257B has 3-state outputs which can interface directly with and drive data lines of bus-oriented systems*

| Function | Type No. | No. of Pins |
|---|---|---|
| **Multiplexers/Demultiplexers** | | |
| **Analog** | | |
| Triple 2-channel | CD4053B | 16 |
| Differential 4-channel | CD4052B | 16 |
| Single 8-channel | CD4051B | 16 |
| Differential 8-channel | CD4097B | 24 |
| Single 16-channel | CD4067B | 24 |
| Quad bilateral switch | CD4016B | 14 |
| | CD4016A | 14 |
| Quad bilateral switch | CD4066B | 14 |
| | CD4066A | 14 |
| **Digital (Data Selectors)** | | |
| Quad AND/OR select | CD4019B | 16 |
| Dual 1-of-4 decoder/demultiplexer (outputs high) | CD4555B | 16 |
| Dual 1-of-4 decoder/demultiplexer (outputs low) | CD4556B | 16 |
| Quad 2-line-to-1-line | CD40257B | 16 |
| 8-channel | CD4512B | 16 |

## CMOS Phase-Locked Loop

- *Very low power consumption: 70μW typical at $V_{DD}$=10V*
- *Max operating-frequency range up to 1.2 MHz typical at $V_{DD}$ = 10V*
- *Low frequency drift: +0.06%/°C*

| Function | Type No. | No. of Pins |
|---|---|---|
| **Phase-Locked Loop** | | |
| Micropower | CD4046B | 16 |
| | CD4046A | 16 |

GE/RCA Products

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# CMOS Digital Logic Integrated Circuits (CD4000-Series)

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## CMOS Bilateral Switches

- *CD4066B is pin-compatible with CD4016B but exhibits a much lower ON-resistance*
- *CD4066B and CD4016B $R_{ON}$ are matched to within 5 ohms at $V_{DD} = 15V$*
- *CD4016B is recommended for sample-and-hold use*

| Function | Type No. | No. of Pins |
|---|---|---|
| **Quad Bilateral Switches** | | |
| For transmission or multiplexing of analog or digital signals | CD4016B | 14 |
| | CD4016A | 14 |
| | CD4066B | 14 |
| | CD4066A | 14 |

## CMOS Arithmetic Circuits

A wide selection of circuits to provide a variety of logic and arithmetic functions, comparison functions, error detection in computer and industrial control applications

- *Propagation delay times from 60 to 100 ns (typical)*
- *CD40181B generates 16 logic and 16 arithmetic functions*
- *CD4063B compares two 4-bit words in 250 ns typ at 10V; expansion to 8-, 12-,16-...4N bits by cascading units*
- *CD40182B generates high-speed carry across 4 adder or adder groups*
- *CD4032B, CD4038B invert inputs provide for complement of sum outputs*

| Function | Type No. | No. of Pins |
|---|---|---|
| **Arithmetic Circuits** | | |
| **Adders/Comparators** | | |
| 4-bit full adder with parallel carry out | CD4008B | 16 |
| Triple serial adder, positive logic | CD4032B | 16 |
| Triple serial adder, negative logic | CD4038B | 16 |
| 4-bit magnitude comparator | CD4063B | 16 |
| | CD4585B | 16 |
| Quad exclusive-OR gate | CD4030B | 14 |
| Quad exclusive-OR gate | CD4070B | 14 |
| Quad exclusive-NOR gate | CD4077B | 14 |
| **ALU/Rate Multipliers** | | |
| 4-bit arithmetic logic unit | CD40181B | 24 |
| BCD rate multiplier | CD4527B | 16 |
| Binary rate multiplier | CD4089B | 16 |
| Look-ahead-carry block | CD40182B | 16 |
| **Parity Generator/Checker** | | |
| 9-bit | CD40101B | 14 |
| **Multiport Register** | | |
| 4 X 4 | CD40108B | 24 |
| 4 X 4 | CD40208B | 24 |
| 8 X 1 | CD4034B | 24 |

# Telecommunication Circuits

| Type. No. | Description | Type Features | No. of Pins |
|---|---|---|---|
| **CMOS DTMF RECEIVERS** | | | |
| CD22202 | 5-volt Low-Power Receiver | • Central office quality — full feature | 18 |
| CD22203 | 5-volt Low Power Receiver | • Same as CD22202, but has Early Detect Output on Pin 6 | 18 |
| CD22204 | 5-volt Low-Power Subscriber Receiver | • Basic functions for subscriber equipment | 14 |
| | | **Family Features**<br>• Low-power CMOS: 50mW typ.<br>• Single low-tolerance (10%) 5-volt supply<br>• No front-end band splitting filters required<br>• Three-state outputs for microprocessor-based systems<br>• Output in either 4-bit hexadecimal code or binary coded 2 of 8<br>• Uses inexpensive 3.58 MHz crystal<br>• Synchronous handshake interface (CD22202, CD22203)<br>• Interchangeable with SSI types SSI 202, 203, and 204 | |

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| Type. No. | Description | Type Features | # of Pins |
|---|---|---|---|
| **CMOS DTMF GENERATOR** | | | |
| CD22859 | Dual-Tone Multifrequency Tone Generator | • Low-power CMOS operation<br>• Device power can either be regulated dc or telephone loop current<br>• Mute driver output on chip<br>• Uses inexpensive 3.58-MHz crystal<br>• Built-in pull ups on keyboard inputs | 16 |
| **CMOS MODEMS** | | | |
| CD22212 | Single-chip 1200 BPS Model | • Provides all functions needed to construct a standard full-duplex modem that meets Bell 212A/103 specifications<br>• CMOS low-power consumption (120mW typ)<br>• Full duplex operation at 0-300 and 1200 BPS<br>• FSK (300 BPS) or PSK (1200 BPS) encoding and decoding<br>• Single +12V supply operation<br>• DTMF tone generation<br>• Compatible with industry-type 8048, 80251 $\mu$P's<br>• Interchangeable with SIK212<br>• TTL and CMOS compatible inputs and outputs | 22, 28 |
| CD22223 | 1200 Baud FSK Modem | • For European and closed-system use<br>• Designed to meet CCITT V.23 signaling frequencies<br>• CMOS low power consumption (10mW typ)<br>• Single +5V supply operation<br>• Low error rate (0.005 at 8-dB SNR)<br>• On-chip oscillator (3.18 MHz crystal or external input)<br>• Built-in loop back fast<br>• Interchangeable with SSI 223 | 16 |
| **CMOS HDB3 Transcoder** | | | |
| CD22103A | High-Density Bipolar 3 Transcoder | • For 2.048/8.448 Mb/s transmission applications<br>• Low-power, high-speed SOS technology 40mW max at 10MHz<br>• HDB3/AMI coding/decoding with data rates from 50 Kb/s to Mb/s<br>• Code error detection<br>• Separate coding and decoding sections<br>• Internal loop test capability<br>• TTL compatible I/O<br>• Operates with a 5V+ 10% power supply<br>• Similar in function and pin compatible to type MJ1471 | 16 |
| **PCM Line Repeater** | | | |
| CD22301 | PCM Line Repeater | • For T1 1.544 Mb/s and T148 2.3 Mb/s carrier systems<br>• Operates from 5.1 volt supply (5% tolerance)<br>• Performs: signal equalization and amplification, auto-line build out (ALBO) threshold detection, clock extraction, pulse timing | 16 |





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| Type. No. | Description | Type Features | # of Pins |
|---|---|---|---|
| **CMOS PCM CODECS** | | | |
| CD22354 | Single-Chip, Full-Feature Type | • Provides AT&T $\mu$-law companding characteristics | 16 |
| CD22357 | Single-Chip, Full-Feature Type | • Provides CCITT A-law companding characteristics | 16 |
| | | **Family Features**<br>• low-power CMOS operation; 80mW typ. operating, 5mW typ. standby<br>• Power supply rejection ratio — 40dB<br>• Adjustable gain for transmit input<br>• Synchronous and asynchronous operation<br>• TTL or CMOS-compatible inputs<br>• Stable on-chip precision voltage reference<br>• Pin and function-compatible with National TP3054 and TP3057<br>• 5 volt operation | 18 |
| **CROSSPOINT SWITCHES — CMOS Types** | | | |
| CD22100 | 4x4x1 Array with Memory Control | • Strobe-type of data enabling<br>• Linearity (% distortion) 0.5%<br>• $\Delta$ON resistance (18 ohm typ.) | 16 |
| CD22101 | 4x4x2 Array with Memory Control | • Strobe-type of data enabling<br>• Linearity (% distortion) 0.25%<br>• $\Delta$ON resistance (8 ohm type.) | 24 |
| CD22102 | 4x4x2 Array with Memory Control | • Set-reset type of data enabling<br>• Linearity (% distortion) 0.25%<br>• $\Delta$ON resistance (8 ohm typ.)<br>**Family Features**<br>• Low power (CMOS operation)<br>• Low On resistance (75 ohm typ.)<br>• Matched switch characteristics<br>• Wide-supply-voltage operating range (8-18V)<br>• High linearity<br>• On-chip control latches<br>• Frequency response (10MHz typ.) | 24 |
| **CROSSPOINT SWITCHES — High-Speed CMOS Types** | | | |
| CD54/74 HC22106 | 8x8x1 Array with Memory Control | • Supply voltage operating range (2-10V)<br>• CMOS CD4000B series compatible control inputs ($I_{IL}$, $I_{IH}$, $\leq 1\mu A$ at $V_{OL}$, $V_{OH}$)<br>• High noise immunity ($N_{IL}+N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5,10V | 28 |
| CD54/74 HCT22106 | 8x8x1 Array with Memory Control | • Supply-voltage operating range (4.5 to 5.5V)<br>• Direct LSTTL compatible control/inputs $V_{IL}$ = 0.8V max., $V_{IL}$ = 25V min.)<br>**Family Features**<br>• 64 analog switches on an 8x8x1 array.<br>• Auto power-up reset with external capacitor<br>• On-chip line decoder and control latches | 28 |




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# 1800 CMOS Microprocessors and Microcomputers

GE Solid State

The CDP1800 Series Microprocessor and Microcomputer family comprises the CDP1802A, CDP1805A, and CDP1806A microprocessors and the CDP1804A microcomputer.

The RCA CDP1802A CMOS microprocessor is an 8-bit silicon-gate CMOS register-oriented central-processing unit (CPU) designed for use as a general-purpose computing or control element in a wide variety of commercial, industrial, and military applications.

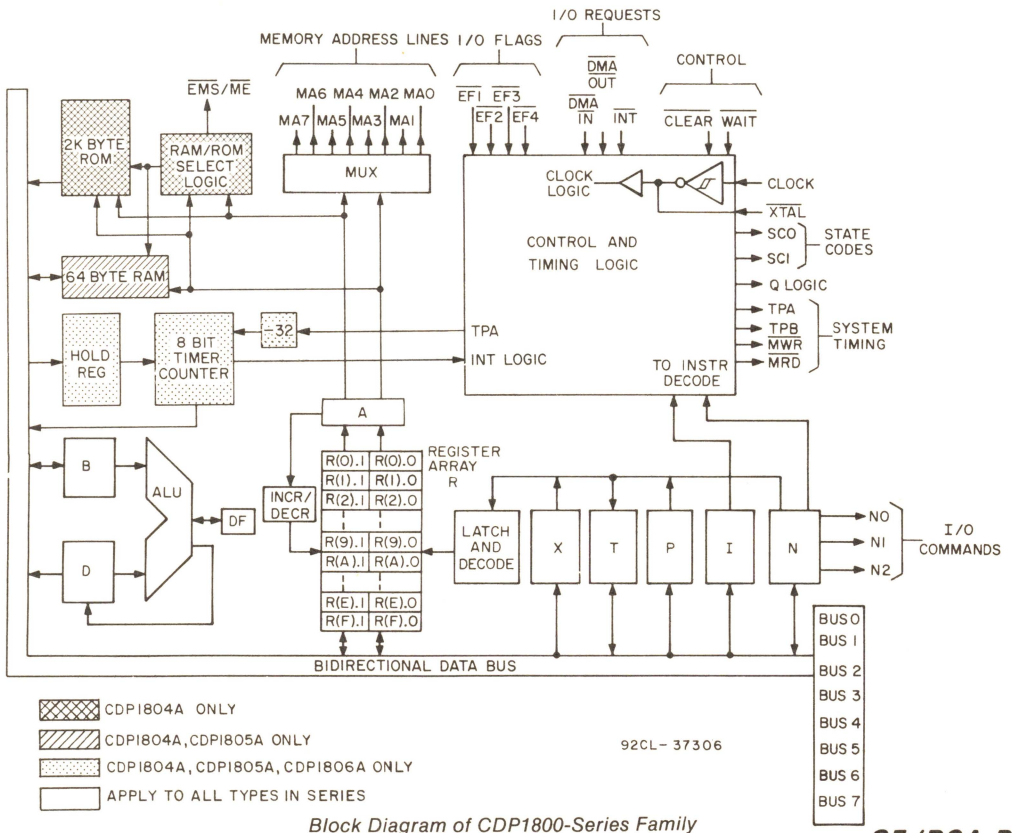
The CDP1802A provides a set of simple, easy-to-use general-purpose instructions to permit the design of programs for CDP1802A-based products with minimum effort.

The CDP1804A, CDP1805A, and CDP1806A represent enhanced, extended versions of the CDP1802A microprocessor family. The hardware and software additions, however, still allow these devices to be upward software and hardware compatible with the CDP1802A microprocessor family.

The CDP1804A, the most complex device in the family, has 2K bytes of mask-programmable ROM, 64 bytes of RAM, an 8-bit counter-timer, 32 new instructions for enhanced data and interrupt handling, and timer-counter control. The internal ROM may be deactivated for prototyping or test and debug purposes. The CDP1805A is a ROM-less version of the CDP1804A, useful for prototyping the CDP1804A function or for systems in which the memory size is greater than 2K bytes, or can change during the development or production cycle. For further economy, a ROM-less, RAM-less CDP1806A version is offered for larger systems that require significant RAM and/or ROM.

## Comparison of RCA CMOS CDP1800-Series Microprocessors and Microcomputers

| Features | CDP-1802A<br>CDP-1802AC | CDP-1802BC | CDP-1804AC | CDP-1805AC | CDP-1806AC |
|---|---|---|---|---|---|
| Memory Addressing | 64K Bytes | 64K Bytes | 64K Bytes | 64K Bytes | 64K Bytes |
| On-Chip ROM | — | — | 2K Bytes | — | — |
| On-Chip RAM | — | — | 64 Bytes | 64 Bytes | — |
| Max. Clock Frequency (MHz) | 3.2 | 5.0 | 5.0 | 5.0 | 5.0 |
| Instruction Time Min./Max. ($\mu$s) | 5.0/7.5 | 3.2/4.8 | 3.2/16.0 | 3.2/16.0 | 3.2/16.0 |
| Timer/ Counter Bits | — | — | 8 | 8 | 8 |
| Prescaler | — | — | ÷32 | ÷32 | ÷32 |
| Bus Structure | Non multiplexed Address Lines | | | | |
| Interrupts | ✓ | ✓ | ✓ | ✓ | ✓ |
| Latched I/O Lines | Off-Chip | | | | |
| Max. Operating Temperature Range | -55 to +125°C | | | | |
| Package No. of Pins | 40 D, E<br>44 Q | 40 D, E<br>44 Q | 40 D, E<br>— | 40 D, E<br>44 Q | 40 D, E<br>44 Q |




*Block Diagram of CDP1800-Series Family*

GE/RCA Products

GE/Solid State

# 6805 CMOS Microprocessors and Microcomputers

GE Solid State

All members of the RCA CDP6805 CMOS Family of MCUs and MPUs are designed around a common core which consists of a CPU, timer, oscillator, control selection (for interrupts and reset) varying amounts of bidirectional I/O lines, and, possibly, ROM. In addition to this common core, other items are added to some versions of the CDP6805, such as additional memory, I/O lines, interrupts, and serial interfaces. Using this versatile common-core design, six different CDP6805 Family micros allow the user to choose the device best suited for a particular application.

The flexible design strategy for the 6805 family enables RCA to develop new upward-compatible 6805 versions by adding additional on-chip features such as serial interfaces or additional memory. This common-core approach results in a family of micros whose software is entirely compatible. Once you learn to program one family member, you can program all additional family members. In addition, you can upgrade your existing systems and design new systems quickly and efficiently.

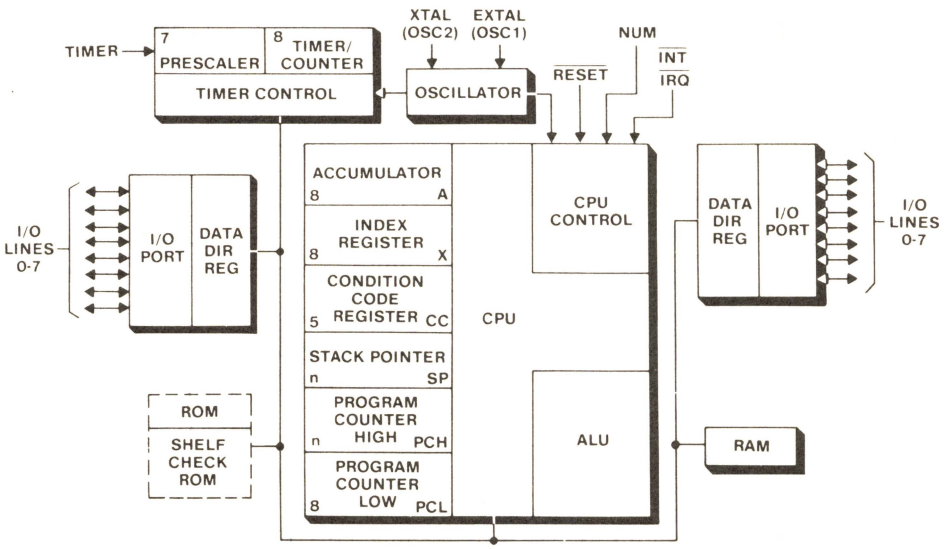
## General 6805 Family Features

### Hardware

- 8-bit architecture
- Fully static operation
- Self-check mode in microcomputers
- Master Reset and Power-on Reset
- Single 3-6 V power supply
- Power-saving STOP AND WAIT modes
- Muxed address/data bus in microprocessors

### Software

- Software compatible with entire 6805 family
- 61 instructions and 10 addressing modes
- indexed addressing for tables
- True bit manipulation
- Memory-mapped I/O
- Efficient use of program space
- Versatile interrupt handling
- 8 x 8 multiply instruction in C4 and D2 versions




*CDP6805 CMOS family basic microcomputer block diagram.*

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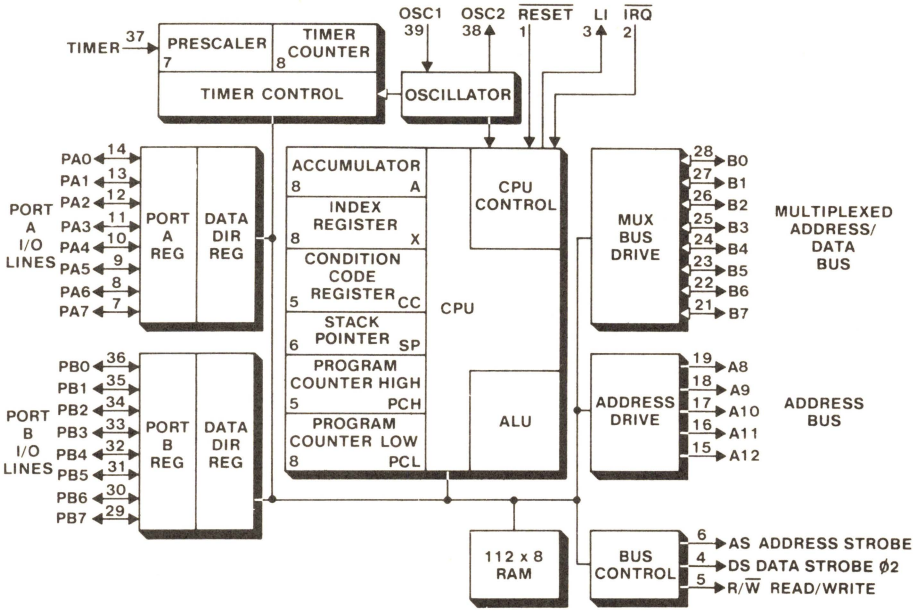


*CDP6805 CMOS family microprocessor block diagram (E2 version shown).*

## Comparison of RCA CMOS CDP6805 Family Microprocessors and Microcomputers

| Features | CDP6805E2<br>CDP6805E2C# | CDP6805E3<br>CDP6805E3C# | CDP6805F2<br>CDP6805F2C# | CDP6805G2<br>CDP6805G2C# | CDP68HC05D2° | CDP68HC05C4° | CDP68HC05C8° |
|---|---|---|---|---|---|---|---|
| Memory Addressing (Bytes) | 8k | 64k | — | — | — | — | — |
| On-Chip RAM (Bytes) | 112 | 112 | 64 | 112 | 96 | 176 | 176 |
| On-Chip ROM (Bytes) | — | — | 1089 | 2106 | 2176 | 4160 | 7744 |
| Max. Clock Frequency (MHz) | 5.0 | 5.0 | 4.0 | 4.0 | 4.2 | 4.2 | 4.2 |
| Instruction Time Min./Max. (μs) | 2.0/10.0 | 2.0/10.00 | 2.0/10.00 | 2.0/10.00 | 0.95/5.23 | 0.95/5.23 | 0.95/5.23 |
| Timer/Counter Bits | 8 | 8 | 8 | 8 | 16 | 16 | 16 |
| Prescalers | Program | Program | Program | Program | ÷4 | ÷4 | ÷4 |
| Bus Structure | Multiplexed Address/Data | | — | — | — | — | — |
| Interrupts | V | V | V | V | V | V | V |
| Latched I/O Lines | 16 | 13 | 16 | 32 | 24 | 24 | 24 |
| Max. Operating Temp. Range (°C) | 0 to +70 | 0 to +70 | 0 to +70 | 0 to +70 | -40 to +125 | -40 to +125 | -40 to +125 |
| Package No. of Pins | 40 D, E<br>44 Q | 40 D, E<br>44 Q | 28 D, E<br>28 Q | 40 D, E<br>— | 40 D, E<br>44 Q | 40 D, E<br>44 Q | 40 D, E<br>44 Q |

V = Vectored address °Multiply instruction in the CDP68HC05C4, CDP68HC05C8, and CDP68HC05D2

# "C" Version has -40 to +85°C operating temperature range.





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## RCA CMOS Peripherals
## Can be used with CMOS and NMOS Processors

| RCA I/O TYPE | DESCRIPTION AND FUNCTION | RCA | MICROPROCESSOR BUS | | | | | INPUT LEVELS | FANOUT$_2$ (TTL LOADS) |
|---|---|---|---|---|---|---|---|---|---|
| | | | MULTIPLEXED | | | NON-MULTIPLEXED | | | |
| | | | RCA/ MOTOROLA | INTEL | INTEL/ NSC | ZILOG | ROCKWELL | | |
| | | 1800 SERIES | 68HC05 6805 | 8048, 8051 80C48,80C51 8049, 80C49 8088 | 8085 80C85 NSC800 | Z80 | 6502 65C02 | | |
| **I/O PORTS** | | | | | | | | | |
| CDP1851 | PROGRAMMABLE I/O PORT | YES | NOTE 1 | NOTE 1 | NOTE 1 | YES | YES | CMOS | 1 |
| CDP1852 | BYTE-WIDE I/O PORT | YES | YES | YES | YES | YES | YES | CMOS | 1 |
| CDP1872 | 8-BIT INPUT PORT | YES | YES | YES | YES | YES | YES | CMOS | 3 |
| CDP1874 | 8-BIT INPUT PORT | YES | YES | YES | YES | YES | YES | CMOS | 3 |
| CDP1875 | 8-BIT INPUT PORT | YES | YES | YES | YES | YES | YES | CMOS | 3 |
| CDP6823 | PARALLEL INTERFACE (MOTEL BUS) | NO | YES | YES | YES | NO | NO | CMOS | 1 |
| **MEMORY I/O DECODERS** | | | | | | | | | |
| CDP1853 | N-BIT 1 OF 8 DECODER | YES | YES | YES | YES | YES | YES | CMOS | 1 |
| CDP1881 | 6-BIT LATCH/DECODER | YES | YES | YES | YES | YES | YES | CMOS | 1 |
| CDP1882 | 6-BIT LATCH/DECODER | YES | YES | YES | YES | YES | YES | CMOS | 1 |
| CDP1883 | 7-BIT LATCH/DECODER | YES | YES | YES | YES | YES | YES | CMOS | 1 |
| **SERIAL I/O** | | | | | | | | | |
| CDP1854A* | UART | YES | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | 1 |
| CDP6402 | UART | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | 1 |
| CDP65C51 | UART (WITH BAUD RATE GEN.) | NOTE 1 | USE 6853 | USE 6853 | USE 6853 | NOTE 1 | YES | TTL | 1 |
| CDP6853 | UART (MOTEL BUS, WITH BAUD RATE GEN.) | USE 65C51 | YES | YES | YES | USE 65C51 | USE 65C51 | TTL | 1 |
| **SPI I/O** | | | | | | | | | |
| CDP68HC68A2 | SPI A/D CONVERTER | NOTE 1 | YES | YES | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | 1 |
| CDP68HC68P1 | SPI SINGLE PORT I/O | NOTE 1 | YES | YES | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | 1 |
| CDP68HC68R1 | SPI RAM 128 x 8-BIT | NOTE 1 | YES | YES | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | 1 |
| CDP68HC68R2 | SPI RAM 256 x 8-BIT | NOTE 1 | YES | YES | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | 1 |
| CDP68HC68T1 | SPI REAL-TIME CLOCK | NOTE 1 | YES | YES | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | 1 |
| **MULTIPLY/ DIVIDE** | | | | | | | | | |
| CDP1855 | 8-BIT PROGRAMMABLE MDU | YES | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | 1 |
| **KEYBOARD INTERFACE** | | | | | | | | | |
| CDP1871A | KEYBOARD ENCODER | YES | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | NOTE 1 | CMOS | |
| **TIMER FUNCTIONS** | | | | | | | | | |
| CDP1878 | DUAL COUNTER-TIMER | YES | NOTE 1 | NOTE 1 | NOTE 1 | YES | YES | CMOS | 1 |
| CDP1879 | REAL-TIME CLOCK | YES | USE 6818 | USE 6818 | USE 6818 | YES | YES | CMOS | 1 |
| CDP6818 | REAL-TIME CLOCK/RAM (MOTEL BUS) | NOTE 1 | YES | YES | YES | NOTE 1 | NOTE 1 | CMOS | 1 |
| **INTERRUPT CONTROL** | | | | | | | | | |
| CDP1877 | PROGRAMMABLE INTERRUPT CONTROLLER (PIC) | YES | NO | NO | NO | NO | NO | CMOS | 1 |

*Operating in 1800 compatible mode (mode 1). Otherwise see CDP6402 for mode 0 information.

NOTES:
1. Yes but requires additional "glue parts".
2. 1 TTL load, i.e., ≤ 0.4 V at 1.6 mA.





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| RAM Type | Organization | Operating-Supply-Voltage Range $V_{SS}$ to $V_{DD}$ Volts | Operating-Temperature Range ($T_A$) °C | Electrical Characteristics at $V_{DD}$ = 5 Volts | | | | | | Max. Address Access Time ns | TTL Input | JEDEC Dual-In-Line Package No. of Pins |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Data Retention | | Max. Standby Current µA | Min. Sink Current mA | Min. Source Current mA | Max. Operating Current (e) mA | | | |
| | | | | Voltage Min. Volts | Quiescent Current Max. µA | | | | | | | |
| CDP1822[a] | 256 x 4 | 4 to 10.5 | -40 to +85 | 2 | 100 | 500 | 2 | -1 | 8 | 450 | No | 22 |
| CDP1823[a] | 128 x 8 | 4 to 10.5 | -40 to +85 | 2 | 100 | 500 | 2 | -1 | 8 | 450 | No | 24 |
| CDP1824[a] | 32 x 8 | 4 to 10.5 | -40 to +85 | 2.5 | 10 | 50 | 1.8 | -0.9 | 8 | 710 | No | 18 |
| CDP1826C | 64 x 8 | 4.5 to 6.5 | -40 to +85 | 2.5 | 25 | 50 | 1.6 | -1 | 10 | 1000 | No | 22 |
| CDP65HC68R1 | 128 x 8 | 3 to 5.5 | -40 to +85 | 2 | 25 | 15 | 1.6 | -1.6 | 10 | f | No | 8 |
| CDP68HC68R2 | 256 x 8 | 3 to 5.5 | -40 to +85 | 2 | 25 | 50 | 1.6 | -1.6 | 10 | f | No | 8 |
| CDM6116A-2 | 2K x 8 | 4.5 to 5.5 | 0 to +70 | 2 | 15[b] | 30 | 2.1 | -1 | 35[d] | 200 | Yes | 24 |
| CDM6116A-3 | 2K x 8 | 4.5 to 5.5 | 0 to +70 | 2 | 25[b] | 50 | 2.1 | -1 | 35[d] | 150 | Yes | 24 |
| CDM6116A-9 | 2K x 8 | 4.5 to 5.5 | -40 to +85 | 2 | 50[b] | 100 | 2.1 | -1 | 40[d] | 250 | Yes | 24 |
| CDM6264-3 | 8K x 8 | 4.5 to 5.5 | 0 to +70 | 2 | 50 | 100 | 2.1 | -1 | 9 | 150 | Yes | 28 |
| CDM6264-2I | 8K x 8 | 4.5 to 5.5 | -40 to +85 | 2 | 100 | 200 | 2.1 | -1 | 15 | 200 | Yes | 28 |
| CDM62256-10 | 32K x 8 | 4.5 to 5.5 | 0 to +70 | 2 | 50[b] | 100 | 4 | -1 | 65 | 100 | Yes | 28 |
| CDM62256-10I | 32K x 8 | 4.5 to 5.5 | -40 to +85 | 2 | 100[b] | 200 | 4 | -1 | 65 | 100 | Yes | 28 |
| CDM62256-12I | 32K x 8 | 4.5 to 5.5 | -40 to +85 | 2 | 100[b] | 200 | 4 | -1 | 65 | 120 | Yes | 28 |
| MWS5101-L2 | 256 x 4 | 4 to 6.5 | 0 to +70 | 2 | 10 | 50 | 2 | -1 | 8 | 250 | No | 22 |
| MWS5101-L3 | 256 x 4 | 4 to 6.5 | 0 to +70 | 2 | 50 | 200 | 2 | -1 | 8 | 350 | No | 22 |
| MWS5101A-L2 | 256 x 4 | 4 to 6.5 | 0 to +70 | 2 | 10 | 50 | 2 | -1 | 8 | 250 | No | 22 |
| MWS5101A-L3 | 256 x 4 | 4 to 6.5 | 0 to +70 | 2 | 50 | 200 | 2 | -1 | 8 | 350 | No | 22 |
| MWS5114-1 | 1K x 4 | 4.5 to 6.5 | 0 to +70 | 2 | 125 | 250 | 2 | -0.4 | 8 | 300 | Yes | 18 |
| MWS5114-2 | 1K x 4 | 4.5 to 6.5 | 0 to +70 | 2 | 50 | 100 | 2 | -0.4 | 8 | 250 | Yes | 18 |
| MWS5114-3 | 1K x 4 | 4.5 to 6.5 | 0 to +70 | 2 | 50 | 100 | 2 | -0.4 | 8 | 200 | Yes | 18 |

[a] Data available for $V_{DD}$ = 10 volts
[b] $V_{DD}$ = 3 volts
[c] $V_{DD}$ = Specified data retention voltage, except as noted
[d] Output open-circuited minimum cycle time
[e] Output open-circuited, cycle time = 1µs, except as noted.
[f] Serial interface

# Read-Only Memories (ROMs)



| ROM Type | Organization | Supply Voltage Range ($V_{SS}$ to $V_{DD}$) Volts | Operating-Temperature Range ($T_A$) °C | Electrical Characteristics at ($V_{DD}$ = 5 Volts) | | | | | Chip Enable Access Time ns | JEDEC Dual-In-Line Package No. of Pins |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Max. Standby Current $I_{DD}$ μA | Min. Sink Current $I_{OL}$ mA | Min. Source Current $I_{OH}$ mA | Max. Operating Current $I_{DD1}$/ $I_{OPER}$ mA | Max. Address Access Time ns | | |
| CDP1831 | 512 x 8 | 4 to 10.5 | -40 to +85° | 50 | 0.55 | -0.35 | 10† | 1000 | — | 24 |
| CDP1831C | 512 x 8 | 4 to 6.5 | -40 to +85° | 200 | 0.55 | -0.35 | 10† | 1000 | — | 24 |
| CDP1832 | 512 x 8 | 4 to 10.5 | -40 to +85° | 50 | 0.55 | -0.35 | 10† | 1000 | — | 24 |
| CDP1832C | 512 x 8 | 4 to 6.5 | -40 to +85° | 200 | 0.55 | -0.35 | 10† | 1000 | — | 24 |
| CDP1833 | 1K x 8 | 4 to 10.5 | −40 to +85° | 50 | 0.8 | −0.8 | 10† | 775 | — | 24 |
| CDP1833BC | 1K x 8 | 4 to 6.5 | −40 to +85° | 200 | 0.8 | −0.8 | 10† | 700 | — | 24 |
| CDP1833C | 1K x 8 | 4 to 6.5 | −40 to +85° | 200 | 0.8 | −0.8 | 10† | 775 | — | 24 |
| CDP1834 | 1K x 8 | 4 to 10.5 | −40 to +85° | 50 | 0.8 | −0.8 | 10† | 750 | — | 24 |
| CDP1834C | 1K x 8 | 4 to 6.5 | −40 to +85° | 200 | 0.8 | −0.8 | 10† | 750 | — | 24 |
| CDP1835C | 2K x 8 | 4 to 6.5 | −40 to +85° | 50 | 0.8 | −0.8 | 10* | 500 | — | 24 |
| CDP1837C | 4K x 8 | 4 to 6.5 | −40 to +85° | 50 | 0.8 | −0.8 | 10* | 500 | — | 24 |
| CDM5332 | 4K x 8 | 4 to 6.5 | −40 to +85° | 50 | 2.4 | −1.2 | 25* | 350 | — | 24 |
| CDM5333 | 4K x 8 | 4 to 6.5 | −40 to +85° | 50 | 2.4 | −1.2 | 25* | 350 | — | 24 |
| CDM5364 | 8K x 8 | 4 to 6.0 | −40 to +85° | 50 | 3.2 | −3.2 | 10* | 250 | — | 24 |
| CDM5364A | 8K x 8 | 4 to 6.0 | −40 to +85° | 50 | 3.2 | −3.2 | 10* | 250 | — | 24 |
| CDM5365 | 8K x 8 | 4 to 6.0 | −40 to +85° | 50 | 3.2 | −3.2 | 10* | 250 | 90 | 28 |
| CDM53128 | 16K x 8 | 4 to 6.0 | −40 to +85° | 50 | 3.2 | −3.2 | 10* | 250 | 90 | 28 |
| CDM53256 | 32K x 8 | 4 to 6.0 | −40 to +85° | 50 | 3.2 | −3.2 | 12* | 200 | 90 | 28 |

‡Output open-circuited; cycle time, 2.5μs. *Output open-circuited; cycle time, 1μs




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# Op-Amps, OTAs, and Comparators

| Type | $V_{IO}$ (Max) mV | $I_{IO}$(Max) nA | $I_I$ Max nA | $I^+$ Max Ma | Max $V^+$, $V^-$ | $A_{OL}$ (Min) V/V | $A_{OL}$ (Min) dB | BW MHz | SR (Typ) V/$\mu$s | Compen-sation | Package Plastic/Ceramic | Package TO-5 Metal CAN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **General Purpose Types Single-Unit Types** | | | | | | | | | | | | |
| CA081 | 15 | 0.030 | 0.050 | 2.8 | ±18 | 25K | 88 | 5 | 13 | Internal | 8E | — |
| CA081A | 6 | 0.020 | 0.040 | 2.8 | ±18 | 50K | 94 | 5 | 13 | Internal | 8E | — |
| CA101 | 5 | 200 | 0.05 | 2.5 | ±44 | 50K | 94 | 1 | — | External | 8E | 8T, 8S |
| CA201, LM201† | 7.5 | 500 | 0.15 | 3 | ±44 | 20K | 85 | 1 | — | External | 8E | 8T, 8S |
| CA301A, LM301A† | 7.5 | 50 | 0.025 | 8 | ±36 | 25K | 88 | 1 | .10 | External | 8E | 8T, 8S |
| CA307, LM307† | 7.5 | 50 | 250 | 3 | ±36 | 25K | 88 | 1 | — | Internal | 8E | 8T, 8S |
| CA741, LM741† | 5 | 200 | 500 | 2.8 | ±44 | 50k | 94 | 1 | 0.5 | Internal | 8E | 8T, 8S |
| CA741C, LM741C† | 6 | 200 | 500 | 2.8 | ±36 | 20K | 86 | 1 | 0.5 | Internal | 14E | 10T |
| CA748, LM748† | 5 | 200 | 500 | 2.8 | ±44 | 50K | 94 | 1 | 0.5 | External | 8E | 8T, 8S |
| CA748C, LM748C† | 6 | 200 | 500 | 2.8 | ±35 | 20K | 86 | 1 | 0.5 | External | 8E | 8T, 8S |
| CA3193 BiMOS | 0.5 | 10 | 40 | 3.5 | ±18 | 100K | 100 | 1.2 | 0.25 | Internal | 8E | 8T, 8S |
| CA3193A BiMOS | 0.2 | 5 | 20 | 3.5 | ±18 | 316K | 110 | 1.2 | 0.25 | Internal | 8E | 8T, 8S |
| CA3420 BiMOS | 10 | 4 pA | 0.05 | 0.65 | ±22 | 10K | 80 | 0.5* | 0.5 | Internal | 8E | 8T, 8S |
| CA3420A BiMOS | 5 | 4pA | 0.05 | 0.65 | ±22 | 20K | 86 | 0.5* | 0.5 | Internal | 8E | 8T, 8S |
| CA3440† BiMOS | 10 | 0.03 | 0.05 | 0.017 | ±12.5 | 10K | 80 | 0.063* | 0.03 | Internal | 8E | 8T, 8S |
| CA3440A BiMOS | 5 | 0.02 | 0.04 | 0.017 | ±12.5 | 10K | 80 | 0.063* | 0.03 | Internal | 8E | 8T, 8S |
| CA3450 (3 GHz) | 15 | 150 | 350 | 35 | ±8.5 | 1K | 60 | 170[4] | 330[5] | External | 16E | — |
| CA3493 BiMOS | 0.5 | 10 | 40 | 3.5 | ±18 | 100K | 100 | 1.2* | 0.25 | Internal | 8E | 8T, 8S |
| CA3493A BiMOS | 0.2 | 5 | 20 | 3.5 | ±18 | 316K | 110 | 1.2* | 0.25 | Internal | 8E | 8T, 8S |
| CA6741 | Low-Noise Version of CA741 | "Popcorn" (Burst) Noise - Dence rejected if total noise voltage (burst & 1/f) referred to input exceeds 20$\mu$V during 30-second test period. | | | | | | | | | | |
| **Dual Unit Types** | | | | | | | | | | | | |
| CA082 BiMOS | 15 | 0.03 | 0.05 | 2.8 | ±18 | 50K | 94 | 5 | 13 | Internal | 8E | — |
| CA082A BiMOS | 6 | 0.02 | 0.04 | 2.8 | ±18 | 50K | 94 | 5 | 13 | Internal | 8E | — |
| CA158 | 5 | 30 | 150 | 1.2 | ±13 | 50K | 94 | 1 | — | Internal | 8E | 8T, 8S |
| CA158A | 2 | 10 | 50 | 1.2 | ±13 | 50K | 94 | 1 | — | Internal | 8E | 8T, 8S |
| CA258 | 5 | 30 | 150 | 1.2 | ±13 | 50K | 94 | 1 | — | Internal | 8E | 8T, 8S |
| CA258A | 3 | 15 | 80 | 1.2 | ±13 | 50K | 94 | 1 | — | Internal | 8E | 8T, 8S |
| CA358, LM358† | 7 | 50 | 250 | 1.2 | ±13 | 25K | 88 | 1 | — | Internal | 8E | 8T, 8S |
| CA358A | 3 | 30 | 100 | 1.2 | ±13 | 25K | 88 | 1 | — | Internal | 8E | 8T, 8S |
| CA747 | 5 | 200 | 500 | 2.8 | ±44 | 50K | 94 | 1 | 0.5 | Internal | 14E | 10T |
| CA747C | 6 | 200 | 500 | 2.8 | ±36 | 20K | 86 | 1 | 0.5 | Internal | 14E | 10T |
| CA1458, LM1458† | 6 | 200 | 500 | 2.8 | ±36 | 20K | 86 | 1 | 0.5 | Internal | 8E | 8T, 8S |
| CA1558, LM1558† | 5 | 200 | 500 | 2.8 | ±44 | 50K | 94 | 1 | 0.5 | Internal | 8E | 8T, 8S |
| CA2904, LM2904† | 7 | 50 | 250 | 1.2 | ±13 | 100K | 100• | 1 | — | Internal | 8E | 8T, 8S |
| CA5422 BiMOS Ampl A | 10 | 0.001 | 0.005 | 0.7 | ±22 | 1K | 60 | 6.16* | 0.25 | External | 14E | — |
| CA5422 BiMOS Ampl B | 10 | 0.015 | 0.025 | 0.7 | | 316 | 50 | 0.001* | 1 | | | |
| **Quad Unit Types** | | | | | | | | | | | | |
| CA084 BiMOS | 15 | 0.03 | 0.05 | 2.8 | ±18 | 50K | 94 | 5 | 13 | Internal | 8E | — |
| CA084A BiMOS | 6 | 0.02 | 0.04 | 2.8 | ±18 | 50K | 94 | 5 | 13 | Internal | 8E | — |
| CA124 | 5 | 30 | 150 | 2 | ±16 | 50K | 94 | 1 | — | Internal | 14E | — |
| CA224 | 7 | 50 | 250 | 2 | ±16 | 25K | 88 | 1 | — | Internal | 14E | — |
| CA324, LM324† | 7 | 50 | 250 | 2 | ±16 | 20K | 86 | 1 | — | Internal | 14E | — |
| CA3401 | — | — | 300 | 10 | ±18 | 1000 | 60 | 5 | 0.6 | Internal | 14E | — |
| CA3410 | 15 | 0.03 | 0.04 | 12 | ±36 | 20K | 86 | 5.4* | 10 | Internal | 16E | — |
| CA3410A | 8 | 0.01 | 0.01 | 10 | ±36 | 20K | 86 | 5.4* | 10 | Internal | 16E | — |
| **Wideband Single-Unit Types** | | | | | | | | | | | | |
| CA3010 | 5 | 5000 | 0.012 | 30 | ±8 | 700 | 57 | 0.2 | 3 | External | 14 | 14T |
| CA3010A | 2 | 1500 | 0.04 | 30 | ±8 | 700 | 57 | 0.2 | 3 | External | — | 14T |
| CA3015 | 5 | 5000 | 0.024 | 30 | ±16 | 2K | 66 | 0.2 | 7 | External | — | 14T |
| CA3015A | 2 | 1600 | 0.06 | 30 | ±16 | 2K | 66 | 0.2 | 7 | External | — | 14T |
| CA3029 | 5 | 5000 | 0.012 | 30 | ±8 | 700 | 57 | 0.2 | 3 | External | 14E | — |
| CA3029A | 2 | 1500 | 0.04 | 30 | ±8 | 700 | 57 | 0.2 | 3 | External | 14E | — |
| CA3030 | 5 | 5000 | 0.024 | 30 | ±16 | 2K | 66 | 0.2 | 7 | External | 14E | — |





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| Type | $V_{IO}$ (Max) mV | $I_{IO}$(Max) nA | $I_I$ Max nA | $I^+$ Max Ma | Max $V^+$, $V^-$ | $A_{OL}$ (Min) V/V | $A_{OL}$ (Min) dB | BW MHz | SR (Typ) V/$\mu$s | Compen-sation | Package Plastic/Ceramic | Package TO-5 Metal CAN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Wideband Single-Unit Types Cont'd.** | | | | | | | | | | | | |
| CA3030A | 2 | 1600 | 0.06 | 30 | ±16 | 2K | 66 | 0.2 | 7 | External | 14E | — |
| CA3037 | 5 | 5000 | 0.012 | 30 | ±8 | 700 | 57 | 0.2 | 3 | External | 14D | — |
| CA3037A | 2 | 1500 | 0.04 | 30 | ±8 | 700 | 57 | 0.2 | 3 | External | 14D | — |
| CA3038 | 5 | 5000 | 0.024 | 30 | ±16 | 2K | 66 | 0.2 | 7 | External | 14D | — |
| CA3038A | 2 | 1600 | 0.06 | 30 | ±16 | 2K | 66 | 0.2 | 7 | External | 14D | — |
| CA3100 BiMOS | 5 | 400 | 0.02 | 10.5 | ±18 | 630 | 56 | 38* | 70 | External | 8E | 8T, 8S |
| CA3130 BiMOS | 15 | 0.03 | 0.05 | 15 | ±8 | 50K | 94 | 4.5* | 9 | External | 8E | 8T, 8S |
| CA3130A BiMOS | 5 | 0.02 | 0.03 | 15 | ±8 | 50K | 94 | 4.5* | 9 | External | 8E | 8T, 8S |
| CA3140 BiMOS | 15 | 0.03 | 0.05 | 6 | ±18 | 20K | 86 | 4.5* | 9 | Internal | 8E | 8T, 8S |
| CA3140A BiMOS | 5 | 0.02 | 0.03 | 6 | ±18 | 20K | 86 | 4.5* | 9 | Internal | 8E | 8T, 8S |
| CA3160 BiMOS | 15 | 0.03 | 0.05 | 15 | ±8 | 50K | 94 | 4* | 10 | Internal | 8E | 8T, 8S |
| CA3160A BiMOS | 5 | 0.02 | 0.03 | 15 | ±8 | 50K | 94 | 4* | 10 | Internal | 8E | 8T, 8S |
| CA3450 (3 GHz) | 15 | 150 | 350 | 35 | ±8.5 | 1K | 60 | 170[4] | 330[5] | External | 16E | — |
| **Wideband Dual-Unit Types** | | | | | | | | | | | | |
| CA3240 BiMOS | 15 | 0.03 | 0.05 | 12 | ±18 | 20K | 86 | 4.5* | 9 | Internal | 8E, 14E1 | 8T, 8S |
| CA3240A BiMOS | 5 | 0.02 | 0.04 | 12 | ±18 | 20K | 86 | 4.5* | 9 | Internal | 8E, 14E1 | 8T, 8S |
| CA3260 BiMOS | 15 | 0.03 | 0.05 | 15.5 | ±8 | 50K | 94 | 4* | 10 | Internal | 8E | 8T, 8S |
| CA3260A BiMOS | 5 | 0.02 | 0.03 | 15.5 | ±8 | 50K | 94 | 4* | 10 | Internal | 8E | 8T, 8S |
| **Wideband High-Slew Rate Types (> 50V/$\mu$s)** | | | | | | | | | | | | |
| CA3080 | 5 | 600 | 5000 | 1.2 | ±18 | gm=9600$\mu$mho | | 2 | 50 | External | 8E | 8T, 8S |
| CA3080A | 2 | 600 | 5000 | 1.2 | ±18 | gm=9600$\mu$mho | | 2 | 50 | External | 8E | 8T, 8S |
| CA3100 BiMOS | 5 | 400 | 0.02 | 10.5 | ±18 | 630 | 56 | 38* | 70 | External | 8E | 8T, 8S |
| CA3280 | 3 | 700 | 5000 | 4.8 | ±18 | 50K | 44 | 9 | 125 | External | 16E | — |
| CA3280A | 0.5 | 700 | 5000 | 4.8 | ±18 | 50K | 94 | 9 | 125 | External | 16E | — |
| CA3450 (3 GHz) | 15 | 150 | 350 | 35 | ±8.5 | 1K | 60 | 170[4] | 330[5] | External | 16E | — |
| **5-Volt BiMOS Logic Types for Low-Supply Voltage, Low-Input-Current Applications** | | | | | | | | | | | | |
| CA5130 | 10 | 0.01 | 0.015 | 0.1 | ±8 | 17.8K | 85 | 4* | 10 | External | 8E | 8T, 8S |
| CA5130A | 4 | 0.005 | 0.01 | 0.1 | ±8 | 31.6K | 90 | 4* | 10 | External | 8E | 8T, 8S |
| CA5160 | 10 | 0.01 | 0.015 | 0.1 | ±8 | 17.8K | 85 | 4* | 10 | Internal | 8E | 8T, 8S |
| CA5160A | 4 | 0.005 | 0.01 | 0.1 | ±8 | 31.6K | 90 | 4* | 10 | Internal | 8E | 8T, 8S |
| CA5260 | 15 | 0.01 | 0.015 | 1.4 | ±8 | 10K | 80 | 4* | 10 | Internal | 8E | 8T, 8S |
| CA5260A | 4 | 0.01 | 0.015 | 1.4 | ±8 | 14.1K | 83 | 4* | 10 | Internal | 8E | 8T, 8S |
| CA5420 | 10 | 0.001 | 0.002<br>0.0250 | 0.55 | ±18 | 17.8K | 85 | 0.5* | 0.5 | Internal | 8E | 8T, 8S |
| CA5420A | 5 | 0.05 | 0.001<br>0.0150 | 0.55 | ±18 | 17.8K | 85 | 0.5* | 0.5 | Internal | 8E | 8T, 8S |
| CA5422 Ampl. A | 10 | 0.001 | 0.005 | 0.7 | ±22 | 1K | 60 | 160• | 0.25 | External | 14E | — |
| CA5422 Ampl. B | 10 | 0.015 | 0.025 | 0.7 | | 316 | 50 | 1• | 1 | External | | |
| **OTA's (Programmable, Variable) Micropower (Single-Unit Types)** | | | | | | | | | | | | |
| CA3060 (Triple Unit) | 5 | 1000 | 5000 | 3.6 | ±18 | gm=30$\mu$mho | | 0.11 | 8 | External | 16E | — |
| CA3078 | 4.5 | 32 | 170 | 0.13 | ±7 | 25K | 88 | 0.002 | 1.5 | External | 14D | — |
| CA3078A | 3.5 | 2.5 | 12 | 0.02 | ±18 | 40K | 92 | 0.0003 | 0.5 | External | 14D | — |
| CA3080 | 5 | 600 | 5000 | 1.2 | ±18 | gm = 9600 $\mu$mho | | 2 | 50 | External | 8E | 8T, 8S |
| CA3080A | 2 | 600 | 5000 | 1.2 | ±18 | | | 2 | 50 | External | 8E | 8T, 8S |
| CA3440 BiMOS | 10 | 0.03 | 0.05 | 0.017 | ±12.5 | 10K | 80 | 0.063* | 0.03 | Internal | 8E | 8T, 8S |
| CA3440A BiMOS | 5 | 0.02 | 0.04 | 0.017 | ±12.5 | 10K | 80 | 0.063* | 0.03 | Internal | 8E | 8T, 8S |
| CA6078A | Low-Noise Version of CA3078A | | "Popcorn" (Burst) Noise. Device rejected if total noise voltage (burst and 1/f) referred to input exceeds 20$\mu$V peak during 30-second test period. | | | | | | | | | |
| **Dual-Unit Types** | | | | | | | | | | | | |
| CA3280 | 3 | 700 | 5000 | 4.8 | ±18 | 50K | 94 | 9 | 125 | External | 16E | — |
| CA3280A | 0.5 | 700 | 5000 | 4.8 | ±18 | 50K | 94 | 9 | 125 | External | 16E | — |




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# Op-Amps, OTAs, and Comparators

GE Solid State

| Type | $V_{IO}$ (Max) mV | $I_{IO}$(Max) nA | $I_I$ Max mA | $I^+$ Max Ma | Max $V^+$, $V^-$ | $A_{OL}$ (Min) V/V | $A_{OL}$ (Min) dB | BW MHz | SR (Typ) V/$\mu$s | Compen-sation | Package Plastic/Ceramic | Package TO-5 Metal CAN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **High Current Types** | | | | | | | | | | | | |
| CA3094 | 5 | 2000 | 5000 | 0.4 | ±12 | 20K | 86 | 30 | 50 | External | 8E | 8T, 8S |
| CA3094A | 5 | 2000 | 5000 | 0.4 | ±18 | 20K | 86 | 30 | 50 | External | 8E | 8T, 8S |
| CA3094B | 5 | 2000 | 5000 | 0.4 | ±22 | 20K | 86 | 30 | 50 | External | 8E | 8T, 8S |
| **Comparators Dual Unit** | | | | | | | | | | | | |
| CA3290 | 20 | 0.03 | 0.05 | 3 | ±18 | 25K | 88 | Response Time[2] | | — | 8E, 14E1 | 8T, 8S |
| CA3290A | 10 | 0.025 | 0.04 | 3 | ±18 | 25K | 88 | Response Time[2] | | — | 8E, 14E1 | 8T, 8S |
| **Quad Unit** | | | | | | | | | | | | |
| CA139 | 5 | 25 | 100 | 8 | ±18 | — | — | Response Time | | — | 14E | — |
| CA139A | 2 | 25 | 100 | 8 | ±18 | 50K | 94 | Response Time | | — | 14E | — |
| CA239 | 5 | 50 | 250 | 2‡ | ±18 | — | — | Response Time | | — | 14E | — |
| CA239A | 2 | 50 | 250 | 2‡ | ±18 | 50K | 94 | Response Time | | — | 14E | — |
| CA339 | 5 | 50 | 250 | 2‡ | ±18 | 50K | 94 | Response Time | | — | 14E | — |
| CA339A | 2 | 50 | 250 | 2‡ | ±18 | 50K | 94 | Response Time[3] | | — | 14E | — |

Note:

1 = 200 ns
2 = $t_r$ = 1.2 $\mu$s, $t_f$ = 200 ns
3 = $t_r$ = 1.3 $\mu$s, $t_f$ = 200 ns
4 = $A_V$ = 1; $R_L$ = 50 Ω // 20 pF, $C_C$ = 5 pF
5 = $A_V \geq 10$; $R_L$ = 50 Ω // 20 pF, $C_C$ = 0 pF
†$T_A$ = 85° C •kHz ‡Total supply current *$f_t$

# BiMOS-E Op Amp Selection Chart

| Type | $V_{IO}$ (Max) mV | $I_{IO}$ (Max) pA | $I_I$ (Max) pA | $I^+$ (Max) Supply mA | Max $V^+$, V | $A_{OL}$ (Min) dB | Unity Gain BW (Typ) MHz | SR (Typ) V/$\mu$s | Compen-sation | Package Plastic/Ceramic | Package TO-5 Metal Can |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **General-Purpose Quad-Unit Types** | | | | | | | | | | | |
| CA5470 (25°C) | 15 | 5 | 10 | 6 | ±8 | 80 | 14 | 5 | Internal | 14E, 14M | — |
| CA5470 (-55 to +125°C) | 18 | 5.5nA | 11nA | 7 | ±8 | 80 | 12 | 5 | Internal | 14E, 14M | — |
| **High-Speed Wideband Dual-Unit Types (Preliminary)** | | | | | | | | | | | |
| CA5202 (-40 to +85°C) | 3 | 0.05 nA | 0.1 nA | 8 | ±8 | 65 | 50 | 100 | Internal | 8E, 8M | 8T, 8S |

# Differential Amplifiers

| Type | Description | Freq. Range DC to MHz | A (typ.) dB | $V_{OUT}$ (p-p) V | BW (3dB Point) (Typ.) kHz | I/F NF (Typ.) dB | AGC Range (Typ.) dB | CMRR (Min.) dB | $R_{IN}$ kΩ | $C_{IN}$ pF | $R_{OUT}$ Ω |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CA3000 | DC Amplifier | 30 | 37 | 6.4 | 650 | — | 90 | 70 | — | — | — |
| CA3001 | Video & Wideband Amplifier | 29 | 19 | 5 | 29■ | 5 | 60 | 70 | 140 | 3.4 | 45 |
| CA3002 | IF Amplifier | 20 | 24 | 5.5 | 11■ | 4# | — | — | 100 | 4 | 70 |
| CA3005 | RF Amplifiers | 100 | 16 | — | — | 7.8# | -60* | 101 | — | — | — |
| CA3006 | | 100 | 16 | — | — | 7.8# | -60* | 101 | — | — | — |
| CA3026 | Dual Independent Differential Amplifier | 120 | 32□ | — | 550† | 3.25 | 75 | 100 | — | — | — |
| CA3028A | Differential/Cascode Amplifiers | 120 | 40□ | — | — | 7.2# | 62 | — | — | — | — |
| CA3028B | | 120 | 40 | 11.5 | 8 | 7.2# | 62 | 110 | $Z_{IN}$ = 5.5 kΩ | | |
| CA3040 | Video & Wideband Amplifier | 55 | 37 | 0.5■ | 5.5 | 7.5 | — | — | 150 | 2.2 | 125 |
| CA3049 | Dual High-Frequency Differential Amplifier | 500 | 22 | — | 1.35▲ | 1.5 | 75 | 100 | — | — | — |
| CA3050 | Dual Differential Amplifiers | 20 | — | — | 4.3•/600† | — | 60 | 65 | $Z_{IN}$ = 460 kΩ | | |
| CA3051 | | 20 | — | — | 4.3•/600† | — | 60 | 65 | $Z_{OUT}$ = 170 kΩ | | |
| CA3053 | Differential/Cascode Amplifier | 120 | 40 | Recommended for IF Amplifier Applications | | | | | | | |
| CA3054 | Dual Independent Differential Amplifier | 120 | 32 | — | 550† | 3.25 | 75 | 100 | — | — | — |
| CA3102 | Dual High-Frequency Differential Amplifier | 500 | 22 | — | 1.35▲ | 1.5 | 75 | 100 | — | — | — |

•Min ■RMS ▲GHZ # NF ° Transistor Array † $f_T$ (mHz) □$G_p$ Min. at 100 MHz: Cascode, 16dB; Diff. Ampl., 14 dB

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# Transistor Arrays

**Electrical Characteristics at $T_A$ = 25° C**

| Type | Description | $V_{(BR)\ CEO}$ (Min.) V | $V_{(BR)\ CBO}$ (Min.) V | $h_{FE}$ (Min.) | $I_C$ (Max.) mA | Remarks |
|---|---|---|---|---|---|---|
| CA3018 | Two Isolated Transistors plus a Darlington Pair | 15 | 20 | 30 | 50 | $h_{FE}$ matched ±10%<br>$V_{BE}$ matched ±2 mV and ±5 mV max.<br>Operation from dc to 120 MHz |
| CA3018A | | 15 | 30 | 60 | 50 | |
| CA3045 | Three Transistors plus a Differential Pair | 15 | 20 | 40 | 50 | $f_t$ > 300 MHz<br>2 matched pairs, ±5 mV |
| CA3046 | | 15 | 20 | 40 | 50 | |
| CA3050 | Dual Differential Amplifiers plus Diode Bias String | 15 | 20 | $f_T$▲600 | 50 | $I_{IO}$ = 70 nA max., $I_{IB}$ = 500 nA max.<br>$V_{IO}$ = 5 mV max. |
| CA3051 | | 15 | 20 | MHz (typ.) | 50 | |
| CA3081 | General-Purpose n-p-n High-Current Transistors | 16 | 20 | 40 | 100 | Seven Common-Emitter |
| CA3082 | | 16 | 20 | 40 | 100 | Seven Common-Collector |
| CA3083 | | 15 | 20 | 40 | 100 | Five independent transistors<br>$Q_1$ and $Q_2$ (at 1 mA): 2.5 μA max. |
| CA3086 | Three Isolated Transistors plus a Differential Pair | 15 | 20 | 40 | 50 | $f_T$ > 550 MHz typ.<br>Operation from dc to 120 MHz |
| CA3127 | Five Independent Transistors | 15 | 20 | 40 | 20/trans. | $f_T$ > 1 GHz<br>Operation from dc to 500 MHZ |
| CA3146 | Three Transistors plus a Differential Pair | 30 | 40 | 30 | 50 | $f_t$ > 500 MHz typ.<br>Operation from dc to 120 MHz |
| CA3146A | | 40 | 50 | 30 | 50 | |
| CA3183 | Five High Current Transistors | 30 | 40 | 40 | 75 | High-voltage versions of CA3083<br>Trans. $Q_1$ & $Q_2$ matched at 1 mA |
| CA3183A | | 40 | 50 | 40 | 75 | |
| CA3227 | Five Independent Transistors | 8 | 12 | 40 | 20/trans. | $f_t$ = 3 GHz typ.<br>Operation from dc to 1.5 GHz |
| CA3246 | Three Transistors plus a Differential Pair | 8 | 12 | 40 | 20 | $f_t$ = 3 GHz typ.<br>Operation from dc to 1.5 GHz. |
| CA3250 | General-Purpose n-p-n High-Current Transistors | 20 | 20 | 40 | 100 | Eight Common-Collector |
| CA3251 | | 20 | 20 | 40 | 100 | Eight Common-Emitter |

| Type | Description | $V_{(BR)\ CEO}$ (Min.) V n-p-n/p-n-p | $V_{(BR)\ CBO}$ (Min.) V n-p-n/p-n-p | $h_{FE}$ (Min.) n-p-n/p-n-p | $I_C$ (Max.) mA n-p-n/p-n-p | Remarks | |
|---|---|---|---|---|---|---|---|
| CA3096 | Five Independent Transistors, 3 n-p-n, 2 p-n-p | 35/-40 | 45/-40 | 150/20 | 50/-10 | n-p-n | p-n-p |
| CA3096A | | 35/-40 | 45/-40 | 150/20 | 50/-10 | $\lvert V_{IO}\rvert$ = 5 mV | 5 mV |
| CA3096C | | 24/-24 | 30/-24 | 100/15 | 50/-10 | $\lvert I_{IO}\rvert$ 0.6 μA | 0.25 μA |
| CA3097 | Thyristor/Transistor Array<br>1 n-p-n, 1 n-p-n/p-n-p trans. pair, 1 zener, 1 PUT, 1 SCR | 30/-40 | 50/-50 | n-p-n/p-n-p pair 8000 typ. | 100/-10 | PUT: $I_P$ = 15 nA, $V_{AK}$ = ±30 V<br>Zener $V_Z$ = 8 V ±10%<br>$Z_Z$ = 15 Ω typ. at 10 mA | |

▲For single transistor

# CMOS Arrays

**Electrical Characteristics at $T_A$ = 25° C**

| Type | Description | Features | Remarks |
|---|---|---|---|
| CA3600 | Three CMOS Pairs | $R_i$ = 100 GΩ, high voltage gain = 53 dB typ.<br>Low gate terminal current = 10pA typ. | Specified and tested for linear circuit operation at frequencies up to 5 MHz (untuned) |
| CD54/74HC/ HCTU04 | QMOs Hex Inverter (Unbuffered) Linear Wideband Amplifiers | $t_{PLH}$, $t_{PHL}$ = 6 ns @ $V_{CC}$ = 5V<br>2-6 volt operation<br>$T_A$ = -40 to + 85° C | For application information, refer to RCA Application Note, ICAN7637 "Linear Application of the CD74HCU04 QMOS Inverter" |




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# Amplifier Arrays



**Electrical Characteristics at $T_A$ = 25° C**

| Type | Description | $f_T$ MHz | $A_{OL}$ (Typ.) dB | NF (Typ.) dB | Push-Pull Input & Output | Features |
|---|---|---|---|---|---|---|
| CA3026<br>CA3054 | Dual Independent Differential Amplifers | 550■ | 32 | 3.25■* | X | Maximum input offset voltage — ±5 mV. Useful from dc to 120 MHz |
| CA3048 | Four Independent AC Amplifiers | 12 | 58 | 2 @ 1kHz | — | Operates from single-ended supply |
| CA3049<br>CA3102 | Dual High-Frequency Differential Amplifiers | 1350 | 23† | 4.6† | X | Independently accessible inputs and outputs. Useful from dc to 500 MHz |
| CA3052 | Four Independent AC Amplifiers | 12 | 58‡ | $V_O$ = 2 Vrms min. | | Operates from single-ended supply |
| CA3060 | Three, Independent, Identical OTA Arrays | For data, see Operational Amplifier Section | | | X | Includes unique zener diode regulator system |

† At 200 MHz  *1/f at 1kHz  ■For single transisitor  △At 100 kHz  ‡Each amplifier

# Diode Arrays

**Electrical Characteristics at $T_A$ = 25° C. Apply for Each Diode Unit Unless Otherwise Specified.**

| Type | Description | $V_{(BR)R}$ (Min.) V | $I_R$ (Max.) μA | $C_D$ (Typ.) pF | $V_{F1} - V_{F2}$ (Max.) mV | Features |
|---|---|---|---|---|---|---|
| CA3019 | Quad Plus 2 Uncommitted | 4 | 10 | 1.8 | 5 ($I_F$ = 1 mA) | • Ultra-fast low-capacitance matched □ diodes |
| CA3039 | 6 Individual Matched | 5 | 0.1 | 0.65 | 5 ($I_F$ = 1 mA) | |
| CA3141 | 10 High Reverse - Breakdown Voltage Diodes□□ | 30 | 0.1 | 0.3 | 0.55 (typ.) (each diode pair) | • Low-noise performance<br>• Low leakage current |

□$V_F$ matched withn 5 Volts  □□Six connected to form 3 common-cathode diode pairs
Four connected to form 2 common-anode diode pairs

# Power-Control Circuits

## CA3177
## Operational Amplifier Comparator

**Electrical Characteristics at $T_A$ = 25°C**

| Characteristics | Limits Min. | Limits Max. | Units |
|---|---|---|---|
| Operational Amplifier | | | |
| Input Offset Voltage, $V_{IO}$ | — | 100 | mV |
| Input Bias Current, $I_{IB}$ | — | 15 | μA |
| Common-Mode Input Voltage Range, $V_{ICR}$ | 2 | 12 | V |
| Amplifier Supply Current | 3 | 10 | mA |
| Q14 Amplifier | | | |
| DC Forward-Current Transfer Ratio, $h_{FE}$ | 45<br>45 | —<br>— | |
| Collector-to-Emitter Saturation Voltage, ($V_{CE\ (SAT)}$) | — | 0.6 | V |
| Q1 Amplifier | | | |
| Collector-to-Emitter Saturation Voltage ($V_{CE\ (sat)}$) | — | 0.4 | V |

## CA3020, CA3020A
## Multi-Purpose Wideband Power Amplifiers

**Typical Electrical Characteristics at $T_A$ = 25°C**

| Characteristics | CA3020 | CA3020A | Units |
|---|---|---|---|
| Maximum Power Output ($P_O$) at THD = 10% | 550 | 1000 | mW |
| Sensitivity ($C_{IN}$) | 35 | 45 | mV |
| Power Gain ($G_P$) | 75 | 75 | dB |
| Input Resistance ($R_{IN}$) | 55 | 55 | kΩ |
| Signal-to-Noise Ratio (I/N) | 70 | 66 | dB |
| Total Harmonic Distortion at 150 mW (THD) | 3.1 | 3.3 | % |
| Bandwidth (-3-dB point) (BW) | 8 | 8 | MHz |

## CA3059, CA3079
## Zero-Voltage Switches

**Electrical Characteristics at $T_A$ = 25°C**

| Characteristics | Max. $V_+$ | Sensor Range KΩ | DC Mode | External Trigger |
|---|---|---|---|---|
| CA3059 | 14 | 2 to 100 | X | X |
| CA3079 | 10 | 2 to 50 | — | — |





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# Power-Control Circuits

## CA3262 Inverting
## CA3219A, CA3252 Non-Inverting
## Quad-Gated Power Drivers

**Electrical Characteristics at $T_A = 25°C$, $V_{cc} = 5V$**

| Characteristics | Limits Min. | Limits Max. | Units |
|---|---|---|---|
| Output Leakage Current ($I_{CEX}$) $V_{CE} = 50$ V $V_{IN} = 0.8$ V | — | 100 | μA |
| Output Sustaining Voltage ($V_{CE\ SUS}$) $I_C = 100$ mA $V_{IN} = 0.8$ V | 25 | — | V |
| Collector Emitter Saturation Voltage $V_{CE\ (sat)}$ $I_c = 600$ mA, $V_{IN} = 2.4$ V | — | 0.7 | V |
| Supply Current - All Outputs ON $I_{CC}$ (ON) $I_C = 700$ mA, $V_{CC} = V_{IH} = 5.5$ V | — | 80 | mA |
| Supply Current - All Outputs OFF $I_{CC}$ (OFF) | — | 5 | mA |
| Clamp Diode Leakage Current ($I_n$) $V_n$ - 50 V | — | 100 | μA |
| Turn-On Delay $t_{PHL}$ CA3262, CA3219A | — | 10 | μs |
| Turn-Off Delay $t_{PLH}$ CA3252 | — | 30 | μs |

## CA3242 Inverting
## Quad-Gated Power Driver

**Electrical Characteristics at $T_A = 40$ to $+85°C$, $V_{cc} = 5V$**

| Characteristics | Limits Min. | Limits Max. | Units |
|---|---|---|---|
| Output Leakage Current ($I_{CEX}$) $V_{CE} = 30$ V $V_{IN} = 22.4$ V | — | 100 | μA |
| Output Sustaining Voltage ($V_{CE\ SUS}$) $I_C = 100$ mA $V_{IN} = 2.4$ V | 25 | — | V |
| Collector Emitter Saturation Voltage $V_{CE\ (sat)}$ $I_c = 600$ mA, $V_{IN} = 0.2$ V | — | 0.8 | V |
| Supply Current - All Outputs ON $I_{CC}$ (ON) $I_C = 700$ mA, $V_{CC} = V_{IH} = 5.5$ V | — | 80 | mA |
| Supply Current - All Outputs OFF $I_{CC}$ (OFF) | — | 5 | mA |
| Clamp Diode Leakage Current ($I_r$) $V_r = 50$ V | — | 100 | μA |
| Turn-On Delay $t_{PHL}$, Turn-Off Delay $t_{PLH}$ | — | 20 | μs |

## CA3169
## Solenoid and Motor Driver (½ H Driver)

**Electrical Characteristics at $T_A = 25°C$, $V_{CC} = 10.5$ to 18 V**

| Characteristics | | Limits Min. | Limits Typ. | Limits Max. | Units |
|---|---|---|---|---|---|
| Output Leakage Current (Pin 2 or Pin 3) | | -110 | ±0.5 | 110 | μA |
| Quiescent Current (Pin 1): Input Terminals Shorted | $V_{CC}$ = 14 V | — | 70 | 100 | mA |
| Input Terminals Open | $V_{CC}$ = 14 V | — | 17 | 40 | mA |
| Overvoltage Shutdown Circuit (Pin 1) Upper Trip Point | | 20 | 25 | 27 | V |
| Lower Trip Point | | 18 | 21.4 | 23 | V |
| Source Output Short Circuit Current (Pin 2-G) | | 0.65 | 1.11 | 2.6 | A |
| Sink Output ($I_{SINK}$ = 600 mA) Output Saturation Voltage ($V_S$) | | — | 0.3 | 0.85 | V |

## CA1524, CA2524, CA3524
## Regulating Pulse-Width Modulators

**Electrical Characteristics at $V^+ = 20$ V, f = 20kHz**
**$T_A = -55$ to $+125°C$ for CA1524;**
**0 to $+70°C$ for CA2524, CA3534**

| Type | $V^+$ Range V | $V_O$ Range V | Load Regulation % $V_O$ (Typ.) | Ripple Rejection db (Typ.) | Total Standby Current Is (Max.) | $V_{CE}$ (sat) V (Typ.) |
|---|---|---|---|---|---|---|
| CA1524 | 8 to 40 | 4.6 to 5.2 | 0.2 | 66 | 10 | 0.8 |
| CA2524 | 8 to 40 | 4.8 to 5.2 | 0.2 | 66 | 10 | 0.8 |
| CA3524 | 8 to 40 | 4.6 to 5.4 | 0.2 | 66 | 10 | 0.8 |

Short-Circuit Current Limit, 100mA typ.
Temperature Stability, 1% max.

## CA1523
## Voltage-Regulator Control Circuit

**Electrical Characteristics at $T_A = 25°C$**

| Characteristics | Limits Min. | Limits Typ. | Limits Max. | Units |
|---|---|---|---|---|
| Maximum Pulse Width | 5.5 | 6.5 | 7.5 | μs |
| Minimum Pulse Width | 2 | 3 | 4 | μs |
| Output High Voltage | 11.1 | 12 | 12.6 | V |
| Output Low Voltage | 0.6 | 1 | 1.3 | V |
| Rise Time | 250 | 600 | 1250 | ns |
| Fall Time | 50 | 200 | 350 | ns |
| Error Voltage Reference | 6 | 6.8 | 7.6 | V |
| Charge Current | 190 | 220 | 250 | μA |
| Discharge Current | 95 | 110 | 125 | μA |
| Slow Start Discharge Current | 20 | 30 | 40 | μA |
| Discharge Voltage | 1.7 | 2.4 | 3.2 | V |
| Output Inhibit Voltage | 7.8 | 8.4 | 8.9 | V |
| Overcurrent Temp. Voltage | 1.1 | 1.25 | 1.4 | V |
| Supply Voltage | — | 13 | — | V |
| Supply Current ($V_S = +50$V) | — | 30 | — | mA |

## CA3085, CA3085A, CA3085B
## CA723, CA723C, LM723, LM723C
## Voltage Regulators

**Electrical Characteristics at $T_A = 25°C$**

| Type | $V_I$ Range V | $V_O$ Range V | $I_O$ (max.) mA | Load Regulation % $V_O$ (max.) | $V_I$-$V_O$ V (min.) | Short-Circuit Current Limit mA (typ.) |
|---|---|---|---|---|---|---|
| CA3085 | 7.5 to 30 | 1.8 to 26 | 12 | 0.1 | 4 | 96 |
| CA3085A | 7.5 to 40 | 1.7 to 36 | 100 | 0.15 | 4 | 96 |
| CA3085B | 7.5 to 50 | 1.7 to 46 | 100 | 0.15 | 3.5 | 96 |
| CA723 | 9.5 to 40 | 2 to 37 | 150 | 0.03 | 3 | 65 |
| CA723C | 9.5 to 40 | 2 to 37 | 150 | 0.03 | 3 | 65 |

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| Type | Technology | Resolution (Bits) | Resolution (Digits) | Clock Rate (MHz) | Conversion Time (μs) | Conversion Times (ms) | At Supply Voltage (V) | Typ. Power Dissip. (mW) | Integral Linearity (LSB) | Integral Linearity (Count) | Diff. Linearity (LSB) | At Full-Scale Input (V) | Package Size (Pins) | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A/D Converters** | | | | | | | | | | | | | | |
| **Parallel (Flash) Types** | | | | | | | | | | | | | | |
| CA3304 | CMOS/SOS | 4 | — | 20 | — | — | 5 | 30 | ¼ | — | ¼ | 2 | 16 | Has data change output |
| CA3304A | CMOS/SOS | 4 | — | 25 | — | — | 5 | 35 | ⅛ | — | ⅛ | 2 | 16 | Upgrade of CA3304 |
| CA3306C | CMOS/SOS | 6 | — | 10 | — | — | 5 | 55 | ½ | — | ½ | 4.8 | 18 | Improved retrofit for CA3300 |
| CA3306 | CMOS/SOS | 6 | — | 15 | — | — | 5 | 70 | ½ | — | ½ | 4.8 | 18 | Higher-speed version of CA3306C |
| CA3306A | CMOS/SOS | 6 | — | 15 | — | — | 5 | 70 | ¼ | — | ¼ | 4.8 | 18 | CA3306 with improved linearity |
| CA3318C | CMOS/SOS | 8 | — | 15 | — | — | 5 | 150 | 1.5 | — | +1/ -0.8 | 6.4 | 24 | Improved retrofit for 41051. Has input bandwidth restriction of 2 MHz. |
| CA3318 | CMOS/SOS | 8 | — | 15 | — | — | 5 | 150 | 1.5 | — | ±0.8 | 6.4 | 24 | CA3318C with 5-MHz input bandwidth restriction |
| **Successive Approximation Types** | | | | | | | | | | | | | | |
| CA3310 | CMOS | 10 | — | — | 6.5 | — | 5 | 15 | 0.75 | — | 0.75 | 4.608 | 24 | Integral track and hold, rail-to-rail input range |
| CA3310A | CMOS | 10 | — | — | 6.5 | — | 5 | 15 | ½ | — | ½ | 4.608 | 24 | CA3310 with improved linearity |
| CDP68HC68A2 | CMOS | 10 | — | — | 100 | — | 5 | 15 | 2 | — | 2 | 5.30 | 16 | Standard Serial Peripheral Interface bus and eight multiplexed analog inputs |
| **Integrating Types** | | | | | | | | | | | | | | |
| CA3162 | $I^2L$ | — | 3 | — | — | 10 | 5 | 60 | — | 1 | NMC | +1/ -0.1 | 16 | Part of 2-chip set. To make complete DPM, add CA3161 and 3 PNP transistors. |
| CA3162A | $I^2L$ | — | 3 | — | — | 10 | 5 | 60 | — | 1 | NMC | +1/ -0.1 | 16 | -40°C to +85°C specified version of CA3162 |
| **D/A Converters** | | | | | | | | | | | | | | |
| **High-Speed R-2R Types** | | | | | | | | | | | | | | |
| CA3338 | CMOS/SOS | 8 | — | 50 | — | — | 5 | 100 | 1 | — | ¾ | 5 | 16 | Data complement control and input latch |
| CA3338A | CMOS/SOS | 8 | — | 50 | — | — | 5 | 100 | ¾ | — | ½ | 5 | 16 | Linearity upgrade of CA3338 |

NOTES: TBE = To be established NMC = No missing codes
Power dissipation is at given sampling rate, at given supply voltage, and does not include reference current.
All converters operate from single supply. Specifications are limit values unless noted as typical.
All flash and successive approximation A/D converters have three-state CMOS bus driver outputs.
Unless noted, all flash and successive approximation A/D converters will accept Nyquist rate input bandwidths.



## CA3304, CA3304A
## CMOS Video-Speed 4-Bit Flash Analog-to-Digital Converters

**Features:**

- *CMOS/SOS low power with video speed*
- *Parallel conversion technique*
- *Single power supply voltage (3 to 7.5V)*
- *25-MHz sampling rate (40-ns conversion time) at 5-V supply*
- *4-bit latched 3-state output with overflow and data change outputs*
- *1/8 LSB maximum nonlinearity (A version)*
- *Inherent resistance to latch-up due to SOS process*
- *Bipolar input range with optional second supply*

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## CA3306, CA3306A, CA3306C
## CMOS Video-Speed 8-Bit R-2R Digital-to-Analog Converters

**Features:**

- *CMOS low power with video speed*
- *Parallel conversion technique*
- *Single power supply voltage (3 to 7.5V)*
- *15-MHz sampling rate with single 5-V supply*
- *6-bit latched 3-state output with overflow bit*
- *Pin-for-pin retrofit for the CA3300*

## CA3318, CA3318C
## CMOS Video-Speed 8-Bit Flash A/D Converters

**Features:**

- *Pin compatible with 41051/CA3308*
- *CMOS/SOS low power*
- *Flash (Parallel) conversion technique*
- *15 MSPS conversion rate at 5V (CA3318C)*
- *20 MSPS conversion rate at 5V (CA3318)*
- *1 LSB differential linearity*
- *1.5 LSB integral linearity*
- *Single 4 to 6.5V supply*
- *8 latched bit outputs plus overflow*
- *May be stacked for higher resolution*
- *May be paralleled for double speed*

## CA3310, CA3310A
## CMOS 10-Bit A/D Converters With Internal Track and Hold

**Features:**

- *CMOS low power*
- *Single 3-to-6 volt supply*
- *13-μs conversion time at 5V*
- *Built-in track and hold*
- *Rail-to-rail input range*
- *Latched 3-state output drivers*
- *Microprocessor-compatible control lines*
- *Internal or external clock*

## CDP68HC68A2
## CMOS Serial 10-Bit A/D Converter

**Features:**

- *10-bit resolution*
- *8-bit accuracy*
- *8-bit mode*
- *SPI (Serial Peripheral Interface)*
- *Operates ratiometrically referencing $V_{DD}$ or an external source*
- *100-μs conversion time*
- *8 multiplexed analog input channels*
- *Independent channel select*
- *Multiple modes of operation*
- *On-chip oscillator*
- *Low-power CMOS circuitry*
- *16 pin dual-in-line plastic package*

## CA3162, CA3162A
## A/D Converters

**Features:**

- *Dual-slope A/D conversion*
- *Ultra-stable internal band-gap voltage reference*
- *Capable of reading 99 mV below ground with single supply*
- *Internal timing - no external clock required*
- *Choice of low-speed (4-Hz) or high-speed (96-Hz) conversion rate*
- *"Hold" inhibits conversion but maintains display*
- *Multiplexed operation for high efficiency*
- *Overload indication "EEE" for reading greater than +999 mV, "—" for reading more negative than -99mV when used with the CA3161 BCD-to-7-segment decoder/driver*
- *Multiplexed BCD display*
- *Different at input*
- *Supply voltage operating range: 4.5 to 5.5 volts*

## CA3338, CA3338A
## CMOS Video Speed 8-Bit R-2R Digital-to-Analog Converters

**Features:**

- *CMOS/SOS low power*
- *R-2R output, segmented for low "Glitch"*
- *CMOS or TTL compatible inputs*
- *Fast setting: 20 ns (typ.) to 1/2 LSB*
- *High update rate: 50 MHz (typ.)*
- *Feedthrough latch for clocked or unclocked use*
- *Single or dual supplies, 4.5 to 7.5V total*
- *Unipolar or bipolar operation*
- *1/2 LSB accuracy (typ.)*
- *Data complement control*




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| Type. No. | Description | Type Features | # of Pins |
|---|---|---|---|
| **ANALOG INTERFACE UNIT** | | | |
| CA3247 | TV and CATV Tuning/Interface Control | • Frequency synthesizer for TV and CATV channels (with 4.0 mHz crystal oscillator for reference)<br>• Interfaces to μP & tuner for receiver controls<br>• Circuit to decode remote-control transmissions<br>• On-screen display (OSD) with RGB signal output<br>• 9 D/A converters for analog control functions<br>• PLL control of tuner interface circuits<br>• Three-wire serial bus interface | 40 |
| **DISPLAY DRIVERS**<br>**LED DISPLAY DRIVERS**<br>**Arrays** | | | |
| CA3081 | 7-Transistor Common-Emitter Array | • Permit a wide range of applications in either a common-emitter or common-collector configuration<br>• High $I_C$: 100 mA max<br>• Low $V_{CE(sat)}$ at 50mA: 0.4V typ. | 16 |
| CA3251 | 8-Transistor Common-Emitter Array | | 18 |
| CA3082 | 7-Transistor Common-Emitter Array | | 16 |
| CA3250 | 8-Transistor Common-Emitter Array | | 18 |
| **Decoder/Drivers** | | | |
| CA3161 | BCD-7 Segment Decoder/Driver | • When used with a CA3162 A/D converter, the CA3161 provides a complete digital readout system with a minimum number of external parts<br>• TTL compatible input levels<br>• Pin compatible with other industry standard decoders<br>• Features constant current segment drivers (25mA typ. outputs) | 16 |
| CA3168 | 2-Digit BCD-7 Segment Decoder/ Drivers (For Common-Anode LED displays) | • Intended for 2-digit displays such as "TV" and "CB" channel selection numbers and other 0-99 numerical or counting numbers<br>• Separate BCD inputs and segment outputs for each digit<br>• Each of 8 input terminals draws less than 15μA | 24 |
| **LCD Display Drivers** | | | |
| CD7211<br>CD7211A<br>CD7211M<br>CD7211AM | CMOS Non-Multiplexed, Four-Digit, Seven-Segment Liquid-Crystal Display Decoder/Drivers | • Decode multiplexed binary to hexadecimal (CD7211, CD7211M) and decimal (CD7211A, CD7211AM) outputs<br>• Contains all the circuitry necessary to drive conventional LED displays (no external components necessary)<br>• 6-volt supply-voltage rating<br>• Back-plane signal common to all 4-digit displays | 40 |





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| Type. No. | Description | Type Features | | # of Pins |
|---|---|---|---|---|
| **DISPLAY DRIVERS (Cont'd.)**<br>**Vacuum Fluorescent Display Drivers** | | | | |
| CA3207<br><br>CA3208 | BiMOS Sequencer Driver and Segment Latch Driver For Vacuum Fluorescent Displays | **Sequencer Driver (CA3207)**<br>• Sequentially turns on 1 of 14 characters or 2 of 28 when used with 2 CA3208's<br>• Signal dimming through gates 1 or 2<br>**Latch Driver (CA3208)**<br>• Drives any combination of 14 outputs selected by DATA input<br>• Two or more CA3208's can be interconnected to drive more than 14 characters | | 22 |
| **Relay or Motor Driver Currents** | | | | |
| CA3169 | Solenoid and Motor Driver (1/2 H Driver) | • For driving lamps and other devices that can be changed between 2 states (ON or OFF)<br>• Output short-circuit protection<br>• Thermal overload protection | | 5 |
| CA3219A | Quad-Gated Inverting Power Driver | • For interfacing low-level logic to high-current loads.<br>• Driver outputs capable of switching 600mA without spurious change in output state<br>• Inputs compatible with TTL or 5-volt CMOS logic | • Has fast $t_{PHL}$, $t_{PLH}$ (3$\mu$s typ) | 16 |
| CA3242 | Quad-Gated Inverting Power Driver | | • Has overload protection circuitry | 16 |
| CA3262 | Quad-Gated Inverting Power Driver | | • Has independent over-current limiting on each output and independent over-temperature limiting on each output | 16 |
| CA3252 | Quad-Gated Non-Inverting Power Driver | | • Has input latch with external feedback resistor | 16 |
| **SCHMITT TRIGGER CIRCUITS** | | | | |
| CA3098 | Programmable Schmitt Trigger | • Dual input precision level detector for controlling high operating current (up to 150mA) loads such as thyristors, lamps, relays, etc.<br>• Programmable operating current<br>• Micropower standby dissipation | | 8 |
| **VIDEO LINE DRIVER CIRCUIT** | | | | |
| CA3450 | Video Line Driver, High-Speed Operational Amplifier | • Capable of driving 50-ohm transmission lines and flash A/D converters in video or high-speed instrumentation (accurate) applications with up to 10 MHz bandwidth with a 20 MHz clocking rate<br>• $A_{OL} > 40$ dB at f=5 MHz<br>• SR 330 V/$\mu$s ($A_V \geq 10$ at full load) | | 16 |



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# High-Reliability Products



RCA Solid State is a leading supplier of high-reliability integrated circuits to the military and aerospace community. Years of commitment, dedication, experience, and know-how make possible shipment of hundreds of thousands of quality high-reliability microcircuits annually.

## Military JAN and DESC Product

RCA is committed to provide JAN product as a first option to a customer, where available. The CD4000B series is offered in a number of JAN Class S and Class B MIL-M-38510 slash-sheet types. RCA also offers CD54HC-series parts to DESC specifications. These types are identical to the CD54HC/HCT-series /3A product described later. RCA is in the process of qualifying CD54HC types to the MIL-M-38510/650 series and these types should be available in 1986 and 1987.

## Standard-Product High-Reliability ICs

RCA offers high-reliability versions of virtually its entire line of standard-product integrated circuits from the CD4000 series of CMOS digital logic types, the CD54HC and CD54HCT high-speed CMOS types, the CDP1800 series of microprocessor and associated memory and input/output (I/O) types, and the CA3000 series of bipolar linear types. These integrated circuits are processed and screened to Class B requirements.

RCA also offers high-reliability versions of standard-product types that are processed and screened to special customized specifications, especially for the aerospace user and others who procure types to Class S specifications.

RCA maintains an extensive computer file of customer specifications and has the methodology required to translate these customized specifications into internal RCA standards and factory operating procedures. In addition to the detailed device specifications, the computer file lists the customer specification number, any revision number, and the RCA custom number assigned to a specific device type.

## High-Reliability Custom and Semicustom ICs

RCA has complete custom- and semicustom-circuit capabilities for various CMOS and bipolar integrated-circuit technologies. Custom circuits are offered whenever this approach to integrated-circuit design is determined to be economically feasible. RCA high-reliability custom integrated circuits can be processed and screened to Class S or Class B specifications.

- EPIC 8-bit slice microcomputer family and associated memory (RAM) complement
- Application Specific Integrated Circuit (ASIC) products —
  Automated gate arrays
  Automated standard cells
  Aegis antenna phase array
  Bipolar SPARROW ICs
  COMSEC digital CMOS arrays
  FUSE digital CMOS timing ICs

## Radiation-Hardened High-Reliability ICs

RCA also offers radiation-hardened versions of high-reliability (Class S and Class MS) CD4000-series CMOS integrated circuits. Radiation-hardened types, which are identified by addition of an "R" or "H" suffix to the device type number, are electrically and mechanically identical to their prototype with the exception that they are processed and screened to withstand a total gamma-radiation dosage of $10^5$ rads(Si) for R-suffix types or $10^6$ rads(Si) for H-suffix types. RCA also offers CD4000B-series (H suffix) that are resistant to neutron irradiation and exhibit improved latch-up protection.

RCA also offers a broad line of radiation-hardened integrated circuits that utilize CMOS/SOS technology and provide exceptional tolerance for withstanding transient radiation, total-dose radiation, and single-event-upset (SEU). The device complement includes the EPIC 8-bit-slice microcomputer chip-set family, which contains an 8-bit slice, RAMs, ROMs, controllers, and semicustom gate arrays for customizing computer architecture or emulating existing software. Rad-hard RAMs are available for stand-alone memory systems. These devices are screened to Class S-type specifications.

## Reliability Classes

The purpose of the JAN M38510 program is to achieve standardization among integrated-circuit suppliers and to assure delivery of devices whose long-term life will satisfy the requirements of the system for which they were intended.

Two reliability classes — S and B — are described in MIL-M-38510; the screening classes are performed according to MIL-STD-883, method 5004. Class S devices are of the highest reliability level and are intended for critical applications where replacement of components is not practical.

The Qualification and Quality Conformance Inspection tests delineated in MIL-STD-883 Method 5005 consist of:

**Groups A and B** — device electrical and mechanical construction evaluation tests respectively.

**Groups C and D** — accelerated stress tests that subject devices to stress levels greater than those normally experienced in a typical application.

Group A consists of electrical tests defined by the Device specification. (MIL-STD-883 Method 5005)

Group B (Class B) consists of Package and Internal Mechanical Strength tests. (MIL-STD-883 Method 5005)

Group B (Class S) consists of Package and Internal Mechanical Strength and Long-Term Reliability tests. (MIL-STD-883 Method 5005)

Group C (Class B only) consists of Chip-Related Long-Term Reliability tests. (MIL-STD-883 Method 5005)

Group D consists of Package and Construction Environmental tests. (MIL-STD-883 Method 5005)

Group E Radiation-Hardness Verification Testing. (MIL-STD-883 Method 5005)

Qualification Inspection Tests (QI) are those tests defined by MIL-M-38510 as required for initial qualification of a device or package type to a given reliability class. Quality Conformance Inspection (QCI) Tests are those tests defined by MIL-M-38510 to evaluate production line quality of qualified devices. QCI tests are an on-going inspection





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process performed at periodic intervals defined by MIL-M-38510. QCI testing is the foundation of statistical process evaluation. Electrical end-point test limits are defined by MIL-M-38510 and are more demanding of CMOS than of TTL in areas of quiescent current and input leakage current. DC and AC parameters are measured at -55°C, +25°C and +125°C.

In summary, then, devices are manufactured and tested in accordance with the MIL-M-38510 (detailed and general) specification, which includes methods and procedures of the Military Standard MIL-STD-883.

CMOS integrated circuits are supplied to MIL-M-38510 under a series of /050 and /170 numbers. Detailed ratings and characteristics for these integrated circuits are given in the /050 and /170 detailed electrical specifications. MIL-M-38510 specifications can be obtained from the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA, 19120.

## RCA JAN M38510 CD4000 Series

### RCA JAN Qualified-Parts Listing and MIL-M-38510 Detail Specifications (Slash Sheets) as of May 1985.

| Detail Specification | RCA Type | Available JAN Devices S | B | $1 \times 10^5$ Rad Si |
|---|---|---|---|---|
| MIL-M-38510/5001 | CD4011A | | A | A |
| 02 | CD4012A | | A | A |
| 03 | CD4023A | | A | A |
| 51 | CD4011B | A | A | A |
| 52 | CD4012B | A | A | A |
| 53 | CD4023B | A | A | A |
| MIL-M-38510/5101 | CD4013A | | A | A |
| 02 | CD4027A | | A | I |
| 03 | CD4043A | | | |
| 51 | CD4013B | A | A | A |
| 52 | CD4027B | I | A | I |
| 53 | CD4043B | | | |
| MIL-M-38510/5201 | CD4000A | | A | |
| 02 | CD4001A | | A | A |
| 03 | CD4002A | | A | A |
| 04 | CD4025A | | A | I |
| 51 | CD4000B | | | |
| 52 | CD4001B | A | A | A |
| 53 | CD4002B | A | A | A |
| 54 | CD4025B | I | A | I |
| MIL-M-38510/5301 | CD4007A | | A | I |
| 02 | CD4019A | | A | I |
| 03 | CD4030A | | | |
| 04 | CD4048A | | | |
| 51 | CD4007UB | I | I | I |
| 52 | CD4019B | I | I | I |
| 53 | CD4030B | I | A | A |
| 54 | CD4048B | | | |
| MIL-M-38510/5401 | CD4008A | | | |
| 51 | CD4008B | I | I | I |
| MIL-M-38510/5501 | CD4009A | | | |
| 02 | CD4010A | | | |
| 03 | CD4049A | | A | A |
| 04 | CD4050A | | A | A |
| 05 | CD4041A | | | |
| 51 | CD4009UB | | | |
| 52 | CD4010B | | | |
| 53 | CD4049UB | A | A | A |
| 54 | CD4050B | A | A | A |
| 55 | CD4041UB | I | I | I |
| MIL-M-38510/5601 | CD4017A | | A | I |
| 02 | CD4018A | | | |
| 03 | CD4020A | | A | I |
| 04 | CD4022A | | A | I |
| 05 | CD4024A | | A | I |
| 51 | CD4017B | A | A | A |
| 52 | CD4018B | I | A | I |
| 53 | CD4020B | A | A | A |
| 54 | CD4022B | I | I | I |
| 55 | CD4024B | I | A | I |

| Detail Specification | RCA Type | Available JAN Devices S | B | $1 \times 10^5$ Rad Si |
|---|---|---|---|---|
| MIL-M-38510/5701 | CD4006A | | A | |
| 02 | CD4014A | | A | I |
| 03 | CD4015A | | A | I |
| 04 | CD4021A | | A | I |
| 05 | CD4031A | | A | |
| 06 | CD4034A | | | |
| 51 | CD4006B | | | |
| 52 | CD4014B | I | A | I |
| 53 | CD4015B | I | I | I |
| 54 | CD4021B | I | A | I |
| 55 | CD4031B | | | |
| 56 | CD4034B | | | |
| MIL-M-38510/5801 | CD4016A | | | |
| 02 | CD4066A | | | |
| 51 | CD4016B | | | |
| 52 | CD4066B | I | I | I |
| MIL-M-38510/5901 | CD4028A | | | |
| 51 | CD4028B | I | I | I |
| MIL-M-38510/17001 | CD4081B | A | A | A |
| 02 | CD4082B | A | A | A |
| 03 | CD4073B | A | A | A |
| MIL-M-38510/17101 | CD4071B | A | A | A |
| 02 | CD4072B | A | A | A |
| 03 | CD4075B | A | A | A |
| MIL-M-38510/17201 | CD4085B | A | A | A |
| 02 | CD4086B | A | A | A |
| 03 | CD4070B | A | A | A |
| 04 | CD4077B | A | A | A |
| MIL-M-38510/17301 | CD4514B | | | |
| 02 | CD4515B | | | |
| 03 | CD4532B | | | |
| 04 | CD4555B | | | |
| 05 | CD4556B | | | |
| MIL-M-38510/17401 | CD4069UB | A | A | A |
| 02 | CD40107B | | | |
| 03 | CD4502B | A | A | A |
| 04 | CD40109B | | | |
| MIL-M-38510/17501 | CD4076B | | | |
| 02 | CD4095B | | | |
| 03 | CD4096B | | | |
| 04 | CD4098B | A | A | A |
| 05 | CD40174B | | | |
| MIL-M-38510/17601 | CD4099B | A | A | A |
| 02 | CD4508B | | | |
| MIL-M-38510/17701 | CD4093B | | | |
| 02 | CD40106B | | | |
| MIL-M-38510/17801 | CD4067B | | | |
| 02 | CD4097B | | | |
| 03 | CD40257B | | | |

A = available P = proposed qual. I = in process 1985 (MIL-M-38510 detailed electrical test programs are available.)

For current availability, call your RCA authorized distributor or nearest sales office.

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## High-Reliability CD4000B-Series High-Voltage CMOS ICs

The RCA high-reliability CD4000B series of high-voltage CMOS integrated circuits consists of a broad range of SSI, MSI-1, and MSI-2 (LSI) functions from simple gates to complex counters, registers, and arithmetic circuits. Specific design features for CMOS devices and the performance advantages of CMOS technology — low power consumption, high noise immunity, high speed, high fanout, TTL and DTL logic compatibility, excellent temperature stability, and fully protected inputs and outputs — provide the logic system designer with a capability to achieve outstanding performance, high reliability, and simplified circuitry in a wide variety of equipment designs.

**Features**

- *100% tested for quiescent current at 20V*
- *Maximum input current (leakage) of 1μA at 18V over full package-temperature range; 100 nA at 18V at 25°C*
- *Standardized symmetrical output characteristics*
- *5-V, 10-V, and 15-V parametric ratings*
- *Noise margin (over full package-temperature range): 1V at $V_{DD}$ = 5V, 2V at $V_{DD}$ = 10V, 2.5V at $V_{DD}$ = 15V*
- *Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for description of 'B' Series CMOS Devices"*

### RCA Compliance to MIL-STD-883, Rev. C

RCA provides CD4000-series parts that are in full compliance with MIL-STD-883C, Paragraph 1.2.1. Two different types of product are provided to meet the requirements of this paragraph, Class S and Class B.

**Slash MS (.../MS)** meets Class S requirements when the optional Group B life conformance test is performed.

**Slash 3A (.../3A)** meets Class B requirements.

RCA also provides CD4000-series parts that meet the requirements of MIL-STD-883C, Paragraph 1.2.2. This family of parts has the following designation.

**Slash 3 (.../3)** meets most of the requirements of a Class B part.

## The 54HC/HCT High-Reliability Product Line

The RCA 54HC/HCT series of high-speed CMOS logical integrated circuits include an extensive line of products that are pin compatible with many existing bipolar 54LSTTL and CMOS 4000 series of digital logic types. The new 54HC/HCT IC's provide high-speed CMOS replacements for the most popular LSTTL devices in existing designs and also offer low-power all-CMOS designs for new digital systems. Key family features of the RCA 54HC/HCT types include:

- *Speeds equivalent to LSTTL types with typical gate delays of 10 ns.*
- *Fanout to 10 54-LSTTL loads; 15 loads using Bus Driver 54 types.*
- *Operating frequencies equivalent to LSTTL types, typically 30 MHz.*
- *The high-voltage noise-immunity characteristic of CMOS, typically 45 percent of $V_{CC}$, a two to three times improvement over LSTTL.*
- *Wide range of power supply operating voltages, 2 to 6 volts.*
- *CMOS low static power consumption, typically less than 1 microwatt.*

With the broad line of CMOS MSI-function types currently available, together with performance offered by the RCA 54HC/HCT series of high-speed CMOS integrated circuits, the designer need not sacrifice speed for power consumption. Add the other classical advantages of CMOS, including high noise immunity and wide power-supply and temperature ranges, and the decision to use high-speed CMOS logic is the choice for the 80's. This new family provides for the design of more cost-effective systems to serve high-speed market applications.

The RCA 54HC/HCT high-reliability product line consists primarily of CD54HC-series types, which feature CMOS input-voltage-level compatibility, and CD54HCT-series types, which are input-voltage-level compatible with LSTTL devices. The 54HC/HCT high-reliability line also includes a limited number of single-stage, unbuffered inverter types (CD54HCU-series) for added versatility in oscillator and amplifier applications.

## High-Reliability Slash-Series LSI Products

### 8-Bit CMOS Microprocessor Family

The RCA high-reliability slash-series of CMOS LSI microprocessor, memories, and peripherals are ideally suited for military applications such as mobile ground equipment that must be battery operated and exposed to harsh environments. Use of a highly-reliable, all CMOS LSI technology provides low power operation throughout the military temperature range.

**Features:**

- *Low power consumption*
- *Fully static*
- *Single power supply*
- *Full temperature range*
- *High noise immunity*
- *Complete family which includes RAMs, ROMs, and I/Os*
- *Leadless-chip-carrier packaging option for selected types*
- *Full CMOS CDP1802A microprocessor*





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# Radiation-Hardened CMOS/SOS LSI Devices for Aerospace

RCA offers a complete family of CMOS Silicon-on-Sapphire devices that are specifically designed and hardened for use in aerospace systems that require high tolerance to total-dose, transient, and cosmic radiation single-event-upset. These devices are screened to RCA/1R specifications.

The family consists of RAMs, ROMs, and selected members of the EPIC 8-bit-slice family. Special I/O and support circuits are provided with both gate-array and standard-cell semicustom circuits.

## The EPIC Family

The emulation and programmable IC family formerly known as the GPU chip set, composed of several CMOS/SOS chips, is a high-performance microcomputer "building block" set which can be used to replace existing minicomputers by emulating (adapting) the minicomputers software for a wide variety of new applications with unique architecture, at comparable or increased speed and greatly reduced power.

The EPIC family contains a number of LSI CMOS/SOS chips which, in various combinations, can be configured into microprogrammable computers with great flexibility of architecture, data format, and overall capability. In addition to all the advantages of CMOS technology, the SOS technology offers excellent tolerance to radiation, an important factor in aerospace applications.

The EPIC family centers around an 8-bit slice, two controllers or sequencers, an interrupt controller, an 8 x 8 bit multiplier slice, RAM and ROM, and a number of automated gate arrays that integrate the logic required to join the major system blocks into a minimum parts computer system.

**Currently Available Devices**

| | |
|---|---|
| General Processor | GP001 |
| Emulating Controller | GP501 |
| "2910" Type Controller | GP502 |
| Multiplier (8 x 8) | GP503 |
| Double Address Select Unit | GP514 |
| Double Register Select Unit | GP515 |
| Bus Interface Unit | GP516 |
| Interrupt Control Unit | GP517 |
| Voltage Level Converter and Buffer | GP511 |
| Mask-Programmable ROM (512 x 8) | GP301 |
| Mask-Programmable ROM (256 x 16) | GP302 |
| Mask-Programmable ROM (512 x 16) with Pipeline Register | GP305 |

**Applicable memories: Static CMOS/SOS**

| | |
|---|---|
| RAM (4096 x 1) | CMM5104/1RZ |
| RAM (1024 x 4) | CMM5114/1RZ |
| RAM (16384 x 1) | CMM6167/1RZ |

A system is built around the 8-bit slice GP001 with the GP501 or the GP502 as a sequencer in the control section.

The GP503 and GP517 are stand-alone devices that enhance system performance. The multiplier (GP503) is useful where multiplication in software is too slow.

The level converter GP511 allows interfacing between 5- and 10-volt systems in either direction.

All EPIC parts are available in both radiation-hardened [to 100K rads (Si)] and non-radiation-hardened versions.

## GP001A/1RZ CMOS/SOS 8-Bit General Processor Unit (GPU)

**Features:**

- *Fully static operation to 10 MHz*
- *Full military temperature range operation*
- *16 dual-access 8-bit general-purpose registers*
- *8-bit parallel Arithmetic Logic Circuit (ALC)*
- *Expandable*
- *Separate data input and data output*
- *Tri-state outputs*
- *Pipeline operation*
- *Latch-up free under transient radiation*
- *Resistance to upset under transient radiation rate of up to 1 x $10^{10}$ rads (Si)/sec*

## GP301/1RZ, GP302/1RZ CMOS 4096-Bit Mask-Programmable Static Read-Only Memories

**Features:**

- *Typical, 10-V operation*
- *High-speed access time — typically 60 ns at 10V, 25°C*
- *Metal-mask programmable*
- *Low power — 50 µA typical at 10V, 25°C*
- *Tri-state outputs*
- *Output latch capability*
- *Pipeline operation*

## GP501A/1RZ Emulating Controller

**Features:**

- *Provides efficient implementation of computer control section combining high speed and efficient micro-memory use*
- *13-bit command word*
- *10-bit address generator*
- *Storage registers for bus registers and masks*
- *Latch-up free under transient radiation*
- *Resistance to upset under transient radiation rate of up to 1 x $10^{10}$ rads (Si)/sec*

## GP502B/1RZ Microprogram Sequencer "2910"

**Features:**

- *Typical 10-V operation*
- *Tri-state outputs*
- *12 bits wide — 4096 words of N code*
- *Internal 12-bit loop counter for repeating instructions and counting loop iterations*
- *16 powerful microinstructions*

## GP503/1RZ 8-Bit by 8-Bit Multiplier

**Features:**

- *Typical 10-V operation*
- *8-bit by 8-bit multiplication requiring no additional logic*
- *Expandable to greater bit lengths*
- *Completely asynchronous operation*
- *Input operands may be latched*
- *Typical multiply time: 150 ns for 8 bits at 10V*

GE/Solid State

# High-Reliability Products

## RCA High-Reliability CA3000 Slash-Series Linear ICs

RCA-CAXXXX "Slash" (/) Series types are high-reliability linear integrated circuits intended for applications in aerospace, military, and industrial equipment. These devices are electrically and mechanically identical to the standard types described in commercial databook SSD-240C entitled "Linear Integrated Circuits and MOSFETs", but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microcircuit devices.

Screening levels /1, /3, and /3W are based on guidelines established for military product. Chip versions of the standard product and quality conformance packages are offered on a custom basis only.

Electrical characteristics may be found in RCA data bulletins on specific slash (/) series types. For applications information refer to RCA databooks SSD-240C, "Linear Integrated Circuits and MOSFETs," and SSD-245, "Applications-Linear Integrated Circuits and MOSFETs."

### Radiation Effects on Linear ICs

There is no dedicated process for radiation hardening of the Linear ICs. Gammacell exposure of various devices representing both the bipolar and BiMOS wafer technologies has resulted in information useful for design guidance when considering radiation hardness.

Devices processed under bipolar technologies tend to withstand Gamma radiation to exposure levels of $1 \times 10^5$ rads(Si) prior to experiencing significant parameter degradation, while those processed with BiMOS techniques can withstand Gamma Ray exposure levels up to $1 \times 10^4$ rads(Si) before parameter degradation takes place. RCA does not guarantee rad-hard levels for linear IC's but will conduct rad-hard testing on a custom basis.

## RCA High-Reliability ASIC Capabilities

RCA high-reliability application specific integrated circuits include both gate arrays and standard cells that are processed and screened to MIL-STD-883 modified Class S and B requirements.

RCA has high-reliability capabilities in:

Gate Arrays (Automated)
- PA40000 (3-micron, bulk silicon-gate, CMOS)
- PA50000 (3-micron, double-level metal, silicon-gate, CMOS)
- PA60000 (4-micron, silicon-gate, radiation-hardened, CMOS/SOS)
- CGA10 (2-micron double-level metal, bulk silicon)
- CGA100 (1.5-micron double-level metal, bulk silicon)

Standard-Cell Families
- SC2800 CMOS/SOS (3-micron, silicon-gate, radiation-hardened, CMOS/SOS)
- SC2000 CMOS II (3-micron, bulk silicon-gate, CMOS)
- SC2500 CMOS IID (3-micron, double-level metal, bulk silicon-gate CMOS)
- SC3000 CMOS III (2-micron, double-level metal, bulk silicon-gate CMOS)

Special radiation-hardened ASIC circuits are fabricated using the RCA radiation-hardening CMOS silicon-on-sapphire technology. This CMOS/SOS technology provides exceptional tolerance for withstanding transient radiation, total-dose radiation, and single-event-upset (SEU).

### Radiation-Hardened CMOS/SOS 3-Micron Standard Cell Family

The RCA high-reliability radiation-hardened CMOS silicon-on-sapphire (CMOS/SOS) 3-micron standard-cell family makes possible the design of Application Specific Integrated Circuits (ASICs) capable of withstanding stringent radiation and environmental effects encountered in such demanding applications as strategic missiles and survivable military satellite systems. This CMOS/SOS 3-micron standard-cell family is designed to withstand total dose radiation of up to 100 krads (Si) and can be screened to modified MIL-M-38510, Class S requirements. The CMOS/SOS standard-cell family can also be screened to modified Class B levels for ASIC products required to withstand less demanding conditions, such as battlefield tactical radiation levels and avionic system requirements, at considerably lower cost.

ASICs designed using the radiation-hardened CMOS/SOS standard-cell family operate without upset in transient radiation environments that exceed $10^{10}$ rad (Si)/second. In cosmic-ray (SEU) environments, upset levels less than $10^{-10}$ upsets/bit/day are achieved.

**Features:**
- *Gate Length: 3μm*
- *Gate Oxide Thickness: 500A*
- *Number of Cells: 46 MP2D*
- *Performance, 5-Volt Operation: 2.3 ns at 25°C (Typ.)*
- *Operating Voltage: 4.5 to 6.5 Volts*
- *Interconnect: SLM, $n^+$ polysilicon with 25 ohms/square*
- *Chip Size*
  *Denisty: 6 mil²/Transistor*
  *Gates: 3300 (typ.)*
  *Pads: 132 (typ.)*
  *Area: 320 x 320 mils (typ.)*





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# ISP9210
## 65ns (Commercial)
## 75ns (Military)
## Multiplier/Accumulator

### GENERAL DESCRIPTION

The ISP9210 is a high-speed 16 x 16-Bit Parallel Multiplier/Accumulator which operates at a 65ns clock rate (more than 15MHz Multiply/Accumulate rate). The 2 input registers, x and y, accept 16-bit two's complement or unsigned magnitude operands and produce a 32-bit product, with accumulation up to 35-bits.

To simplify bus interfacing and maximize system throughput, product outputs, x-inputs and y-inputs are individually and independently clocked. The Least Significant Product (the LSP) is multiplexed with the y-inputs, Most Significant Product (MSP), and Extended Product (XTP) are independently tri-stateable. These registers are positive edge-triggered D-type flip-flops.

Individual three-state output ports for the XTP and the MSP are provided. Preloading during tri-state is accomplished through the tri-stated output pins for the MSP and XTP, and through the y-input pins for the LSP. Operation of the Accumulator is controlled by the signals ACC (Accumulate), SUB (Subtract), and PREL (Preload).

The ISP9210 16 x 16-Bit Multiplier/Accumulator is pin and function compatible with the industry standard TDC1010. Depending on the multiply-accumulate rate, the device operates with the same speed at one-sixth or less power dissipation than the bipolar versions. (Worst Case CMOS power consumption decreases with decreasing clock rate).

The ISP9210 can operate as a 16 x 16-Bit Multiplier only as well as a 16 x 16-Bit Multiplier/Accumulator.

### FEATURES

- Low-Power CMOS
- 65ns Multiply/Accumulate Time
- 16 x 16-Bit Parallel Multiplication/Accumulation to 35-Bits
- Selectable Accumulate, Subtract, Round, and Preload of Accumulator
- Fully TTL Compatible I/O
- Three-State Outputs
- Two's Complement or Unsigned Magnitude Arithmetic
- 64-Lead DIP, 68-Pin PLCC
- Pin Compatible with Industry Standard MACs/Multipliers
- Full Mil Screening Available

### APPLICATIONS

- Radar/Sonar Signal Processors
- Array Processors
- Video Processors
- FFT Processors
- Beam Formers
- Image Processors
- FIR Filters

### ORDERING INFORMATION

| PART NUMBER | CLOCK SPEED | TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|
| ISP9210CP64<br>ISP9210CN68 | 65ns | 0°C to +70°C<br>0°C to +70°C | 64-Pin DIP<br>68-Lead PLCC |
| ISP9210ID64 | 70ns | -40°C to +85°C | 64-Pin DIP, Ceramic |
| ISP9210MD64 | 75ns | -55°C to +125°C | 64-Pin DIP, Ceramic |

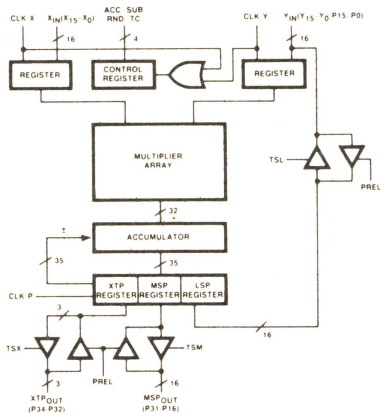


Figure 1: Functional Diagram

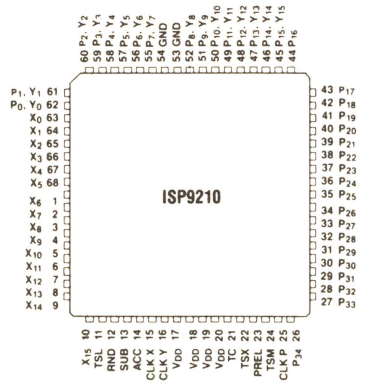


Figure 2: Pin Configuration

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*NOTE: All typical values have been characterized but are not tested.*

601105-002
September 1987



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# ISP9216
## 16 x 16-Bit Multiplier

### GENERAL DESCRIPTION

The ISP9216 is a high-speed 16 x 16-Bit Parallel Multiplier which is capable of multiplying 2 input operands in 48ns, (worst case, commercial temp.).

The x-input, y-input, and most significant and least significant product outputs are independently clocked into separate registers by the rising edge of the CLKX, CLKY, CLKM, and CLKL signals, respectively. The Least Significant Product (LSP) is multiplexed with the y-input, or can be multiplexed with the Most Significant Product (MSP) through the MSP outputs (e.g., for use with a 16-bit data bus) by utilizing the MSPSEL signal.

The output registers can be made transparent by the Feed Through (FT) signal, although the fully clocked implementation will be capable of higher throughput. The format adjust, FA, causes a right shift of the MSP and deletes the MSB of the LSP, i.e., the sign bit of the LSP. The device is available in a 64-Pin DIP and 68-Contact PLCC.

### FEATURES

- Low-Power CMOS
- Fully TTL Compatible I/O
- Three-State Outputs
- Two's Complement or Unsigned Magnitude Arithmetic
- 64-Lead DIP, 68-Pin PLCC
- Pin Compatible with Industry Standard MACs/ Multipliers
- Full Mil Screening Available

### APPLICATIONS

- Radar/Sonar Signal Processors
- Array Processors
- Video Processors
- FFT Processors
- Beam Formers
- Image Processors
- FIR Filters

### ORDERING INFORMATION

| PART NUMBER | CLOCK SPEED | TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|
| ISP9216CP64<br>ISP9216CN68 | 65ns | 0°C to +70°C<br>0°C to +70°C | 64-Pin DIP<br>68-Lead PLCC |
| ISP9216ID64 | 70ns | −40°C to +85°C | 64-Pin DIP, Ceramic |
| ISP9216MD64 | 75ns | −55°C to +125°C | 64-Pin DIP, Ceramic |

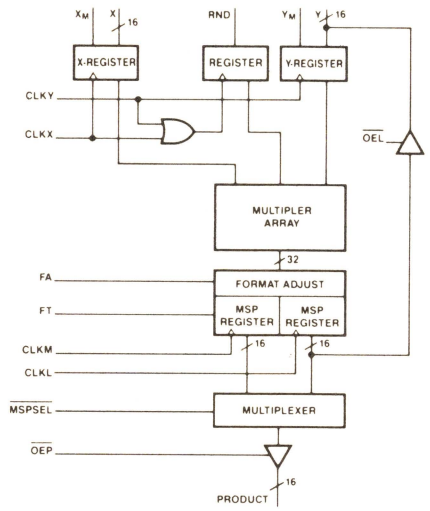


**Figure 1: Functional Diagram**



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601120-001
September 1987

GE Solid State

INTEGRATED SIGNAL PROCESSING

# ISP9128
## Finite Impulse Response Filter Controller

### GENERAL DESCRIPTION

The 16-bit FIR Filter Controller (FFC) provides all the data history, storage and programmable filter cycle control logic required to implement FIR filters of up to 128 filter points. When used in conjunction with an external filter coefficient memory, of up to 128 words by 16-bits, and an industry standard 16-bit Multiplier-Accumulator (MAC), the FFC provides the system designer with the ability to implement a powerful FIR filter with only three ICs. The FFC provides all the control signals required to operate the MAC and the coefficient memory as tri-stateable devices, allowing multiplexed usage of these resources. The FFC's asynchronous interface enables easy integration of the FIR filter in any system environment. It incorporates a 16-bit data I/O path, a 128 word by 16-bit RAM memory, and programmable filter control logic capable of handling filter order lengths of up to 128 points.

### FEATURES

- FIR Filter Building Block
- 128 Tap Filter at 100kHz Sample Rate
- Filter Orders from 1 to 128 Taps
- 128 Words by 16-Bit Data Memory
- Works with ISP9210 Multiplier-Accumulator (MAC) or Equivalent
- 80nS Per Tap Data Rate
- Low-Power CMOS Technology
- Full TTL Compatibility
- 68-Pin PLCC and 64-Pin DIP

### ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| ISP9128CP64 | 0°C to 70°C | 64-Pin Dip |
| ISP9128CN68 | 0°C to 70°C | 68-Lead PLCC |
| ISP9128ID64 | −40°C to 85°C | 64-Pin Ceramic |
| ISP9128MD64 | −55°C to +125°C | 64-Pin Dip Ceramic |

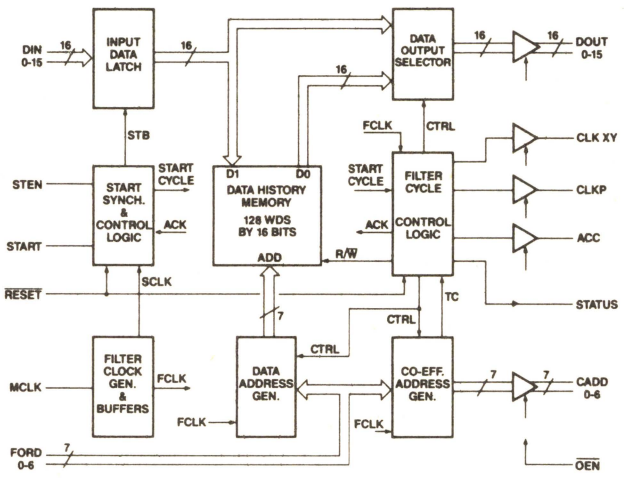


Figure 1: Functional Diagram

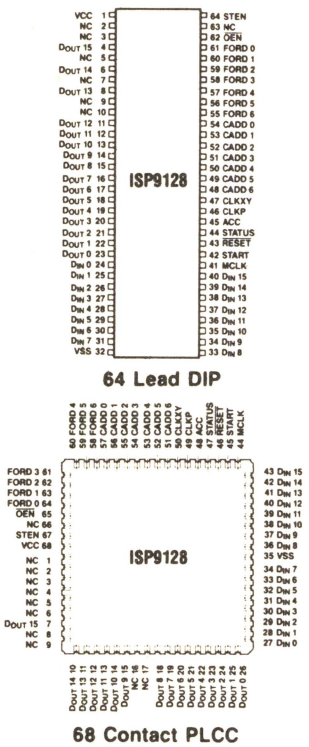


Figure 2: Pin Configurations

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601100-004
September 1987

# ISP9520/1
## Bytewide Multi-level Pipeline Register

### GENERAL DESCRIPTION

The Intersil ISP9520 and ISP9521 Bytewide Multi-level Pipeline Registers are pin-for-pin compatible with the AMD Am29520/1. Implemented in 1.5$\mu$ CMOS, the ISP9520/1 contain four registers which can be configured as two independent two-level pipelines or as one four-level pipeline. The configuration implemented is determined by the instruction code control inputs ($I_1$,$I_0$). The register selected for output is determined by the multiplexer select control inputs ($S_1$,$S_0$). The 8-bit three-state output is controlled by the level of the $\overline{OE}$ input. The registers may be written to and read from simultaneously due to the independence of the I and S control lines. The two ICs differ in the treatment of existing data in the first register level. The ISP9520 allows for the shifting of data to the next level, whereas the ISP9521 causes the data in the first level to be overwritten.

### FEATURES

- Four 8-Bit Registers
- Implements Double 2-Stage Pipeline or 4-Stage Pipeline Register
- Three-State Outputs
- Fully TTL Compatible
- High-Speed, Low-Power CMOS Technology
- 24-Pin 300-Mil Package: Plastic and Cerdip
- Hold, Transfer and Load Instructions
- $t_{PD}$ (Clock to Output) = 22ns
- $I_{DD}$ (Supply Current) = 12mA

### APPLICATIONS

- Array Processor
- Digital Signal Processor
- Bytewide Shift Register
- A/D Buffer
- Telecommunication

### ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| ISP9520CPX<br>ISP9521CPX | 0°C to 70°C | 24-Pin Dip |
| ISP9520IJX<br>ISP9521IJX | −40°C to +85°C | 24-Pin Cerdip |
| ISP9520MDX<br>ISP9521MDX | −55°C to 125°C | 24-Pin Side Braze |

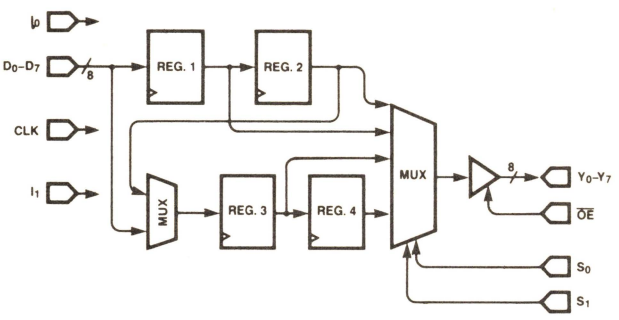


Figure 1: Functional Diagram

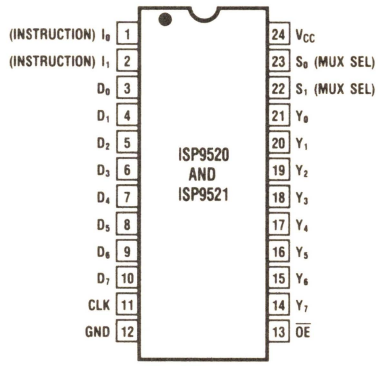


Figure 2: Pin Configuration

INTERSIL PRODUCTS

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601115-001
September 1987

*NOTE: All typical values have been characterized but are not tested.*

# ISP9326
## 32-Bit Floating-Point MAC

### GENERAL DESCRIPTION

The ISP9326 is a high-speed floating-point processor unit. It performs 32-bit single-precision floating-point addition, subtraction, and multiplication operations in a single CMOS VLSI integrated circuit using the format specified by the proposed IEEE floating-point standard P754. The DEC single-precision floating-point format is also supported. Conversion between IEEE and DEC formats are provided as are 32-bit integer format to floating-point formats. All operations can be performed in a single clock cycle.

Six flags monitor the status of operations: Invalid, Not-A-Number (NAN), Inexact, Zero, Overflow, and Underflow.

Three bus configurations are user selectable. A 3-bus, 32-bit architecture with two 32-bit inputs, and a single 32-bit output provides high I/O bandwidth, and access to all buses. All buses are registered, with each register provided with an enable control pin. Alternatively, the ISP9326 can be configured as a 16-bit, 3-bus or a 32-bit, 2-bus architecture, easing interface to a wide variety of systems.

Internal 32-bit data paths and registers support single cycle Multiply and Accumulate operations, effectively doubling the throughput when compared to devices that support only one floating-point operation per cycle.

Fabricated with the Intersil Advanced 1.25$\mu$ VLSI CMOS technology, the ISP9326 is powered from a single 5-volt supply and packaged in a 144-pin PGA.

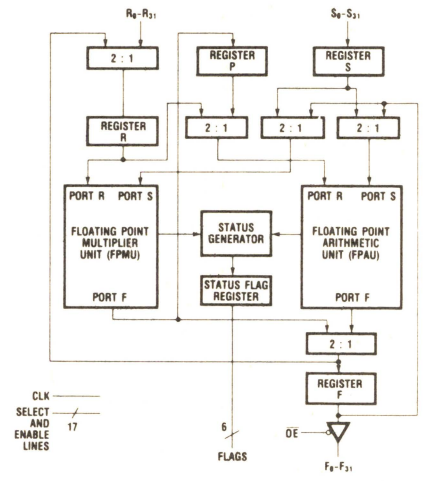


**Figure 1: Functional Diagram**

### FEATURES

- **Single VLSI Device Performs High-Speed Floating-Point Addition, Subtraction, and Multiplication**
- **IEEE and DEC Formats. Performs Conversion Between Both Formats, and Conversion Between Floating-Point and 2's Complement**
- **Supports Single Cycle MAC Operation**
- **All Operations Complete Within Single 150nS Cycle**
- **32-Bit, 3-Bus Flow Through Architecture**
- **Programmable I/O for 16 or 32-Bit Bus Interface**
- **Inputs and Outputs Registered, Can Independently Be Made Transparent, or Enabled Independently**
- **Six Flags Indicate Status of Operations**
- **Superset of AM29325**
- **Low-Power CMOS Device**

### APPLICATIONS

- **Radar/Sonar Signal Processors**
- **FFT Processors**
- **General Purpose Digital Signal Processors**
- **Image Processors**

### ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | CYCLE TIME | PACKAGE |
|---|---|---|---|
| Commercial: ISP9326CG144D150 | 0°C to +70°C | 150nS | 144 PGA |
| Industrial: ISP9326IG144D175 | −40°C to +85°C | 175nS | 144 PGA |
| Military: ISP9326MG144D200 | −55°C to +125°C | 200nS | 144 PGA |

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601108-001
September 1987



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# EVK-128
## Data Conversion and FIR Filtering System

## GENERAL DESCRIPTION

The Intersil EVK-128 provides a moderate speed data acquisition, conversion, and digital filtering system for the IBM PC and most compatibles. Consisting of a board which plugs into and occupies a single slot on the PC, the card digitally filters data with a filter length of 0 (unfiltered) to 128 taps, utilizing the Intersil IM29C128 Finite Impulse Response Filter Controller (FFC) and 29C510 16 bit Multiplier-Accumulator (MAC). Throughput is a function of required filter length, with an 80 nS per tap processing rate.

The ICL7115 converts analog signals to 14 bit words at up to 32.727 KHz rate, while the ICL7121 converts a 16 bit digital data stream to analog. Edge mounted connectors allow simple analog I/O. The A/D and/or D/A converters may be bypassed for processing of digital data, input or output via externally accessible edge mounted connectors or the PC bus. This also allows nonreal time processing or storage of data to or from a disk, for example.

Also included is a floppy disk with an easy-to-use menu driven FIR filter design program for the PC, including coefficient calculations, time and frequency calculations and plotting capabilities, and prompts for controlling the different modes of operation of the board. The package contains complete documentation, including detailed schematics, printed circuit layout, parts list, timing diagrams, and applications literature. The user may copy any of this for his own system design, if desired.

## FEATURES

- **Occupies Single IBM PC Slot**
- **On Board 14 Bit ICL7115 A/D Converter**
- **On Board 16 Bit ICL7121 D/A Converter**
- **All Necessary Software Provided**
- **Digital Filters of 1 to 128 Taps**
- **Versatile I/O Options**
- **On Board Digital Noise Generator**
- **Complete Documentation Package**
- **Fully Tested, Ready to Plug In and Use**
- **S/N > 84 dB**

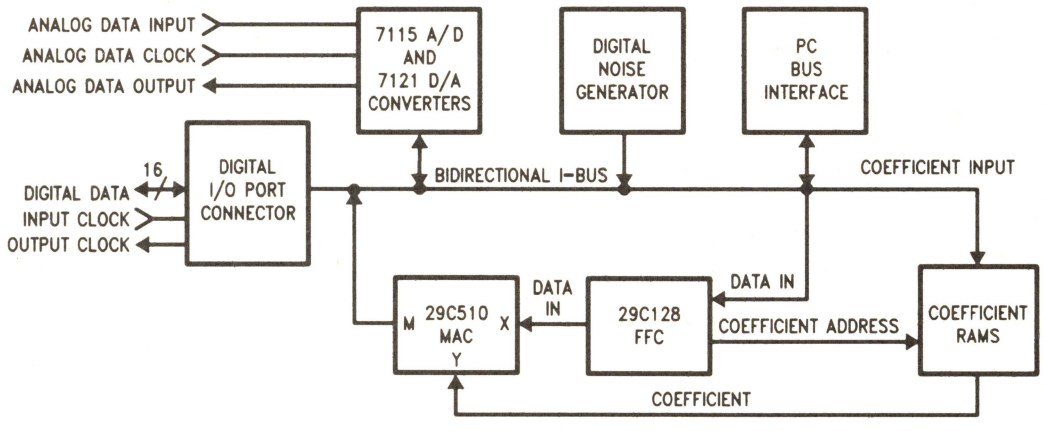


**Figure 1: Functional Diagram**

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B60109

601120-002
March 1987

## DATA ACQUISITION CIRCUITS

The proliferation of microprocessors and the general swing to digital signal processing has caused an explosion in the need for data acquisition products. In turn, the associated data translation requirements from the analog world to digital format, and vice versa, have spurred considerable effort toward making A/D-D/A converters progressively smaller, cheaper, and more reliable. Toward that end, Intersil has developed a family of integrated circuits designed to meet the varying requirements of the system designer.

All of Intersil's converters are fabricated using CMOS technology, which equates, inherently, to extremely low power consumption. All maximize on-chip componentry for the intended application in order to reduce the external component requirements to a minimum.

To facilitate acquaintance with Intersil products, a number of A/D converters are available in the form of low-cost Evaluation Kits. The Kits combine the specified converter with a number of additional components required to assemble a functional subsystem. They include components PC board and appropriate assembly instructions.

### Content:

A/D Converter Systems
- Digital Multimeter
- Instrumentation
- Bargraph

A/D Converters
- Display Type
- μP Type
- Evaluation Kits

D/A Converters

## Analog To Digital Converters

### A/D Converters with Display Drivers

Integrating A/D Converters are characterized by high inherent accuracy, excellent noise rejection, non-critical associated components and low cost. They are relatively slow with conversion rates up to 30 conversions per second. All Intersil integrating converters provide fully precise Auto-Zero, Auto-Polarity (including ± null indication), single reference operation, very high input impedance, true input integration over a constant period (for maximum EMI rejection), fully ratiometric operation, overrange indication and a medium-quality built-in reference.

**3¾ Digit LCD**
**7-Segment Displays** **ICL7139**
**For Low-Cost Autoranging Digital Multimeters** **ICL7149**

These monolithic autoranging multimeter circuits always display the results of a conversion on the correct range. Measure AC and DC voltage, DC current and resistance in the following ranges:

DC Voltage — 400mV, 4V, 40V, 400V
AC Voltage — 400V (ICL7139)
(Optional ac circuit with 2 ranges (ICL7149))
DC Current — 4mA, 40mA, 400mA, 4A
Resistance — 4K, 40K, 400K, 4M

On-chip duplex display drive includes three decimal points and 11 annunciators. Less than 20mW power dissipation provides 1000 hours typical battery life. Continuity output drives piezoelectric beeper. Guaranteed zero reading for 0 Volts input on all ranges.

**101-Segment LCD Bargraph**
**A-D Converter** **ICL7182**

The ICL7182 is a complete analog-to-digital converter that directly drives a multiplexed liquid crystal display. Included are a charge-balance A/D converter, a 2.56V bandgap reference, display decode and driver, and a 50KHz oscillator. A complete analog bargraph generator requires only the addition of an external display, two passive components and a 350μA, 5V power source.

**4½ Digit LCD**
**7-Segment Displays** **ICL7129**
**For High Quality Battery Operated Instruments**

Very high performance A/D Converter for direct drive of multiplexed LCDs. Ideal for high-resolution, hand-held digital multimeters and other battery powered (9V) instruments. Accuracy is better than 0.005% of full scale, with resolution down to 10μV per count. Overrange and underrange outputs permit design of autoranging instruments with 10:1 range changing input. Instant continuity check gives both visual indication and a logic-level output for enabling an external audible transducer. Provisions for detection and indication of Low Battery condition.

**For 3½ Digit LCD/LED** **ICL7106/7116, ICL7135/7126**
**7-Segment Displays** **ICL7137-7107, ICL7117**

These 3½-digit A/D Converters contain all the necessary active devices on a single CMOS integrated circuit. Included are A/D Converters, 7-segment decoders, display drivers, a reference and a clock. All feature auto-zero to less than 10μV, zero-input drift of less than 1μV/°C, input bias current of 10pA max., and rollover and linearity errors of less than one count. True differential inputs and reference provide wide applications versatility over a temperature range from 0 to +70°C.

| | |
|---|---|
| **For Liquid Crystal Displays** | **ICL7106** — Direct drive; 0.1 to 15 conversions per second; supply current = 1.8mA max.<br>**ICL7116** — Similar to above, but features a Hold Reading input which allows indefinite retention of a display reading<br>**ICL7136** — Low-power version of ICL7106, but with maximum supply current of only 100μA gives 8000 hours typical 9V battery life. 0.1 to 4 conversions per second.<br>**ICL7126** — Earlier version of ICL7136. Recommended for exact replacement requirement only. |
| **For LED Displays** | **ICL7137** — Low-power, direct drive ADC for common-anode, 7-segment LED displays. Requires positive and negative 5V supply voltages, with supply current of less than 200μA. 0.1 to 4 conversions per second.<br>**ICL7107** — Earlier version of ICL7137. Recommended for exact replacement requirements only.<br>**ICL7117** — Similar to ICL7137, but requires 1.8mA (max.) of supply current and provides up to 15 conversions per second. Hold Reading allows indefinite retention of display reading. |

INTERSIL PRODUCTS


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# μP Compatible A/D Converters

## Integrating

Intersil integrating μP-Compatible A/D Converters contain both monolithic versions and 2-chip sets, with up to 16-bit resolution. All utilize CMOS processing for lowest power consumption, and all have a guaranteed accuracy of 1 count.

**4½ Digit A/D Converter with Multiplexed BCD Output** — **ICL7135**

This precision A/D Converter is suitable for display applications as well as microprocessor and UART interface. Count accuracy of ±1 in 20,000 makes it ideal for the visual display DVM/DPM market, while added functions such as Strobe, Run/Hold, Busy, Overrange and Underrange allow operation in more sophisticated systems. Chip contains all necessary active devices except display drivers, reference and clock. All outputs are TTL compatible.

**12-Bit μP-Compatible A/D Converter** — **ICL7109**

This monolithic 12-bit binary A/D converter may be directly accessed under control of two byte-Enable inputs, and a Chip Select input, for a simple parallel-bus interface. A UART handshake mode operates in conjunction with industry-standard UARTs to provide serial data transmission. Operates at up to 30 conversions per second. Available in three temperature ranges: −55°C to +125°C, −25°C to +85°C, and 0°C to +70°C.

**14/16-Bit μP-Compatible Two-Chip A/D Converter Sets** — **ICL8052/ICL7104, ICL8068/ICL7104**

Available with 14-bit and 16-bit resolution, this two-chip set performs the analog signal processing on one chip (ICL8052 or ICL8068) and the switching and digital functions on the other (ICL7104). A combination of chips may be ordered for either 14-bit or 16-bit operation and for low-noise or low-leakage alternatives. All combinations, however, offer three-state, latched, binary outputs plus Polarity and Overrange. All combinations operate over a temperature range of 0°C to +70°C.

**ICL7104-14** 14-Bit DC Converters
**ICL7104-16** 16-Bit DC Converters
**ICL8052** Low input leakage current (30pA max.) analog processing circuit. Typical noise = 30μV.
**ICL8068** — Low noise (2μV typical) analog processing circuit. Input leakage current = 165pA.

## Successive Approximation

Successive Approximation Converters are generally associated with high speed, ranging up to 100,000 conversions per second. All Intersil Successive Approximation Converters are μP compatible.

**8-Bit A/D Converters for 8080A MPU Interface** — **ADC0802, ADC0803, ADC0804**

This Successive Approximation A/D Converter was designed to operate with the 8080A or Z-80 microprocessor control bus via three-state outputs with no additional interfacing requirements, but permits easy interface to most other microprocessors. Differential analog input range is 0 to 5V with a single +5V supply. With a conversion time of less than 100 μs, it provides up to 8888 conversions per second with a clock frequency of 640KHz.

**ADC0802** Total unadjusted error = ± 1/2LSB
**ADC0803** Total full-scale adjust error = ± 1/2LSB
**ADC0804** Total unadjusted error = ± 1LSB

**14-Bit High-Speed A/D Converter** — **ICL7115**

With a conversion speed of 40μs (max), this 12-bit ADC has a byte organized digital output for bus interface to 8 and 16-bit microprocessor systems. CMOS circuitry, thin-film resistors and an on-chip PROM calibration table combine to achieve 14-bit linearity (without laser trimming) and a very low (60mW) power performance dissipation. Available in three temperature ranges: 0°C to +70°C, −25°C to +85°C, and −55°C to +125°C.





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## Digital to Analog Converters

Intersil supplies digital-to-analog converters (D/A converters) with 8-bit, 10-bit, 12-bit, 14-bit and 16-bit resolution. All are four-quadrant multiplying D/A converters using thin-film resistors and CMOS circuitry for high accuracy and low power dissipation. All are microcomputer compatible, with input protection against damage from electrostatic discharge.

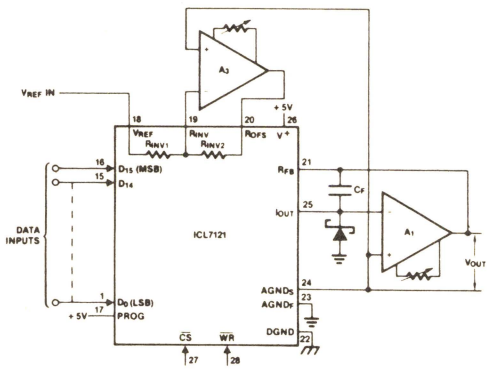
| Type | Digital Input Format | Settling Time (To 0.05% FS) | Output Current (Max) | Non Linearity% FS (Suffix) | Gain Error (% FS) | Gain Linearity Tempo PPM/°C | Power Supply $\frac{V_{(Typ)}}{I(Max)}$ |
|---|---|---|---|---|---|---|---|
| **8-BIT** | | | | | | | |
| AD7523 | Binary/ Offset Binary | 200 ns (Max) | $\frac{\pm V_{REF}}{10K\Omega}$ A | 0.2% (J)<br>0.1% (K)<br>0.05% (L) | 1.5% (Max) | 10<br>2 | $\frac{+15V}{100\mu A}$ |
| **10-BIT** | | | | | | | |
| AD7520*<br>AD7530 | Binary/ Offset Binary | 500 ns (Typ) | $\frac{\pm V_{REF}}{10K\Omega}$ A | 0.2% (J)<br>0.1% (K)<br>0.05% (L) | 0.3% (Max) | 10<br>2 | $\frac{+15V}{2mA}$ |
| AD7533 | Binary/ Offset Binary | 600 ns (Typ) | $\frac{\pm V_{REF}}{10K\Omega}$ A | 0.2% (J)<br>0.1% (K)<br>0.05% (L) | 1.4% (Max) | 10<br>2 | $\frac{+15V}{2mA}$ |
| **12-BIT** | | | | | | | |
| AD7521*<br>AD7531 | Binary/ Offset Binary | 500 ns (Typ) | $\frac{\pm V_{REF}}{10K\Omega}$ A | 0.2% (J)<br>0.1% (K)<br>0.05% (L) | 0.3% (Typ) | 10<br>2 | $\frac{+15V}{2mA}$ |
| AD7541 | Binary/ Offset Binary | 1 μs (Max) | $\frac{\pm V_{REF}}{10K\Omega}$ A | 0.02% (J)<br>0.01% (K)<br>0.01% (L) | 0.3% (Max) | —<br>2 | $\frac{+15V}{2mA}$ |
| **14-BIT** | | | | | | | |
| ICL7134 | Binary μ 2's Complement B | 3 μs (Max) | $\frac{\pm V_{REF}}{10K\Omega}$ A | 0.1% (J)<br>0.006% (K)<br>0.003% (L) | 0.02% (J)<br>0.012% (K)<br>0.006% (L) | 5<br>1 | $\frac{+15V}{0.5mA}$ |

*AD7530 and AD7531 are identical to AD7520 and AD7521, respectively, except for output leakage current and feed-through specifications.

### ICL7121
### 16-Bit μP-Compatible D/A Converter

This high-performance 16-bit D/A converter achieves 0.003% linearity without laser trimming by combining the converter with a unique on-chip PROM-controlled correction circuit. This insures long-term stability and accuracy even over the full military temperature range. Silicon-gate CMOS circuitry keeps the power dissipation to a very low 25 mW.

Designed and programmed for bipolar operation, it can be connected to provide a true 2's complement input transfer function without any external resistors. Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. The device is available in a 28-pin CERDIP package in both 0°C to +70°C, and −55°C to +125°C temperature ranges.




**ICL7121 Example of Bipolar, Four Quadrant Operation**

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## TIMER/COUNTERS

Available with and without on-board display drivers, Intersil's broad range of Timer/Counters circuits serves a wide variety of control functions. For separate Display Driver circuits, see separate section.

### Timer/Counters With Display Drivers

| TYPE | DISPLAY: LED: Common Anode, Non-MUX | DISPLAY: LED: Common Cathode, MUX | DISPLAY: LED: Common Anode, MUX | DISPLAY: LCD: Direct Drive, Non-MUX | DISPLAY: VF: Non-MUX | FUNCTIONS: UNIT COUNT: Up/Down | FUNCTIONS: UNIT COUNT: Up Only | FUNCTIONS: UNIT COUNT: Decade | FUNCTIONS: UNIT COUNT: Modulo 60 (Hr/Min/Sec) | FUNCTIONS: UNIVERSAL COUNTERS: Frequency | FUNCTIONS: UNIVERSAL COUNTERS: Period | FUNCTIONS: UNIVERSAL COUNTERS: Frequency Ratio | FUNCTIONS: UNIVERSAL COUNTERS: Time Interval | FUNCTIONS: MUX BCD Outputs | FUNCTIONS: Display Latch | FUNCTIONS: Display Blanking | FUNCTIONS: Count Enable | FUNCTIONS: Leading Zero Blanking | FUNCTIONS: Preset Count | FUNCTIONS: Comparison Register | FUNCTIONS: Equal and Zero Output | MAX COUNT SPEED (MHz) | Evaluation Kit Available | TYPICAL APPLICATIONS AND COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **4 DIGIT** | | | | | | | | | | | | | | | | | | | | | | | | | |
| ICM7217 | | | ● | | | ● | | ● | | ■ | | | | ● | ● | ● | | ● | ● | ● | ● | 2 | | Industrial control: preset/predetermining counters, sequencers, on/off delay timers, batch counters. Presets and loads compare register from thumbwheel switches. |
| ICM7217A | | ● | | | | ● | | ● | | ■ | | | | ● | ● | ● | | ● | ● | ● | ● | 2 | | |
| ICM7217B | | | ● | | | ● | | | ● | | | | | ● | ● | ● | | ● | ● | ● | ● | 2 | | |
| ICM7217C | | ● | | | | ● | | | ● | | | | | ● | ● | ● | | ● | ● | ● | ● | 2 | | |
| ICM7227 | | | ● | | | ● | | ● | | | | | | ● | ● | ● | | ● | ● | ● | ● | 2 | | Microprocessor compatible interface. Industrial control; preset/predetermining counters, sequencers, on/off delay timers, batch counters. Presets and loads compare register from a microprocessor. |
| ICM7227A | | ● | | | | ● | | ● | | | | | | ● | ● | ● | | ● | ● | ● | ● | 2 | | |
| ICM7227B | | | ● | | | ● | | | ● | | | | | ● | ● | ● | | ● | ● | ● | ● | 2 | | |
| ICM7227C | | ● | | | | ● | | | ● | | | | | ● | ● | ● | | ● | ● | ● | ● | 2 | | |
| **4½ DIGIT** | | | | | | | | | | | | | | | | | | | | | | | | | |
| ICM7224 | | | | ● | | | ● | ● | | ■ | | | | | ● | | ● | ● | | | | 15 | ● | 10 μA operating current. Can be cascaded for more digits. |
| ICM7224A | | | | ● | | | ● | | ● | | | | | | ● | | ● | ● | | | | 15 | | |
| ICM7225 | ● | | | | | | ● | ● | | ■ | | | | | ● | ● | ● | ● | | | | 15 | ● | Has brightness adjustment, 10 μA current with display blanked, cascadable. |
| ICM7225A | ● | | | | | | ● | | ● | | | | | | ● | ● | ● | ● | | | | 15 | | |
| **5½ DIGIT** | | | | | | | | | | | | | | | | | | | | | | | | | |
| ICM7249 | | | | ● | | | ● | ● | | | | | ● | | | | | | ● | | | | | Event timer/counter, hour meter. 14 programmable modes. Selectable input filtering. |
| **6 DIGIT** | | | | | | | | | | | | | | | | | | | | | | | | | |
| ICM7215 | | ● | | | | | ● | | ● | | | | ● | | | ● | ● | | | | | | | 4 functions: start/stop/reset, split, taylor, time out. 1/100's seconds and low battery. |
| **7 DIGIT** | | | | | | | | | | | | | | | | | | | | | | | | | |
| ICM7208 | | ● | | | | | ● | ● | | ■ | | | | | ● | ● | ● | ● | | | | 2.5 | | Use with ICM7207/A for a 7-digit frequency counter. |
| **8 DIGIT** | | | | | | | | | | | | | | | | | | | | | | | | | |
| ICM7216A | | | ● | | | | ● | ● | | ● | ● | ● | ● | | ● | ● | | ● | | | | 10 | | Universal frequency counter with display drivers. 4 internal gate times, auto decimal point, leading zero blanking, overflow indication. Display off, hold, and reset inputs. |
| ICM7216B | | ● | | | | | ● | ● | | ● | ● | ● | ● | | ● | ● | | ● | | | | 10 | | |
| ICM7216C | | | ● | | | | ● | ● | | ● | | | | | ● | ● | | ● | | | | 10 | | |
| ICM7216D | | ● | | | | | ● | ● | | ● | | | | | ● | ● | | ● | | | | 10 | | |
| ICM7226A | | | ● | | | | ● | ● | | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | 10 | ● | Same as ICM7216 plus period and time interval averaging, BDC outputs, μP PIA compatible. |
| ICM7226B | | ● | | | | | ● | ● | | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | 10 | | |

■ These counters will measure frequency when used with the ICM7207 (0.01 and 0.1 second timebase) or the ICM7207A (0.1 and 1.0 second timebase)





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## Timers/Counters Without Display Drivers

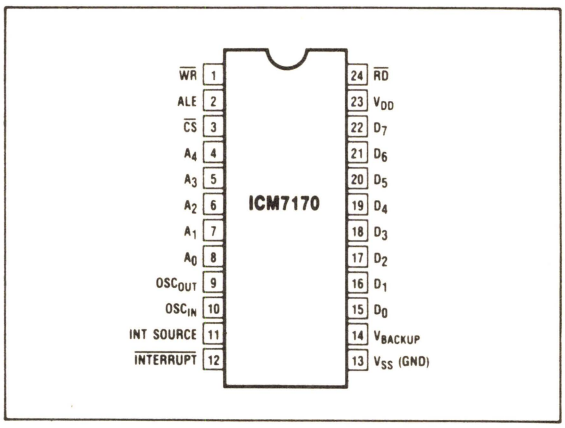
| Type | Special Features | Description |
|---|---|---|
| ICM7555 | | Low power CMOS equivalent of industry standard 555 timer—only 80 μA (max) supply current. ICM7555 does not have the large supply current transients of the bipolar 555 and does not require the large bypassing capacitors needed by the 555. Low leakage threshold and trigger inputs allow use of higher impedance RC timing components for extra long time delays. |
| ICM7556 | | An ICM7556 is a dual ICM7555, a CMOS, low power equivalent of the Bipolar 556 Timer. |
| ICM7240<br>ICM7250 | Binary 0–225<br>BCD 0–99 | Programmable CMOS counter/timer. Uses on-board RC oscillator or an external clock. The count is programmed by wire-AND connection of the outputs. Excellent for ON/OFF delay timers, ÷N counters, and long period delays. |
| ICM7242 | Fixed 128/255 | RC oscillator + 8-bit counter, similar to ICM7240 but with fixed 256 count. Used for extremely long time delays. Cascadable. |

## Oscillator/Divider Selector Guide

| Type | Output Frequency | Supply Voltage (V) | Typical Current (μA) | Pulse Width (ms) | Crystal Frequency | Other Outputs/Comments |
|---|---|---|---|---|---|---|
| ICM7213 | 1 Pulse/Min | 2–4 | 100 | 125, 1000 | 4.19 MHz | 1 Pulse/Sec., 2048, 1024, 34.133, 16 Hz |
| | 1 Hz | 2–4 | 100 | 7.8 | 4.19 MHz | 1 Pulse/Min., 2048, 1024, 34.133, 16 Hz |
| | 16 Hz | 2–4 | 100 | Sq. Wave | 4.19 MHz | 1 Pulse/Min., 2048, 1024, 34.133, 1 Hz |
| | 1000 Hz<br>1024 Hz | 2–4<br>2–4 | 100<br>100 | Sq. Wave<br>Sq. Wave | 4.096 MHz<br>4.19 MHz | 2000, 2000 Pulses/Min.<br>1 Pulse/Min., 2048, 34.133, 16, 1 Hz |
| | 2048 Hz | 2–4 | 100 | Sq. Wave | 4.19 MHz | 1 Pulse/Min., 1024, 34.133, 16, 1 Hz |
| ICM7209 | 250 kHz–10 MHz | 4.5–5.5 | 11,000 | Sq. Wave | 1–10 MHz | Two buffered outputs — Crystal Frequency and ÷ 8 output. Drives up to 5 TTL loads. |

### ICM7170
### μP-Compatible
### Real-Time Clock, CMOS

This real-time clock circuit is set or read by accessing eight internal separately addressable and programmable counters from 1/100 seconds to 99 years. An 8-bit bidirectional bus is used for the data I/O circuitry. Access time of 300 ns eliminates the need for mpu wait states or software overhead. An Address Latch Enable input is provided to permit both multiplexed and direct addressing. These features allow easy interface with any available microprocessor. Other features include full calendar with automatic leap-year correction, on-chip battery backup switch over circuit and on-chip alarm comparator and RAM. Available in 24-pin plastic DIP and CERDIP package with temperature range from −40°C to +85°C.




INTERSIL PRODUCTS



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## DISPLAY DRIVERS

Intersil's complete complement of monolithic Display Driver circuits provides a suitable interface for virtually any display application.

- Choice of Displays:
  LED, LCD, Vacuum Fluorescent
- Choice of Characters or Digits:
  4, 8 or 10 7-Segment Digits
  14, 16 or 18-Segment Characters
- Choice of Font:
  Hexadecimal, Code B, ASCII
- Choice of Interface:
  Multiplexed or Direct Drive; BCD, Random Access, Serial or Parallel

All Intersil Drivers are fabricated with CMOS technology for low power dissipation, and most are available in CERDIP and Plastic Dual In-line packages, as well as in die form. All are completely self-contained, requiring few, if any, external components to accomplish their intended basic functions.

The following table offers a quick-glance overview of available functions for a first-order selection.

| TYPE | # OF CHARACTERS OR DIGITS | | | | | | DISPLAY TYPE | | | | | | | FONT | | | INTERFACE | | | | | FEATURES AND COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | # of 7-Segment Digits | # of Decimal Points or Annunciators | # of Alphanumeric 14 Segments + D.P. | # of Alphanumeric 16 Segments + D.P. | # of Alphanumeric 18 Segments | # of Dot Matrix | LED, Common Anode Non-MUX | LED, Common Cathode MUX | LED, Common Anode MUX | LCD, Direct Drive | LCD, # of Ways MUX'D | Vacuum Fluorescent | | Hexadecimal (0–9, A–F) | Code B (0–9, H, E, L, P, -, and Blank) | ASCII | MUX BCD (BCD + Digit Select Strobes) | Random Access (Data + Address + WR) | Bit Parallel, Digit Serial | Bit Serial | Cycle Time (ns) | |
| ICM7211 | 4 | | | | | | | | | • | | | | • | | | • | | | | 1000 | Drives Conventional LCD Displays. Includes RC Oscillator, Divider Chain, Latches, Interface and LCD Drivers. Evaluation Kit Available. |
| ICM7211A | 4 | | | | | | | | | • | | | | | • | | • | | | | 1000 | |
| ICM7211M | 4 | | | | | | | | | • | | | | • | | | | • | | | 200 | |
| ICM7211AM | 4 | | | | | | | | | • | | | | | • | | | • | | | 200 | |
| ICM7212 | 4 | | | | | | • | | | | | | | • | | | • | | | | 1000 | Drives Common Anode LED Displays. 28 Current Controlled Outputs. Includes Latches, Interface and Brightness Control. Evaluation Kit Available. |
| ICM7212A | 4 | | | | | | • | | | | | | | | • | | • | | | | 1000 | |
| ICM7212M | 4 | | | | | | • | | | | | | | • | | | | • | | | 200 | |
| ICM7212AM | 4 | | | | | | • | | | | | | | | • | | | • | | | 200 | |
| ICM7218A | 8 | 8 | | | | | | | • | | | | | • | • | | | | • | | 550 | 3 Decode Formats Drives UP to 64 Independent LED's. Includes 8 × 8 Memory, Multiplexed LED Drivers, Decoders, Interface and control. Applications Include Bar Graphs. |
| ICM7218B | 8 | 8 | | | | | | • | | | | | | • | • | | | | • | | 550 | |
| ICM7218C | 8 | 8 | | | | | | | • | | | | | • | • | | | • | | | 500 | |
| ICM7218D | 8 | 8 | | | | | | • | | | | | | • | • | | | • | | | 500 | |
| ICM7218E | 8 | 8 | | | | | | | • | | | | | • | • | | | • | | | 500 | |
| ICM7228A | 8 | 8 | | | | | | | • | | | | | • | • | | | | • | | 550 | |
| ICM7228B | 8 | 8 | | | | | | • | | | | | | • | • | | | | • | | 550 | |
| ICM7228C | 8 | 8 | | | | | | | • | | | | | • | • | | | • | | | 500 | |
| ICM7228D | 8 | 8 | | | | | | • | | | | | | • | • | | | • | | | 500 | |
| ICM7231A | 8 | 16 | | | | | | | | | 3 | | | • | | | | • | | | 500 | 8 Digits, 16 Annunciators on COM, Hexadecimal |
| ICM7231B | 8 | 16 | | | | | | | | | 3 | | | | • | | | • | | | 500 | 8 Digits, 16 Annunciators on COM 3, Code B |
| ICM7231C | 8 | 16 | | | | | | | | | 3 | | | | • | | | • | | | 500 | 8 Digits, 16 Annunciators on COM 1 + 3, Code B |
| ICM7232A | 10 | 20 | | | | | | | | | 3 | | | • | | | | | | • | 350 | 10 Digits, 20 Annunciators on COM 3, Hexadecimal |
| ICM7232B | 10 | 20 | | | | | | | | | 3 | | | | • | | | | | • | 350 | 10 Digits, 20 Annunciators on COM 3, Code B |
| ICM7232C | 10 | 20 | | | | | | | | | 3 | | | | • | | | | | • | 350 | 10 Digits, 20 Annunciators on COM 1 + 3, Code B |
| ICM7233A | | | | | 4 | | | | | | 3 | | | | | • | | • | | | 500 | 4 Alphanumeric Characters. Evaluation Kit Available |
| ICM7233B | | | | | 4 | | | | | | 3 | | | | | • | | • | | | 500 | 4 Alphanumeric Characters. Full-Width Numbers |
| ICM7243A | | | | 8 | | | | • | | | | | | | | • | | • | | | 250 | 8 Alphanumeric Characters + Decimal Pt. can be Daisy Chained or Cascaded. Evaluation Kit Avail. |
| ICM7243B | | | 8 | | | | | • | | | | | | | | • | | • | | | 250 | |





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## Special Purpose Amplifiers

### ICL420/421/422/423
### ±15V Chopper Stabilized Operational Amplifier

These chopper-stabilized CMOS operational amplifiers are designed for signal conditioning, precision and instrumentation type applications. They offer a wide input and operating supply range, allowing virtual plug-in replacements for conventional lower-performance amplifiers, requiring only two additional external capacitors.

The ICL420 (8-pin) and ICL421 (14-pin) devices draw a maximum supply current of 2 mA and are available in all temperature ranges. The ICL422 and ICL423 are lower power devices with a maximum supply current of 0.5μA.

### ICL7605/7606
### Commutating Auto-Zero (CAZ) Instrumentation Amplifier, CMOS

The ICL7605/ICL7606 CMOS commutating auto-zero (CAZ) instrumentation amplifiers are intended for low-frequency operation in applications such as strain gauge amplifiers which require voltage gains from 1 to 1000 and bandwidths from DC to 10Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. This, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

Available in three temperature ranges.

### ICL8048/ICL8049
### Log/Antilog Amplifier

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change in the input.

## Content:

Special Purpose Amplifiers
- Instrumentation Amplifiers
- Log/Antilog Amplifiers
- Drive Amplifier for Power Transistors

Operational Amplifiers
- General Purpose
- Low Power
- Low Input Offset Voltage
- Low Input Bias Current

**Features:**

- **Input Offset Voltage — 2μV**
- **Input Offset Voltage Drift — 0.2μV/Year**
- **Common Mode Input Voltage Range — 0.3V Above Supply Rail**
- **Common Mode Rejection Ration — 100 dB**
- **Operates at Supply Voltages As Low As ±2V**
- **Short Circuit Protection On Outputs**
- **Compensated (ICL7605) or Uncompensated (ICL7606) Versions**

**Features:**

- **½% Full Scale Accuracy**
- **Temperature Compensated for 0°C to +70°C**
- **Scale Factor 1V/Decade, Adjustable**
- **120dB Dynamic Current Range (8048)**
- **60dB Dynamic Voltage Range (8048 & 8049)**
- **Dual JFET-Input Op-Amps**





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## Operational Amplifiers

Intersil offers a range of single and multiple monolithic operational amplifiers suitable for a number of specific applications categories. Included are bipolar Super-Beta and Chopper-Stabilized CMOS devices for very low input offset requirement, a selection of PMOS and JFET-input devices for very low bias currents, as well as general-purpose and low-power amplifiers for a broad range of applications.

All monolithic operational amplifiers are available in a variety of packages and in die form.

## Operational Amplifiers: General Purpose

| Type | Description | $V_{OS}$ (mV Max) | $I_{BIAS}$ (pA Max) | Slew Rate (V/μs) | GBW (MHz) | Compensation | $V_{SUPPLY}$ (V Max) | Temperature Range (°C) |
|---|---|---|---|---|---|---|---|---|
| **SINGLES** | | | | | | | | |
| ICL7611 | CMOS, Selectable $I_Q$ | 2, 5, 15 | 50 | 1.6 | 1.4 | INT | ±9 | 0 to +70<br>−55 to +125 |
| ICL8007M | JFET Input Op-Amp | 20 | 20 | 6 | 1.0 | INT | ±18 | −55 to +125 |
| ICL8007C | JFET Input Op-Amp | 50 | 50 | 6 | 1.0 | INT | ±18 | 0 to +70 |
| **DUALS** | | | | | | | | |
| ICL7621 | CMOS, Fixed $I_Q$ | 2, 5, 15 | 50 | 0.16 | 0.48 | INT | ±9 | 0 to +70<br>−55 to +125 |
| ICL8043M | JFET Input Op-Amp | 20 | 20 | 6 | 1.0 | INT | ±18 | −55 to +125 |
| ICL8043C | JFET Input Op-Amp | 50 | 50 | 6 | 1.0 | INT | ±18 | 0 to +70 |
| **TRIPLES** | | | | | | | | |
| ICL7631 | CMOS, Selectable $I_Q$ | 5, 10, 20 | 50 | 1.6 | 1.4 | INT | ±9 | 0 to +70<br>−55 to +125 |
| **QUADS** | | | | | | | | |
| ICL7641 | CMOS, Fixed $I_Q$ | 5, 10, 20 | 50 | 1.6 | 1.4 | INT | ±9 | 0 to +70<br>−55 to +125 |

### Low Power

| Type | Description | $I_{QUIESCENT}$ (Per Channel) (μA Typ) | $V_{SUPPLY}$ (V Max) | $V_{OS}$ (mV Max) | $I_{BIAS}$ (nA Max) | GBW (MHz) | Compensation | Temperature Range (°C) |
|---|---|---|---|---|---|---|---|---|
| **SINGLES** | | | | | | | | |
| ICL7611 | CMOS, Selectable $I_Q$ | 10 | ±9 | 2, 5, 15 | 0.05 | 0.044 | INT | 0 to +70 & |
| ICL7612 | CMOS, Extended CMVR | 10 | ±9 | 2, 5, 15 | 0.05 | 0.044 | INT | −55 to +125 |
| ICL8021M | Bipolar, Selectable $I_Q$ | 30 | ±18 | 3 | 20 | 0.27 | INT | −55 to +125 |
| ICL8021C | Bipolar, Selectable $I_Q$ | 30 | ±18 | 6 | 30 | 0.27 | INT | 0 to +70 |
| **TRIPLES** | | | | | | | | |
| ICL7631 | CMOS, Selectable $I_Q$ | 10 | ±9 | 5, 10, 20 | 0.05 | 0.044 | INT | 0 to +70 & |
| ICL8023M | Triple 8021M | 30 | ±18 | 3 | 20 | 0.27 | INT | −55 to +125 |
| ICL8023C | Triple 8021C | 30 | ±18 | 6 | 30 | 0.27 | INT | 0 to +70 |
| **QUADS** | | | | | | | | |
| ICL7642 | CMOS, Fixed $I_Q$ | 10 | ±9 | 5, 10, 20 | 0.05 | 0.044 | INT | 0 to +70 &<br>−55 to +125 |





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# Operational Amplifiers: Special Purpose

## Low/Ultra-low Input Offset Voltage

| Type | Description | $V_{OS}$ ($\mu$V Max) | $\Delta V_{OS}/\Delta T$ ($\mu$V/°C) (Max) | $\Delta Vos/\Delta t$ (nV/month) (Typ) | $I_{BIAS}$ (pA Max) | GBW (MHz) | $V_{SUPPLY}$ (V Max) | Temperature Range (°C) |
|---|---|---|---|---|---|---|---|---|
| **SINGLES** | | | | | | | | |
| ICL7650SC | CMOS, Chopper-stabilized | ±8 | ±0.02 | 100 | 20 | 2.0 | ±9 | 0 to +70 |
| ICL7650SI | CMOS, Chopper-stabilized | ±10 | ±0.02 | 100 | 50 | 2.0 | ±9 | −25 to +85 |
| ICL7650SM | CMOS, Chopper-stabilized | ±20 | ±0.03 | 100 | 500 | 2.0 | ±9 | −55 to +125 |
| ICL7652SC | Low-noise 7650SC | ±7 | ±0.01 | 100 | 30 | 0.5 | ±9 | 0 to +70 |
| ICL7652SI | Low-noise 7650SI | ±10 | ±0.02 | 100 | 30 | 0.5 | ±9 | −25 to +85 |
| ICL7652SM | Low-noise 7650SM | ±50 | ±0.1 | 100 | 500 | 0.5 | ±9 | −55 to +125 |
| ICL420C | ±15V CMOS Chopper-stabilized | ±10 | ±0.05 | 100 | 100 | 500 | ±16.5 | 0 to +70 |
| ICL420I | ±15V CMOS Chopper-stabilized | ±5 | ±0.05 | 100 | 30 | 500 | ±16.5 | −40 to +85 |
| ICL420M | ±15V CMOS Chopper-stabilized | ±5 | ±0.05 | 100 | 30 | 500 | ±16.5 | −55 to +125 |
| ICL421C | ±15V CMOS Chopper-stabilized | ±10 | ±0.05 | 100 | 100 | 500 | ±16.5 | 0 to +70 |
| ICL421I | ±15V CMOS Chopper-stabilized | ±5 | ±0.05 | 100 | 30 | 500 | ±16.5 | −40 to +85 |
| ICL421M | ±15V CMOS Chopper-stabilized | ±5 | ±0.05 | 100 | 30 | 500 | ±16.5 | −55 to +125 |
| ICL422C | Low-Power ICL420 | ±10 | ±0.05 | 100 | 100 | 400 | ±16.5 | 0 to +70 |
| ICL422I | Low-Power ICL420 | ±5 | ±0.05 | 100 | 30 | 400 | ±16.5 | −40 to +85 |
| ICL422M | Low-Power ICL420 | ±5 | ±0.05 | 100 | 30 | 400 | ±16.5 | −55 to +125 |
| ICL423C | Low-Power ICL421 | ±10 | ±0.05 | 100 | 100 | 400 | ±16.5 | 0 to +70 |
| ICL423I | Low-Power ICL421 | ±5 | ±0.05 | 100 | 30 | 400 | ±16.5 | −40 to +85 |
| ICL423M | Low-Power ICL421 | ±5 | ±0.05 | 100 | 30 | 400 | ±16.5 | −55 to +125 |

## Low Input Bias Current

| Type | Description | $I_{BIAS}$ (pA Max) | $I_{OS}$ (pA Typ) | $V_{OS}$ (mV Max) | GBW (MHz) | Compen-sation | $V_{SUPPLY}$ (V Max) | Temperature Range (°C) |
|---|---|---|---|---|---|---|---|---|
| **SINGLES** | | | | | | | | |
| ICL7611 | CMOS, Selectable $I_Q$ | 50 | 0.5 | 2, 5, 15 | 1.4 | INT | ±9 | 0 to +70 & |
| ICL7612 | CMOS, Extended CMVR | 50 | 0.5 | 2, 5, 15 | 1.4 | INT | ±9 | −55 to +125 |
| ICL8007M | JFET Input Op-Amp | 20 | 0.5 | 20 | 1.0 | INT | ±18 | −55 to +125 |
| ICL8007AM | JFET Input, Low Bias | 4.0 | 0.2 | 30 | 1.0 | INT | ±18 | −55 to +125 |
| ICL8007C | JFET Input Op-Amp | 50 | 0.5 | 50 | 1.0 | INT | ±18 | 0 to +70 |
| ICL8007AC | JFET Input, Low Bias | 4.0 | 0.2 | 30 | 1.0 | INT | ±18 | 0 to +70 |
| ICH8500 | PMOS Input | 0.1 | — | 50 | 0.7 | INT | ±18 | −25 to +85 |
| ICH8500A | PMOS Input, Low Bias | 0.01 | — | 50 | 0.7 | INT | ±18 | −25 to +85 |
| **DUALS** | | | | | | | | |
| ICL7621 | CMOS, Fixed $I_Q$ | 50 | 0.5 | 2, 5, 15 | 0.48 | INT | ±9 | 0 to +70 & −55 to +125 |
| ICL8043M | JFET Input Op-Amp | 20 | 0.5 | 20 | 1.0 | INT | ±18 | −55 to +125 |
| ICL8043C | JFET Input Op-Amp | 50 | 0.5 | 50 | 1.0 | INT | ±18 | 0 to +70 |
| **TRIPLES** | | | | | | | | |
| ICL7631 | CMOS, Selectable $I_Q$ | 50 | 0.5 | 5, 10, 20 | 1.4 | INT | ±9 | 0 to +70 & −55 to +125 |
| **QUADS** | | | | | | | | |
| ICL7641 | CMOS, Fixed $I_Q$ | 50 | 0.5 | 5, 10, 20 | 1.4 | INT | ±9 | 0 to +70 & |
| ICL7642 | CMOS, Fixed $I_Q$ | 50 | 0.5 | 5, 10, 20 | 0.044 | INT | ±9 | −55 to +125 |

INTERSIL PRODUCTS





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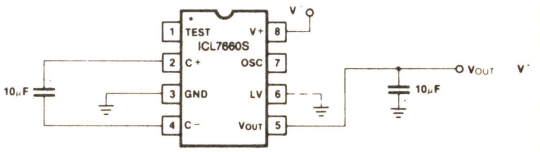
## POWER-SUPPLY SUPERVISORY CIRCUITS

### ICL7660S/ICL7662
### Voltage Converters

These voltage converters transform a positive (+) input voltage from a power supply to a corresponding negative (−) output, resulting in complementary output voltages of −1.5V to −12.0V for the ICL7660S, and −4.5V to −20V for the ICL7662. Only two non-critical external capacitors are needed to perform the conversions. The converters can also be connected as voltage doublers and will generate output voltages of +18.6V and 22.6V, respectively.

Available in three temperature ranges, 0°C to 70°C −25°C to +85°C (ICL7660S only) and −55°C +125°C, and three packages, TO-99, 8-pin MiniDIP and SOIC (ICL7660S only).

The ICL7660S is an enhanced version of the ICL7660 and is recommended for all new designs.




Simple Negative Converter Configuration

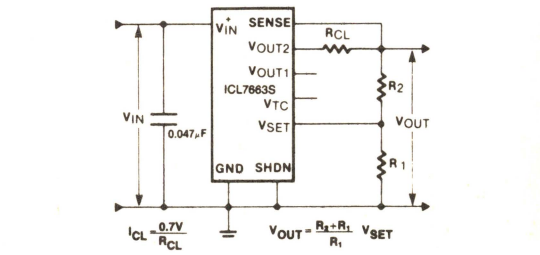
### ICL7663S
### Programmable Micropower Voltage Regulators

The ICL7663S is a low power voltage regulator that provides high-efficiency inputs of 1.6V to 16V and provides adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 4µA, regardless of load.

Output current sensing and remote shutdown are available, thereby providing protection for the regulators and the circuits they power.

The ICL7663S is available in 8-pin plastic, TO-99 metal can, MiniDIP CERDIP, and SOIC packages, in two temperature ranges— 0°C to +70°C and −25°C to +85°C.

The ICL7663S is an enhanced version of the ICL7663 and is recommended for new designs.

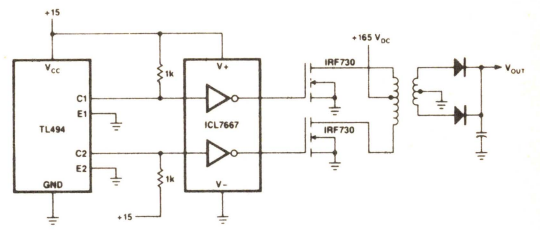



Basic Applications of ICL7663 as Positive Regulator with Current Limit

### ICL7667
### Dual Power MOSFET Driver

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and peak current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters.

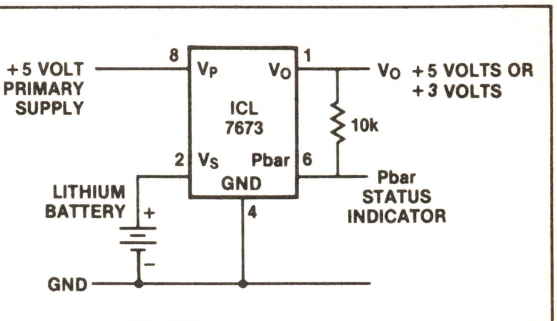
Available in commercial and military temperature ranges, and in 8-pin plastic DIP, SOIC, CERDIP and TO-99 metal packages.




Direct Drive of MOSFET Gates

### ICL7673
### Automatic Battery Back-Up Switch

The ICL7673 automatically switches from the main power supply to a battery back-up supply in the event of power loss, and back again when power is restored. Ideal for on-board battery back-up for real-time clocks, timers, volatile RAMs, or portable instruments. Available in 8-pin MiniDIP TO-99 and SOIC packages.




ICL7673 Battery Backup Circuit

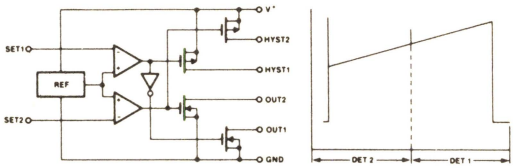
INTERSIL PRODUCTS

### ICL7665S
**Micropower Under/Over Voltage Detector**

The ICL7665S contains two individually programmable voltage detectors on a single chip. Requiring only 3μA, typical, for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and corrections

Available in 8-lead CERDIP, MiniDIP, TO-99 metal can and SOIC packages with temperature ranges from 0°C to 70°C and −25°C to +85°C.

The ICL7665S is an enhanced version of the ICL7665 and is recommended for all new designs.



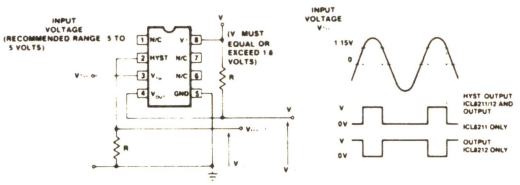

**ICL7665 Functional Diagram and Transfer Characteristics of Simple Threshold Detector**

### ICL8211/ICL8212
**Programmable Voltage Detector**

These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

The ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminals is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Available in 8-lead MiniDip, TO-99 metal can and SOIC packages, in commercial and military temperature ranges.




**Voltage Level Detection with ICL8211/8212**

### ICL8069
**Low Voltage Reference**

ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

Available in TO-92 plastic and TO-52 metal packages with 0°C to 70°C and −55°C to +125°C temperature ranges (metal only) and with temperature coefficients of 50 and 100ppμ/°C.

### ICL7677
**Power Fail Detector**

ICL7677 is a Power Fail Detector which can be incorporated either into the primary or the secondary side of a power supply to give the fastest possible power-fail indication. On the primary side, it can simultaneously monitor AC line voltage, the reservoir capacitor voltage, primary side current and ambient temperature. On the secondary side, it can simultaneously monitor up to two DC voltages, one load current and the ambient temperature. The circuit has an on-chip bandgap-voltage reference to conveniently program the detection thresholds.

### ICL7675/ICL7676
**Switched-Mode Power Supply Controller Set**

The ICL7675/7676 two-chip set provides the necessary control circuitry for regulation of an isolated flyback type switching power supply. Specifically designed to operate in this type of configuration, the Intersil controller chip-set is trimmed to provide a regulated 5V output. The isolated flyback converter is the most widely used configuration for switched-mode power supplies in the 50W to 150W range because of its simplicity. The chip-set features soft-start and power switch over-current protection.

### ICL7680
**5V to ±15V Voltage Converter**

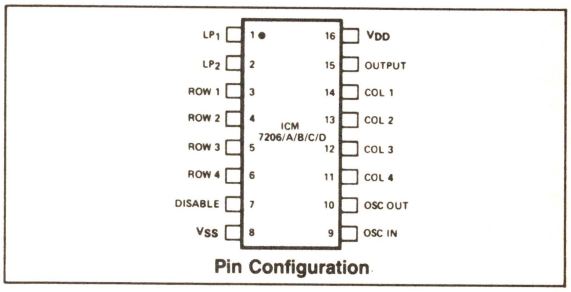
The ICL7680 is a simple boost-type switched-mode converter/inverter chip using minimal external components to convert +5V to ±15V regulated outputs. An internal oscillator is user programmable to optimize efficiency for various load conditions. The device features current limiting protection together with external shut-down.

## SPECIAL ANALOG FUNCTIONS

### ICM7206
### Touch-Tone Encoder

The ICM7206 is a 2-of-8 sinewave DTMF generator for use in telephone dialing systems. The ICM7206 requires a 3.58 MHz crystal and will operate with both 3x4 and 4x4 keypads. This low-cost circuit has a high current bipolar output driver providing low harmonic distortion. Supply voltage range is 3 to 6 volts with power dissipation of less than 5.5mW at 5.5 volts. Single and dual tone capability.

Available in 16-pin plastic DIP with a temperature range from −40°C to +85°C.

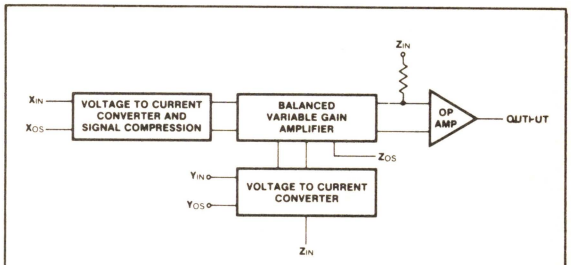


Pin Configuration

### ICL8013
### Four Quadrant Analog Multiplier

The ILC8013 is a bipolar, four-quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to adjust or trim gain accuracy, offset voltage and feedthrough performance.

Available in 10-pin TO-100 metal package in both commercial and military temperature ranges.

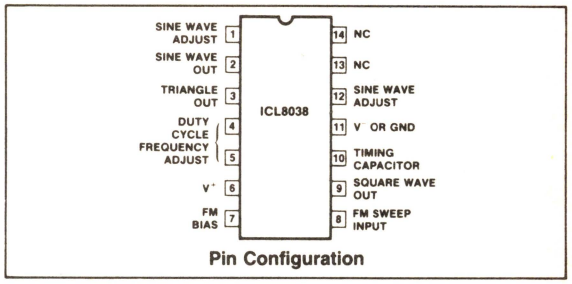


ICL8013 Functional Diagram

### ICL8038
### Precision Waveform Generator/Voltage Controlled Oscillator

The ICL8038 Waveform Generator is capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300KHz using either resistors or capacitors, and frequency modulation, and sweeping can be accomplished with an external voltage.

The 14-pin plastic and CERDIP package are available with 0°C to +70°C, and −55°C to +125°C temperature ranges.



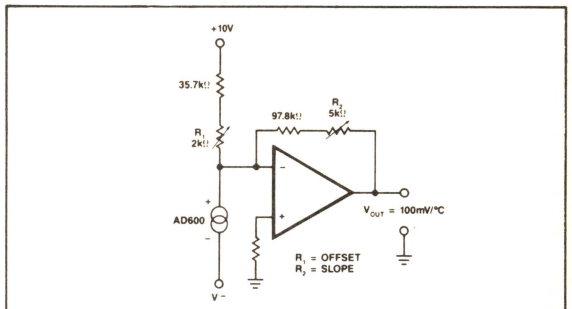
Pin Configuration

### AD590
### 2-Wire, Current-Output Temperature Transducer

The AD590 is a 2-wire integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator producing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin-film resistors is used to calibrate the device to 298.2 μA output at 298.2°K (+25°C).

The AD590 could be used in any temperature-sensing application between −55°C and +150°C in which conventional electrical temperature sensors are currently employed.

Metal packaged device (TO-52) covers −55°C to +150°C range. With slope and offset trimming circuit it is possible to adjust devices to give less than 0.1% error over the temperature range from 0°C to 90°C.



AD590 Slope and Offset Trimming Circuit





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## Microperipheral and Interface Circuits

### IM6402/IM6403
### Universal Asynchronous Receiver Transmitter (UART)

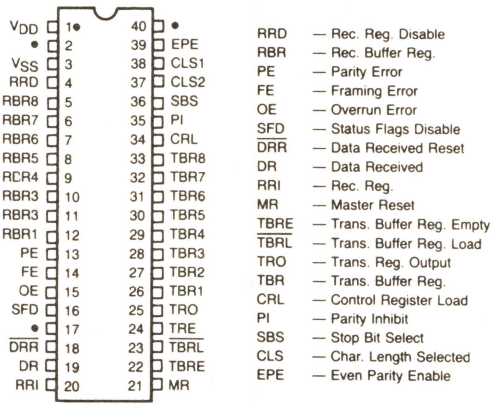
The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. CMOS/LSI technology permits clock frequencies up to 6.0 MHz (250K Baud).

Variations include the following:

| Device | Fc (MHz) | Device | Fc (MHz) |
|---|---|---|---|
| IM6402 | 1 | IM6403 | 2.46 |
| IM6402-1 | 2 | IM6403-1 | 3.58 |
| IM6402A | 4 | IM6403A | 6.00 |

The IM6403 Series differs from the IM6402 Series primarily by having an on-board crystal oscillator and baud rate generator. Available in plastic and ceramic packages, in commercial and military temperature ranges.




**Pin Configuration**

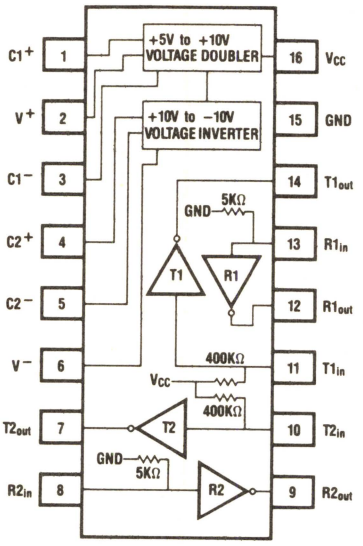
### IM4702/4712
### Baud Rate Generator

The IM4702/12 Baud Rate Generators provide necessary clock signals for digital data transmission systems, such as UARTs, using a 2.4576 MHz crystal oscillator as an input. They control up to 8 output channels and can be cascaded for output expansion.

Multi-channel operation allows up to eight simultaneous Baud rates to be generated. Provides 14 most commonly used baud rates from zero through 9600 Baud. In addition, 19200 Baud is possible via hardwiring.

IM4712 integrates oscillator feedback resistor and two load capacitors on-chip.

Available in 16-pin plastic DIP and CERDIP packages with a temperature range from −40°C to +85°C.




**ICL232 Functional Diagram**

### ICL232
### +5V Powered Dual RS-232
### Transmitter/Receiver

The ICL232 requires only a few non-critical external components to perform the RS-232 driver/receiver function with either CMOS or TTL inputs. It features two on-board charge-pump voltage converters which generate the required ±10V supplies from a single 5V power supply. The ICL232 meets all EIA RS-232C specifications. It is available in a variety of packages (including the 16-pin SOIC) and operating temperature ranges.





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# ANALOG SWITCHES AND MULTIPLEXERS

**Content:**

General Purpose Analog Switches
Drivers for FET Switches
Low Cost, Virtual Ground Switch Family
RF/Video Switch Family
Multiplexers

## General Purpose Analog Switches

Intersil offers two general-purpose switch lines, each with various switch configurations. The first consists of bipolar drivers controlling an associated set of field-effect switching transistors in a multi-chip structure that provides a wide choice of parameters at low cost. The second is a monolithic CMOS structure capable of improved performance and greater reliability. All have break-before-make switch action.

All switches are available in commercial and military temperature ranges. Package options include Plastic DIP, CERDIP, Flat Pack and Metal Can (not all options are available for all device types).

## General Purpose Analog Switches

| Switch Family | Special Features | Switch Type | Switch Parameters | | | | |
|---|---|---|---|---|---|---|---|
| | | | $R_{DS(ON)}$ (Ω Max) | $I_{D(OFF)}$ (nA Max) | $t_{ON}$ (ns Max) | $t_{OFF}$ (ns Max) | Analog Voltage Range ($V_{SUPPLY}$ = ±15V) |
| **Multichip** | | | | | | | |
| DG123-125 | Inverting/non-inverting logic inputs | PMOS | 600 | 4 | 300 | 1000 | — |
| DG126-154<br>DG139-164 | Dual Channel<br>Single Channel | N-JFET | 10<br>15<br>30<br>50<br>80 | 10<br>10<br>1<br>1<br>1 | 1000<br>1000<br>600<br>600<br>600 | 2500<br>2500<br>1600<br>1600<br>1600 | — |
| DG180-191 | Mature, Industry-standard switch, JAN38510 Approved | N-JFET | 10<br>30<br>75 | 10<br>1<br>1 | 300<br>150<br>250 | 250<br>130<br>130 | −7.5 to +15<br>−7.5 to +15<br>−10 to +15 |
| **Monolithic** | | | | | | | |
| DGM181-191 | Monolithic replacement for DG180 family | CMOS | 50<br>75 | 2.0<br>0.5 | 250<br>450 | 200<br>250 | −15 to +15<br>−15 to +15 |
| DG200/201 | Industry-standard low cost | CMOS | 70/80 | 2.0 | 1000 | 500 | −15 to +15 |
| DG211<br>DG212 | Inverting<br>Noninverting | CMOS | 175 | 5.0 | 1000 | 500 | −15 to +15 |
| DG300A-303A | TTL compatible, low power | CMOS | 50 | 1.0 | 300 | 250 | −15 to +15 |
| IH311<br>IH312 | High Speed Inverting<br>Noninverting | CMOS<br>CMOS | 175 | 100 | 300 | 150 | −15 to +15 |
| IH5040-47<br>IH5048-51<br>IH5052-53 | Low quiescent current<br>Low $R_{DS(ON)}$ | CMOS | 75<br>40<br>75 | 1.0<br>1.0<br>1.0 | 750<br>500<br>500 | 350<br>250<br>250 | −10 to +10<br>−10 to +10<br>−11 to +11 |
| IH5140-45 | High speed, low power, low leakage | CMOS | 50 | 0.5 | 100 | 75 | −11 to +11 |
| IH5148-51 | Low $R_{DS(ON)}$, high speed, low power | CMOS | 25 | 0.5 | 250<br>350<br>500 | 200<br>250<br>250 | −14 to +14 |
| **Separate Driver/Switch Combinations** | | | | | | | |
| IH6201 | TTL level translator/driver | N-JFET | 30 | 0.5 | 50 (Typ) | 150 (Typ) | 15 p-p (Min) |
| IH401/A | Low charge injection switch | | 30/50 | 0.5 | 50 (Typ) | 150 (Typ) | 20 p-p (Min) |

## Drivers for FET Switches

Monolithic bipolar drivers convert low-level positive logic to high-level positive and negative voltages necessary to drive FET switches.

| Type | Number of Channels | Output Swing | | $t_{ON}$ ns Max | $t_{OFF}$ ns Max |
|---|---|---|---|---|---|
| | | Positive (V Max) | Negative (V Max) | | |
| D123 | 6 TTL/DTL | $V_{Supply}$ | −19.7 | 250 | 400-800 |
| D125 | 6 TTL | $V_{Supply}$ | −19.7 | 250 | 400-800 |
| D129 | 4 TTL/DTL | $V_{Supply}$ | −19.3 | 250 | 1000 |
| IH6201 | 2 TTL | +14.0 | −14.0 | 200 | 300 |





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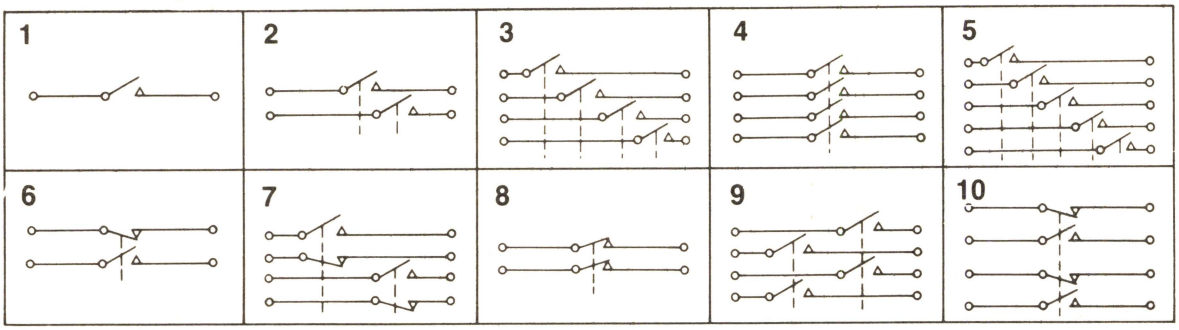
## Switch Configurations




| Switch Configuration (Diagram) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| SPST (1) | Dual SPST (2) | Quad SPST (3) | 4PST (4) | Five SPST (5) | SPDT (6) | Dual SPDT (7) | DPST (8) | Dual DPST (9) | DPDT (10) |
| | | | | DG123<br>DG125 | | | | | |
| | DG141<br>DG151<br>DG133<br>DG152<br>DG134 | | | | DG146<br>DG161<br>DG144<br>DG162<br>DG143 | | | DG140<br>DG153<br>DG129<br>DG154<br>DG126 | DG145<br>DG163<br>DG139<br>DG164<br>DG142 |
| | DG180<br>DG181<br>DG182 | | | | DG186<br>DG187<br>DG188 | DG189<br>DG190<br>DG191 | | DG183<br>DG184<br>DG185 | |
| | DGM182 | | | | | DGM190<br>DGM191 | | DGM184<br>DGM185 | |
| | DG200 | DG201 | | | | | | | |
| | | DG211<br>DG212 | | | | | | | |
| DG301A | DG300A | | | | | DG303A | | DG302A | |
| | | IH311<br>IH312 | | | | | | | |
| IH5040 | IH5041<br>IH5048 | IH5052/53 | IH5047 | | IH5042<br>IH5050 | IH5043<br>IH5051 | IH5044 | IH5045<br>IH5049 | IH5046 |
| IH5140 | IH5141 | | | | IH5142 | IH5143 | IH5144 | IH5145 | |
| | IH5148 | | | | IH5150 | IH5151 | | IH5149 | |
| | | IH401/A | | | | | | | |





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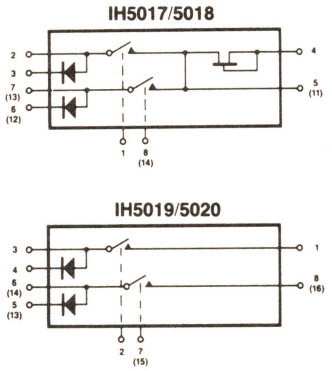
## Virtual Ground Switches, JFETs (P-Channel)

Each package contains up to four channels of analog gating designed to eliminate the need for external drivers. The odd-numbered devices are designed to be driven directly from TTL open-collector logic (15V). Each channel simulates a SPDT switch. The parts are intended for high-performance multiplexing and commutating use. All have turn-on/turn-off times of 500 ns and a leakage current ($I_{D(off)}$) of 0.2 nA.

| Switch Configuration | | | | Special Features | Switch Type | $r_{DS(on)}$ (Ω Max) |
|---|---|---|---|---|---|---|
| SPST | Dual SPST | Triple SPST | Quad SPST | | | |
| IH5021 | IH5017 | IH5013 | IH5009 | Common Output | P-JFET | 100 |
| IH5022 | IH5018 | IH5014 | IH5010 | | | 150 |
| IH5023 | IH5019 | IH5015 | IH5011 | Separate Output | | 100 |
| IH5024 | IH5020 | IH5016 | IH5012 | | | 150 |

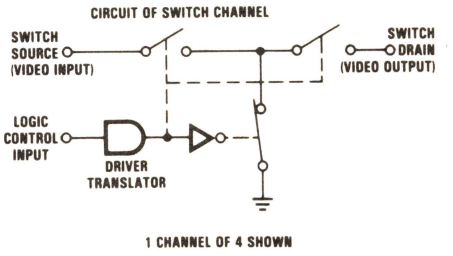



Examples of Common Output and Separate Output Switch Configurations

## RF/Video Switches, CMOS

Designed for high-frequency operation, these switches utilize a "T" configuration where a shunt switch is closed when the switch is open. This provides superior isolation between input and output and greatly improves performance in the video and RF region. Switch attenuation varies less than 3 dB from dc to 100 MHz. Available in three (commercial and military) temperature ranges and in 14-pin plastic DIP and 10-pin TO-100 metal package.

| Switch Configuration | | $r_{DS(on)}$ (Ω Max) | $I_{D(off)}$ (nA Max) | $t_{ON}$ (ns Max) | $t_{OFF}$ (ns Max) |
|---|---|---|---|---|---|
| Dual SPST | Quad SPST | | | | |
| IH5341 | IH5352 | 75 | 1.0 | 300 | 150 |

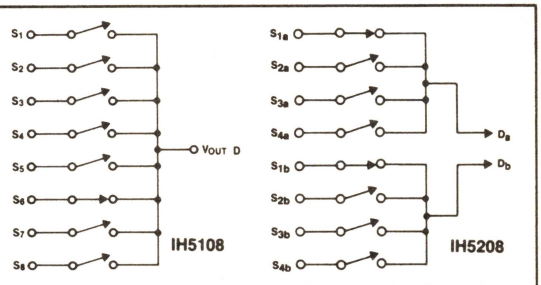



Internal Switch Configuration

## Multiplexers

Intersil provides three multiplexer families — a standard IH6000 Family featuring low $r_{DS(ON)}$; an equivalent fault-protected IH5000 series which ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ± 25 V, even with the supply voltage at zero; a multiplex/demultiplex unit with on-board data latches and control pins for microprocessor interface. All utilize CMOS technology for extremely low quiescent operating current.

The new IH9000 series provides input voltage operation (±50V) and low leakage.




Examples of Single-Ended and Differential Configurations

| Switch Family | Special Features | $r_{DS(ON)}$ (Ω Max) | $I_{D(OFF)}$ (nA Max) | $t_{ON}$ (ns Max) | $t_{OFF}$ (ns Max) | Analog Voltage Range $V_{Supply}$ = (±15V) | Configuration: 8 Channel Single Ended | Configuration: 4 Channel Differential | Configuration: 16 Channel Single Ended | Configuration: 8 Channel Differential |
|---|---|---|---|---|---|---|---|---|---|---|
| IH5000 Series | Industry standard pinouts, fault protection up to ±25V input, low leakage, low input current | 900 | 1.0 | 1500 | 1000 | −25 to +25 (Input) | IH5108 | IH5208 | | |
| | | 1000 | 1.0 | 1500 | 1000 | −25 to +25 (Input) | | | IH5116 | IH5216 |
| IH6000 Series | Industrial standard pinouts, low leakage, low $R_{DS(ON)}$ break before make switching | 300 | 2.0 | 1500 | 1000 | −14 to +14 | IH6108 | IH6208 | | |
| | | 600 | 2.0 | 1500 | 1000 | −14 to +14 | | | IH6116 | IH6216 |
| IH9000 Series | Multiplexer/Demultiplexer with latches for μP based systems | 120 | 2.5 | 2000 | 1000 | −50 to +50 | IH9108 | | | |

INTERSIL PRODUCTS



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# MIL-STD-883B Rev. C Compliant Devices

### Data Acquisition Products

#### 883B Rev C.

AD7520SD/883B
AD7520TD/883B
AD7520UD/883B
AD7521SD/883B
AD7521TD/883B
AD7521UD/883B
AD7533SD/883B
AD7533TD/883B
AD7533UD/883B
AD7541SD/883B
AD7541TD/883B
ICL7134UJMJ1/883B
ICL7134UKMJ1/883B
ICL7134ULMJI/883B

### Special Analog Functions

#### 883B Rev C.

ICL7660MTY/883B
ICL7660MTV/883B
ICL7662MTV/883B
ICL7667MJA/883B
ICL7667MTV/883B
ICL8038AMJD/883B
ICL8038BMJD/883B
ICL8069CMSQ/883B
ICL8069DMSQ/883B
ICL8211MTY/883B
ICL8212MTY/883B

### Timer/Counter Circuits

#### 883B Rev C.

ICM7555MTV/883B
ICM7556MJD/883B

### Amplifiers-Operational

#### 883B Rev C.

ICL8021MTY/883B
ICL8023MJE/883B
LM4250H/883B

### Analog Switch Products

#### 883B Rev C.

D123AK/883B
D123AL/883B
D125AK/883B
D125AL/883B
D129AK/883B
D129AL/883B
DG123AL/883B
DG123AP/883B
DG125AL/883B
DG125AP/883B
DG126AK/883B
DG126AL/883B
DG129AK/883B

### Analog Switch Products

#### 883B Rev C. (cont.)

DG129AL/883B
DG133AK/883B
DG133AL/883B
DG134AK/883B
DG134AL/883B
DG139AK/883B
DG139AL/883B
DG140AL/883B
DG140AP/883B
DG141AL/883B
DG141AP/883B
DG142AK/883B
DG142AL/883B
DG143AK/883B
DG143AL/883B
DG144AK/883B
DG144AL/883B
DG145AL/883B
DG145AP/883B
DG146AL/883B
DG146AP/883B
DG151AK/883B
DG151AL/883B
DG152AK/883B
DG152AL/883B
DG153AL/883B
DG153AP/883B
DG154AK/883B
DG154AL/883B
DG161AL/883B
DG161AP/883B
DG162AK/883B
DG162AL/883B
DG163AL/883B
DG163AP/883B
DG164AK/883B
DG164AL/883B
DG180AA/883B
DG180AK/883B
DG181AA/883B
DG181AK/883B
DG181AL/883B
DG182AA/883B
DG182AK/883B
DG182AL/883B
DG183AL/883B
DG183AP/883B
DG184AK/883B
DG184AL/883B
DG185AK/883B
DG185AL/883B
DG186AA/883B
DG186AL/883B
DG186AP/883B
DG187AA/883B
DG187AK/883B
DG187AL/883B
DG188AA/883B

### Analog Switch Products

#### 883B Rev C. (cont.)

DG188AK/883B
DG188AL/883B
DG189AP/883B
DG190AK/883B
DG190AL/883B
DG191AK/883B
DG191AL/883B
DG200AA/883B
DG200AJ/883B
DG201AJ/883B
DG202AK/883B
DG300AAA/883B
DG300AAK/883B
DG301AAA/883B
DG301AAK/883B
DG302AAK/883B
DG303AAK/883B
DG308AAK/883B
DG309AK/883B
DGM181AA/883B
DGM181AK/883B
DGM182AA/883B
DGM182AK/883B
DGM184AK/883B
DGM185AK/883B
DGM190AK/883B
DGM191AK/883B
IH5009MJD/883B
IH5010MJD/883B
IH5011MJE/883B
IH5012MJE/883B
IH5013MJD/883B
IH5014MJD/MJE883B
IH5015MJE/883B
IH5016MJE/883B
IH5017MJD/883B
IH5018MJD/883B
IH5019MJE/883B
IH5020MJE/883B
IH5021MJD/883B
IH5022MJD/883B
IH5023MJE/883B
IH5024MJE/883B
IH5040MFD/883B
IH5040MJE/883B
IH5041MFD/883B
IH5041MJE/883B
IH5042MFD/883B
IH5042MJE/883B
IH5043MFD/883B
IH5043MJE/883B
IH5044MFD/883B
IH5044MJE/883B
IH5045MFD/883B
IH5045MJE/883B
IH5046MFD/883B
IH5046MJE/883B
IH5047MFD/883B

### Analog Switch Products

#### 883B Rev C. (cont.)

IH5047MJE/883B
IH5052MJE/883B
IH5053MJE/883B
IH5108MJE/883B
IH5116MJI/883B
IH5140MFD/883B
IH5140MJE/883B
IH5141MFD/883B
IH5141MJE/883B
IH5142MFD/883B
IH5142MJE/883B
IH5143MFD/883B
IH5143MJE/883B
IH5144MFD/883B
IH5144MJE/883B
IH5145MFD/883B
IH5145MJE/883B
IH5148MFD/883B
IH5148MJE/883B
IH5149MFD/883B
IH5149MJE/883B
IH5150MFD/883B
IH5150MJE/883B
IH5151MFD/883B
IH5151MJE/883B
IH5208MJE/883B
IH5216MJI/883B
IH5341MTW/883B
IH5352MJE/883B
IH6108MJE/883B
IH6116MJI/883B
IH6201MJE/883B
IH6208MJE/883B
IH6216MJI/883B

### Microcontrollers, Microperipherals, Memory

#### 883B Rev C.

ICM7170AMDG/883B
ICM7170MDG/883B
ICM7228AMJI/883B
ICM7228BMJI/883B
ICM7228CMJI/883B
ICM7228DMJI/883B
IM6402-1MJL/883B
IM6402AIJL/883B
IM6402AMJL/883B
IM6402IJL/883B
IM6653AMJG/883B
IM6653MJG/883B
IM6654IJG/883B
IM6654AMJG/883B
IM6654MJG/883B
IM6654IJG/883B

**INTERSIL PRODUCTS**





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# QPL/Hi Rel Devices

### Data Acquisition Products

#### JM38510

| | |
|---|---|
| 12702BEA | AD7520UD |
| 12703BVA | AD7521UD |
| 12704BVC | AD7541TD |

### Analog Switch Products

#### JM38510

| | |
|---|---|
| 10501BEA | IH5040MDE |
| 10501BEC | IH5040MDE |
| 10502BEA | IH5041MDE |
| 10502BEC | IH5041MDE |
| 10503BEA | IH5042MDE |
| 10503BEC | IH5042MDE |
| 10504BEA | IH5043MDE |
| 10504BEC | IH5043MDE |
| 10505BEA | IH5044MDE |
| 10505BEC | IH5044MDE |
| 10506BEA | IH5045MDE |
| 10506BEC | IH5045MDE |
| 11101BAC | DG181AL |
| 11101BCC | DG181AP |
| 11101BIA | DG181AA |
| 11101BIC | DG181AA |
| 11101BCA | DG181AP |
| 11102BIA | DG182AA |
| 11102BAC | DG182AL |
| 11102BCC | DG182AP |
| 11102BIC | DG182AA |
| 11102BCA | DG182AP |
| 11103BAC | DG184AL |
| 11103BEC | DG184AP |
| 11103BEA | DG184AP |
| 11104BAC | DG185AL |
| 11104BEC | DG185AP |
| 11104BEA | DG185AP |
| 11105BAC | DG187AL |
| 11105BCC | DG187AP |
| 11105BIA | DG187AA |
| 11105BIC | DG187AA |
| 11105BCA | DG187AP |
| 11106BAC | DG188AL |
| 11106BCC | DG188AP |
| 11106BIA | DG188AA |
| 11106BIC | DG188AA |
| 11106BCA | DG188AP |
| 11107BAC | DG190AL |
| 11107BEC | DG190AP |
| 11107BEA | DG190P |
| 11108BAC | DG191AL |
| 11108BEC | DG191AP |
| 11108BEA | DG191AP |
| 11601BCC | DG300AAP |
| 11601BCA | DG300AAP |
| 11602BCC | DG301AAP |
| 111602BCA | DG301AAP |
| 11603BCC | DG302AAP |
| 11603BCA | DG302AAP |
| 11604BCC | DG303AAP |
| 11604BCA | DG303AAP |
| 12302BEA | DG201AP |
| 12302BEC | DG201AP |
| 19007BEA | IH6108MDE |
| 19007BEC | IH6108MDE |
| 19008BEA | IH6208MDE |
| 19008BEC | IH6208MDE |

### Analog Switch Products

#### Standard Military Dwg.

| | |
|---|---|
| 7705201EA | IH6108MJE |
| 7705201EC | IH6108MDE |
| 7705201EA | IH6108MDE |
| 7705203EA | IH5108MJE |
| 7705203EA | IH5108MDE |
| 7705301EA | DG201AK |
| 7705301EC | DG201AP |
| 7705301EA | DG201AP |
| 7801401CA | DG129AK |
| 7801401CC | DG129AP |
| 7801401CA | DG129AP |
| 8100601AC | IH5040MFD |
| 8100601EC | IH5040MDE |
| 8100601EA | IH5040MDE |
| 8100602AC | IH5041MFD |
| 8100602EC | IH5041MDE |
| 8100602EA | IH5041MDE |
| 8100602IA | IH5041MTW |
| 8100602IC | IH5041MTW |
| 8100602IB | IH5041MTW |
| 8100603AC | IH5042MFD |
| 8100603EC | IH5042MDE |
| 8100603EA | IH5042MDE |
| 8100604AC | IH5043MFD |
| 8100604EA | IH5043MJE |
| 8100604EC | IH5043MDE |
| 8100604EA | IH5043MDE |
| 8100605AC | IH5044MFD |
| 8100605EA | IH5044MJE |
| 8100605EC | IH5044MDE |
| 8100605EA | IH5044MDE |
| 8100605IA | IH5044MTW |
| 8100605IC | IH5044MTW |
| 8100605IB | IH5044MTW |
| 8100606AC | IH5045MFD |
| 8100606EA | IH5045MJE |
| 8100606EC | IH5045MDE |
| 8100606EA | IH5045MDE |
| 8100607AC | IH5046MFD |
| 8100607EA | IH5046MJE |
| 8100608AC | IH5047MFD |
| 8100608EA | IH5047MJE |
| 8100609EA | IH5140MJE |
| 8100609EC | IH5140MDE |
| 8100609EA | IH5140MDE |
| 8100610EA | IH5141MJE |
| 8100610EC | IH5141MDE |
| 8100610EA | IH5141MDE |
| 8100611EA | IH5142MJE |
| 8100611EC | IH5142MDE |
| 8100611EA | IH5142MDE |
| 8100612EA | IH5143MJE |
| 8100612EC | IH5143MDE |
| 8100612EA | IH5143MDE |
| 8100613EA | IH5144MJE |
| 8100613EC | IH5144MDE |
| 8100613EA | IH5144MDE |
| 8100614EA | IH5145MJE |
| 8100614EC | IH5145MDE |
| 8100614EA | IH5145MDE |
| 8100615EA | IH5046MJE |
| 8100615EC | IH5046MDE |
| 8100615EA | IH5046MDE |
| 8100616EA | IH5047MJE |
| 8100616EC | IH5047MDE |
| 8100616EA | IH5047MDE |

### Analog Switch Products

#### Standard Military Dw. (Cont.)

| | |
|---|---|
| 8100617EA | IH5146MJE |
| 8100617EC | IH5146MDE |
| 8100617EA | IH5146MDE |
| 8100618EA | IH5147MJE |
| 8100618EC | IH5147MDE |
| 8100618EA | IH5147MDE |
| 8100619EA | IH5148MJE |
| 8100619EC | IH5148MDE |
| 8100619EA | IH5148MDE |
| 8100620EA | IH5149MJE |
| 8100620EC | IH5149MDE |
| 8100620EA | IH5149MDE |
| 8100621EA | IH5150MJE |
| 8100621EC | IH5150MDE |
| 8100621EA | IH5150MDE |
| 8100622EA | IH5151MJE |
| 8100622EC | IH5151MDE |
| 8100622EA | IH5151MDE |
| 5962-8513104XA | IH5116MJI |
| 5962-8513104XA | IH5116MDI |
| 5962-8513104XC | IH5116MDI |
| 5962-8513105XA | IH5216MJI |
| 5962-8513105XA | IH5216MDI |
| 5962-8513105XC | IH5216MDI |
| 5962-8513106EA | IH5028MJE |
| 5962-8513106EA | IH5028MDE |
| 5962-8513106EC | IH5028MDE |

### MIL-S-19500 Transistors

| | |
|---|---|
| 2N3821JAN | 2N4858JAN |
| 2N3821JTX | 2N4858JTX |
| 2N3821JTXV | 2N4858JTXV |
| 2N3823JAN | 2N4859JAN |
| 2N3823JTX | 2N4859JTX |
| 2N3823JTXV | 2N4859JTXV |
| 2N4091JAN | 2N4860JAN |
| 2N4091JTX | 2N4860JTX |
| 2N4091JTXV | 2N4860JTXV |
| 2N4092JAN | 2N4861JAN |
| 2N4092JTX | 2N4861JTX |
| 2N4092JTXV | 2N4861JTXV |
| 2N4093JAN | 2N5114JAN |
| 2N4093JTX | 2N5114JTX |
| 2N4093JTXV | 2N5114JTXV |
| 2N4856JAN | 2N5115JAN |
| 2N4856JTX | 2N5115JTX |
| 2N4856JTXV | 2N5115JTXV |
| 2N4857JAN | 2N5116JAN |
| 2N4857JTX | 2N5116JTX |
| 2N4857JTXV | 2N5116JTXV |

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**INTERSIL PRODUCTS**

900352-004

# ORDERING & MARKING INFORMATION

## DEVICE FAMILY PREFIXES

**AD** – Analog Devices Alternate Source
**D** – Siliconix Driver/Level Translator IC Alternate Source
**DG** – Siliconix Analog Switch Alternate Source
**DGM** – Monolithic DG Analog Switch Replacement
**ICL** – Linear IC
**ICM** – Microperipheral IC
**ICH** – Hybrid IC
**IM** – Microcontroller and Digital Signal Processing IC
**LH** – National Semiconductor Hybrid Alternate Source
**LM** – National Semiconductor Linear Alternate Source
**MM** – National Semiconductor Analog Switch Alternate Source
**NE** – Signetics Alternate Source
**SE** – Signetics Alternate Source
**2N** – Industry Standard Discrete Transistor
**3N** – Industry Standard Discrete Transistor
**IT** – Discrete Transistor
**ITE** – Discrete Transistor
**J** – Discrete Transistor
**M** – Discrete Transistor
**NF** – Discrete Transistor
**P** – Discrete Transistor
**PN** – Discrete Transistor
**U** – Discrete Transistor
**VCR** – Discrete Transistor
**ID** – Low Leakage Diodes
**G** – Siliconix Analog Gate Alternate Source
**IH** – Analog Switch Family
**ADC** – National Semiconductor A/D Alternate Source
**μa** – Fairchild Linear Alternate Source

## PACKAGE TYPE DESIGNATORS

**A** – TO-237
**B** – Small Outline IC (SOIC)
**C** – TO-220
**D** – Ceramic Dual-In-Line
**E** – Small TO-8
**F** – Ceramic Flat Pack
**H** – TO-66
**I** – 16 Pin (.6 × .7 Pin Spacing) Hermetic Hybrid Dip
**J** – CERDIP Dual-In-Line
**K** – TO-3
**L** – Leadless Ceramic
**P** – Plastic Dual-In-Line
**S** – TO-52
**T** – TO-5 Type (also TO-78,TO-99,TO-100)
**U** – TO-72 Type (also TO-18,TO-71)
**V** – TO-39
**Z** – TO-92
**/W** – Wafer
**/D** – Dice

## EXCEPTIONS TO PACKAGE TYPE DESIGNATORS

| DG & DGM SERIES | AD SERIES |
|---|---|
| **A** – 10 Pin Metal Can | **H** – TO-52 |
| **L** – 14 Pin Flatpack | **D** – CERDIP,Ceramic DIP |
| **P** – Ceramic DIP (Special Order Only) | **N** – Epoxy DIP |
| **K** – CERDIP | **R** – TO-92 |

## PIN COUNT DESIGNATOR

**A** – 8
**B** – 10
**C** – 12
**D** – 14
**E** – 16
**F** – 22
**G** – 24
**H** – 42
**I** – 28
**J** – 32
**K** – 35
**L** – 40
**M** – 48
**N** – 18
**P** – 20
**Q** – 2
**R** – 3
**S** – 4
**T** – 6
**U** – 7
**V** – 8 (0.200″ Pin Circle Isolated Case)
**W** – 10 (0.230″ Pin Circle Isolated Case)
**Y** – 8 (0.200″ Pin Circle Case to Pin 4)
**Z** – 10 (0.230″ Pin Circle Case to Pin 5)

## EXCEPTIONS TO PIN COUNT DESIGNATORS

| DG & DGM SERIES | AD SERIES |
|---|---|
| **A** – 10 Pin Metal Can | **D** – 20,18,16 or 14 |
| **L** – 14 Pin Flatpack | **H** – 3 Pin |
| **P** – Ceramic DIP (Special Order Only) | **N** – 20,18,16 or 14 |
| **K** – CERDIP | |

## HIGH RELIABILITY DESIGNATOR

**JM38510/XXXXX-XXX** – Mil-M-38510 Device
**/883B** – Mil-STD-883B Screened Device
**/HR** – High Reliability Device
**/BR** – Cost Effective High Reliability Device
**/BI** – Burn-In Only Process Flow

## TEMPERATURE RANGE DESIGNATORS

**C** – Commercial 0°C to +70°C
**I** – Industrial: Either −25°C to +85°C or −40°C to +85°C (Specified on Datasheet)
**M** – Military −55°C to +125°C

## EXCEPTIONS TO TEMPERATURE RANGE DESIGNATORS

| DG & DGM SERIES | AD SERIES |
|---|---|
| **A** – Military: −55°C to +125°C | **A,B,C** – Industrial: −20°C to +85°C |
| **B** – Industrial: −20°C to +85°C | **J,K,L,M** – Commercial: 0°C to +70°C |
| **B** – Commercial: 0°C to +70°C | **S,T,U** – Military: −55°C to +125°C |

INTERSIL PRODUCTS


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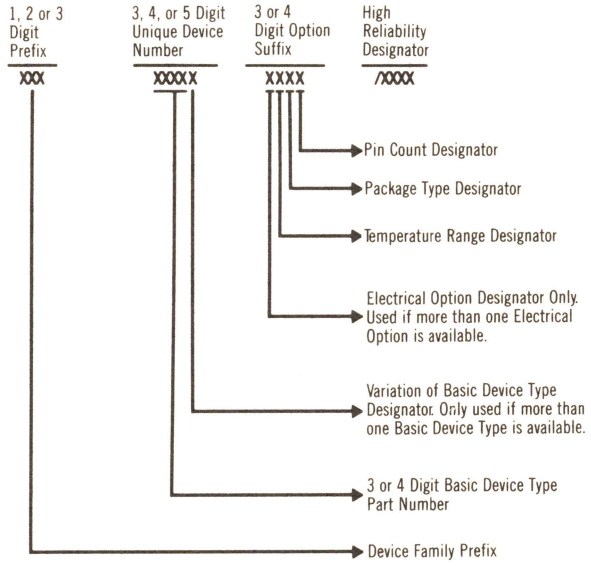
## PART NUMBERING SYSTEM

All Intersil Part Numbers consist of a Device Family Prefix, a Basic Numeric Part Number, and an Option Suffix, as follows:




## PART NUMBER SYSTEMS EXAMPLES

**1.** ICL7129CPL

- 40 Pins on Package
- Plastic Dual-In-Line Package
- 0°C to +70°C Temp. Range
- Basic Part Number: 7129 A/D Converter
- Linear IC Family Device

**2.** ICM7170IDG

- 24 Pins on Package
- Ceramic Dual-In-Line Package
- −40°C to +85°C Temp. Range
- Basic Part Number: 7170 Real Time Clock
- Microperipheral IC Family Device

**3.** IH5043BMFD

- 14 Pins on Package
- Ceramic Flat-Pack Package
- −55°C to +125°C Temp. Range
- B Type Electrical Option
- Basic Part Number: 5043 Analog Switch
- Hybrid IC Family Device

## PART NUMBER SYSTEMS EXAMPLES/CONTINUED

**4.** IH5009MJD/883B

- Mil-STD-883B Screened Device
- 14 Pins on Package
- CERDIP Dual-In-Line Package
- −55°C to +125°C Temp. Range
- Basic Part Number: 5009 Analog Switch
- Hybrid IC Family Device

**5.** JM38510/11107BEC

- Lead Finish — A-Hot Solder Dip, B-Tin Plate, C-Gold Plate
- Case Outline
- Device Class
- Detail Specification and Device Type
- Military Designator

**6.** ITSXXXX

- Four or Five Digit Number
- First Digit Indicator Product Family i.e.
  1 or 3-Discrete 7-Analog
  6-Linear 8-Data Acquisition
  9-Low Power
- Intersil Special–Normally Selected To an SCD

**7.** 65SXXX

- 2 or 3 Digit Number
- Intersil Digital Special–Normally Selected To an SCD

**8.** DG181AA

- Package — A-10 Pin Metal Can, L-14 Pin Flat Pack, P-Ceramic DIP (Special Order Only), K-CERDIP
- Temperature Range — A-Military, B-Industrial
- Device Type
- Analog Switch

**9.** AD7541TD

- 18 Pin CERDIP
- Mil Temp. Range
- Device Type
- Analog Devices
- Alternate Source

## INTERSIL CODE AND FSCM NUMBER INFORMATION

**CDPR**— Letter Code for Intersil Assigned by the U.S. Government
**32293**— Intersil FSCM Number Assigned by the U.S. Government

**INTERSIL PRODUCTS**



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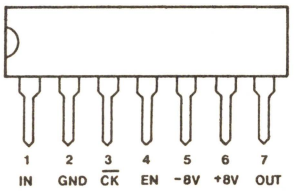
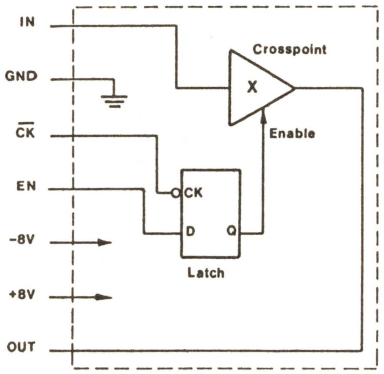
## MONOLITHIC 1×1 VIDEO CROSSPOINT SWITCH — LR401

- 30MHz bandwidth (±1.0dB)
- insertion loss 0.05dB at 100kHz
- frequency response DC to 10MHz I.L. ±0.05dB
- differential gain at 3.58 MHz 0.04% (max)
- differential phase at 3.58 MHz 0.02° (max)
- TTL and 5V CMOS compatible logic inputs compatible with all popular video standards
- 7-pin single-in-line package
- built-in enable latch allows synchronous selection



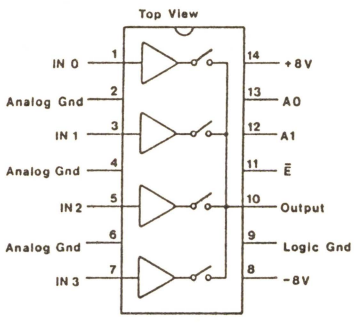

Pin–Out



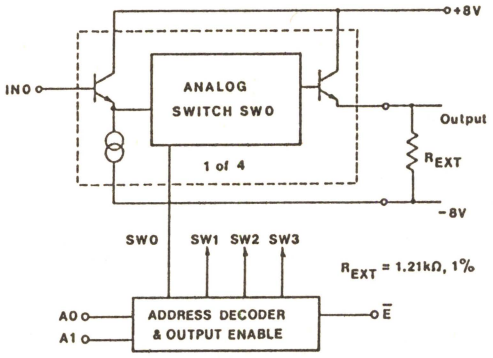

Simplified Block Diagram

## 4×1 VIDEO SWITCH — LR404

- 30 MHz bandwidth (±1.0dB)
- insertion loss 0.155dB (max)
- frequency response DC to 5MHz ± 0.05dB
- low all hostile crosstalk −86dB (typ) at 3.58MHz
- differential gain at 3.58MHz 0.05% (max)
- differential phase at 3.58MHz 0.05° (max)
- TTL and CMOS compatible logic inputs
- up to five LR404s can be paralleled for 20 inputs and a common output
- low cost 14 pin molded DIP package
- for NTSC, PAL, SECAM applications
- make before break switching




Pin–Out




Functional Schematic

Complete data and applications information is available. Call us toll-free 1-800-263-9353.

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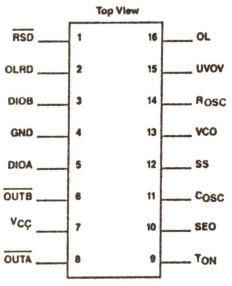
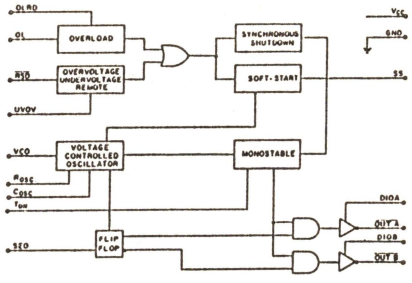
## RESONANT MODE POWER SUPPLY CONTROLLER – LD405

- frequency range of 10 kHz to 1 MHz.
- operating frequency range (min. and max.) set by a resistor and capacitor.
- pulse width set by a resistor and capacitor.
- synchronous overload shutdown with delayed restart.
- synchronous overvoltage, undervoltage and remote shutdown.
- soft start
- single ended or complementary outputs
- drives power MOSFETs directly.
- low cost 16 pin DIP.



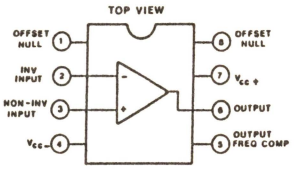

Pin–Out



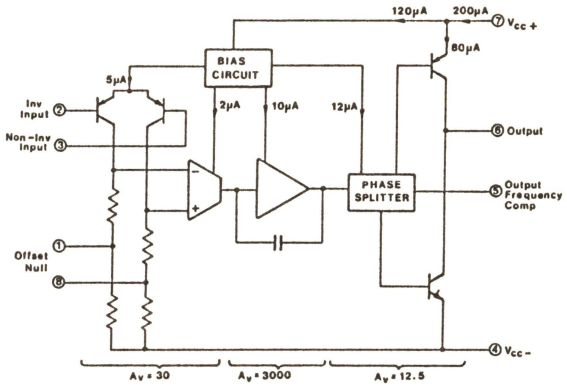

Functional Block Diagram

## LOW VOLTAGE, LOW POWER OPERATIONAL AMPLIFIER – LC810

- low voltage design — operates down to 1.0 V total supply voltage
- low power consumption — 200$\mu$A typical quiescent supply current
- single or dual supply operation
- class AB output stage swings virtually rail-to-rail



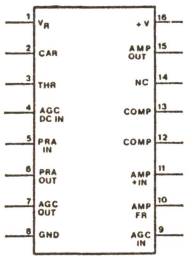

Pin–Out




Functional Schematic

## LOW DISTORTION AGC AMPLIFIER – LC403

- high stability of output level
- 34 dB AGC operating range
- adjustable AGC threshold
- adjustable attack and release time
- levels adjustable with external components
- can be operated as a voltage controlled gain amplifier
- two gain blocks may be used separately
- maximum frequency 100 kHz
- low carrier (threshold) detector
- operates from standard 5V power supply

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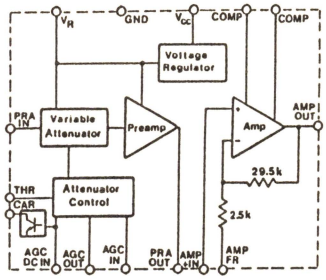


Functional Block Diagram

Complete data and applications information is available. Call us toll-free 1-800-263-9353.

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Gennum Corporation

# GENNUM
CORPORATION

Gennum Corporation is a public Canadian company begun in 1973 with less than twenty employees. Since then the enterprise has grown to an organization with one hundred and eighty employees and sales in excess of fifteen million dollars annually.

In 1986 Gennum Corporation formed an RF (radio frequency) product development group to bring to market integrated circuits to satisfy the rapidly expanding needs of the high frequency industry. This new business group fitted well with the company's other product groups which manufacture integrated circuits for a wide variety of industrial electronic systems such as communications, controls and medical systems. Now the first products from the RF group are coming to market designed to be applied in high frequency applications like cellular radio, radar, microwave and military electronic systems.

Gennum Corporation is located in Burlington, Ontario, a few miles West of Toronto. There the company operates two plants which form a complete facility for the manufacture of integrated circuits including product design and technology R&D, silicon diffusion, chip packaging, test and quality control.

## DMOS MONOLITHIC WIDEBAND RF AMPLIFIER 10-500 MHz - LB950

- **17 dBm output**
- **Single supply**
- **Low in/out return loss**
- **650 MHz, 3dB bandwidth**

### DESCRIPTION

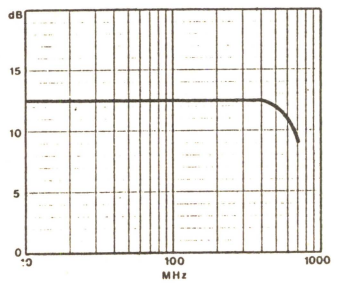
The LB950 monolithic RF amplifier is designed with LTI's LDMOS (Lateral, Double diffused MOS) technology. This unique process offers improved linearity and matching, and higher voltage and power capability when compared with conventional silicon bipolar approaches. This general purpose broadband amplifier is designed as a stable, cascadable gain block, with 50 ohm matched input and output, low distortion, and medium output power. All necessary passive elements, including inductors, have been implemented monolithically.

### TYPICAL SPECIFICATIONS

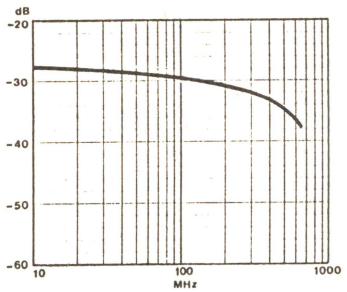
Electrical Characteristics

(at $V_{DD}$ = 12 V, $Z_S = Z_L = Z_O = 50\Omega$, $T_A = 25°$ C)

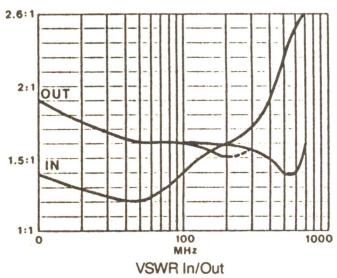
| | Test Conditions | LB950 |
|---|---|---|
| Frequency range | ± 1.0 dB<br>± 3.0 dB | 10–500 MHz<br>5–650 MHz |
| Insertion gain $S_{21}$ | 500 MHz | 12 dB |
| Noise figure | 10–500 MHz | 7.0 dB |
| Input VSWR | 10–500 MHz | < 2.2 : 1 |
| Output VSWR | 10–500 MHz | < 1.5 : 1 |
| 1 dB Gain compression | 500 MHz | 17 dBm |
| Third order intermodulation (0 dBm input) | | −40 dB |
| Recommended power (other supplies opt.) | | 12V, 100 mA |
| Packaging | | Stripline, TO5 |
| Reverse isolation $S_{12}$ | 10–500 MHz | > 25 dB |



Insertion Gain $S_{21}$



Reverse Isolation $S_{12}$



VSWR In/Out

Complete data and applications information is available. Call us toll-free 1-800-263-9353.

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GBL GigaBit Logic

# PICOLOGIC™ DIGITAL AND ANALOG GaAs ICs

## FEATURES

- **Industry's broadest family of GaAs ICs**
- DC to 3 GHz clock and data rates
- 150 ps output transition times
- 100 to 150 ps loaded gate delays
- Radiation hardness approaching $10^8$ rads
- Moderate power comparable to ECL 100K logic
- Demonstrated high reliability stemming from a higher activation energy (1.4 eV) than silicon ICs
- 0° to 85° commercial operating temperature range and extended Mil. temp. range (-55°C to +125°C) for some products
- ECL and GaAs compatible I/O levels and inherent TTL compatible outputs

| DEVICE DESCRIPTION | PART NO. | SPEED | PACKAGES* |
|---|---|---|---|
| GATES | | | |
| Quad 3 Input NOR | 10G000A | 290 ps | C,L,L36,F,X |
| Quad 2 Input NOR | 10G001 | 290 ps | C,L,L36,F,X |
| Quad 2-input XOR/XNOR and Line Receiver | 10G002 | 1.8 GHz | C,L,X |
| Dual AO/AOI 4-Wide 5,4,3,2 / 2-Wide 3,2 | 10G003 | 800 ps | C,L,X |
| DRIVERS/RECEIVERS/COMPARATORS | | | |
| Dual 2:1 Multiplexed Fanout Buffer | 10G010 | 1.5 GHz | C,L,X |
| Dual 1:4 Fanout Buffer | 10G011B | 1.6 GHz | C,L,L36,X |
| Dual Complementary Driver/Comparator | 10G012B/ 10G013 | 1.75 GHz | C,L,L36,F,X |
| FLIP FLOPS AND REGISTERS | | | |
| Dual Precision D Flip Flop | 10G021A | 2.7 GHz | C,L,L36,F,X |
| Octal Register/Shift Register and PN Code Generator | 10G022 | 1.5 GHz | C,L,X |
| Quad D Flip Flop With 2:1 Muxed Inputs | 10G023 | 1.9 GHz | C,L,X |
| Quad D Flip Flop With XOR Inputs | 10G024 | 1.9 GHz | C,L,X |
| REGISTER FILES | | | |
| 16 X 4 3-Port Register File (1Q88) | 10G030 | 1 ns | C,L,X |
| MULTIPLEXERS/DEMULTIPLEXERS | | | |
| Quad 2:1 MUX | 10G004 | 1.8 GHz | C,L,X |
| 3:8 or Dual 2:4 Decoder/DEMUX | 10G044 | 650 ps | C,L,X |
| Quad 4:1 or Dual 8:1 MUX | 10G046 | 600 ps | C,L,X |
| COUNTERS/PRESCALERS | | | |
| 2-Stage Ripple Counter/Divider | 10G060 | 3.0 GHz | F,L36,X |
| 4-Bit Synchronous Programmable Counter | 10G061 | 1.3 GHz | C,L,X |
| 7-Stage Ripple Counter/Divider | 10G065 | 3.0 GHz | F,L36,X |
| Variable Modulus Divider | 10G070 | 2.0 GHz | F,L36,X |
| ARITHMETIC OPERATORS | | | |
| Dual 9-Bit Parity Generator/Checker and 8-Bit Equivalence Checker | 10G045 | 850 ps | C,L,X |
| High Speed 4-Bit Adder | 10G100 | 1200 ps | C,L,X |
| Carry Lookahead Generator | 10G101 | 675 ps | C,L,X |
| 4-Bit ALU (10181 ECL Equivalent, 1Q88) | 10G181 | 2 ns | C,L,X |
| MONOLITHIC FET AND DIODE ARRAYS | | | |
| 15 mA Schottky Diode Array | 16G010 | | F,L36,X |
| 100 mA Schottky Diode Array | 16G011 | | F,L36,X |
| Single Gate MESFET Array | 16G020 | 15 GHz | F,L36,X |
| Dual Gate MESFET Array | 16G021 | 15 GHz | F,L36,X |
| ANALOG & FIBER COMMUNICATION PRODUCTS | | | |
| 8:1 Time Division MUX | 10G040A | 1.5 Gb/s | C,L,X |
| 1:8 Time Division DEMUX | 10G041A | 1.5 Gb/s | C,L,X |
| Clock and Data Recovery Circuit | 16G040 | 2.4 Gb/s | C,L,X,H |
| 16G040 Demo Board | 90GCDR | 800 Mb/s | Board |
| Phase/Frequency Comparator | 16G044 | 1.0 GHz | C,L,X |
| Time Delay Generator (1Q 88) | 16G060 | 20 ns Prog. Delay 1 ps resolution | C,L,X |
| Pin Driver (1Q 88) | 16G061 | 1.0 GHz | C,L,X |

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GigaBit Logic Inc.

GigaBit Logic

# NANORAM™ & NANOROM™ MEMORY

**NanoRam™ Features**

- 256 X 4-bit organization
- Equal read and write cycle times
- Fully registered design with 3 selectable output register modes
- Internally generated write pulse (self-timed)
- ECL/GaAs compatible
- Wire-OR output capability

**NanoRom™ Features**

- 512 X 8-bit organization
- 500 ps typical OE access time
- ECL compatible power supplies
- ECL/GaAs compatible I/O levels
- Wire-OR output capability
- On-chip OE decoder (14GD048)

| DEVICE DESCRIPTION | PART NO. | SPEED | PACKAGES* |
|---|---|---|---|
| 256 X 4-bit Registered Self-Timed RAM | 12G014-2 | 2.5 ns cycle time | C,L,X |
| 256 X 4-bit Registered Self-Timed RAM | 12G014-3 | 3.5 ns cycle time | C,L,X |
| 512 X 8-bit Mask Programmable ROM | 14GM048 | 1.5 ns address access | C,L,X |
| 512 X 8-bit Mask Programmable ROM w/on-chip decoder | 14GD048 | 1.5 ns address access | C,L,X |

# PROTOTYPING AND SUPPORT PRODUCTS

**PROTOTYPE DEVELOPMENT KIT**

- Complete kit for prototyping and testing all GigaBit GaAs ICs
- Low cost, quick turnaround solution to initial device performance testing and evaluation needs
- Compatible with all GigaBit package styles
- Kit components available separately for expanded applications
- 90GUPB Universal Printed Circuit Board accepts up to eight GigaBit Logic GaAs surface mount ICs and up to eight 300 or 400 mil wide DIP ICs
- Supports signals with 100 ps rise and fall times and up to 3 GHZ clock rate

| | PART # | DESCRIPTION |
|---|---|---|
| PROTOTYPE DEVELOPMENT KIT | 90GUPK | Contains 1 90GUPB, 1 90G102, 1 10GBPS, 2 90G101. Board standoffs and power supply connectors included. |
| KIT ACCESSORIES | 90GUPB<br>90G101<br>90G102 | Universal Prototyping Board.<br>Package of 5 right angle SMA connectors for 90GUPB mounting.<br>Components package for 90GUPB (20 ea. chip resistors, capacitors, 2.5' coax). |
| OTHER PROTOTYPING AND SUPPORT PRODUCTS | 90GSKT-40L<br>90GHS40A/B<br>90GHS36A | Package of 5 high speed sockets for 40 I/O "L" package . Mounts on 90GUPB.<br>Heatsinks for 40 I/O "L" and "C" package.<br>Heatsink for 36 I/O "F" and "L36" package. |

GigaBit Logic Inc.

# APPLICATION NOTES

AB-1 Application and Performance of GigaBit's 40 I/O Chip Carrier
AB-2 Minimizing Clock Skew Through Use of the 10G010 and 10G011B Fanout Buffer
AN-2 Guidelines for the Use of Digital GaAs ICs
AN-3 Thermal Management of PicoLogic™ and NanoRam™ GaAs Digital IC Families
AN-4 Interfacing PicoLogic™ and NanoRam™ ICs to Other Logic Families
AN-5 Guidelines for the Use of the 12G014 400 MHz Registered RAM
AN-6 Applying the 10G061 as a Universal Programmable Counter

RELIABILITY AND QUALITY ASSURANCE
GaAs Reliability and Quality Assurance Handbook

# ARTICLE REPRINTS

- Integrated Circuits: the case for gallium arsenide
AR-5 CDFL Circuit Approach for GaAs D-MESFET ICs
AR-6 Pipelined static RAM Endows Cache Memories with 1ns Speed
AR-11 GaAs Digital ICs Impact Fiber System Design
AR-12 The First GaAs Compiler is Already Producing Chips
AR-13 Standard Cells Libraries Simplify GaAs Design
AR-14 GaAs Integrated Circuit Manufacturing Comes of Age
AR-15 An Ultra-High Performance Manufacturable GaAs E/D Process
AR-16 Cray-3: A GaAs Implemented Supercomputer System
AR-17 Baseline Reliability of Commercial Gallium Arsenide ICs
AR-18 Launching GaAs Wafer Fab Technology Into LSI
AR-19 Two Applications for the 10G024 Quad GaAs Flip Flop
AR-20 Compiled Gallium Arsenide ASICs

# *AVAILABLE PACKAGES

- C = 40 I/O C-Leaded Chip Carrier
- L = 40 I/O Leadless Chip Carrier
- F = 36 I/O Flat Package
- L36* = 36 I/O Leadless Chip Carrier
- X = Unpackaged Dice
- H = Hybrid Package

*Note: Character "36" not marked on package

# GIGABIT SALES OFFICES

| WEST | CENTRAL | EAST |
|---|---|---|
| GigaBit Logic Inc.<br>1908 Oak Terrace Ln.<br>Newbury Park, CA<br>91320<br>Tel: (805) 499-0610 | GigaBit Logic Inc.<br>5001 W.80th. St.<br>Suite 790<br>Bloomington, MN<br>55437<br>Tel: (612) 831-0886 | GigaBit Logic Inc.<br>945 Concord St.<br>Suite 217<br>Framingham, MA<br>01701<br>Tel: (617) 626-0241 |

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# Z80 FAMILY

## • Z80® CPU/ Central Processing Unit

| Part Number | FEATURE |
|---|---|
| Z8400 | • 158 instructions, 8080A software compatibility<br>• 8 MHz, 6 MHz, 4 MHz and 2.5 MHz clocks for the Z80H, Z80B, Z80A and Z80<br>• The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers together with indexed and relative addressing.<br>• The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system to be daisy-chained.<br>• Duplicate sets of both general-purpose and flag registers, two 16-bit index registers.<br>• On-chip dynamic memory refresh counter. |

## • Z80® PIO/ Parallel Input/ Output Controller

| Part Number | FEATURE |
|---|---|
| Z8420 | • A direct interface between Z80 microcomputer systems and peripheral devices.<br>• Both ports have interrupt-driven handshake for fast response.<br>• 4 programmable operating modes: byte input, byte output, byte input/output (Port A only), and bit input/output.<br>• Programmable interrupts on peripheral status conditions.<br>• Standard Z80 Family bus-request and prioritized interrupt request daisy-chain implemented without external logic.<br>• Port B outputs can drive Darlington transistors (1.5 mA 1.5V) |

## • Z80® CTC/ Counter/ Timer Circuit

| Part Number | FEATURE |
|---|---|
| Z8430 | • Four independently programmable counter/timer channels<br>• Zero Count/Timeout outputs capable of driving Darlington transistors.<br>• Selectable positive or negative trigger initiates timer operation.<br>• Standard Z80 Family daisy-chain interrupt structure.<br>• Interfaces directly to the Z80 CPU or for baud rate generation to the Z80 SIO |

## • Z80® SIO/ Serial Input/ Output Controller

| Part Number | FEATURE |
|---|---|
| Z8440 | • 2 independent full-duplex channels, with separate control and status lines for modems or other devices.<br>• Data rates of 0 to 800K bits/second in the ×1 clock mode.<br>• Synchronous protocols and Asynchronous protocols.<br>• Receiver data registers quadruply buffered transmitter registers doubly buffered.<br>• Highly sophisticated and flexible daisy-chain interrupt vector |

## • Z80® DART/ Dual Asynchronous Receiver/ Transmitter

| Part Number | FEATURE |
|---|---|
| Z8470 | • 2 independent full-duplex channels with separate modem controls.<br>• In ×1 clock mode, data rates are 0 to 800K bits/second with Z80A DART.<br>• Receiver data registers are quadruply buffered; the transmitter is doubly buffered<br>• Programmable options include 1½ or 2 stop bits; even, odd or no parity: and ×1, ×16, ×32 and ×64 clock modes.<br>• On-chip logic for ring indication and carrier detect status. |

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# RAMs, ROMs

## • Static RAM

| Process | Organization | Part Number | Access Time | Power Supply Current | | Package Type |
|---|---|---|---|---|---|---|
| | | | | Operating | Standby | |
| CMOS | 2,048×8 | GM76C28-35 | 35NS | 100 mA | 20 mA | 24 DIP |
| | | GM76C28-45 | 45NS | | | |
| | | GM76C28-55 | 55NS | | | |
| | 8,192×8 | GM76C88-60 | 60NS | 110 mA | 3 mA | 28 DIP |
| | | GM76C88-70 | 70NS | | | |
| | | GM76C88-85 | 85NS | | | |
| | 65,536×1 | GM76C64-45 | 45NS | 70 mA | 5 mA | 22 DIP |
| | | GM76C64-55 | 55NS | | | |
| | | GM76C64-70 | 70NS | | | |
| | 16,384×4 | GM76C164-25 | 25NS | 100 mA | 20 mA | 22 DIP |
| | | GM76C164-35 | 35NS | | | |
| | | GM76C164-45 | 45NS | | | |
| | 32,768×8 | GM76C256-45 | 45NS | 100 mA | 20 mA | 28 DIP |
| | | GM76C256-55 | 55NS | | | |

* Under Development

## • Dynamic RAM

| Process | Organization | Part Number | Access Time | Power Supply Current | | Package Type |
|---|---|---|---|---|---|---|
| | | | | Operating | Standby | |
| NMOS | 65,536×1 | GM7164-10 | 100NS | 330 mA | 22 mA | 16 DIP |
| | | GM7164-12 | 120NS | | | |
| | | GM7164-15 | 150NS | | | |
| | 1,048,576×1 | GM7C1024-60 | 60NS | 60 mA | 3 mA | 18 DIP |
| | | GM7C1024-80 | 80NS | | | |

## • EPROM, ROM

| Process | Organization | Part Number | Access Time | Power Supply Current | | Package Type |
|---|---|---|---|---|---|---|
| | | | | Operating | Standby | |
| CMOS EPROM | 8,192×8 | GM57HC64-35 | 35NS | 100 mA (Max.) | | 24 DIP* |
| | | GM57HC64-45 | 45NS | | | |
| | | GM57HC64-55 | 55NS | | | |
| NMOS ROM | 65,536×8 | GM23512-10 | 100NS | 100 mA (Max.) | 20 mA (Max.) | 28 DIP* |
| | | GM23512-15 | 150NS | | | |
| | | GM23512-20 | 200NS | | | |
| | 131,072×8 | GM231024-20 | 200NS | 100 mA (Max.) | 20 mA (Max.) | |
| | | GM231024-25 | 250NS | | | |
| | | GM231000-25 | 250NS | | | |

* Industry PROM Pin Compatible

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# LOW POWER SCHOTTKY/SCHOTTKY TTL GD74LS/S

## • Low Power Schottky TTL

| PART NO | FUNCTION |
|---|---|
| GD74LS00 | Quad 2-Input NAND Gate |
| GD74LS02 | Quad 2-Input NOR Gate |
| GD74LS04 | Hex Inverter |
| GD74LS05 | Hex Inverter, OC |
| GD74LS06 | Hex Inverter Buffer/Driver, OC (30V) |
| GD74LS07 | Hex Buffer/Driver, OC (30V) |
| GD74LS08 | Quad 2-Input AND Gate |
| GD74LS09 | Quad 2-Input AND Gate, OC |
| GD74LS10 | Triple 3-Input NAND Gate |
| GD74LS11 | Triple 3-Input AND Gate |
| GD74LS14 | Hex Schmitt Trigger Inverter |
| GD74LS16 | Hex Inverter Buffer/Driver, OC (15V) |
| GD74LS17 | Hex Buffer/Driver, OC (15V) |
| GD74LS20 | Dual 4-Input NAND Gate |
| GD74LS21 | Dual 4-Input AND Gate |
| GD74LS26 | Quad 2-Input NAND Gate |
| GD74LS27 | Triple 3-Input NOR Gate |
| GD74LS30 | 8-Input NAND Gate |
| GD74LS32 | Quad 2-Input OR Gate |
| GD74LS38 | Quad 2-Input NAND Buffer, OC |
| GD74LS42 | BCD-to-Decimal Decoder |
| GD74LS51 | Dual 2-Wide 2-Input AND-OR-Invert Gate |
| GD74LS55 | 2-Wide 2-Input AND-OR-Invert |
| GD74LS73 | Dual J-K Master-Slave Flip-Flop |
| GD74LS74A | Dual D-Type Positive Edge-Triggered Flip-Flop |
| GD74LS75 | 4-Bit Bistable Latch |
| GD74LS85 | 4-Bit Magnitude Comparator |
| GD74LS86 | Quad 2-Input Exclusive-OR Gate |
| GD74LS90 | Decade Counter |
| GD74LS92 | Divide-by-12 Counter |
| GD74LS93 | 4-Bit Binary Counter |
| GD74LS95 | 4-Bit Shift Register (PIPO) |
| GD74LS107 | Dual J-K Master-Slave Flip-Flop |
| GD74LS109 | Dual J-K Positive Edge-Triggered Flip-Flop |
| GD74LS112 | Dual J-K Negative Edge-Triggered F/F |
| GD74LS123 | Dual monostable multivibrator with clear |
| GD74LS125A | Quad 3-State Buffer |
| GD74LS132 | Quad 2-Input Schmitt NAND Gate |
| GD74LS138 | 3-to-8 Decoder/Demultiplexer |
| GD74LS139 | Dual 2-to-4 Decoder/Demultiplexer |
| GD74LS145 | BCD-to-Decimal Decoder/Driver, |
| GD74LS148 | 8 Line to-3 Line Priority Encoder |
| GD74LS151 | 8-to-1 Multiplexer |
| GD74LS153 | Dual 4-to-1 Multiplexer |
| GD74LS154 | 4-to-16 Decoder/Demultiplexer |
| GD74LS155 | Dual 2-to-4 Decoder/Demultiplexer |
| GD74LS157 | Quad 2-to-1 Multiplexer |
| GD74LS158 | Quad 2-to-1 Multiplexer (Inverting) |

| PART NO | FUNCTION |
|---|---|
| GD74LS161A | Synchronous 4-Bit Binary Counter |
| GD74LS163A | Synchronous 4-Bit Binary Counter |
| GD74LS164 | 8-Bit SIPO Shift Register |
| GD74LS165 | 8-Bit PISO Shift Register |
| GD74LS166 | 8-Bit PIPO Shift Register |
| GD74LS174 | Hex. D-Type Flip-Flop with Clear |
| GD74LS175 | Quad D-Type Flip-Flop with Clear |
| GD74LS191 | 4-Bit Binary Up/Down Counter |
| GD74LS193 | 4-Bit Binary Up/Down Counter with clear |
| GD74LS194A | 4-Bit Bidirectional Shift Register (PIPO) |
| GD74LS195 | 4-Bit Parallel-Access Shift Register |
| GD74LS221 | Dual Monostable Multivibrator |
| GD74LS240 | Octal 3-State Buffer (Inverting) |
| GD74LS241 | Octal 3-State Buffer (Noninverting) |
| GD74LS243 | Quad Bus Transceiver |
| GD74LS244 | Octal 3-State Buffer |
| GD74LS245 | Octal Bus Transceiver, 3 State |
| GD74LS251 | 8-to-1 Multiplexer, 3-State |
| GD74LS257A | Quad 2-to-1 Multiplexer, 3-State |
| GD74LS258 | Quad 2-to-1 Multiplexer, 3-State (Inverting) |
| GD74LS259 | 8-Bit Addressable Latch |
| GD74LS273 | Octal D Flip-Flop |
| GD74LS280 | 9-Bit Odd/Even Parity Generator / Checker |
| GD74LS283 | 4-Bit Binary Full Adder |
| GD74LS298 | Quadruple 2-Input Multiplexer with Storage |
| GD74LS299 | 8-Bit Shift/Storage Register, 3 State |
| GD74LS322 | 8-Bit Shift Register, with Sign Extend |
| GD74LS365A | Hex bus buffer, 3 state |
| GD74LS366 | Hex bus buffer (Inverting) |
| GD74LS367A | Hex bus buffer 3-state |
| GD74LS368 | Hex Inverter bus Driver, 3-state |
| GD74LS373 | Octal Latch, 3-State |
| GD74LS374 | Octal D Flip-Flop, 3-State |
| GD74LS377 | Octal D-Type Flip-Flop with Enable |
| GD74LS390 | Dual Decade Counter |
| GD74LS393 | Dual Binary Counter |
| GD74LS395A | 4-Bit Cascadable Shift Register, 3-State |
| GD74LS590 | 8-Bit Binary Counter with Output Register, 3 State |
| GD74LS612 | Memory Mappers, 3-state Map Output |
| GD74LS640 | Octal bus transceiver 3-state |
| GD74LS646 | Octal bus transceiver/register |
| GS74LS688 | 8-Bit Magnitude Comparator |
| GD74LS670 | 4 word×4 bit register file 3-state |

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# LOW POWER SCHOTTKY/SCHOTTKY TTL GD74LS/S

## • Schottky TTL

| PART NO | FUNCTION |
|---|---|
| GD74S00 | Quad 2-Input NAND Gate |
| GD74S02 | Quad 2-Input NOR Gate |
| GD74S04 | Hex Inverter |
| GD74S05 | Hex Inverter, OC |
| GD74S08 | Quad 2-Input AND Gate |
| GD74S10 | Triple 3-Input NAND Gate |
| GD74S20 | Dual 4-Input NAND Gate |
| GD74S30 | 8-Input NAND |
| GD74S32 | Quad 2-Input OR Gate |
| GD74S51 | Dual 2-Wide 2-Input AND-OR-Invert Gate |
| GD74S64 | 4-2-3-2 Input AND-OR-Invert Gate |
| GD74S74 | Dual D-Type Positive Edge-Triggered Flip-Flop |
| GD74S85 | 4 Bit Magnitude Comparator |
| GD74S86 | Quad 2-Input Exclusive-OR Gate |
| GD74S112 | Dual J-K Negative Edge-Triggered Flip-Flop |
| GD74S133 | 13-Input NAND Gate |
| GD74S138 | 3-to-8 Decoder/Demultiplexer |
| GD74S139 | Dual 2-to-4 Decoder/Demultiplexer |
| GD74S153 | Dual 4-to-1 Multiplexer |
| GD74S157 | Quad 2-to-1 Multiplexer |
| GD74S163 | Synchronous 4-Bit Binary Counter |
| GD74S164 | 8-Bit Parallel Output Serial Shift Register |
| GD74S169 | 4-Bit Up/Down Binary Counter |
| GD74S174 | Hex D-Type Flip-Flop with Clear |
| GD74S175 | Quad D-Type Flip-Flop |
| GD74S240 | Octal 3-State Buffer (Inverting) |
| GD74S251 | 8-to-1 Multiplexer, 3-State |
| GD74S257 | Quad Data Select/MUX, Noninverted |
| GD74S280 | 9-Bit Odd/Even parity Generator/ Checker |
| GD74S299 | 8-Bit Shift/Storage Register, 3-State |
| GD74S374 | Octal D Flip-Flop, 3-State |

Suffix: Blank ··· Plastic, J ··· Ceramic, D ··· Small Outline Package

## • Miscellaneous

| PART NO | FUNCTION |
|---|---|
| GD75188 | Line Driver |
| GD75189A | Line Receiver |
| GD8T28 | 4-Bit Paralle Bus Transceiver |
| GD8T26 | 4-Bit Transceiver |
| GD8T26A | 4-Bit Parallel Bus Transceiver |
| GD9620 | I/Q Parallel Sixteen 8 Bit Ports |
| GD8307 | Bidirectional Bus Transceiver |
| GD25LS2520 | Octal D Register: Common Clear and Enable, 3 State |
| GD25LS2548 | 3-Line to 8-Line Decoder/Demultiplexer |
| GD75150 | Octal Line Driver |
| GD75154 | Octal Line Receiver |
| GD26LS29 | Quad Line Driver |
| GD26LS31 | Quad Diff Line Driver |
| GD26LS32 | Quad Diff. Line Receiver |
| GD26LS33 | Quad Diff. Line Receiver |

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# HIGH SPEED CMOS LOGIC

## • 74HC/HCT/HCU

| PART NO | FUNCTION |
|---|---|
| HC/HCT00 | Quad 2-Input NAND gates |
| HC/HCT02 | Quad 2-Input NOR gates |
| HC/HCT03 | Quad 2-Input NAND gates with Open Drain |
| HC/HCT04 | Hex Inverters |
| HCU 04 | Hex Unbuffered Inverters |
| HC/HCT05 | Hex Inverter with Open Drain |
| HC/HCT08 | Quad 2-Input AND gates |
| HC/HCT09 | Quad 2-Input AND gates with Open Drain |
| HC/HCT10 | Triple 3-Input NAND gates |
| HC/HCT11 | Triple 3-Input AND gates |
| HC/HCT14 | Hex Schmitt Trigger Inverters |
| HC/HCT20 | Dual 4-Input NAND gates |
| HC/HCT21 | Dual 4-Input AND gates |
| HC/HCT27 | Triple 3-Input NOR gates |
| HC/HCT30 | 8-Input NAND gates |
| HC/HCT32 | Quad 2-Input OR gates |
| HC/HCT34 | Hex Buffers |
| HC/HCT42 | 1 of 10 Decoder (BCD to Decimal) |
| HC/HCT51 | 2-Wide 2-Input & 2-Wide 3-Input AND-OR invert gates |
| HC/HCT58 | 2-Wide 2-Input & 2-Wide 3-Input AND-OR gates |
| HC/HCT73 | Dual JK F/Fs with Clear |
| HC/HCT74 | Dual D Type Positive Edge Triggered F/Fs with Preset & Clear |
| HC/HCT75 | Dual 2-Bit(4-Bit) Bistable Latches |
| HC/HCT76 | Dual JK F/Fs with Preset & Clear |
| HC/HCT85 | 4 Bit Magnitude Comparator |
| HC/HCT86 | Quad 2-Input Exclusive OR gates |
| HC/HCT93 | 4 Bit Binary Ripple Counter |
| HC/HCT107 | Dual JK F/Fs with Clear |
| HC/HCT109 | Dual JK F/Fs with Preset & Clear |
| HC/HCT112 | Dual JK F/Fs with Preset & Clear |
| HC/HCT113 | Dual JK F/Fs with Preset |
| HC/HCT123 | Dual Retriggerable Monostable Multivibrators |
| HC/HCT125* | Quad 3-State(Active-Low) Noninverting Buffer |
| HC/HCT126* | Quad 3-State(Active-High) Noninverting Buffer |
| HC/HCT132 | Quad 2-Input Schmitt Trigger NAND gates |
| HC/HCT133 | 13-Input NAND gate |
| HC/HCT137 | 3 to 8 Line Decoder/Demultiplexer with Address Latch |
| HC/HCT138 | 3 to 8 Line Decoder/Demultiplexer |
| HC/HCT139 | Dual 2 to 4 Line Decoder/Demultiplexer |
| HC/HCT147 | 10 to 4 Line (Decimal to BCD) Priority Encoder |
| HC/HCT148 | 8-to-3 Line Priority Encoder |
| HC/HCT151 | 8-to-1 Line Data Selector/Multiplexer |
| HC/HCT153 | Dual 4-to-1 Line Selector |
| HC/HCT154 | 4-to-16 Line Decoder/Demultiplexer |
| HC/HCT155 | Dual 2-to-4 Line Decoder/Demultiplexer |
| HC/HCT157 | Quad 2-Input Selectors/Multiplexers with Noninverted Outputs |
| HC/HCT158 | Quad 2-Input Selectors/Multiplexers with Inverted Outputs |
| HC/HCT160 | Sync. Decade Counter with Asyn. Clear |
| HC/HCT161 | Sync. Binary Counter with Asyn. Clear |
| HC/HCT162 | Sync. BCD Decade Counter with Sync. Clear |
| HC/HCT163 | Sync. Binary Counter with Sync. Clear |
| HC/HCT164 | 8 Bit Serial-In/Parallel-Out Shift Counter |
| HC/HCT165 | 8 Bit Parallel-In/Serial-Out Shift Counter |
| HC/HCT166 | 8 Bit Serial or Parallel-In/Serial-Out Shift Reg. with Clear |
| HC/HCT173* | Quad 3 State D Type F/Fs with Common Clock & Clear |

* Types with a bus-driver outputs stage.

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# HIGH SPEED CMOS LOGIC

## • 74HC/HCT

| PART NO | FUNCTION |
|---|---|
| HC/HCT174 | Hex D Type F/Fs with Common Clock & Clear |
| HC/HCT175 | Quad D Type F/Fs with Clear |
| HC/HCT190 | Sync. Decade U/D Counter with Mode Control |
| HC/HCT191 | Sync. 4 Bit Binary U/D Counter with Mode Control |
| HC/HCT192 | Sync. Decade U/D Counter with Clear & Dual Clocks |
| HC/HCT193 | Sync. 4 Bit Binary U/D Counter with Clear & Dual Clocks |
| HC/HCT194 | 4 Bit Bidirectional Universal Shift Reg. |
| HC/HCT195 | 4 Bit Parallel Access Shift Reg. |
| HC/HCT221 | Dual Non-Retriggerable Monostable Multivibrators |
| HC/HCT240* | Octal Inverting 3 State Buffers |
| HC/HCT241* | Octal Noninverting 3 State Buffers |
| HC/HCT242* | Quad Inverting 3 State Transceivers |
| HC/HCT243* | Quad Noninverting 3 State Transceivers |
| HC/HCT244* | Octal Noninverting 3 State Buffers |
| HC/HCT245* | Octal Noninverting 3 State Transceivers |
| HC/HCT251 | 8-to-1 Line Selectors/Multiplexer with 3 State |
| HC/HCT253* | Dual 4-to-1 Line Data Selectors/Multiplexer with 3 State |
| HC/HCT257* | Quad 2-to-1 Data Selectors/Multiplexer with 3 State |
| HC/HCT258 | Quad 2-Input Selectors |
| HC/HCT259 | 8 Bit Addressable Latch/3-to-8 Line Decoder |
| HC/HCT266 | Quad 2 Input Exclusive NOR gate |
| HC/HCT273 | Octal D F/Fs with Common Clock & Clear |
| HC/HCT280 | 9 Bit Odd/Even Parity Generator/Checker |
| HC/HCT283 | 4 Bit Binary Full Adder with Fast Carry |
| HC/HCT298 | Quad 2-Input Multiplexers with Output Latch |
| HC/HCT299* | 8 Bit 3 State Universal Shift Reg. |
| HC/HCT322* | 8 Bit 3 State Reg with Sign Extend |
| HC/HCT354* | Dual 4-to-1 Line Multiplexers with Latches & 3 State |
| HC/HCT356* | Dual 4-to-1 Line Multiplexers/Reg. |
| HC/HCT365* | Hex 3 State Noninverting Buffers |
| HC/HCT366* | Hex 3 State Inverting Buffers |
| HC/HCT367* | Hex 3 State Noninverting Buffers |
| HC/HCT368* | Hex 3 State Inverting Buffers |
| HC/HCT373* | Octal 3 State Noninverting D Type Transparent Latches |
| HC/HCT374* | Octal 3 State Noninverting D Type F/Fs |
| HC/HCT377 | Octal D Type F/Fs with Common Clock & Enable |
| HC/HCT386 | Quad 2-Input Exclusive OR gates |
| HC/HCT390 | Dual 4 Bit Decade Counter |
| HC/HCT393 | Dual 4 Bit Binary Counter |
| HC/HCT423 | Dual Retriggerable Monostable Multivibrators |
| HC/HCT533* | Octal 3 State Inverting D Type Transparent Latches |
| HC/HCT534* | Octal 3 State Inverting D Type F/Fs |
| HC/HCT540* | Octal Inverting 3 State Buffers |
| HC/HCT541* | Octal Noninverting 3 State Buffers |
| HC/HCT563* | Octal 3 State Inverting D Type Transparent Latches |
| HC/HCT564* | Octal 3 State Inverting Transceivers & D Type F/Fs |
| HC/HCT573* | Octal 3 State Noninverting & D Type F/Fs |
| HC/HCT574* | Octal 3 State Noninverting D Type F/Fs |
| HC/HCT590 | 8 Bit Binary Counter with 3 State Transceivers |
| HC/HCT640* | Octal Inverting 3 State Transceivers |
| HC/HCT643* | Octal Inverting & Noninverting 3 State Transceivers |
| HC/HCT646* | Octal 3 State Noninverting Transceivers & D Type F/Fs |
| HC/HCT648* | Octal 3 State Inverting Transceivers & D Type F/Fs |
| HC/HCT670* | 4 By 4 Reg File with 3 State |
| HC/HCT688 | 8 Bit Magnitude Comparator/Equality Detector |

Suffix: Blank ··· Plastic DIP
J ··· Ceramic DIP
D ··· Small Outline Package

Standard Z80 Family bus-request and prioritized interrupt request daisy-chain implemented without external logic.

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# CMOS 4000B SERIES

| PART NO | FUNCTION |
|---|---|
| GD4001B | Quad 2-Input NOR Gate |
| GD4002B | Dual 4-Input NOR Gate |
| GD4006B | 18-Stage Static Shift Register |
| GD4007UB | Dual Complementary Pair Plus Inverter |
| GD4008B | 4-Bit Binary Full Adder |
| GD4011B | Quad 2-Input NAND Gate |
| GD4012B | Dual 4-Input NAND Gate |
| GD4013B | Dual D Flip-Flop |
| GD4014B | 8-Bit Shift Register |
| GD4015B | Dual 4-Bit Shift Register |
| GD4016B | Quad Bilateral Switch |
| GD4017B | 5-Stage Johnson Decade Counter |
| GD4018B | Presettable Divide-by-N Counter |
| GD4019B | Quad 2-Input Multiplexer |
| GD4020B | 14-State Binary Counter |
| GD4021B | 8-Bit Shift Register |
| GD4022B | 4-State Divide-by-8 Johnson Counter |
| GD4023B | Triple 3-Input NAND Gate |
| GD4024B | 7-State Binary Counter |
| GD4025B | Triple 3-Input NOR Gate |
| GD4027B | Dual JK Flip-Flop |
| GD4028B | 1-of-10 Decoder |
| GD4029B | Synchronous Up/Down, Binary/Decade Counter |
| GD4030B | Quad Exclusive-OR Gate |
| GD4031B | 64-Stage Static Shift Register |
| GD4034B | 8-Bit Universal Bus Register |
| GD4035B | 4-Bit Universal Shift Register |
| GD4040B | 12-Stage Binary Counter |
| GD4041B | Quad True/Complement Buffer |
| GD4042B | Quad D Latch |
| GD4043B | Quad R/S Latch with 3-State Outputs |
| GD4044B | Quad R/S Latch with 3-State Outputs |
| GD4045B | 21-Stage binary Counter |
| GD4046B | Micropower Phase-Locked Loop |
| GD4047B | Low Power Monostable/Astable Multivibrator |
| GD4049B | Hex Inverting Buffer |
| GD4050B | Hex Non-Inverting Buffer |
| GD4051B | 8-Channel Analog Multiplexer/Demultiplexer |
| GD4052B | Dual 4-Channel Analog Multiplexer/Demultiplexer |
| GD4053B | Triple 2-Channel Analog Multiplexer/Demultiplexer |
| GD4066B | Quad Bilateral Switch |
| GD4067B | 16-Channel Analog Multiplexer/Demultiplexer |
| GD4068B | 8-Input NAND Gate |
| GD4069UB | Hex Inverter |
| GD4070B | Quad Exclusive-OR Gate |
| GD4071B | Quad 2-Input OR Gate |
| GD4072B | Dual 4-Input OR Gate |
| GD4073B | Triple 3-Input AND Gate |
| GD4075B | Triple 3-Input OR Gate |
| GD4076B | Quad D Flip-Flop with 3-State Outputs |
| GD4077B | Quad Exclusive-NOR Gate |
| GD4078B | 8-Input NOR Gate |
| GD4081B | Quad 2-Input AND Gate |
| GD4082B | Dual 4-Input AND Gate |
| GD4085B | Dual 2-Wide, 2-Input AND-OR-Invert Gate |
| GD4086B | 4-Wide, 2-Input AND-OR-Invert Gate |
| GD4093B | Quad 2-Input NAND Schmitt Trigger |
| GD4104B | Quad Low Voltage-to-High Voltage Translater with 3-State Outputs |
| GD4510B | BCD Up/Down Counter |
| GD4511B | BCD to 7-Segment Latch/Decoder/Driver |
| GD4512B | 8-Input Multiplexer with 3-State Outputs |
| GD4514B | 1-of-16 Decoder/Demultiplexer with Input Latch |
| GD4515B | 1-of-16 Decoder/Demultiplexer with Input Latch |

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Gold Star Semiconductor

# CMOS 4000B SERIES

| PART NO | FUNCTION |
|---|---|
| GD4516B | Binary Up/Down Counter |
| GD4518B | Dual 4-Bit Decade Counter |
| GD4519B | Quad 2-Input Multiplexer |
| GD4520B | Dual 4-Bit Binary Counter |
| GD4521B | 24-Stage Binary Counter |
| GD4522B | 4-Bit BCD Programmable Down Counter |
| GD4526B | 4-Bit Binary Programmable Down Counter |
| GD4527B | BCD Rate Multiplier |
| GD4528B | Dual Monostable Multivibrator |
| GD4532B | 8-Input Priority Encoder |
| GD4534B | Real Time 5-Decade Counter |
| GD4538B | Dual Precision Monostable Multivibrator |
| GD4539B | Dual 4-Input Multiplexer |
| GD4543B | BCD to 7-Segment Latch/Decoder/Driver for Liquid Crystals |
| GD4553B | 3-Digit BCD Counter |
| GD4555B | Dual 1-of-4 Decoder with Active HIGH Outputs |
| GD4556B | Dual 1-of-4 Decoder with Active LOW Outputs |
| GD4557B | 1-to-64-Bit Variable Length Shift Register |
| GD4560B | BCD Adder |
| GD4561B | 9s Complementer |
| GD4566B | Industrial Time-Base Generator |
| GD4581B | 4-Bit Arithmetic Logic Register Unit |
| GD4582B | Lookahead Carry Generator |
| GD4583B | Dual Schmitt Trigger |
| GD4702B | Programmable Bit Rate Generator |
| GD4703B | 16×4 Parallel/Serial FIFO |
| GD4704B | Data Path Switch |
| GD4705B | Arithmetic Logic Register Stack |
| GD4706B | Program Stack |
| GD4707B | Data Access Register |
| GD4708B | Microprogram Sequencer |
| GD4710B | 16×4-Bit Clooked RAM with 3-State Output Register |
| GD4720B | 256-Bit CMOS RAM |
| GD4721B | 1024-Bit CMOS RAM (256×4) |
| GD4722B | Programmable Counter/Timer |
| GD4723B | Dual 4-Bit Addressable Latch |
| GD4724B | 8-Bit Addressable Latch |
| GD4725B | 64-Bit CMOS RAM |
| GD4727B | 7-Stage Counter |
| GD4731B | Quad 64-Bit Static Shift Register |
| GD4734B | BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking |
| GD4735B | 2048-Bit CMOS ROM (256×8) |
| GD4736B | 1024-Bit CMOS RAM (1024×1) |
| GD4737B | 7-Stage Counter |
| GD4741B | 4×4 Cross Point Switch |
| GD40014B | Hex Schmitt Trigger |
| GD40085B | 4-Bit Magnitude Comparator |
| GD40097B | 3-State Hex Non-Inverting Buffer |
| GD40098B | 3-State Hex Inverting Buffer |
| GD40160B | 4-Bit Synchronous Decade Counter with Asynchronous Reset |
| GD40161B | 4-Bit Synchronous Binary Counter with Asynchronous Reset |
| GD40162B | 4-Bit Synchronous Decade Counter with Synchronous Reset |
| GD40163B | 4-Bit Synchronous Binary Counter with Synchronous Reset |
| GD40174B | Hex D Flip-Flop |
| GD40175B | Quad D Flip-Flop |
| GD40192B | 4-Bit Up/Down Synchronous Decade Counter |
| GD40193B | 4-Bit Up/Down Synchronous Binary Counter |
| GD40194B | 4-Bit Bi-directional Universal Shift Register |
| GD40195B | 4-Bit Universal Shift Register |

* No Mark Code in Samples Column is under development.

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# CONSUMER/INDUSTRIAL

## TV

| PART NO | PKG | FUNCTION | FEATURE |
|---|---|---|---|
| GL1130 | 7SIP H/S | Vertical Deflection Output | High Output, On Chip Pump-Up Circuit and Low Power Dissipation, Minimun Number of External Parts Required |
| GL1150 | 20DIP | Sync. Deflecton Circuit | Horizontal Oscillation Frequency Adjustment from 15KHz to 100KHz Horizontal Display Shift, Good Linearity, Duty Setting |
| GL1170 | 16DIP | Low noise Vertical Def. System | Synchronization Circuit, Oscillator and Ramp Generator Flyback Generator, High Power Gain Amp |
| GL3120 | 30DIPS | [VIF+SIF] circuits | Peak IF AGC, High Gain VIF AMP, Video Det, B/W noise Canceller, RF AGC SIF Limiter, FM Det, DC ATT |
| GL3201A | 14DIP | TV Sound IF AMP | IF Amp. Limiter, FM Detector, Electronic Attenuator Zener Diode Regulated, High Stability, Low Harmonic Distortion |
| GL3202 | 28DIP | Dual Sound IF AMP | IF Amp. Limiter, FM Detector, Electronic Attenuator Zener Diode Regulated, High Stability, Low Harmonic Distortion |
| GL3320 | 30DIPS | Video, Chroma, Def. Circuits | Small-Sized Package, Minimum Number of Parts Required, Fewer Adjustment Required, Multifunction |
| GL3361 | 28DIP H/S | Video Chroma(PAL) & RGB | Combination of All Functions Required for the Identification of PAL Signal Luminance Amp. RGB Matrix and Amp. |
| GL3503 | 24DIP | Multi Sound dBX Decoder | Dual dBX Decoder and Encoder, Noise Reduction Circuit RMS detector, Current Controlled Amplifier |
| GL3504A | 40DIP | Multisound one Chip | SAP Dtector, Stereo Detector, Phase Compensation Buffer, Muting, One Touch Switch, Carrier Detector, Lamp Driver |
| GL3711 | 16DIP | Tuner Controller | 2-Input 5-Output Band Switch, Meets CATV Tuner Requirements, Small Saturation Voltage |
| GL3812 | 22DIP | Audio/Video Switch | Video/Stereo 4 Input Switch, Mute Function |
| GL3813 | 30DIPS | Bilingual Singal Processor | Highly Resistant to Vibration/Impact, Good Characteristics in Weak Electric Field |
| GL3917 | 14DIP | Teletext Analog Component | Composite Sync. Slice, Teletext Clock Slicing, Teletext Data Slicing |
| GL3920 | 20DIP | TV Chroma & External RGB Switch | TV Chroma and External RGB Switch, Matrix, Auto Kine Bias, Timing Generation, RGB Blanking |

## VTR

| PART NO | PKG | FUNCTION | FEATURE |
|---|---|---|---|
| GL3130 | 20DIP | [VIF+SIF] Circuits | VIF Amp. Video DET, Peak IF AGC, B/W Noise Canceller, RF AGC, AFT, Video Mute, SIF Limiter, FM DET. |
| GL3615 | 18DIP | VCR Audio Play/Record | Low Power Comsumption, Minimum Number of External Parts. |
| GL3667 | 18DIP | VCR Fine Slow/Still Motion Control | Fine Slow, Fine Still, Frame Advance, Head Drum Noise Reduction |
| GL3620 | 30DIPS | VDP Video Signal processor | FM Demodulator, Drop Out Compensation, Character Mix, Sync. Process. |

## AUDIO

| PART NO | PKG | FUNCTION | FEATURE |
|---|---|---|---|
| GL1223 | 9SIP | 5 DOT LED Driver | Wide Operating Voltage Range (3.5V~16V), Logarithmic Indicator for 5 Dot LED, Low Radiation Noise, High Gain Rectifying AMP |
| GL3230 | 16DIP | Dual Volume Balance Tone Control | Wide Volume Control Range, Excellent Cross Talk, Suitable for Temp Drift, Wide Tone Control Range. |
| GL3630 | 42DIPS, 44PLCC | CDP Servo Control | Focus Preamp, Tracking Preamp, Disc Drive Amp. HF Edge Detection. |
| GL3640 | 28DIP | VDP Time Base Error Correction | Horizontal Sync, Color Burst Signal Phase Err. Gen., Color Pulse Generation for CCD Drive, Two Times of Horizontal Sync During Vertical Operation. |
| GL5501 | 14DIP | Audio EQ AMP | Dual Preamp with Built-in ALC, High Gain, ALC Direct Meter Driver, Fast Stabilization. |
| GL5529 | 20DIP | 1 Chip EQ AMP | 2 Channel EQ Amp. 2 Channel Mic Amp, 2 Channel Line Amp, ALC. |
| GL5808 | 16DIP | AM/FM IF Tuner | FM IF Quadrature Detector, AM RF Amplifier, AM Local Oscillation, AM Det, Tuning Indication Drive Output |
| GL5901 | 16DIP | AM/FM Radio Receiver | High Sensitivity Low Noise, Very Low Tweet Modulation Very Simple DC Switching of AM-FM, Very High Singnal Handling |
| GL386 | 8DIP | Low Voltage Audio Power AMP | Battery Operation, Minimum External Parts, Wide Supply Voltage Range, Low Quiescent Current Drain, Low Distortion, Ground Referenced Input. |

GS

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# CONSUMER/INDUSTRIAL

## OPERATIONAL AMPLIFIER/ COMPARATOR

| PART NO | PKG | FUNCTION | $V_{IO}$(max).mV | $I_B$(max).mA | BAND WIDTH (MHz) | OFFSET ADJUSTMENT | MAX. Supply Voltage |
|---|---|---|---|---|---|---|---|
| GL358/A | 8DIP | General Dual Type (internal compensation type) | 7/3 | 250 | 0.8 | No | ±18 or 36 |
| GL324/A | 14DIP | General Quad Type (internal compensation type) | 7/3 | 250 | 0.8 | No | ±18 or 36 |
| GL4558 | 8DIP | Low Noise Dual (internal compensation type) | 6 | 500 | 3 | No | ±18 |
| GL4559 | 14DIP | Low Noise Quad (internal compensation type) | 6 | 500 | 3 | No | ±18 |
| GL348 | 14DIP | General Quad Type (internal compensation type) | 6 | 200 | 1 | YES | ±18 |
| GLC9458 | 8DIP | CMOS Dual Type (internal compensation) | 5 | 50pA | 0.48 | No | ±8 |
| GLC9459 | 14DIP | CMOS Quad Type (internal compensation) | 5 | 50pA | 0.48 | No | ±8 |
| GL393/A | 8DIP | Dual Comparator (open collector) | 5/2 | 250 | — | No | ±18 or 36 |
| GL339/A | 14DIP | Quad Comparator (open collector) | 5/2 | 250 | — | No | ±18 or 36 |

## REMOTE CONTROL

| PART NO | PKG | FUNCTION | FEATURE |
|---|---|---|---|
| GM3043 | 20DIP | Remote Control Transmitter | Low Voltage Operation, Low Power Consumption (CMOS) 32 Function Key, 256 Custom Code, 16 Bit Pulse Code |
| GM3044 | 20DIP | Remote Control Transmitter | Low Voltage Operation, Power Consumption (Include Ext. Diode) 32 Function Key, 256 Custom Code, 16 Bit Pulse Code |
| GL3273 | 8DIP | Remote Control Preamplifier | High Gain Pre-AMP, Envelope Detector, Minimum External Conponents, Low Current Drain, Wide Operating Supply Voltage |
| GL3274 | 8DIP | Remote Control Preamplifier | Low Power Consumption, Limiter Amp., Direct Connection to a Photodiode Open Collector Output |

## TIMER

| PART NO | PKG | FUNCTION | FEATURE |
|---|---|---|---|
| GLC555 | 8DIP | Timer | Single CMOS Version Industrial Standard 555 Timer 2-18V Power Supply, 1MHz |
| GLC556 | 16DIP | Dual Timer | Dual CMOS Version Industrial Standard 555 Timer 2-18V Power Supply, 1MHz |

## MOTOR DRIVER/ A-D CONVERTER

| PART NO | PKG | FUNCTION | FEATURE |
|---|---|---|---|
| GL7401 | 10SIP | Bidirectional Motor Driver | Built-in Braking Function, Built-in Diode to Absorb Dash Current, Direct Drivable with TTL. |
| GL7438 | 10SIP H/S | Dual Bidirectional Motor Driver | Logic Control, Power Driver, Thermal Shutdown. |
| GL7445 | 10SIP H/S | Bidirectional Motor Driver | Built-in Braking Function, Input Connectable Direct to MOS LSI, Output Voltage Variable by use of External Zener Diode |
| GM7136 | 40DIP | 3½ Digit LCD A/D Converter | 3½ Dight Low Power, 7 Segment Decoders, Display Driver, Reference and Clock True Polarity at Zero for Precise Null Detection |
| ADC0832 | 8DIP | 8Bit Serial I/O A/D Converter | TTL/MOS Input/Output Compatible, Remote Operation Serial Digital Data Link, No Zero or Full Scale Adjust Required. |

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# CONSUMER/INDUSTRIAL

## MISCELLANEOUS ICs

| PART NO | PKG | FUNCTION | FEATURE |
|---|---|---|---|
| GL7101 | 8DIP | Earth Leakage Breaker | Low Power Consumption, Few External Components, Built-in Voltage Regulator, High Gain Differential AMP. |
| GL317 | TO-220 | Adjustable Voltage Regulator | Guaranteed Output Current Capability of 1.5A Ripple Rejection Typically 80dB, Good Regulation |
| GL494 | 16DIP | PWM Control Circuit | Switch Mode Pulse Width Modulation Control, Adjustable Dead Time Control, Easy Sychronization. |
| GL574 | TO-92 | 33V Voltage Stabilizer | Low Temperature Coefficient, Low Dynamic Resistance, Typical 33V Reference Voltage |
| GL8901 | 18DIP 9SIP H/S | SMPS Controller | Low Start-Up Current, Direct Control of Switching Transistor Collector Current Proportional to Base-Current Input. |

## VOLTAGE REGULATOR

### GL79XX Series

| Device | Typical Input Voltage | Output at $I_O$ = 500mA | Ripple Rejection at $I_O$ = 500mA f = 120Hz | |
|---|---|---|---|---|
| | $V_{in}$(V) | $V_{out}$(V) | TYP(dB) | MIN(dB) |
| GL7905 | −10 | −5 | 60 | 54 |
| GL7909 | −15 | −8 | 60 | 54 |
| GL7912 | −19 | −12 | 60 | 54 |
| GL7915 | −23 | −15 | 60 | 54 |
| GL7924 | −33 | −24 | 58 | 54 |

### GL78XX Series

| Device | Typical Input Voltage | Output at $I_O$ = 500mA | Ripple Rejection at $I_O$ = 500mA f = 120Hz | |
|---|---|---|---|---|
| | $V_{in}$(V) | $V_{out}$(V) | TYP(dB) | MIN(dB) |
| GL7805 | 10 | 5 | 80 | 62 |
| GL7806 | 11 | 6 | 80 | 59 |
| GL7808 | 14 | 8 | 80 | 56 |
| GL7809 | 15 | 8 | 80 | 56 |
| GL7812 | 19 | 12 | 80 | 55 |
| GL7815 | 23 | 15 | 70 | 54 |
| GL7824 | 33 | 24 | 70 | 50 |

## Telephone

| PART NO | PKG | FUNCTION | FEATURE |
|---|---|---|---|
| GL6801 | 16 DIP | DTMF Generator | Wide Operating Line Voltage and Current Range Short Start Up Time, Internal Protection of All Inputs |
| GL6901 | 16 DIP | Speech Circuit | Mask Programmable Speech Circuit, Low Voltage Operation High Output Swing On Long Lines, Very Short Start Up Time |
| GM3054/7 | 16CERDIP | Serial CODEC/FILTER | Complete CODEC and Filtering μ-law(GM3054) A-law (GM3057) Exceeds all D3/D4 CCITT Specifications, Automatic Power Down |
| GM5370 | 18DIP | Tone/Pulse Dialer | Stand-alone DTMF and Pulse Signaling, Recall of LND (Up to 28 Digits) Pacifier Tone |
| GM5371/2 | 18/24DIP | Single Number Tone/Pulse Dialer | Stand-alone DTMF and Pulse Signaling, Recall of LND(Lp to 28 Digits) Timed PABX Pause, Pacifior tone, 10/20 Salect Option MPU Interface (BCD Inputs) for Smart Telephone |
| GM5373 | 18DIP | Single Number Tone/Pulse Dialer | Stand-alone DTMF and Pulse Signaling, Recall of LND(up to 28 Digits) Timed PABX Pause, Pacifier Tone, MPU Interface for Smart Telephone |
| GM5375 | 18DIP | 10 Number Repertory Tone/Pulse Dialer | LND Privacy, Pacifier tone and PBX Pause Stores ten 16 Digit Numbers, Variable Dialing Rate |
| GM5376 | 24DIP | 10 Number Repertory Tone/Pulse Dialer | Store ten-16digit Number, LND Privacy Pacifier Tone and PBX Pause, Manual and Auto Dialing |
| GM5380 | 16DIP | Tone Dialer | Minimum External Parts Count, Improved Loop Compensations Multiple Key Entry Pin-Selectable to Either Single Tone or no Tone |
| GM62093 | 40DIP | Multiplexer | 12×8 Cross Point Switch with Control Memory, Latch Control, Low On Resistance |
| GM6840 | 8DIP | Electronic Two Tone Ringer | Low Current Consumption, Little External Circuitry, Bridge Output Configuration, Integrated Voltage and Current Hysteresis |

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# MILITARY PRODUCT REFERENCE GUIDE

Harris Semiconductor has long been a major supporter of the military market. The knowledge and expertise gained from this association is manifested in our latest military efforts; Military Drawing and 883-compliant products. This Military Product Guide gives you a complete overview of our commitment to military support. For more information on these products, please contact Harris Semiconductor or your nearest Harris sales office or representative.

## Radiation Hardened Products

| Part Number | JAN Part Number | DESC Drawing Number | 883 Part Number |
|---|---|---|---|
| HS-6504RH | 24503BVB | — | HS-6504RH/883 |
| HS-6514RH | 24504BVB | — | HS-6504RH/883 |
| HS-65C262RH | 29107SJB | — | HS-65C262RH/883 |
| HS-65T262RH | 29108SJB | — | HS-65T262RH/883 |
| HS-508ARH | — | 5962R8753701EX | HS-508ARH/883 |
| HS-1840RH | — | 5962R8753801XX | HS-1840RH/883 |

## Microprocessor Products

| Part Number | JAN Part Number | Military Drawing Number | 883 Part Number |
|---|---|---|---|
| MD80C86 | — | 8405201QA | — |
| MR80C86 | — | 84052012C | — |
| MD80C88 | — | — | *MD80C88/883 |
| MR80C88 | — | — | *MR80C88/883 |
| MD82C37A | — | *IN DEVELOPMENT | — |
| MR82C37A | — | *IN DEVELOPMENT | — |
| MD82C50A-5 | — | — | *MD82C50A-5/883 |
| MR82C50A-5 | — | — | *MR82C50A-5/883 |
| MD82C52 | — | 8501501XA | — |
| MR82C52 | — | 85015013C | — |
| MD82C54 | — | 8406501JA | — |
| MR82C54 | — | 84065013C | — |
| MD82C55A-5 | — | 8406601QA | — |
| MR82C55A-5 | — | 8406601XC | — |
| MD82C55A | — | 8406602QA | — |
| MR82C55A | — | 8406602XC | — |
| MD82C59A-5 | — | 8501601YA | — |
| MR82C59A-5 | — | 85016013C | — |
| MD82C59A | — | 8501602YA | — |
| MR82C59A | — | 85016023C | — |
| MD82C82 | — | 8406701RA | — |
| MR82C82 | — | 84067012C | — |
| MD82C83H | — | 8406702RA | — |
| MR82C83H | — | 84067022C | — |
| MD82C84A | — | 8406801VA | — |
| MR82C84A | — | 84068012C | — |
| MD82C85 | — | *IN DEVELOPMENT | — |
| MR82C85 | — | *IN DEVELOPMENT | — |
| MD82C86H-5 | — | 8757701RA | — |
| MR82C86H-5 | — | 87577012C | — |
| MD82C87H-5 | — | 8757702RA | — |
| MR82C87H-5 | — | 87577022C | — |
| MD82C88 | — | 8406901RA | — |
| MR82C88 | — | 84069012C | — |
| MD82C89 | — | 8552801RA | — |
| MR82C89 | — | 85528012C | — |

* Scheduled for Q1 1988





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| Microprocessor Products (continued) | | | |
|---|---|---|---|
| Part Number | JAN Part Number | Military Drawing Number | 883 Part Number |
| HD1-4702 | — | — | HD1-4702/883* |
| HD1-6402 | — | — | HD1-6402/883* |
| HD1-15530 | — | 7802901JA | — |
| HD4-15530 | — | 78029013C | — |
| HD1-15531 | — | — | HD1-15531/883* |

* Scheduled for Q1CY88

| Data Acquisition Products | | | |
|---|---|---|---|
| Part Number | JAN Part Number | Military Drawing Number | 883 Part Number |
| HA-2420 | — | 8001601CA | HA-2420/883 |
| HI-506 | 38510/190-01BXC | — | HI-0506/883 |
| HI-506A | 38510/190-02BXC | 8513101XA | — |
| HI-507 | 38510/190-03BXC | — | HI-0507/883 |
| HI-507A | 38510/190-04BXC | 8513102XA | — |
| HI-508 | 38510/190-07BEC | 7705201EC | HI-0508/883 |
| HI-508A | 38510/190-05BEC | 7705202EA | — |
| HI-509 | 38510/190-08BEC | — | HI-0509/883 |
| HI-509A | 38510/190-06BEC | 85131-03 | — |
| HI-516 | — | — | HI-0516/883 |
| HI-518 | — | — | HI-0518/883 |
| HI-524 | — | — | HI-0524/883 |
| HI-546 | — | 8513101XA | HI-0546/883 |
| HI-547 | — | 8513102XA | HI-0547/883 |
| HI-548 | — | 7705202EA | HI-0548/883 |
| HI-549 | — | 8513103EA | HI-0549/883 |
| HI-562A | — | — | HI-0562A/883 |
| HI-1818A | — | — | HI-1818/883 |
| HI-1828A | — | — | HI-1828A/883 |
| HI-2420 | — | — | HI-2420/883 |
| HA-5320 | — | — | HI-5320/883 |
| HA-5330 | — | — | HI-5330/883 |
| HI-562A | — | — | HI-562A/883 |
| HI-5687 | — | 83003-02 | HI-5687/883 |
| HI-5697 | — | — | HI-5697/883 |
| HI-574ASD | — | — | HI-574ASD/883 |
| HI-574ATD | — | 85127-04 | HI-574ATD/883 |
| HI-674ASD | — | — | HI-674ATD/883 |
| HI-674ATD | — | 85127-06 | HI-674ATD/883 |



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# MILITARY PRODUCT REFERENCE GUIDE

## CMOS Memory Products

| Part Number | JAN Part Number | DESC Drawing Number | 883 Part Number |
|---|---|---|---|
| **1K CMOS Static RAMs** | | | |
| HM1-6508 | — | — | HM1-6508/883 |
| HM1-6508B | — | — | HM1-6508B/883 |
| HM1-6518 | — | — | HM1-6518/883 |
| HM1-6518B | — | — | HM1-6518B/883 |
| HM1-6551 | — | — | HM1-6551/883 |
| HM1-6551B | — | — | HM1-6551B/883 |
| HM1-6561 | — | — | HM1-6561/883 |
| HM1-6561B | — | — | HM1-6561B/883 |
| **4K CMOS Static RAMs** | | | |
| HM1-6504 | — | 8102405VA | HM1-6504/883 |
| HM1-6504B | — | 8102403VA | HM1-6504B/883 |
| HM1-6504S | 24501BVX | 8102401VA* | HM1-6504S/883 |
| HM1-6514 | — | 8102406VA | HM1-6514/883 |
| HM1-6514B | — | 8102404VA | HM1-6514B/883 |
| HM1-6514S | 24502BVX | 8102402VA* | HM1-6514S/883 |
| HM4-6514 | — | — | HM4-6514/883 |
| HM4-6514B | — | — | HM4-6514B/883 |
| HM1-6514S | — | — | HM4-6514S/883 |
| **16K CMOS Synchronous Static RAMs** | | | |
| HM1-6516 | 29102BJX | 8403601JA | HM1-6516/883 |
| HM1-6516B | — | 8403607JA | HM1-6516B/883 |
| HM4-6516 | — | 8403601ZC | HM4-6516/883 |
| **16K CMOS Asynchronous Static RAMs** | | | |
| HM1-65162 | 29104BJX | 8403602JA | HM1-65162/883 |
| HM1-65162B | — | 8403606JA | HM1-65162B/883 |
| HM1-65162C | — | 8403603JA | HM1-65162C/883 |
| HM1-65162S | — | — | — |
| HM4-65162 | — | 8403602XC | HM4-65162/883 |
| HM4-65162B | — | 8403606XC | HM4-65162B/883 |
| HM4-65162C | — | 8403603XC | HM4-65162C/883 |
| HM1-65262 | 29103BJX | 8413201RA | HM1-65262/883 |
| HM1-65262B | — | 8413203RA | HM1-65262B/883 |
| HM4-65262 | — | 8413201YC | HM4-65262/883 |
| HM4-65262B | — | 8413203YC | HM4-65262B/883 |
| **64K CMOS Static RAMs** | | | |
| HM1-65642 | 29201BJX | 8552503YA | HM1-65642/883 |
| HM4-65642 | — | 8552503XC | HM4-65642/883 |
| HM1-65642B | — | — | HM1-65642B/883 |

*Obsolete - may still be purchased for contracts prior to 10/22/85.





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# MILITARY PRODUCT REFERENCE GUIDE

| CMOS Memory Products (continued) | | | |
|---|---|---|---|
| **Part Number** | **JAN Part Number** | **DESC Drawing Number** | **883 Part Number** |
| **CMOS Static RAM Modules**<br>HM5-6564<br>HM5-8808<br>HM5-8808B<br>HM5-8808S<br>HM5-8808A<br>HM5-8808AB<br>HM5-8808AS<br>HM5-8816H<br>HM5-8832B<br>HM5-91M2<br>HM5-92560<br>HM5-92570 | Harris CMOS static RAM modules are available for military and high-reliability applications processed to our high-rel DASH 8 program flow. This includes burn-in and value-added processing (temperature cycling, SEM inspection, etc.). Please contact your local Harris sales office or representative for details. | | |
| **CMOS Fuse Link PROMs** | | | |
| HM1-6642 | — | — | HM1-6642/883 |
| HM4-6642 | — | — | HM4-6642/883 |
| HM6-6642 | — | — | HM6-6642/883 |
| HM1-6617 | — | — | HM1-6617/883 |
| HM4-6617 | — | — | HM4-6617/883 |
| HM6-6617 | — | — | HM6-6617/883 |

| Linear Products | | | |
|---|---|---|---|
| **Part Number** | **JAN Part Number** | **DESC Drawing Number** | **883 Part Number** |
| HA240X | — | — | HA1-2400/883 |
| HA2500 | 12204BGC | — | HA2-2500/883 |
| | — | — | HA7-2500/883 |
| HA2502 | — | — | HA2-2502/883 |
| | — | — | HA7-2502/883 |
| HA2510 | 12205BGC | — | HA2-2510/883 |
| | — | — | HA7-2510/883 |
| HA2512 | — | — | HA2-2512/883 |
| | — | — | HA7-2512/883 |
| HA2520 | 12206BGC | — | HA2-2520/883 |
| | — | — | HA7-2520/883 |
| HA2522 | — | — | HA2-2522/883 |
| | — | — | HA7-2522/883 |
| HA2541 | — | — | HA2-2541/883 |
| | — | — | HA1-2541/883 |

# MILITARY PRODUCT REFERENCE GUIDE

| Linear Products (continued) | | | |
|---|---|---|---|
| Part Number | JAN Part Number | DESC Drawing Number | 883 Part Number |
| HA2600 | 12202BGC | — | HA2-2600/883 |
| | — | — | HA7-2600/883 |
| HA2602 | — | — | HA2-2602/883 |
| | — | — | HA7-2602/883 |
| HA2620 | 12203BGC | — | HA2-2620/883 |
| | — | — | HA7-2620/883 |
| HA2622 | — | — | HA2-2622/883 |
| | — | — | HA7-2622/883 |
| HA2640 | — | 7800302GC | HA2-2640/883 |
| | — | — | HA7-2640/883 |
| HA4741 | — | — | HA1-4741/883 |
| HA4900 | — | — | — |
| HA4902 | — | — | HA1-4902/883 |
| HA5033 | — | — | HA2-5033/883 |
| HA5002 | — | — | HA2-5002/883 |
| | — | — | HA7-5002/883 |
| HA5102 | — | — | HA2-5102/883 |
| | — | — | HA7-5102/883 |
| HA5104 | — | — | HA1-5104/883 |
| HA5112 | — | — | HA2-5112/883 |
| | — | — | HA7-5112/883 |
| HA5114 | — | — | HA1-5114/883 |
| HA5135 | — | — | HA2-5135/883 |
| | — | — | HA7-5135/883 |
| HA5141 | — | — | HA2-5141/883 |
| | — | — | HA7-5141/883 |
| HA5142 | — | — | HA2-5142/883 |
| | — | — | HA7-5142/883 |
| HA5144 | — | — | HA1-5144/883 |
| HA5151 | — | — | HA2-5151/883 |
| | — | — | HA7-5151/883 |
| HA5152 | — | — | HA2-5152/883 |
| | — | — | HA7-5152/883 |
| HA5154 | — | — | HA1-5154/883 |
| HA5160 | — | — | HA2-5160/883 |
| HA5170 | — | — | HA2-5170/883 |
| | — | — | HA7-5170/883 |
| HA5180 | — | — | HA2-5180/883 |





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# MILITARY PRODUCT REFERENCE GUIDE

**Linear Products (continued)**

| Part Number | JAN Part Number | DESC Drawing Number | 883 Part Number |
|---|---|---|---|
| HA5180 | — | — | HA7-5180/883 |
| HA5190 | — | — | HA1-5190/883 |
| | — | — | HA2-5190/883 |
| HI200 | — | — | HI1-200/883 |
| | — | — | HI2-200/883 |
| HI201 | 12302BEA | — | HI1-201/883 |
| | 12302BEC | — | — |
| HI201HS | — | 8671601EX | HI1-201HS/883 |
| HI300 | — | 86716012X | HI2-300/883 |
| | — | — | HI1-300/883 |
| HI301 | — | — | HI2-301/883 |
| | — | — | HI1-301/883 |
| HI302 | — | — | HI1-302/883 |
| HI303 | — | — | HI1-303/883 |
| HI304 | — | — | HI1-304/883 |
| | — | — | HI2-304/883 |
| HI305 | — | — | HI1-305/883 |
| | — | — | HI2-305/883 |
| HI306 | — | — | HI1-306/883 |
| HI307 | — | — | HI1-307/883 |
| HI381 | — | — | HI1-381/883 |
| | — | — | HI2-381/883 |
| HI384 | — | — | HI1-384/883 |
| HI387 | — | — | HI1-387/883 |
| | — | — | HI2-387/883 |
| HI390 | — | — | HI1-390/883 |
| HI5040 | — | 8100609EX | HI1-5040/883 |
| HI5041 | — | — | HI1-5041/883 |
| HI5042 | — | 8100611EX | HI1-5042/883 |
| HI5043 | — | 8100612EX | HI1-5043/883 |
| | — | 81006122X | HI4-5043/883 |
| HI5044 | — | 8100613EX | HI1-5044/883 |
| HI5045 | — | 8100614EX | HI1-5045/883 |
| | — | 81006142X | HI4-5045/883 |
| HI5046 | — | 8100615EX | HI1-5046/883 |
| HI5046A | — | 8100621EX | HI1-5046A/883 |
| HI5047 | — | 8100616EX | HI1-5047/883 |
| HI5047A | — | 8100622EX | HI1-5047A/883 |
| HI5048 | — | — | HI1-5048/883 |
| HI5049 | — | 8100620EX | HI1-5049/883 |
| | — | 81006202X | HI4-5049/883 |
| HI5050 | — | 8100618EX | HI1-5050/883 |
| HI5051 | — | 8100619EX | HI1-5051/883 |
| | — | 81006192X | HI4-5051/883 |

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# RAD-HARD
# CMOS MICROPROCESSOR PRODUCTS

## 8-Bit Microprocessor
## HS-80C85RH

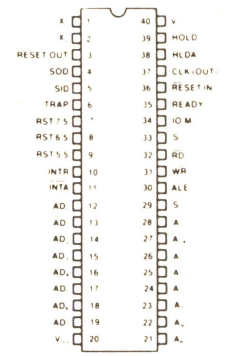
### Features

- Specifically designed for radiation hardness
- Low standby power: 2.7 mW max.
- Low operating power: 26 mW/MHz max.
- Multiplexed address/data bus
- 5 Volt operation
- Software and pin compatibility with Intel 8085
- Equivalent to Sandia SA3000
- Full military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec

### Pinout




## 16-Bit Microprocessor
## HS-80C86RH

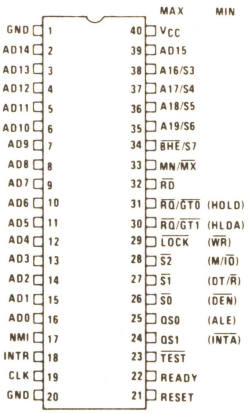
### Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 80C86
- Completely static design
  - ▶DC to 5 MHz
- Low-power operation
  - ▶ICCSB = 500 $\mu$A maximum
  - ▶ICCOP = 10 mA/MHz max.
- 1 Mbyte of direct memory addressing capability
- 24 operand addressing modes
- Bit, byte, word, and block move operations
- 8 and 16-bit signed/unsigned arithmetic
  - ▶Binary or decimal
  - ▶Multiply and divide
- Single 5V power supply
- Military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec
- Functional after 1 x $10^6$ rads (Si) total dose

### Pinout

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# RAD-HARD
# CMOS MICROPROCESSOR PRODUCTS

## 8-Bit Bidirectional CMOS/TTL Level Converter
## HS-3374RH

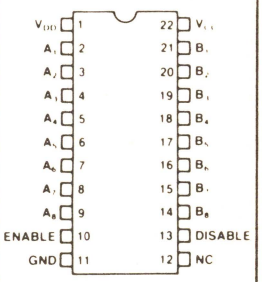
### Features

- Specifically designed for radiation hardness
- Static operation for low power consumption
- Non-inverting outputs
- Low propagation delay
- Full military temperature range
- Equivalent to Sandia SA2996

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec

### Pinout




## 3-Line to 8-Line Decoder/Demultiplexer
## HS-54C138RH

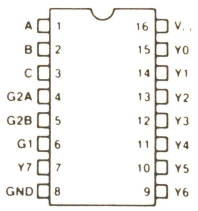
### Features

- Specifically designed for radiation hardness
- Static operation for low power consumption
- High noise immunity
- Active low outputs
- 5 Volt operation
- Full military temperature range
- Equivalent to Sandia SA2995

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec

### Pinout




## 2K (256x8) RAM with I/O and Timer
## HS-81C55RH, HS-81C56RH

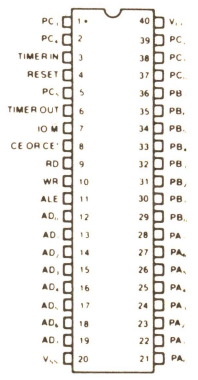
### Features

- Specifically designed for radiation hardness
- Static operation for low power consumption
- Pin compatible with Intel 8155/56
- Equivalent to Sandia SA3001
- 5 Volt operation
- 3 programmable I/O ports
- 14-Bit programmable timer
- Multiplexed address and data bus
- Full military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec

### Pinout

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# RAD-HARD
# CMOS MICROPROCESSOR PRODUCTS

## 8-Bit Bus Transceiver
## HS-82C08RH

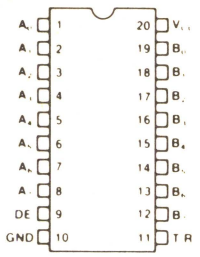
### Features

- Specifically designed for radiation hardness
- Static operation for low power consumption
- Bidirectional three-state input/outputs
- Low propagation delay
- 5 Volt operation
- Full military temperature range
- Equivalent to Sandia SA2997

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec
- Increased tolerance to cosmic radiation

### Pinout




## 8-Bit Input/Output Port
## HS-82C12RH

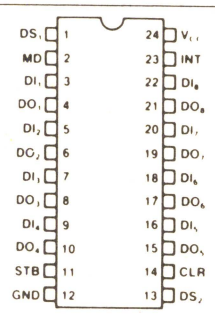
### Features

- Specifically designed for radiation hardness
- Static operation for low power consumption
- Asynchronous register clear
- 8-bit data register and buffer
- Service request flip-flop
- Three-state outputs
- Full military temperature range
- Equivalent to Sandia SA3026

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec

### Pinout





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# RAD-HARD
# CMOS MICROPROCESSOR PRODUCTS

## Programmable DMA Controller
## HS-82C37ARH

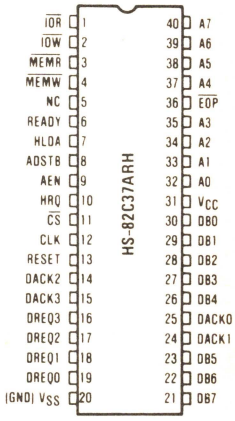
### Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C37A
- High-speed data transfers up to 2.5 MBPS with 5 MHz clock
- Four independent maskable channels with autoinitialization capability
- Expandable to any number of channels
- Memory-to-memory transfer capability
- Software-accessible internal registers
- Single 5V power supply
- Low power consumption
  >IDDOP = 2 mA/MHz maximum
  >IDDSB = 20 $\mu$A maximum
- Full military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to $1 \times 10^5$ rads (Si)
- Latch-up free $> 10^{12}$ rads (Si)/sec
- Upset: $> 10^8$ rads (Si)/sec
- Functional after $1 \times 10^6$ rads (Si) total dose

### Pinout




## Serial Controller Interface
## HS-82C52RH

COMING SOON

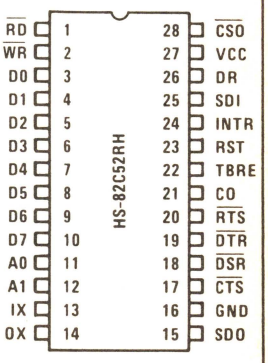
### Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C52
- Uses either parallel mode crystal circuit or external frequency source
- DC to 16 MHz operation (DC to 1M Baud rate)
- Microprocessor bus oriented interface
- Modem interface
- Line break generation and detection
- Loopback and echo modes
- Interrupt mode with mask capability
- TTL/CMOS compatible inputs/outputs
- Single 5V supply
- Low power consumption: 1 mA/MHz typical
- Full military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to $1 \times 10^5$ rads (Si)
- Latch-up free $> 10^{12}$ rads (Si)/sec
- Upset: $> 10^8$ rads (Si)/sec
- Functional after $1 \times 10^6$ rads (Si) total dose

### Pinout

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# RAD-HARD
# CMOS MICROPROCESSOR PRODUCTS

## Programmable Interval Timer
## HS-82C54RH

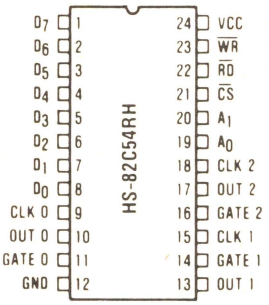
### Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C54A
- High speed, no "wait state" operation with 5MHz HS-80C86RH
- Three independent 16 bit counters
- Six programmable counter modes
- Binary or BCD counting
- Status read back command
- Fully TTL compatible
- Single 5V power supply
- Low power consumption
  >IDDSB = 20 $\mu$A
  >IDDOP = 10 mA
- Full military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec
- Functional after 1 x $10^6$ rads (Si) total dose

### Pinout




## Programmable Peripheral Interface
## HS-82C55ARH

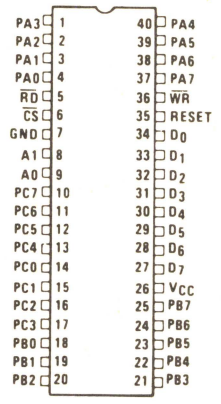
### Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C55A
- High speed, no "wait state" operation with 5 MHz HS-80C86 RH
- Fully TTL compatible
- 24 programmable I/O pins
- Direct bit set/reset capability
- Enhanced control word read capability
- Single 5V power supply
- 2.0 mA drive capability on all I/O port outputs
- Low standby power
  >ICCSB = 20 $\mu$A
- Full military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec
- Functional after 1 x $10^6$ rads (Si) total dose

### Pinout

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# RAD-HARD
# CMOS MICROPROCESSOR PRODUCTS

## Programmable Interrupt Controller
## HS-82C59ARH

COMING SOON

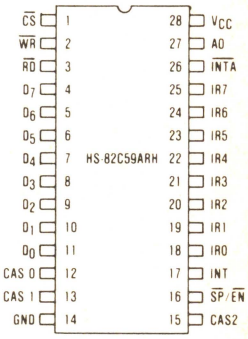
### Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C59A
- High speed, no "wait state" operation with 5 MHz HS-80C86RH
- Eight level priority controller
- Expandable to 64 priority levels
- Fully TTL compatible
- Programmable interrupt modes
- HS-80C85RH and HS-80C86RH compatible operation
- Individual request mask capability
- Fully static design
- Single 5V power supply
- Low standby power 20 $\mu$A
- Full military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec
- Functional after 1 x $10^6$ rads (Si) total dose

### Pinout




## Static Clock Controller/Generator
## HS-82C85RH

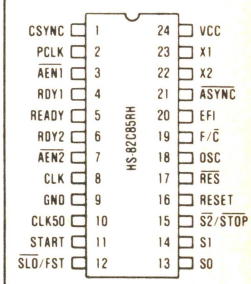
### Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C85
- Generates system clocks for microprocessors and peripherals
- Complete control over system clock operation for very low system power
  - ▶Stop-oscillator
  - ▶Stop-clock
  - ▶Low-frequency (slo) mode
  - ▶Full-speed operation
- DC to 15 MHz operation (DC to 5 MHz system clock)
- Uses either parallel mode crystal circuit or external frequency source
- TTL/CMOS compatible inputs/outputs
- Single 5V power supply
- Very low power consumption
- Full military temperature range

### Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x $10^5$ rads (Si)
- Latch-up free > $10^{12}$ rads (Si)/sec
- Upset: > $10^8$ rads (Si)/sec
- Functional after 1 x $10^6$ rads (Si) total dose

### Pinout

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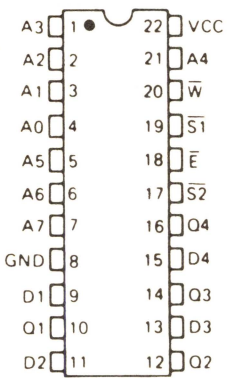
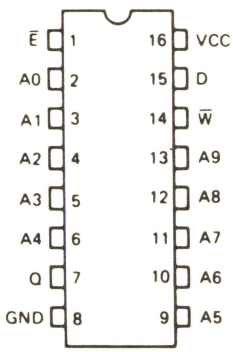
# RAD-HARD CMOS STATIC RAMs 1K, 4K

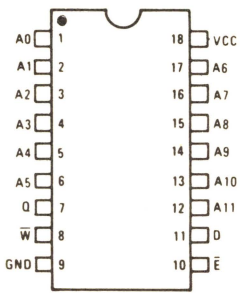
## 256 x 4 — 1K
## HS-6551RH

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Low standby power (max): — 550 $\mu$W<br>• Low operating power (max): — 22 mW/MHz<br>• TTL compatible output<br>• High noise immunity<br>• On-chip address register<br>• Three-state output<br>• Full military temperature range | • Each lot screened for total dose hardness<br>• Total dose guaranteed to 2 x $10^4$ rads (Si)<br>• Post rad standby current (typ): — 5 mA<br>• Access time: (typical): 160 ns (max): 300 ns<br>• Latch-up free<br>• Upset: > $10^8$ rads (Si)/sec<br>• Increased immunity to cosmic radiation |  |

## 1024 x 1 — 1K
## HS-6508RH

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Low standby power (max): — 550 $\mu$W<br>• Low operating power (max): — 25 mW/MHz<br>• TTL compatible output<br>• High noise immunity<br>• On-chip address register<br>• Three-state output<br>• Full military temperature range | • Each lot screened for total dose hardness<br>• Total dose guaranteed to 2 x $10^4$ rads (Si)<br>• Post rad standby current (typ): — 5 mA<br>• Access time: (typical): 160 ns (max): 300 ns<br>• Latch-up free<br>• Upset: > $10^8$ rads (Si)/sec<br>• Increased immunity to cosmic radiation |  |

## 4096 x 1 — 4K
## HS-6504RH

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Low standby power (max): — 1100 $\mu$W<br>• Low operating power (max): — 38.5 mW/MHz<br>• TTL compatible output<br>• Three-state output<br>• On-chip address register<br>• Standard JEDEC pinout<br>• Full military temperature range | • Each lot screened for total dose hardness<br>• Total dose guaranteed to 1 x $10^5$ rads (Si)<br>• Post rad standby current (max): — 200 $\mu$A<br>• Post rad access time: (typical): 120 ns (max): 200 ns<br>• Latch-up free<br>• Upset: > $10^8$ rads (Si)/sec<br>• SEU immune option available |  |

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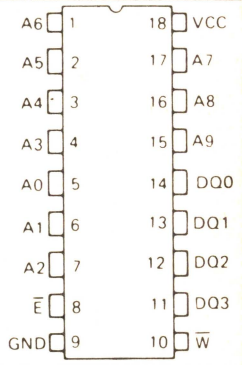
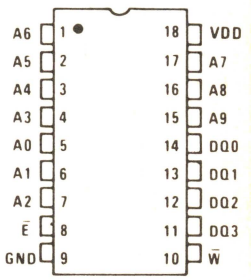
# RAD-HARD CMOS STATIC RAMs 4K & 16K

## 1024 x 4 — 4K
## HS-6514RH

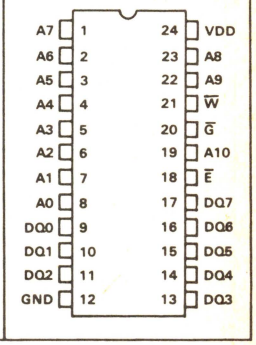
| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Low standby power (max): — 1100 $\mu$W<br>• Low operating power (max): — 38.5 mW/MHz<br>• TTL compatible output<br>• Three-state output<br>• Common data in/out<br>• Standard JEDEC pinout<br>• Full military temperature range | • Each lot screened for total dose hardness<br>• Total dose guaranteed to $1 \times 10^5$ rads (Si)<br>• Post rad standby current (typ): — 6 $\mu$A<br>• Post rad access time: (typical): 120 ns (max): 225 ns<br>• Latch-up free<br>• Upset: $> 10^8$ rads (Si)/sec<br>• SEU immune option available |  |

## (1024 x 4) Fast 4K
## HS-65142RH

COMING SOON

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation environment<br>• Asynchronous operation<br>• Fast access time: 75 ns max.<br>• Fast write cycle: 75 ns max.<br>• Low standby current: 200 $\mu$A max.<br>• Low operating current (max): 40 mA + 4 mA/MHz<br>• Data retention current @ 3V: 120 $\mu$A max.<br>• Full military temperature range | • Parametrics guaranteed to 500K rads (Si)<br>• Functional > 1000K rads (Si)<br>• Transient upset: Short pulse $> 5 \times 10^9$ rads (Si)/sec Long pulse $> 1 \times 10^9$ rads (Si)/sec<br>• Latch-up free $> 1 \times 10^{12}$ rads (Si)/sec<br>• Neutron fluence $> 10^{14}$ n/cm$^2$ |  |

## (2048 x 8)—16K
## HS-65C162RH, HS-65T162RH

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Asynchronous operation<br>• CMOS or TTL compatible input/output<br>• Low standby power (max): CMOS: 1100 $\mu$W<br>• Low operating current (max): 40 mA + 4mA/MHz<br>• Three-state outputs<br>• Full military temperature range | • Each lot screened for radiation hardness<br>• Total dose guaranteed to $2 \times 10^5$ rads (Si)<br>• Access time (max., CMOS): 150 ns<br>• Access time (typ., CMOS): 80 ns<br>• Access time (typ., TTL): 100 ns<br>• Data upset $\geq 5 \times 10^8$ rads (Si)/s<br>• Latch-up free $> 1 \times 10^{12}$ rads (Si)/s<br>• SEU immune option available |  |

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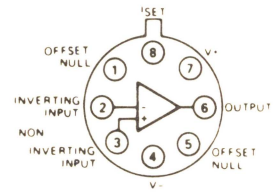
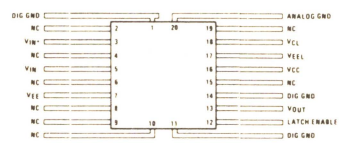
# RAD-HARD
# OPERATIONAL AMPLIFIERS, COMPARATOR AND REGULATOR

## Low-Power/Programmable Operational Amplifier
## HS-3530RH

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Wide range AC programming:<br>— Slew rate: 0.06 to 3 V/$\mu$s<br>— Gain x bandwidth: 100 kHz to 5 MHz<br>• Wide range DC programming:<br>— Power supply: $\pm$ 1.5 to $\pm$ 18 V<br>— Supply current: 10 $\mu$A to 1.2 mA<br>• Short circuit protection<br>• Full military temperature range | • Dielectric Isolation technology<br>• Each lot screened for total dose hardness<br>• Parametrics guaranteed to 1 x $10^6$ rads (Si)<br>• Latch-up free<br>• Tolerant to neutron fluence > 5 x $10^{12}$ n/cm$^2$ (E $\geq$ 10 KeV)<br>• Tolerant to gamma rate > 1 x $10^9$ rads (Si)/sec |  <br>NOTE: Case tied to V- |

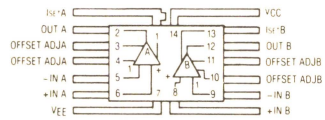
## High Speed Latching Comparator
## HS-3560RH

COMING SOON

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Fast response time: 75 ns<br>• Low offset voltage: 375 $\mu$V<br>• Low offset current: 200 nA<br>• Latching output<br>• Built-in clamp circuit<br>• Laser trimmed input offset voltage | • Dielectric Isolation technology<br>• Hardened to strategic levels |  |

## Dual Programmable Operational Amplifier
## HS-3569RH

COMING SOON

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Programmable AC and DC parameters:<br>—Unity gain bandwidth 3 to 7 MHz<br>—Full power bandwidth 30 to 80 kHz<br>—Slew rate: 2 to 5 V/$\mu$s<br>—Power consumption (typ): 45 to 110 mW<br>• Short circuit protection<br>• Input overload protection<br>• Full military temperature range<br>• Laser trimmed input offset voltage | • Dielectric Isolation technology<br>• Hardened to strategic levels |  |

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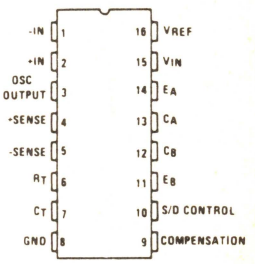
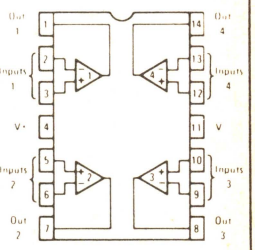
# RAD-HARD ANALOG OPERATIONAL AMPLIFIERS, COMPARATOR AND REGULATOR

## Regulating Pulse Width Modulator HS-3761RH

COMING SOON

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Complete PWM power control circuitry<br>• Frequency adjustable to 290KHz<br>• 10% Frequency stability over temperature<br>• Quiescent supply current $\leq$ 10 mA<br>• 5V, 50mA linear regulator output<br>• Dual alternating output switches for both push-pull and single-ended applications<br>• Output switching transistors protected from saturation and excessive currents<br>• Current limit amplifier for external component protection<br>• Shutdown control for circumvention<br>• Full military temperature range | • Dielectric Isolation technology<br>• Hardened to strategic levels |  |

## High Performance Quad Operational Amplifier HS-5104RH

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Low offset voltage: $\leq$ 3.0 mV<br>• High slew rate: $\geq$ 1.0 V/$\mu$s<br>• Unity gain bandwidth 6.5 MHz<br>• Single 5V supply capability<br>• Short circuit protection<br>• Full military temperature range | • Dielectric Isolation technology<br>• Each lot screened for total dose hardness<br>• Parametrics guaranteed to 1 x $10^6$ rads (Si)<br>• Latch-up free<br>• Tolerant to neutron fluence > 5 x $10^{12}$ n/cm$^2$ (E $\geq$ 10 KeV)<br>• Tolerant to gamma rate > 1 x $10^9$ rads (Si)/sec |  |

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# RAD-HARD
# CMOS ANALOG MULTIPLEXERS

## 8-Channel Multiplexer — Overvoltage Protection
## HS-508ARH

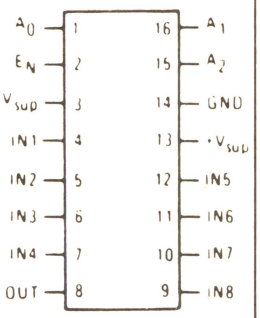
### Features

- Specifically designed for radiation hardness
- Analog/digital overvoltage protection
- Fail-safe with power loss (no latch-up)
- Break-before-make switching
- DTL/TTL/CMOS compatible
- Analog signal range: — ± 15 V
- Access time (typical): — 500 ns
- Supply current @ 1 MHz address toggle (typical): — 4 mA
- Standby power (typical): — 7.5 mW
- Full military temperature range

### Radiation Effects

- Dielectric Isolation technology
- Each lot screened for total dose hardness
- Parametrics guaranteed to $1 \times 10^5$ rads (Si)
- Latch-up free
- Tolerant to neutron fluence $\geq 1 \times 10^{13}$ n/cm² (E ≥ 10 KeV)
- Tolerant to gamma rate $> 1 \times 10^9$ rads (Si)/sec

### Pinout




## 16-Channel Multiplexer-High-Z Analog Input Protection
## HS-1840RH

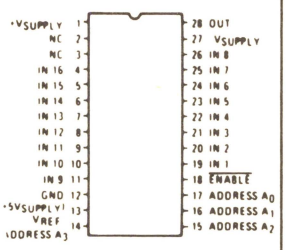
### Features

- Analog signal range: -5 V to + 15 V
- Specifically designed for radiation hardness
- High analog input impedance during power loss (open): — 500 MΩ
- Low standby power consumption (typical): — 600 μW
- Access time (typical): — 500 ns
- Excellent in hi-rel redundant systems
- Full military temperature range
- Break-before-make switching

### Radiation Effects

- Dielectric Isolation technology
- Each lot screened for total dose hardness
- Parametrics guaranteed to $2 \times 10^5$ rads (Si)
- Latch-up free
- Tolerant to neutron fluence $> 1 \times 10^{13}$ n/cm² (E ≥ 10 KeV)
- Tolerant to gamma rate $> 1 \times 10^9$ rads (Si)/sec

### Pinout

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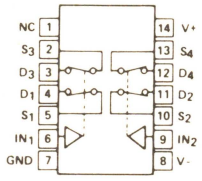
# Radiation Hardened CMOS Analog Switches

## Radiation Hardened CMOS Analog Switches HS-302RH, HS-303RH, HS-306RH, HS-307RH, HS-384RH, HS-390RH

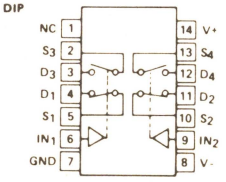
| Features | Radiation Effects |
|---|---|
| • Pin for pin compatible with Harris HI-3XX series analog switches<br>• Analog signal range: ± 15 V<br>• Low leakage (pre RAD typical at 25°C): 90 pA<br>• Low $R_{ON}$ (pre RAD typical at 25°C): 30Ω<br>• Break-before-make delay (typical): 65 ns<br>• Full military temperature range<br>• Low operating power | • Dielectric Isolation technology<br>• Each lot screened for total dose hardness<br>• Parametrics guaranteed to 1 x $10^5$ rads (Si)<br>• Latch-up free<br>• Tolerant to neutron fluence > 5 x $10^{13}$ n/cm² (E ≥ 10 KeV)<br>• Tolerant to gamma rate > 1 x $10^9$ rads (Si)/sec |

### PINOUTS

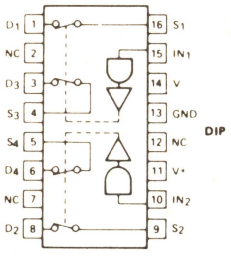
DUAL DPST
HS-302/306RH



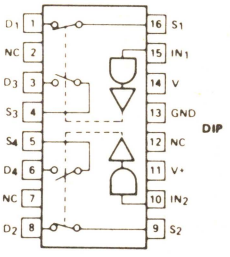

DUAL SPDT
HS-303/307RH




HS-384RH
DUAL DPST

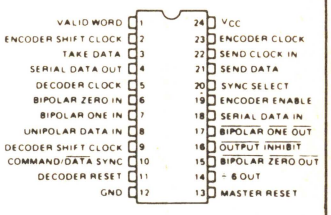



DUAL SPDT
HS-390RH




# RAD-HARD CMOS COMMUNICATION PRODUCTS

## Manchester Encoder/Decoder (MED) HS-15530RH

| Features | Radiation Effects | Pinout |
|---|---|---|
| • Specifically designed for radiation hardness<br>• Support of MIL-STD-1553<br>• 1.0 Mbit/sec data rate<br>• Sync identification and lock-in<br>• Clock recovery<br>• Manchester II encode, decode<br>• Separate encode and decode<br>• Low operating power: 50 mW @ 5 V<br>• Full military temperature range | • Each lot screened for total dose hardness<br>• Parametrics guaranteed to 1 x $10^5$ rads (Si)<br>• Latch-up free<br>• Upset: > $10^8$ rads (Si)/sec |  |



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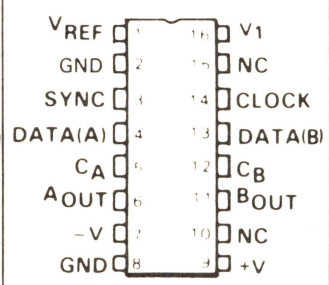
# SPECIALIZED PRODUCTS

## ARINC 429 Bus Interface Line Driver Circuit HS-3182

### Features

- Inputs TTL and CMOS compatible
- Adjustable rise and fall times via two external capacitors
- Programmable output differential range via voltage reference input ($V_{REF}$)
- Outputs are inhibited (0 V) if data (A) and data (B) inputs are both in the "logic one" state
- Can operate up to a 100-Kbit data rate
- Output short circuit proof and contains overvoltage protection
- Data "A" and Data "B" signals are "AND'D" with clock and sync signals
- Full military temperature range

### Pinout

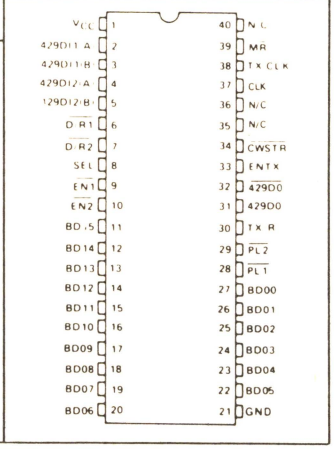



## ARINC 429 Bus Interface Circuit HS-3282

### Features

- ARINC specification 429 compatible
- Data rates of 100 Kbits or 12.5 Kbits
- Separate receiver and transmitter section
- Dual and independent receivers, connecting directly to ARINC bus
- Serial to parallel receiver data conversion
- Parallel to serial transmitter data conversion
- Word lengths of 25 or 32 bits
- Parity status of received data
- Generate parity of transmitter data
- Automatic word gap timer
- Single 5 V supply
- Low power dissipation
- Full military temperature range

### Pinout

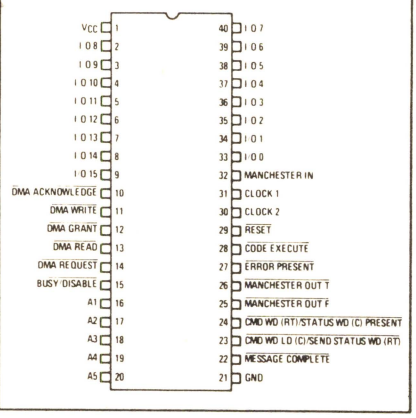



## MIL-STD-1553B Bus Interface Circuit HS-3273

### Features

- MIL-STD-1553C compatible
- Up to 5 MHz data rate for non-MIL-STD-1553C applications
- Parallel to serial transmitter data conversion
- 8/16 bits host I/O interface
- Error interception and recognition
- DMA capability
- Single 5 V power supply
- Full military temperature range

### Pinout

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# RAD-HARD SEMICUSTOM CIRCUIT TECHNOLOGY

## HS-CXXXRH Cell Library

**Features**

- Recommended as the most efficient library for customer circuits implemented in terms of 74 LS or 4000 Series functions
- Over 80 logic functions in cell library
- Soft-coded macros
- Individual data sheets
- 2.5-micorn SLM CMOS and 2.0-micorn DLM CMOS technology
- 40 MHz clock frequency
- TTL/CMOS compatible
- Full military temperature ranges
- Multiple package options
- Processed to either Class B or Class S equivalent flow
- Guaranteed rad-hard to $> 2 \times 10^5$ rads (Si)
- Upset: $\geq 1 \times 10^9$ rads (Si)/sec
- Functional after $1 \times 10^6$ rads (Si) total dose

## HS-DXXXRH High-Density (HD) CMOS Standard Cell Library

**Features**

- Recommended as the most efficient library for customer circuits implemented in terms of logic primitives, i.e., gates and flip flops
- Over 100 logic functions in the HD cell library
- 2.5-micron silicon gate CMOS technology
- 3 ns typical gate delay
- Full military temperature ranges
- Utilizes analog or memory drop in functions
- Multiple package options
- 5000 gate, 120 I/O chip complexity
- Total dose $1 \times 10^5$ rads (Si)
- Latch-up free

## CMOS Gate Array Family HS-G0600RH, HS-G1200RH, HS-G2500RH

| Description | Features |
|---|---|
| 600 gates, 54 I/O pins<br><br>1200 gates, 78 I/O pins<br><br>2500 gates, 100 I/O pins | • 3-micron CMOS technology<br>• 3 ns typical gate delay<br>• 10 MHz clock frequency<br>• 74 LS-SSI/MSI library implemented<br>• Advanced CAD Teledesign™ software support<br>• Individually programmable I/O buffers<br>• Bi-directional and three-state I/O<br>• TTL/CMOS compatible<br>• Full military temperature ranges<br>• Multiple package options<br>• Total dose $1 \times 10^5$ rads (Si) |

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# GaAs FET PRODUCTS

| Products And Services | GaAs FET Products |
|---|---|
| Gallium Arsenide-based standard and custom products are available from Harris Microwave Semiconductor (HMS), located in Milpitas, CA.<br>Standard products include:<br>1. GaAs Field Effect Transistors (GaAs FETs) for RF and microwave applications.<br>2. GaAs Digital Integrated Circuits for high speed signal processing.<br>3. GaAs Monolithic Microwave Integrated Circuits (MMICs) for broadband amplification of RF and microwave signals in receive, transmit, and IF stage applications.<br>Custom design and fabrication services are available whereby customers can design or specify specialized digital, MMIC or FET products for manufacture at HMS. Currently in development is a GaAs cell library of standard logic elements and I/O circuits for use with the GaAs DIGI-1 and DIGI-2 processes. Contact a Harris Design Center for current status and details. Analysis, testing, packaging, and screening options are available for all standard and custom products. | Microwave GaAs FETs from Harris Microwave Semiconductor have been designed and built for performance, reliability and consistency. To achieve these objectives, Harris employs extremely low defect gallium arsenide substrates of its own manufacture, ion implantation, a Ti/Pt/Au metallization system, large cross-section "T" gate structure and integral dielectric scratch and short circuit protection.<br>Each wafer undergoes an extensive reliability and performance qualification procedure exceeding the element evaluation requirements of MIL-STD-883C, Method 5008, Class B. Each die is DC tested and visually inspected prior to packaging and shipment. To accommodate specialized requirements, Harris can provide selections tailored to meet these needs. High-reliability screening and qualification testing are available on all Harris GaAs FET Products. |

# HIGH GAIN FET PRODUCTS

| P/N HMF- | MAG* (dB) | | PMAG (dBm) | $G_{1dB}$ (dB) | $P_{1dB}$* (dBm) | | FREQ (GHz) | BIAS $V_{DS}$.$I_{DS}$ | APPLICATION/ DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | | | MIN | TYP | | | |
| 03100-100 | 6.0 | 7.5 | 11 | 4.5 | 13 | 15 | 18 | 4 V, 20 mA | 2-20 GHz Low Noise |
| 03100-200 | 6.0 | 7.5 | 13.5 | 4.5 | 18 | 19 | 18 | 6 V, 50% $I_{DSS}$ | 2.20 GHz Gain/Drive |
| 03100-300 | 6.0 | 7.5 | 14.5 | 4.5 | 20 | 21 | 18 | 6 V, 50% $I_{DSS}$ | 2-20 GHz Drive |
| 0330 | — | 7.5 | 13.5 | 5.0 | — | 14 | 18 | 4 V, 20 mA | 2-20 GHz Low Noise, Low Current |
| 0610 | 5.0 | 6.0 | 19.5 | 4.0 | 21.5 | 23.5 | 18 | 6 V, 50% $I_{DSS}$ | 2-20 GHz Power |
| 0620 | — | 10 | 17 | 7.0 | — | 20 | 12 | 4 V, 50% $I_{DSS}$ | 2-14 GHz High Transconductance |
| 1210 | — | 6.0 | 22 | 4.0 | — | 25 | 18 | 6 V, 50% $I_{DSS}$ | 2-20 GHz Power |




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# HIGH POWER FET PRODUCTS

| P/N HMF- | $G_{1dB}$ (dB) | $P_{1dB}$* (dBm) | | $\eta$ (%) | FREQ (GHz) | MAG* (dB) | | $P_{MAG}$ (dBm) | FREQ (GHz) | BIAS $V_{DS}$, $I_{DS}$ | APPLICATION/ DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | | | MIN | TYP | | | | |
| 0300 | 8.5 | — | 21.5 | 35 | 8 | — | 12 | 18 | 8 | 8 V, 50% $I_{DSS}$ | 2-18 GHz, 125 mW |
| 0600 | 8 | — | 24.5 | 35 | 8 | — | 10 | 22 | 8 | 8 V, 50% $I_{DSS}$ | 2-18 GHz, 250 mW |
| 12000-100 | 7.5 | 25.5 | 27 | 30 | 8 | 9 | 10 | 25.0 | 8 | 8 V, 50% $I_{DSS}$ | 2-16 GHz, 500 mW |
| 12000-200 | 7.5 | 27.5 | 28.5 | 35 | 8 | 8 | 9 | 25.5 | 8 | 8 V, 50% $I_{DSS}$ | 2-16 GHz, 650 mW |
| 24000-100 | 5.0 | 28.5 | 29.5 | 25 | 8 | 6.0 | 8.0 | 27.0 | 8 | 8 V, 50% $I_{DSS}$ | 2-14 GHz, 800 mW |
| 24000-200 | 5.0 | 30.0 | 31.0 | 30 | 8 | 6.0 | 8.0 | 28.5 | 8 | 8 V, 50% $I_{DSS}$ | 2-14 GHz, 1.2 mW |

*Compliance with microwave performance limits for MAG and P1dB is confirmed by qualifying wafers on sample evaluation basis.

# GaAs MMIC STANDARD PRODUCTS

## HMM Series

Our half-micron (gate length) family of fully integrated MMIC amplifiers is intended for broadband applications where noise figure, gain or output power are key specifications in a system design.

## HMM Product Family — Electrical Specifictions

| Model No. | Frequency Band (GHz) | Small Signal Gain (dB) | | Gain Flatness (Over full BW) (dB) Max | 1dB Gain Compression Output Power (dBm) Typ | Noise Figure (dB) Typ | VSWR | |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | | | | | Max |
| HMM-10610 | 2 — 6 | 10 | 12 | ± .5 | + 19 | 6 | Input<br>Output | 2:1<br>1.75:1 |
| HMM-11810 | 6 — 18 | 4.5 | 5 | ± .75 | + 16.5 | 6.5 | | 2:1 |

$V_{DD}$ = 5V, $I_{DD}$ = 120 mA (typical/HMM-10610) / 100 mA (typical/HMM-11810)

## HMR Series

For lower frequency application, specify the Harris HMR one-micron (gate length) MMIC family. Distributed as gain blocks throughout your system, they often permit relaxing the specifications of other cost-critical components.

## HMR Product Family — Electrical Specifictions

| Model No. | Frequency Band (GHz) | Small Signal Gain (dB) Typ | Gain Flatness (Over full BW) (dB) Max | 1dB Gain Compression Output Power (dBm) Typ | Noise Figure (dB) Typ | VSWR | |
|---|---|---|---|---|---|---|---|
| | | | | | | Typ | Max |
| HMR-10502 | 0.5 — 5 | 9.5 | ± .75 | + 10 | 7 | 1.7:1 | 2:1 |
| HMR-10503 | 1 — 5 | 9.5 | ± .75 | + 10 | 7 | 1.7:1 | 2:1 |

$V_{DD}$ = 10V, $I_{DD}$ = 100 mA



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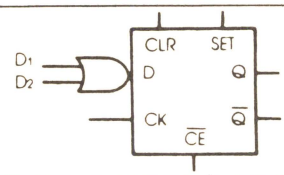
# GaAs DIGITAL IC STANDARD PRODUCTS

## Master/Slave D Flip-Flop HMD-11131-2

**Features**

- 2.5 GHz single clock input speed
- ECL & GaAs compatible I/Os
- Asynchronous clear & set
- Dual phase clock through CK, CE permits higher speed operation

**Logic Symbol**

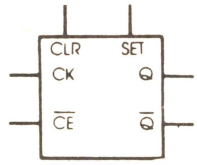



## Divide By 2 Prescaler HMD-11301-2

**Features**

- 2.7 GHz input clock speed
- Complementary ECL outputs
- 50 ohm line driving capability
- CE can be used to tailor device operation

**Logic Symbol**

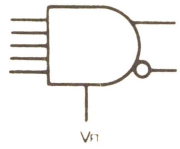



## 5-Input NAND/AND Gate HMD-11104-2

**Features**

- 2.5 GHz data input rate
- ECL and GaAs compatible I/Os
- Propagation delay 500ps typical
- VFT input for optimized propagation delay

**Logic Symbol**

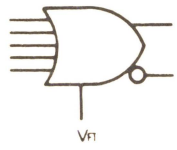



## 5-Input NOR/OR Gate HMD-11101-2

**Features**

- 2.5 GHz data input rate
- Extended temperature range: -55°C to +85°C
- Propagation delay of 500ps typical
- ECL and GaAs compatible I/Os
- VFT input for optimized propagation delay

**Logic Symbol**




## Dual 2-Input Exclusive OR Gate HMD-11113-2

**Features**

- 2.5 GHz data input rate
- Propagation delay 650ps typical
- Extended temperature range: -55°C to +85°C

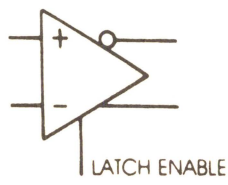
**Logic Symbol**

## Ultra-High Speed Comparator HMD-11685-2

**Features**

- 2.0 GHz input clock speed
- Latch enable for sample and hold mode
- 50 ohm line driving capability
- Propagation delay 500ps typical
- Transition time 150ps typical
  (Contact Harris Microwave Semiconductor for availability)

**Logic Symbol**

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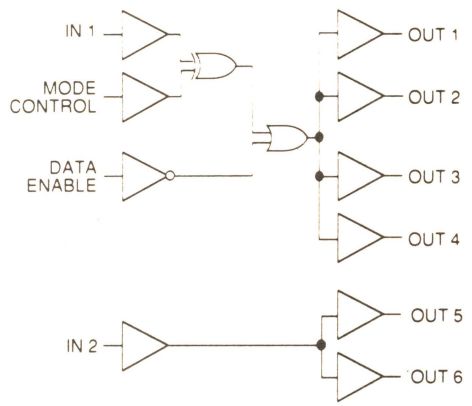
# GaAs DIGITAL IC STANDARD PRODUCTS

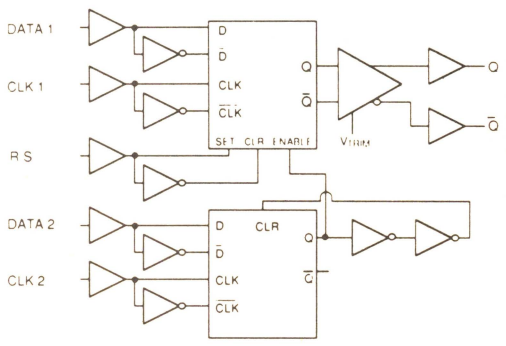
| DUAL, CLOCK DRIVER/FANOUT BUFFER | |
|---|---|
| **Part Number** | **Features** |
| HMD-11188-2 | • 1.8 GHz Input Clock Speed<br>• ECL and GaAs Compatible I/Os<br>• Propagation Delay of 500ps Typical<br>• 50 Ohm Line Driving Capability<br>• Extended Temperature Range: -55°C to +85°C |

**LOGIC DIAGRAM**



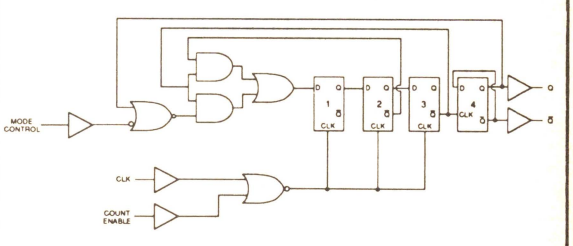

| PROGRAMMER PULSE DRIVER/FORMATTER | |
|---|---|
| **Part Number** | **Features** |
| HMD-11502-2 | • 1.0 GHz Input Clock Speed<br>• ECL and GaAs Compatible I/Os<br>• Propagation Delay of 500ps Typical<br>• 50 Ohm Line Driving Capability<br>• Control of Pulse Width, Pulse Polarity and Number of Pulses |

**LOGIC DIAGRAM**




| DIVIDE BY 10/11 VARIABLE MODULUS DIVIDER | |
|---|---|
| **Part Number** | **Features** |
| HMD-11011-2 | • 2.0 GHz Typical Input Clock Speed<br>• ECL and GaAs Compatible I/Os<br>• Propagation Delay of 950ps Typical<br>• 50 Ohms Impedance Operation<br>• Count Enable Control of Gated Clocking |

**LOGIC DIAGRAM**

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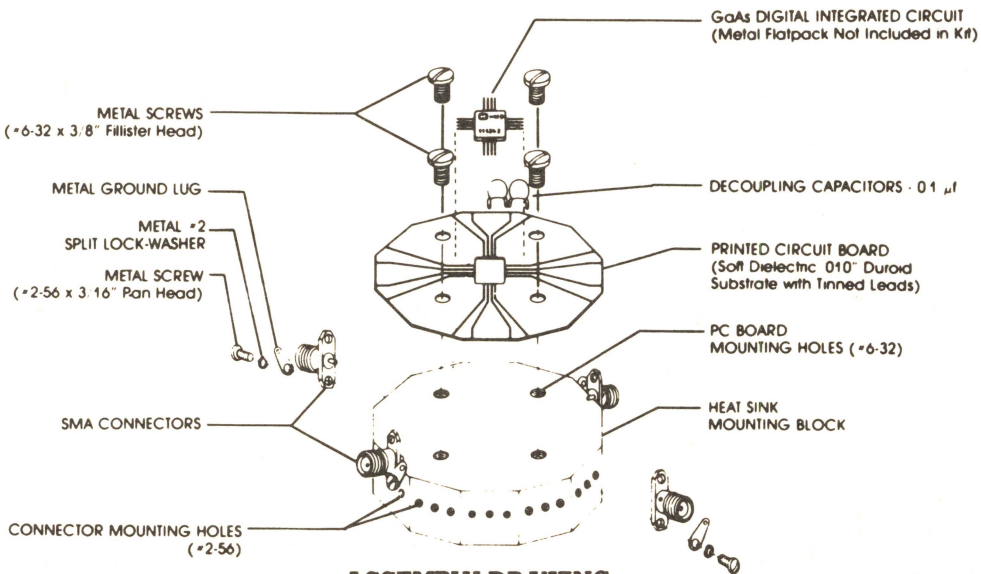
# GaAs DIGITAL IC STANDARD PRODUCTS

## GaAs Digital IC Standard Products

| FOUR-BIT UNIVERSAL SHIFT REGISTER | |
|---|---|
| **Part Number** | **Features** |
| HMD-12141-1 | • 1.3 GHz Clock Speed<br>• Shift Right, Shift Left, Parallel, or Hold<br>• Serial or Parallel Inputs and Outputs<br>• ECL Compatible & GaAs Compatible Input and Outputs<br>• 32 Pin Metal Flatpack Design<br>• Ti/Pt/Au Metallization System |

| DIVIDE BY 2/4/8 HIGH SPEED SYNCHRONOUS COUNTER | |
|---|---|
| **Part Number** | **Features** |
| HMD-11016-1 | • 2.0 GHz Data Input Rate<br>• Synchronous Operation; Simultaneous Divide by 2, 4 and 8 Output<br>• ECL Compatible GaAs Compatible Inputs and Outputs<br>• Extended Temperature Range: -55°C to +85°C<br>• 50 Ohm Impedance System Operation<br>• Asynchronous Master Clear and Enable for Down Counter Operation |

| GaAs DIGITAL IC EVALUATION KITS | |
|---|---|
| **Part Number** | **Features** |
| HMK-11MSI-1<br>HMK-11SSI-2 | • MSI IC Evaluation Kit for 32 Pin Packages<br>• SSI IC Evaluation Kit for 16 Pin Packages<br>(Individual ICs Not Included in Kits) |




**ASSEMBLY DRAWING**





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# GaAs Custom MMIC Programs

| Custom and Fabrication Services | |
|---|---|
| **KEY FEATURES** | **MMIC PROGRAM OPTIONS** |
| • Fully Documented Design Rule Book Includes Microwave and Physical Layout Rules<br>• 0.5 Micron Plated "T"-Gate Technology Based Upon Our Line of Discrete FETs (HMF-0310, -0610, etc.)<br>• Reliable Ti/Pt/Au Metallization<br>• Ion Implantation Processing for Uniformity, Consistency<br>• Circuit Elements<br>▸ "n+" Type (Low Sheet RHO) Resistors<br>▸ "n" Type (High Sheet RHO) Resistors<br>▸ Diodes<br>▸ FETs<br>▸ Dual Gate FETs<br>▸ Transmission Lines<br>▸ Inductors<br>▸ Capacitors<br>▸ Through Substrate Via Holes | • Gain, Power or Low Current FET Models and Processing<br>• Circuit Design from Customer Specs<br>• "Layout" from Customer-Supplied Design<br>• Computer Simulation of Design<br>• Generation of Digitized Data From Customer Drawing<br>• RF Screening of Selected Parts *(i.e., #/Wafer)*<br>• Special Packaging/Assembly<br>• Specialized DC Testing<br>• Volume Quotations on Qualified Wafers<br>• High Reliability Screening<br>• Supplementary Consultation/Training |

**TABLE 2. PROCESSES FOR CUSTOM MMICs**

| PROCESS TYPE (GATE LENGTH) | PRATICAL OPERATING FREQUENCIES | $f_t$ | $f_{max}$ | PROCESS OPTIONS |
|---|---|---|---|---|
| 0.5 Micron | 0.5 to 20 GHz | 18 GHz | 40 GHz | High Gain, Low Current High Power |
| 1.0 Micron | 0.1 to 12 GHz | 12 GHz | 26 GHz | High Gain |

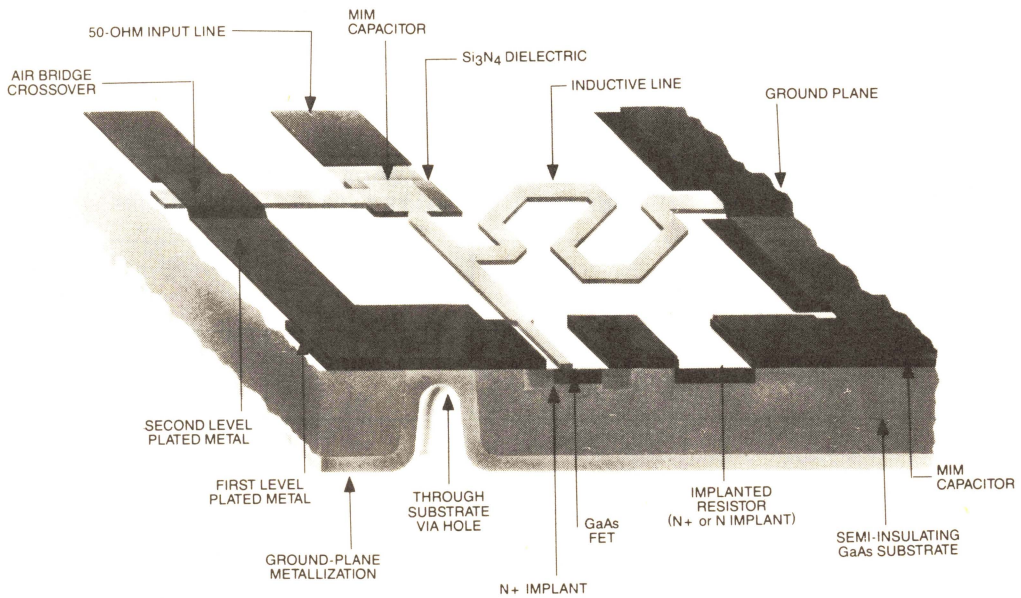


**FIGURE 2. FEATURES OF A TYPICAL MMIC CHIP**

# GaAs CUSTOM DIGITAL PROGRAMS

## HMS CELL LIBRARY

The HMS Library is an open ended collection of logic elements implemented in Harris 1 micron, 1 volt pinch-off technology. The library contains all the information required to support schematic capture simulation, timing analysis, and layout. Each cell has been optimized for speed, and power performance while minimizing die area.

Full GaAs DRC, Extraction, Abstract Generation and Layout vs. Schematic (LVS) comparisons are supported for these cells on UNIX-based workstations. Each cell is defined in terms of rise and fall delay, set-up and hold times, under best, typical, and worst case operating conditions.

## GaAs DIGITAL IC DESIGN AND FABRICATION

The logic family used for custom and standard digital ICs is a buffered FET logic or BFL family based on Harris Microwave Semiconductor's DIGI-1 process. It uses depletion mode FETs with a -2 volt pinch-off level. The DIGI-1 process, with its large internal logic swing, maintains noise margin and resistance to environmental factors without complex circuitry for temperature compensation. It is a very robust logic family that allows large internal fanouts with minimum speed degradation. Speeds up to 3 GHz are possible depending upon circuit complexity.

DIGI-2 is the main process used and characterized for the HMS standard cell family. DIGI-2 allows high speed operation but with an order of magnitude reduction in power dissipation over DIGI-1 by virtue of its -1V pinch-off voltage. Speeds up to 1.5 GHz are possible with DIGI-2 depending upon circuit complexity.

The DIGI-1 and DIGI-2 process characteristics are summarized in Table 1 and the process cross-section is shown in Figure 1.

The process consists of direct ion implantaion into undoped semi-insulating, Liquid-Encapsulated Czochralski (LEC) GaAs substrates to form the active region. A one micron Schottky barrier gate is used to form the depletion mode MESFET transistors and Schottky diodes on the GaAs substrates.

Two levels of interconnect are used, one of which is shared with gate structures on the depletion mode transistors. The second level is a plated airbridge used for interconnect. Silicon nitride protects the GaAs surface and makes up part of the intermetal insulating dielectric area. The process has resulted in chips with fanouts of three and propagation delays of only 100ps.

TABLE 1. PROCESSES FOR DIGITAL IC PROGRAMS

| PROCESS TYPE | MAXIMUM GATE COUNT | TYPICAL CHIP SPEED | TYPICAL GATE DELAY | POWER DISSIPATION |
|---|---|---|---|---|
| 1.0 Micron; -1 Volt Pinch-off | 800 Gates | 1.5 GHz | 180 ps | 3 to 5 mW per Gate |
| 1.0 Micron; -2 Volt Pinch-off | 300 Gates | 2.5 GHz | 120 ps | 20 to 35 mW per Gate |




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# 80C286

## High Performance Microprocessor With Memory Management and Protection

September 1987

### Features

- Compatible with NMOS 80286
- Static CMOS Design for Low Power Operation
  - ICCSB = 5mA Maximum
  - ICCOP = 20mA/MHz Maximum
- High Performance Processor (Up to Nine Times the Throughput of the 8086)
- Large Address Space:
  - 16 Megabytes Physical
  - 1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two 80C86 Upward Compatible Operating Modes:
  - 80C286 Real Address Mode
  - Protected Virtual Address Mode
- Compatible with 80287 Numeric Data Co-processor
- Wide Range of Clock Rates:
  - DC to 12.5MHz (80C286-12)
  - DC to 10MHz (80C286-10)
- High Bandwidth Bus Interface (12.5 Megabyte/Sec)
- Available in 68 Pin PGA (Pin Grid Array) Package

### Description

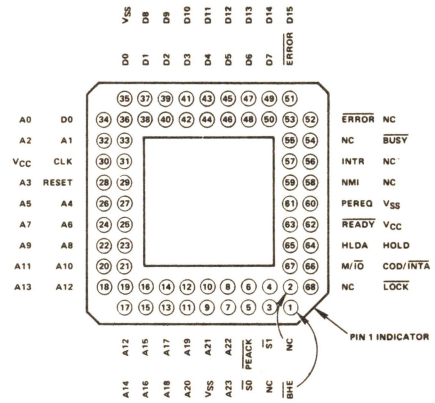
The Harris 80C286 is a static CMOS version of the NMOS 80286 microprocessor. The 80C286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80C286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. A 12.5MHz 80C286 provides nine times or more throughput than the standard 5MHz 8086. The 80C286 includes memory management capabilities that map $2^{30}$ (one gigabyte) of virtual address space per task into $2^{24}$ bytes (16 megabytes) of physical memory.

The 80C286 is upwardly compatible with 80C86 and 80C88 software (the 80C286 instruction set is a superset of the 80C86/80C88 instruction set). Using the 80C286 real address mode, the 80C286 is object code compatible with existing 80C86 and 80C88 software. In protected virtual address mode, the 80C286 is source code compatible with 80C86 and 80C88 software but may require upgrading to use virtual address as supported by the 80C286's integrated memory management and protection mechanism. Both modes operate at full 80C286 performance and execute a superset of the 80C86 and 80C88 instructions.

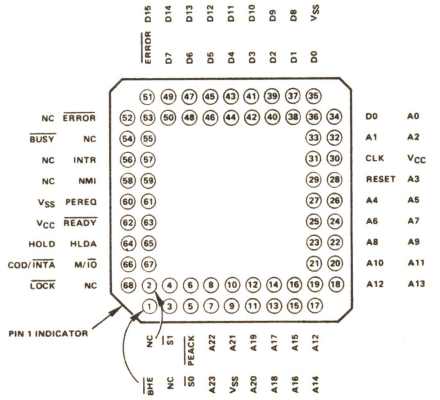
The 80C286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80C286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

### Pin Configurations

**Component Pad Views** — As viewed from underside of the component when mounted on the board.




**P.C. Board Views** — As viewed from the component side of the P.C. board.




CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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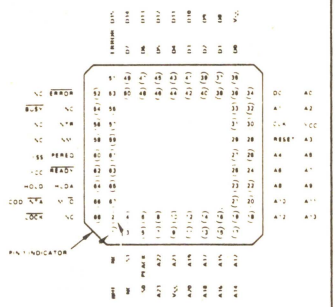
# CMOS STATIC MICROPROCESSORS

## High Performance Microprocessor With Memory Management and Protection
## 80C286

### Features

- Compatible with NMOS 80286
- Static CMOS Design for Low Power Operation
  > ICCSB = 5mA Maximum
  > ICCOP = 20mA/MHz Maximum
- High Performance Processor (Up to Fourteen Times the Throughput of the 8086)
- Two 80C86 Upward Compatible Operating Modes:
  > 80C286 Real Address Mode
  > Protected Virtual Address Mode
- Wide Range of Clock Rates:
  > DC to 16MHz (80C286-16)
  > DC to 12.5MHz (80C286-12)
  > DC to 10MHz (80C286-10)
- Available in 68 Pin PGA (Pin Grid Array) and PLCC (plastic leaded chip carrier) packages

### Pinout

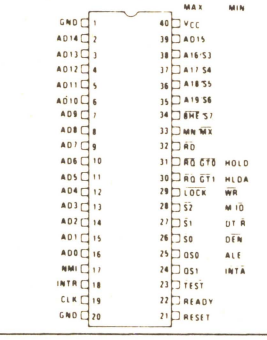


## 16-Bit Microprocessor
## 80C86

### Features

- Compatible with NMOS 8086
- Completely static design
  — DC to 5 MHz (80C86)
  — DC to 8 MHz (80C86-2)
- Low power operation:
  — 10 mA/MHz operating current
  — 500 $\mu$A standby current
- 1 MByte of direct memory addressing capability

### Pinout

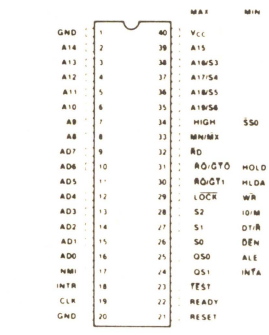



## 8-Bit Microprocessor
## 80C88

### Features

- Compatible with NMOS 8088
- Completely static design
  — DC to 5 MHz (80C88)
  — DC to 8 MHz (80C88-2)
- Low power operation:
  — 10 mA/MHz operating current
  — 500 $\mu$A standby current
- Software compatible with 80C86/8086/8088
- 1 MByte of direct memory addressing capability

### Pinout

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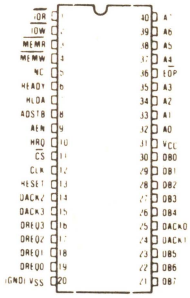
# CMOS PERIPHERAL CIRCUITS

## DMA Controller 82C37A

### Features

- Compatible with NMOS 8237A
- Provides control for direct memory access operation
- Up to 4 Mb/s transfer rate with 8 MHz clock
- Four independently programmable DMA channels
- Low power operation

### Pinout

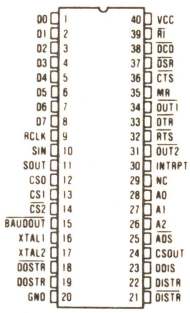



## Asynchronous Communication Element 82C50A

### Features

- Complete serial communication interface
  - — UART
  - — Baud rate generator
- 80C86/88 compatible
- DC to 10 MHz operation (DC to 625 Kbaud)
- Modem interface control lines
- Low CMOS power dissipation
- Compatible with NMOS 8250A

### Pinout

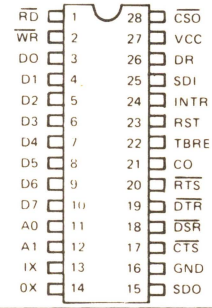



## Serial Controller Interface 82C52

### Features

- UART/Baud rate generator in a single 28-pin package
- Operates from DC to 1 Mbaud with an asynchronous 16X clock
- 72 programmable baud rates
- Low power operation:
  - — 1 mA/MHz operating current, typical
- 40-pin version available (HD-6406)

### Pinout

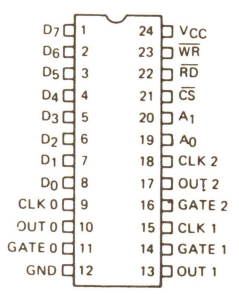



## Programmable Interval Timer 82C54

### Features

- Compatible with NMOS 8254
- Enhanced version NMOS 8253
- Three independent 16-bit counters
- Six programmable counter modes
- Completely TTL compatible
- 8 MHz count frequency
- Low power operation:
  - >ICCOP: 10 mA @ 8 MHz count frequency
  - >ICCSB: 10 $\mu$A maximum

### Pinout



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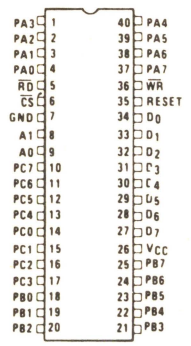
# CMOS PERIPHERAL CIRCUITS

## Programmable Peripheral Interface 82C55A

### Features

- Multiple peripheral functions in a single package
  - — Five 8-bit counters
  - — Two 8-bit programmable I/O ports
  - — Eight-level interrupt controller
  - — UART and baud rate generator
- Low CMOS power dissipation
- Compatible with NMOS 8255A
- High darlington drive outputs

### Pinout

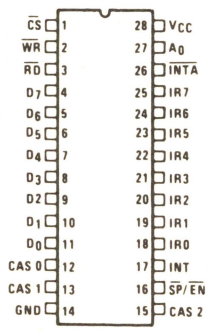



## Priority Interrupt Controller 82C59A

### Features

- Compatible with NMOS 8259A
- Eight maskable interrupt inputs
- Cascade operation allows up to 64 interrupt inputs with no additional circuitry
- Supports both 8080/85 and 80C86/88 formats
- Standby current: 10 $\mu$A, maximum
- Fully TTL compatible
- Programmable interrupt modes

### Pinout

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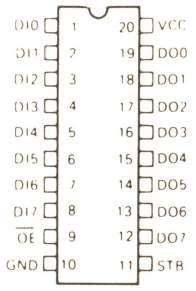
# CMOS BUS SUPPORT CIRCUITS

## Octal Latching Bus Driver
## 82C82

### Features

- Bipolar 8282 function compatible
- Propagation delay guaranteed: 35 ns maximum
  - — Full temperature range
  - — 10% power supply tolerances
  - — Load capacitance: 300 pf
- Gated inputs reduce operating power
- ICCSB: 10 $\mu$A maximum

### Pinout

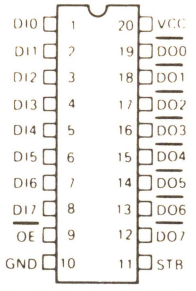



## Octal Latching Inverting Bus Driver
## 82C83H

### Features

- Bipolar 8283 function compatible
- Full eight-bit latching buffer with inverted data output
- Guaranteed propagation delay of 25 ns Max. @ $C_L = 300$ pf
- Gated inputs reduce operating power
- ICCSB: 10 $\mu$A maximum
- High output sink current: 20 mA

### Pinout

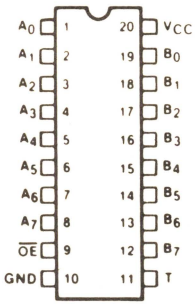



## Octal Transceiver
## 82C86H

### Features

- Bipolar 8286 function compatible
- Eight-bit bidirectional bus transceiver
- Guaranteed propagation delay of 32 ns Max. @ $C_L = 300$ pf
- Gated inputs reduce power dissipation
- ICCSB: 10 $\mu$A maximum
- High output sink current: 20 mA

### Pinout

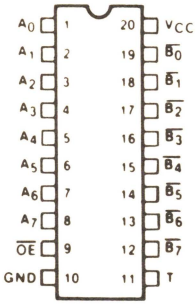



## Octal Inverting Transceiver
## 82C87H

### Features

- Bipolar 8287 function compatible
- Eight-bit bidirectional bus transceiver with inverting data outputs
- Guaranteed propagation delay of 30 ns Max. @ $C_L = 300$ pf
- Gated inputs reduce operating power dissipation
- ICCSB: 10 $\mu$A maximum
- High output sink current: 20 mA

### Pinout

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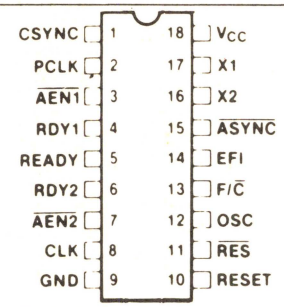
# CMOS BUS SUPPORT CIRCUITS

## Clock Generator/Driver 82C84A

### Features

- Compatible with bipolar 8284A
- Output frequencies up to 8 MHz
- Provides ready synchronization
- Parallel resonant crystal
- ICCOP: 40 mA @ 8 MHz system frequency
- TTL compatible inputs/outputs

### Pinout

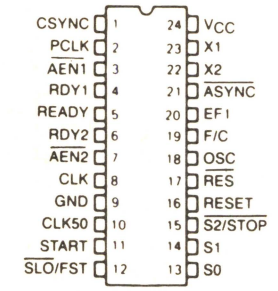



## Static Clock Controller/Generator 82C85

### Features

- Provides complete static clock control for 80C86 and 80C88 systems
- Supports stop-clock, stop-oscillator and low-frequency operation
- 80C86/88 status line interface allows software control
- DC to 8 MHz system clock
- Low CMOS power dissipation
- 24 pin slimline package

### Pinout

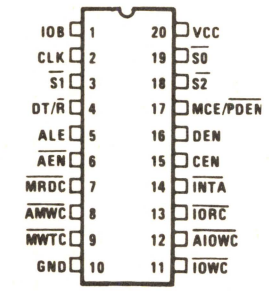



## Bus Controller 82C88

### Features

- Pin compatible with bipolar 8288
- Generates system control signals for maximum mode 80C86/88, 8086/88
- Bipolar drive capability
- Low power operation:
  - — ICC standby: 10 $\mu$A maximum
  - — ICC operating: 1 mA/MHz maximum

### Pinout

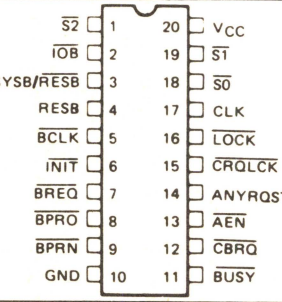



## Bus Arbiter 82C89

### Features

- Pin compatible with bipolar 8289
- Provides bus control arbitration in multi-master processor systems
- Low power operation:
  - — ICCSB: 10 $\mu$A maximum
  - — ICCOP: 1 mA/MHz maximum
- Bipolar drive capability

### Pinout

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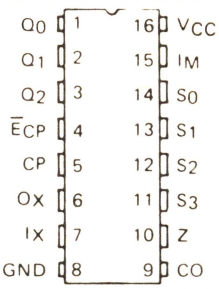
# CMOS DATA COMMUNICATION

## Bit Rate Generator (BRG) HD-4702

### Features

- Low power dissipation
- Programmable bit rate selection
- 13 commonly used bit rates
- Uses standard 2.4575 MHz crystal
- Conforms to EIA RS-404
- On-chip input pull-up circuits

### Pinout

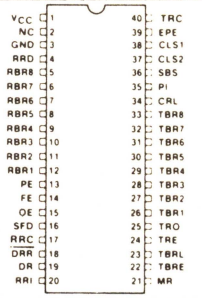



## Universal Asynchronous Receiver/Transmitter (UART) HD-6402R, HD-6402B

### Features

- Operates from DC to 8 MHz (DC to 500 Kbaud)
- Programmable word length, stop bits and parity
- Industry standard pinout
- Single +5 V power supply
- Fully TTL compatible
- Automatic data formatting and status generation

### Pinout

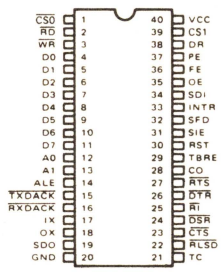



## Programmable Asynchronous Communications Interface HD-6406

### Features

- UART/Baud rate generator in a single 40-pin package
- Data rates from DC to 1 Mbaud with an asynchronous 16X clock
- 72 programmable baud rates
- Complete modem interface signals
- DMA handshaking operation
- Low power operation:
  — 1 mA/MHz, typical
- 28-pin version available (82C52)

### Pinout

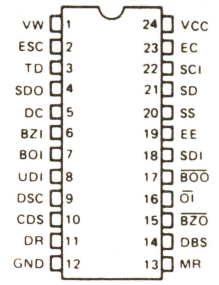



## Asynchronous Serial Manchester Adapter (ASMA) HD-6408

### Features

- 1 Mb/s data rate
- Sync identification and lock-in
- Clock recovery
- Manchester II encode and decode
- Low bit error rate
- Industrial temperature range
  — 40°C to +85°C

### Pinout

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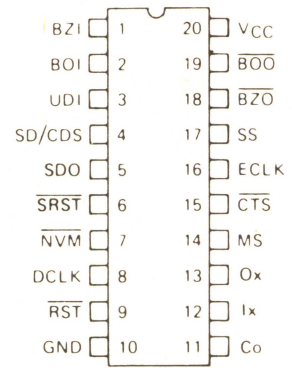
# CMOS DATA COMMUNICATION

## Manchester Encoder/Decoder (MED) HD-6409

### Features

- 1 Mb/s data rate
- Digital PLL clock recovery
- On chip oscillator
- Independent Manchester II encode and decode
- Wide temperature ranges available
  -40°C to +85°C
  -55°C to +125°C

### Pinout

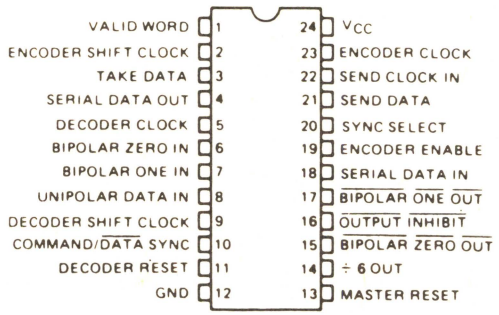



## Manchester Encoder/Decoder (MED) HD-15530

### Features

- Support of MIL-STD-1553
- 1.25 Mb/s data rate
- Sync identification and lock-in
- Clock recovery
- Independent Manchester II encode, decode
- Separate encode and decode
- Low operating power: 50 mW @ 5 Volts
- Full temperature range: -55°C to +125°C

### Pinout

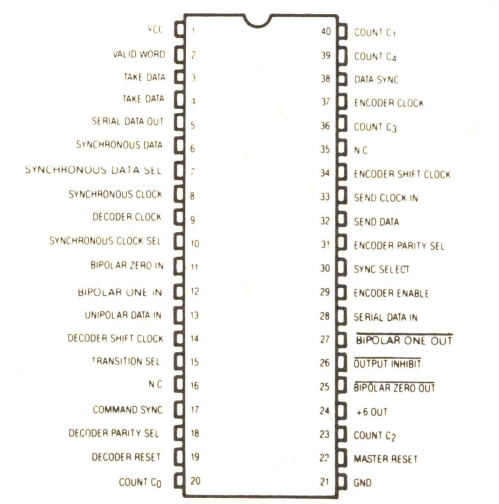



## Manchester Encoder/Decoder (MED) HD-15531

### Features

- Support of MIL-STD-1553
- 1.25 Mb/s data rate
- 2.5 Mb/s option (HD-15531B)
- Sync identification and lock-in
- Clock recovery
- Variable frame length to 32 bits
- Independent Manchester II encode, decode
- Separate encode and decode
- Low operating power: 50 mW @ 5 Volts
- Full temperature range: -55°C to +125°C

### Pinout

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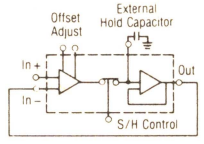
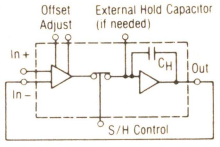
## Analog Switches

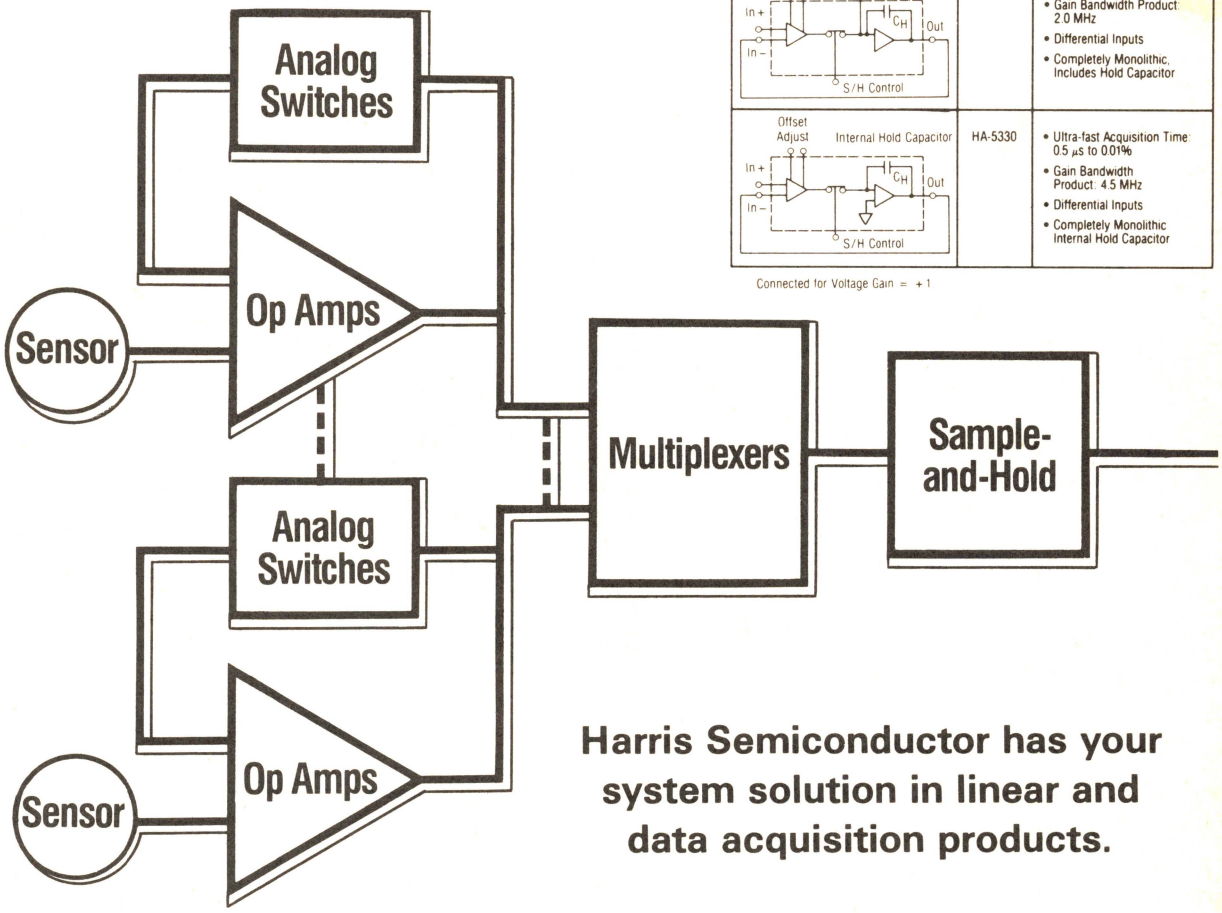
| Functions | General Purpose | Low $R_{ON}$ | Low Leakage (0.04 nA) | High Speed |
|---|---|---|---|---|
| SPST | — | HI-5040 (50Ω) | — | — |
| 2X SPST | HI-200 | HI-5041 (50Ω)<br>HI-5048 (25Ω) | HI-300 (TTL compatible)<br>HI-304 (CMOS compatible)<br>HI-381 (TTL compatible) | |
| 4X SPST | HI-201 | — | — | HI-201HS (30 ns) |
| SPDT | — | HI-5042 (50Ω)<br>HI-5050 (25Ω) | HI-301 (TTL compatible)<br>HI-305 (CMOS compatible)<br>HI-387 (TTL compatible) | |

| Functions | General Purpose | Low $R_{ON}$ | Low Leakage (0.04 nA) |
|---|---|---|---|
| 2X SPDT | — | HI-5043 (50Ω)<br>HI-5051 (25Ω) | HI-303 (TTL compatible)<br>HI-307 (CMOS compatible)<br>HI-390 (TTL compatible) |
| DPST | — | HI-5044 (50Ω) | — |
| 2X DPST | — | HI-5045 (50Ω)<br>HI-5049 (25Ω) | HI-302 (TTL compatible)<br>HI-306 (CMOS compatible)<br>HI-384 (TTL compatible) |
| DPDT | — | HI-5046 (50Ω)<br>HI-5046A (25Ω) | — |
| 4PST | — | HI-5047 (50Ω)<br>HI-5047A (25Ω) | — |

## Sample-and-Hold Amplifiers

| Configuration | Part Number | Features |
|---|---|---|
|  | HA-2420<br>HA-2425 | • DESC 80016CX<br>• Fast Acquisition Time: 3.2 μs to 0.01%<br>• Gain Bandwidth Product: 2.5 MHz<br>• Low Droop Rate: 5 μV/ms<br>• Differential Inputs<br>• Monolithic Construction |
|  | HA-5320 | • Ultra-fast Acquisition Time: 1 μs to 0.01%<br>• Gain Bandwidth Product: 2.0 MHz<br>• Differential Inputs<br>• Completely Monolithic, Includes Hold Capacitor |
|  | HA-5330 | • Ultra-fast Acquisition Time: 0.5 μs to 0.01%<br>• Gain Bandwidth Product: 4.5 MHz<br>• Differential Inputs<br>• Completely Monolithic Internal Hold Capacitor |

Connected for Voltage Gain = +1

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## Operational Amplifiers

| High Speed | | Precision | | Low Power | | General Purpose | | High Speed | Low Power Fixed Supply Current | | General Purpose | Precision |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bipolar | J-FET | Bipolar Programmable | Bipolar Fixed Supply Current | | | | | | | |
| **HA-2620:** 100 MHz<br>35 V/μs | **HA-2542:** 60 MHz<br>375 V/μs | **HA-5130:**<br>10 μV $V_{IO}$<br>0.4 μV/°C | **HA-5147:**<br>3 nV/√Hz<br>10 μV $V_{IO}$ | **HA-5170:**<br>100 μV $V_{IO}$<br>3 μV/°C | **HA-2720:**<br>±1.2 V/±18 V<br>15 μA | **HA-2600:**<br>12 MHz<br>7 V/μs<br>3 mV $V_{IO}$ | Duals | **HA-5112:** 60 MHz<br>20 V/μs<br>Low Noise | **HA-5142:**<br>Single Supply<br>+2 V/+40 V<br>45 μA | **HA-5152:**<br>200 μA<br>4.5 V/μs<br>1.3 MHz | **HA-5102:**<br>8 MHz<br>3 V/μs<br>Low Noise | |
| **HA-2520:** 20 MHz<br>120 V/μs<br>200 ns | | 35 V/μs<br>120 MHz | | **HA-5180:**<br>0.3 pA<br>$I_{BIAS}$ | **HA-5141:**<br>Single Supply<br>+2V/+40 V<br>45 μA | **HA-5101:**<br>10 MHz<br>10 V/μs<br>Low Noise<br>3.3 nV/√Hz | Quads | **HA-5114:** 60 MHz<br>20 V/μs<br>Low Noise | **HA-5144:**<br>Single Supply<br>+2 V/+40 V<br>45 μA | **HA-5154:**<br>200 μA<br>4.5 V/μs<br>1.3 MHz | **HA-4741:**<br>3.5 MHz<br>1.6 V/μs<br>1 mV $V_{IO}$<br>Low Noise | **HA-5134:**<br>4 MHz<br>1 V/μs<br>50 μV $V_{IO}$<br>Low Noise |
| **HA-5160:** 120 MHz<br>120 V/μs<br>J-FET | **HA-5147:** 120 MHz<br>35 V/μs<br>3 nV/√Hz | **HA-5127:**<br>3 nV/√Hz<br>10 μV $V_{IO}$<br>10 V/μs | | | | | | **HA-2400 (PRAM):**<br>40 MHz<br>30 V/μs<br>4 channel<br>Addressable | | | **HA-5104:**<br>8 MHz<br>3 V/μs<br>Low Noise | |
| **HA-5190:** 150 MHz<br>200 V/μs<br>70 ns | 10 μV $V_{IO}$ | **HA-5137:**<br>3 nV/√Hz<br>10 μV $V_{IO}$<br>20 V/μs | | | | | | | | | | |
| **HA-2540:** 400 MHz<br>400 V/μs | **HA-2544:** 33 MHz<br>@ $A_{CL}$ = 1<br>150 V/μs S.R. | | | | | | | | | | | |
| **HA-2539:** 600 MHz<br>600 V/μs | $I_{CC}$ = 10 mA<br>**HA-2529:** 20 MHz<br>160 V/μs | | | | | | | | | | | |
| **HA-2541:** 40 MHz<br>@ $A_{CL}$ = 1<br>280 V/μs<br>90 ns | 200 ns<br>30 mA $I_{out}$ | | | | | | | | | | | |

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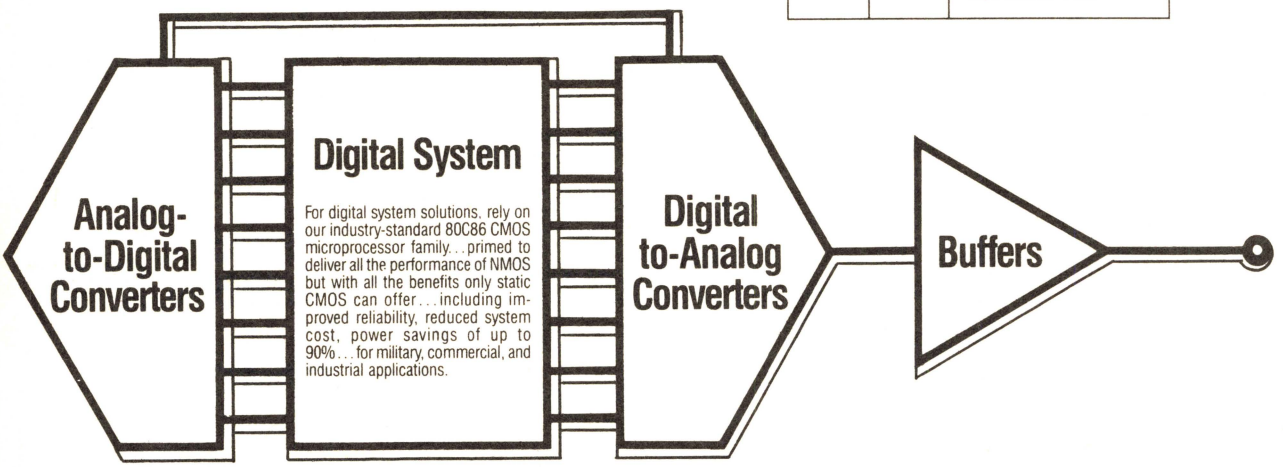
## Analog-to-Digital Converters

| Resolution (bits) | Part Number | Features |
|---|---|---|
| 12 | HI-574A | • DESC 8512704XC<br>• Complete A/D Converter with Clock and Reference<br>• μP Compatible<br>• ±12 V to ±15 V Operation<br>• Typical Conversion Time: 20 μs<br>• Bus Access Time: 150 ns<br>• Superior Alternate Source for AD574A |
| 12 | HI-674A | • Typical Conversion Time: 12 μs<br>• Same pinouts and operating characteristics as HI-574A |
| 12 | HI-774A | • Typical Conversion Time: 8 μs<br>• Same pinouts and operating characteristics as HI-574A and HI-674A<br>• Digital Error Correction |

## Buffers

| Classification | Part Number | Features |
|---|---|---|
| Current Buffers | HA-5002 | • Voltage Gain: 0.995V/V<br>• Output Current: ±100 mA<br>• High Slew Rate: 1300 V/μs<br>• Full Power Bandwidth: DC to 80 MHz<br>• Low Supply Current: 8.3 mA |
| | HA-5033 | • Output Current: ±100 mA<br>• Differential Gain (Phase): 0.1% (0.1°)<br>• High Slew Rate: 1000 V/μs<br>• Wide Power bandwidth: DC to 80 MHz<br>• Fast Rise Time: 3 ns |
| High-Voltage Operational Amplifier | HA-2640 | • Output Voltage Swing: ±35 V<br>• Supply Voltage: ±10 to ±40 V<br>• Bandwidth: 4 MHz<br>• Slew Rate: 5 V/μs<br>• Common Mode Input Voltage Swing: ±35 V<br>• Output Overload Protection |




## CMOS Analog Multiplexers

| Classification | Number of Channels | Part Number | Typical Specifications (@ 25°C) Max Input Voltage | Typical Specifications (@ 25°C) $R_{ON}$ (ohms) | Military Part Number |
|---|---|---|---|---|---|
| Industry Standard | 16 Single-ended | HI-506 | | 180 | JAN 19001BXC |
| | 8 Differential | HI-507 | | 180 | JAN 19003BXC |
| | 8 Single-ended | HI-508 | | 180 | JAN 19007BEC |
| | 4 Differential | HI-509 | 30 V p-p | 180 | JAN 19008BEC |
| | 8 Single-ended, Low-power | HI-1818A | | 250 | |
| | 4 Differential Low-power | HI-1828A | | 250 | |
| Overvoltage Protected | 16 Single-ended | HI-546 | | 1.2K | JAN 19002BXC DESC 8513101XA, in LCC, 85131013A |
| | 8 Differential | HI-547 | 70 V p-p | 1.2K | JAN 19004BXC DESC 8513102XA, in LCC, 85131023A |
| | 8 Single-ended | HI-548 | | 1.2K | JAN 19005BEC DESC 77050202EA, in LCC, 770502022A |
| | 4 Differential | HI-549 | | 1.2K | JAN 19006BEC DESC 8513103EA, in LCC, 85131032A |
| High Speed, Mode Programmable | 16/Dual 8 100 ns | HI-516 | 30 V p-p | 620 | |
| | 8/Dual 4 80 ns | HI-518 | | 480 | |
| Video, Wideband L[illegible]vel | 4 Channel, 10 MHz | HI-524 | 30 V p-p | 700 | |
| | 4 Differential | HI-539 | | 4 (typ. $R_{ON}$) | |

## Digital-to-Analog Converters

| Classification | Resolution (bits) | Part Number | Output: Current | Output: Voltage | Settling Time (To ½ LSB @ 25°C) Typical |
|---|---|---|---|---|---|
| High Resolution, High Speed | 16 | HI-DAC16 | ✓ | | 1.0 μs to 0.003% |
| | 12 | HI-562A | ✓ | | 300 ns |
| | 12 | HI-5660 | ✓ | | 250 ns |
| (Includes Ref.) | 12 | HI-565A | ✓ | | 350 ns |
| (Includes Ref.) | 12 | HI-5680I | ✓ | | 300 ns |
| (Includes Ref.) | 12 | HI-5680V | | ✓ | 1.5 μs |
| (Includes Ref.) | 12 | HI-5685I | ✓ | | 300 ns |
| (Includes Ref.) | 12 | HI-5685V | | ✓ | 1.5 μs |
| (Includes Ref.) | 12 | HI-5687I | ✓ | | 300 ns |
| (Includes Ref.) | 12 | HI-5687V | | ✓ | 1.5 μs |
| (Includes Ref.) | 12 | HI-5690V | | ✓ | 750 ns |
| (Includes Ref.) | 12 | HI-5695V | | ✓ | 750 ns |
| (Includes Ref.) | 12 | HI-5697V | | ✓ | 750 ns |

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# HI-546/547

## Single 16/Differential 8 Channel CMOS Analog Multiplexer with Active Overvoltage Protection

### Features

- Analog Overvoltage Protection . . . . . 70 Vpp
- No Channel Interaction During Overvoltage
- ESD Resistant . . . . . > 4,000 Volts
- Guaranteed $R_{ON}$ Matching
- 44 V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range . . . . . ±15 V
- Access Time (Typical) . . . . . 500 ns
- Standby Power (Typical) . . . . . 7.5 mW

### Applications

- Data Acquisition
- Industrial Controls
- Telemetry

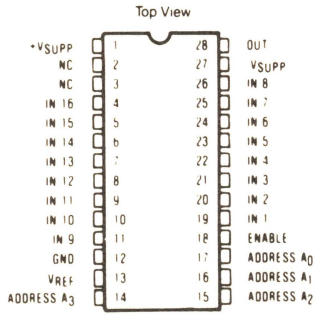
### Description

The HI-546 and HI-547 are analog multiplexers with Active Overvoltage Protection and guaranteed $R_{ON}$ matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-546 and HI-547 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The 546 is a 16 channel device and the 547 is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

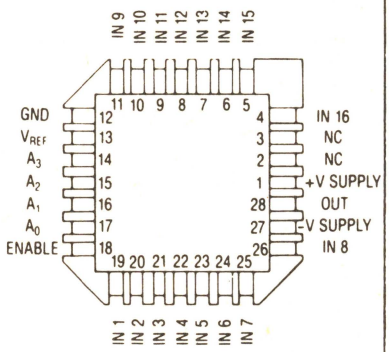
The HI-546/547 are offered in both commercial and military grades. Additional Hi-Rel screening to MIL-STD-883 available, specified by the "/883" suffix. For details, see the separate "883" data sheet.

Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC or 20 pin plastic LCC (PLCC) package.

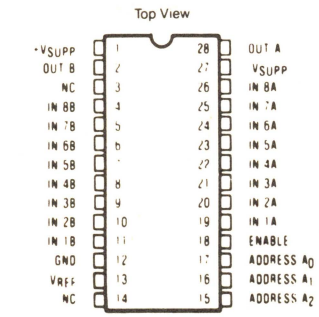
### Pinouts



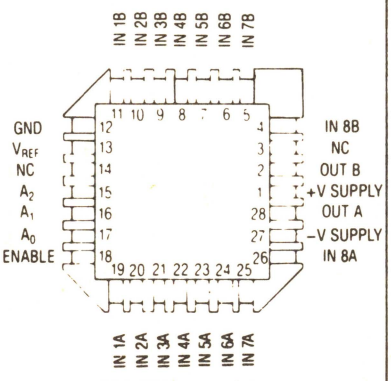

**HI1-546 (ceramic)**
**HI3-546 (plastic)**




**HI4-546 (ceramic)**
**HI4P546 (plastic)**

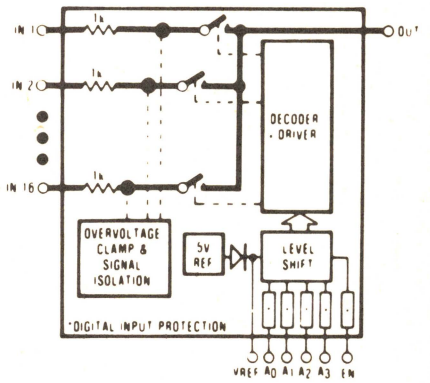



**HI1-547 (ceramic)**
**HI3-547 (plastic)**

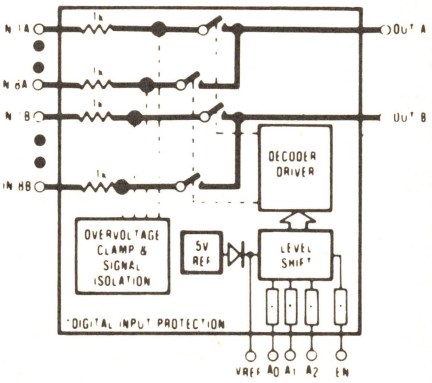



**HI4-547 (ceramic)**
**HI4P547 (plastic)**

### Functional Diagrams




**HI-546**




**HI-547**

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# HI-548/549

## Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

### Features

- Analog Overvoltage Protection . . . . . 70 Vpp
- No Channel Interaction During Overvoltage
- ESD Resistant . . . . . >4,000 Volts
- Guaranteed $R_{ON}$ Matching
- 44 V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range . . . . . ±15 V
- Access Time (Typical) . . . . . 500 ns
- Standby Power (Typical) . . . . . 7.5 mW

### Applications

- Data Acquisition
- Industrial Controls
- Telemetry

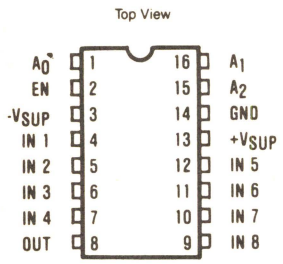
### Description

The HI-548 and 549 are analog multiplexers with Active Overvoltage Protection and guaranteed $R_{ON}$ matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The 548 is an 8 channel device and the 549 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

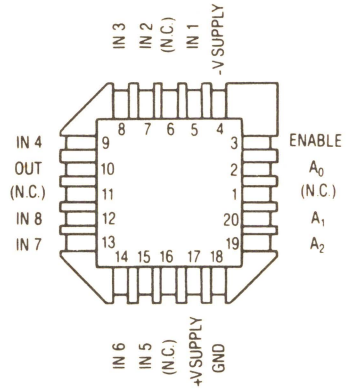
The HI-548/549 are offered in both commercial and military grades. Addition Hi-Rel screening to MIL-STD-883 available, specified by the "/883" suffix. For details, see the separate "883" data sheet.

Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC or 20 pin plastic LCC (PLCC) package.

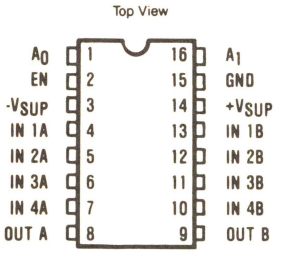
### Pinouts



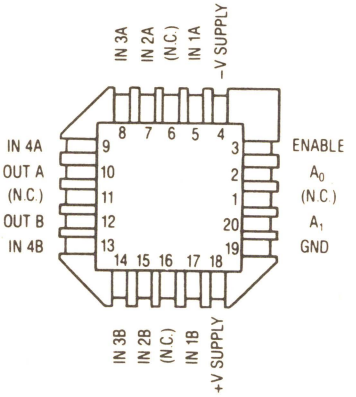

HI1-548 (ceramic)
HI3-548 (plastic)




HI4-548 (ceramic)
HI4P548 (plastic)

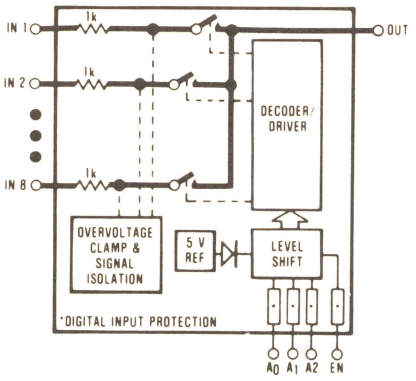



HI1-549 (ceramic)
HI3-549 (plastic)

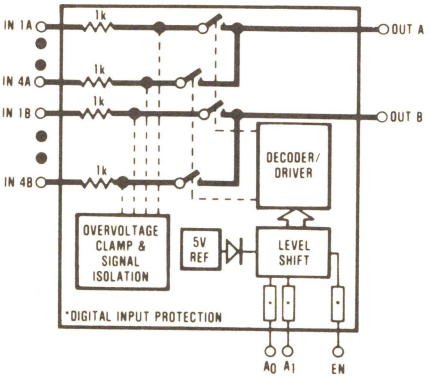



HI4-549 (ceramic)
HI4P549 (plastic)

### Functional Diagrams




HI-548




HI-549

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# HI-5690V/95V/97V

## High Speed, 12-Bit Low Cost Monolithic Digital-to-Analog Converter

April 1987

### Features

- Voltage Output with Fast Settling ..... 750ns
  High Slew Rate ..... 50V/$\mu$s
- Industry Standard Pinout - AD-DAC 80 & HI-5680 Compatible
- Two-Supply Operation ..... 11.4V to 16.5V
  -11.4V to -16.5V
- Low Noise Voltage Reference
  1/F (0.1Hz to 10Hz) ..... 15$\mu$Vp-p
- Guaranteed Monotonic Over Full Temperature Range
- Application Resistors On-Chip
- Complementary Binary Input Code
- Voltage Output
- Complete Family of Temperature Grades

### Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

### Description

The HI-5690V series of complete 12 bit digital to analog converters includes a low noise, low temperature coefficient buried zener reference and a fast settling output amplifier. The series consists of the HI-5690V, -5695V and -5697V, for the commercial, industrial and military temperature ranges. Monolithic (single chip) construction along with several design innovations make these converters an optimum choice for high speed, high reliability applications.

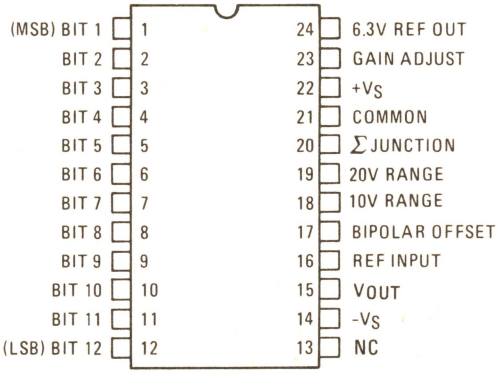
The Harris unique Dielectric Isolation (DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. Wafer-level laser trimming of span resistors and bit current cells ensures high accuracy and exceptional tracking over temperature.

Internally, the HI-5690V series eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents, allowing virtually zero variation in current through the package common, thus minimizing analog ground noise seen by the converter.

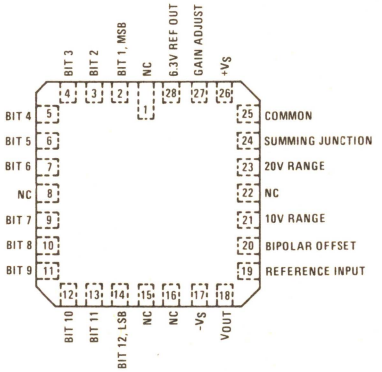
The HI-5690V series operates from two supplies $\pm V_S$ in the range of $\pm$11.4 Volts to $\pm$16.5 volts. It is pin compatible with the AD-DAC 80 series and HI-5680 series, and since Pin 13 is not internally connected (Logic supply on standard 5680's) this device is compatible in applications with or without +5 Volts applied to Pin 13. The converter performance is guaranteed over the full power supply operating range, but not all output ranges are available with low supply voltages. Hi-Rel screening including a 160 hour burn-in, may be specified by adding the suffix -8. The package is a 24 pin side-brazed, ceramic DIP and a 28 pin Leadless Chip Carrier. For Mil-Std-883 compliant parts, request the HI-5697V/883 data sheet.

### Pinouts

**DIP**
TOP VIEW




**LCC**
TOP VIEW

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# HA-2420/25

June 1987

## Fast Sample and Hold

### Features

- Maximum Acquisition Time (10V Step to 0.1%) .....4μs
  (10V Step to 0.01%).....6μs
- Low Droop Rate ($C_H$ = 1000pF).....5μV/ms
- Bandwidth .....2.5MHz
- Low Effective Aperture Delay Time .....30ns
- TTL Compatible Control Input
- ±12V to ±15V Operation

### Applications

- 12-Bit Data Acquisition
- D to A Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Op Amp

### Description

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

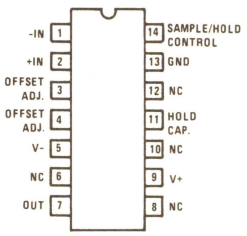
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note number 517.

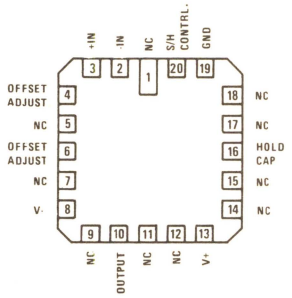
The HA-2420/25 is offered in a 14 pin ceramic or plastic dip, and a 20 pin ceramic leadless chip carrier or 20 pin plastic leaded chip carrier. For MIL-STD-883 compliant parts, request the HA-2420/883 data sheet.

### Pinouts

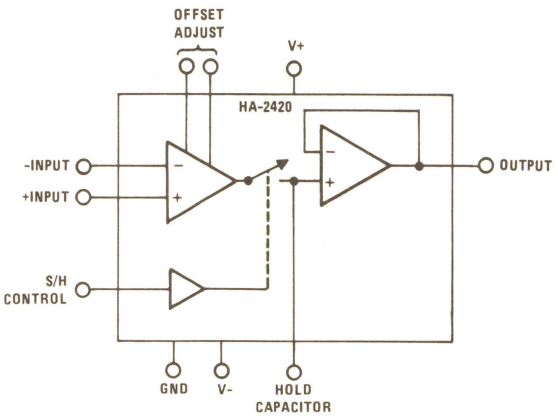
**CERAMIC/PLASTIC DIP**
TOP VIEW




**LCC/PLCC**
TOP VIEW




### Functional Diagram

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# HA-5330

## Very High Speed Precision Monolithic Sample and Hold

July 1987

### Features

- Very Fast Acquisition.....350ns (0.1%)
  500ns (0.01%)
- Low Droop Rate .....0.01$\mu$V/$\mu$s
- Very Low Offset.....0.2mV
- High Slew Rate.....90V/$\mu$s
- Wide Supply Range..... $\pm$11V to $\pm$18V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

### Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

### Description

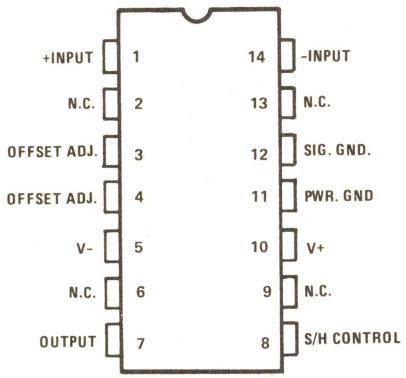
The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 500ns acquisition time to 12-bit accuracy and a droop rate of 0.01$\mu$V/$\mu$s. The circuit consists of an input transconductance amplifier capable of producting large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of $V_{IN}$. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

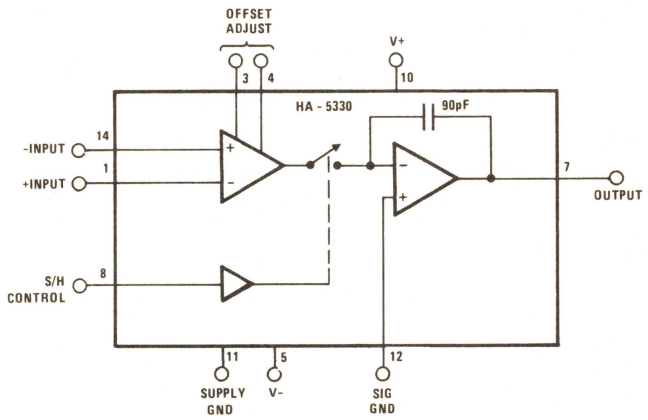
The HA-5330 will operate at reduced supply voltages (to $\pm$11V) with a reduced signal range. This monolithic device is available in a ceramic 14-pin DIP. The MIL-STD-883 data sheet for this device is available on request.

### Pinout

TOP VIEW




### Functional Diagram

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# HI-574A

## Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

January 1987

### Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 25$\mu$s Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle ($A_0$ Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Improved Second Source for AD574A and HS574
- $\pm$12V to $\pm$15V Operation

### Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

### Description

The HI-574A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

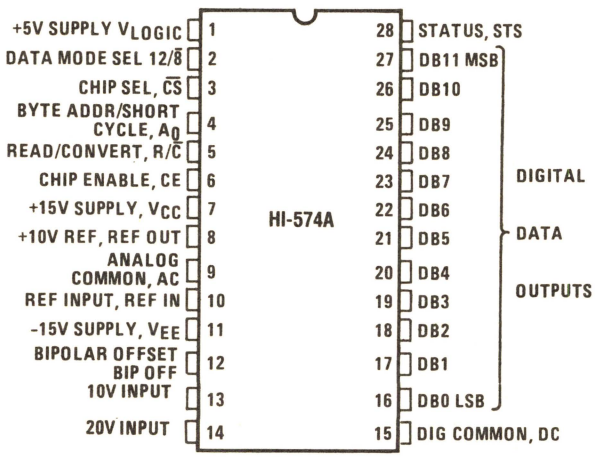
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 $\pm$ 1$\mu$s.

The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and $\pm$12V to $\pm$15V, with typical dissipation of 385mW at $\pm$12V. Three electrical grades each are offered for 0°C to +75°C and -55°C to +125°C temperature ranges. All models are available in a 28 pin Sidebrazed DIP. For MIL-STD-883 compliant parts, request the HI-574A/883 data sheet.

### Pinouts

SIDEBRAZE DIP
TOP VIEW

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# HI-674A

## 12μs, Complete 12-Bit A/D Converter with Microprocessor Interface

January 1987

### Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 15μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle ($A_0$ Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A
- Same Pinout as the HI-574A
- ±12V to ±15V Operation

### Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

### Description

The HI-674A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

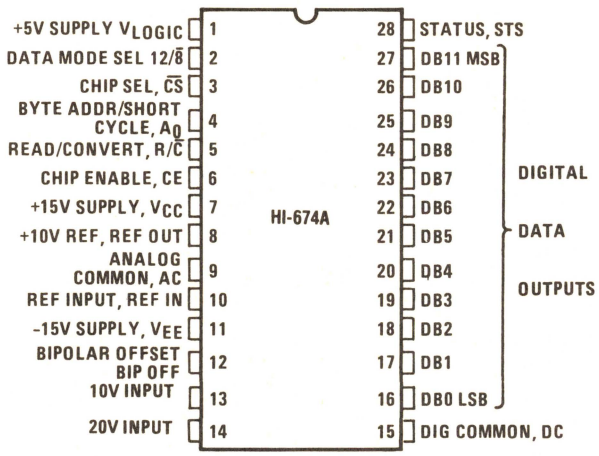
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12 ± 1μs.

The HI-674A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. Three electrical grades each are offered for 0°C to +75°C and -55°C to +125°C temperature ranges. All models are available in a 28 pin Sidebrazed DIP. For MIL-STD-883 compliant parts, request the HI-674A/883 data sheet.

### Pinout

CERAMIC DIP
TOP VIEW

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# HI-774A

ADVANCED

## 7μs, Complete 12-Bit A/D Converter With Microprocessor Interface

### Features

- Complete 12 Bit A/D Converter With Reference and Clock
- Digital Error Correction
- Full 8-, 12-, or 16-Bit Microprocessor Bus Interface
- 150 nS Buss Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time For Control Signals
- 8μs Maximum Conversion Time Over Temperature
- Low Noise, Via Current-mode signal transmission between chips
- Byte enable/short cycle (Ao Input)
- ▸ Guarantees break-before-make action, eliminating bus contention during read operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A and HI-674A
- Same Pin-Out as HI-574A and HI-674A
- ±12V to ±15V Operation

### Applications

- Military and Industrial Data Acquisition Systems
- Electronics Test and Scientific Instrumentation
- Process Control Systems

### Description

The HI-774A is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, whch provides enhanced AC performance and freedom from latch-up. The digital die features the smart SAR (SSAR™), which includes a digital error correction circuit.

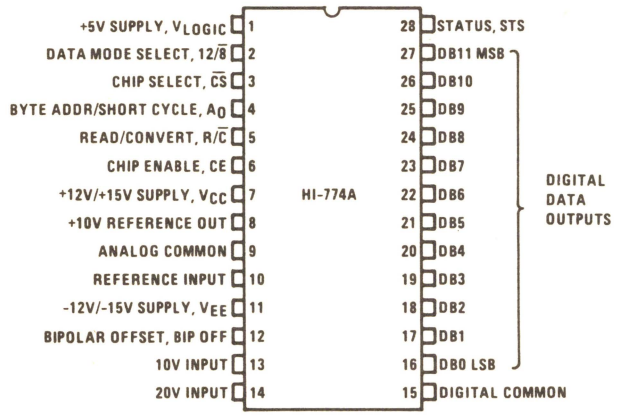
Custom design of each IC (bipolar and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature. The oscillator is trimmed for a guaranteed conversion time of 7 ± 1μs over temperature.

The HI-774A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 390mW at ±12V. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin side-brazed, ceramic DIP. For information on MIL-STD-883 compliant device's request the HI-774A/883 data sheet.

### Pinout

TOP VIEW

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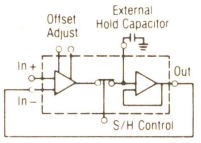
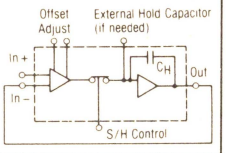
## Analog Switches

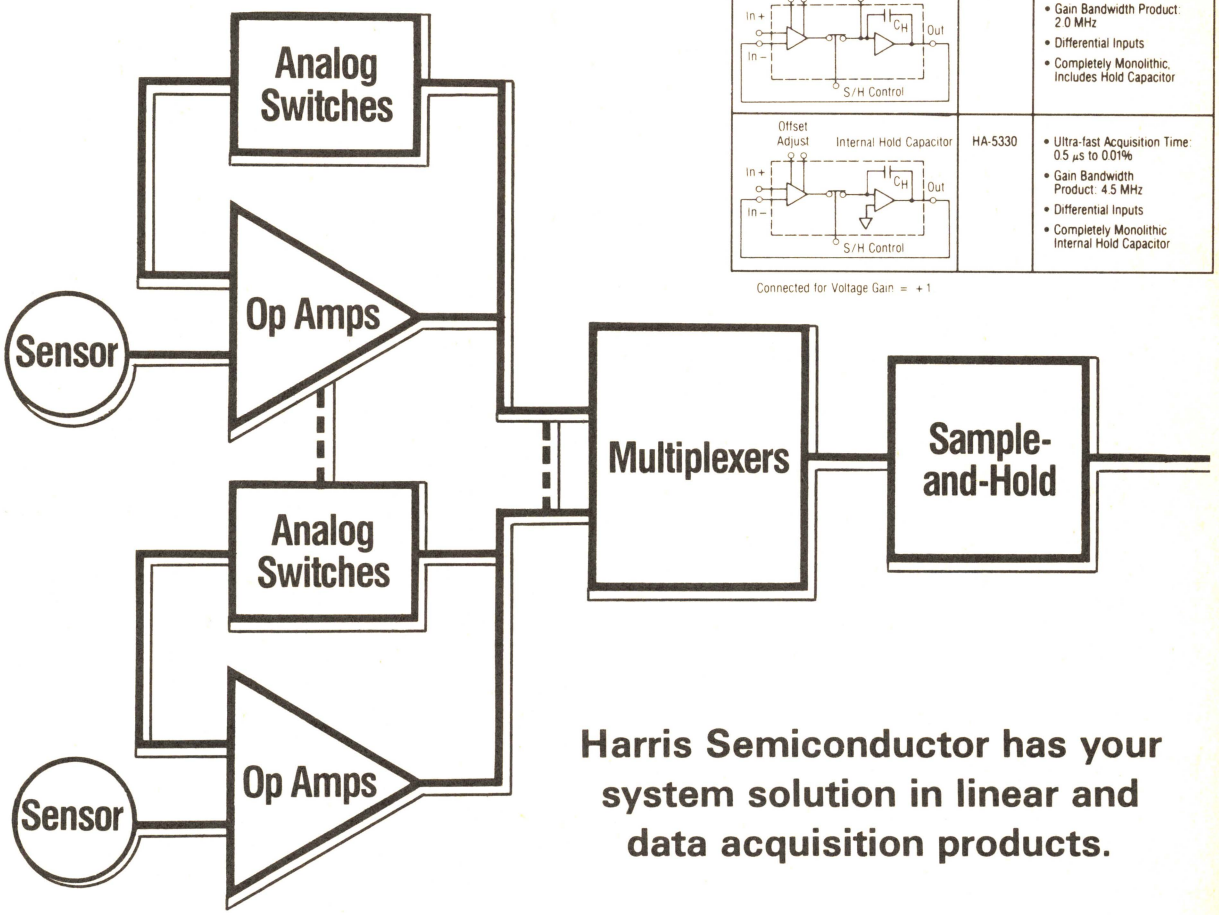
| Functions | General Purpose | Low $R_{ON}$ | Low Leakage (0.04 nA) | High Speed |
|---|---|---|---|---|
| SPST | — | HI-5040 (50Ω) | — | — |
| 2X SPST | HI-200 | HI-5041 (50Ω)<br>HI-5048 (25Ω) | HI-300 (TTL compatible)<br>HI-304 (CMOS compatible)<br>HI-381 (TTL compatible) | |
| 4X SPST | HI-201 | — | — | HI-201HS (30 ns) |
| SPDT | — | HI-5042 (50Ω)<br>HI-5050 (25Ω) | HI-301 (TTL compatible)<br>HI-305 (CMOS compatible)<br>HI-387 (TTL compatible) | |

| Functions | General Purpose | Low $R_{ON}$ | Low Leakage (0.04 nA) |
|---|---|---|---|
| 2X SPDT | — | HI-5043 (50Ω)<br>HI-5051 (25Ω) | HI-303 (TTL compatible)<br>HI-307 (CMOS compatible)<br>HI-390 (TTL compatible) |
| DPST | — | HI-5044 (50Ω) | — |
| 2X DPST | — | HI-5045 (50Ω)<br>HI-5049 (25Ω) | HI-302 (TTL compatible)<br>HI-306 (CMOS compatible)<br>HI-384 (TTL compatible) |
| DPDT | — | HI-5046 (50Ω)<br>HI-5046A (25Ω) | — |
| 4PST | — | HI-5047 (50Ω)<br>HI-5047A (25Ω) | — |

## Sample-and-Hold Amplifiers

| Configuration | Part Number | Features |
|---|---|---|
|  | HA-2420<br>HA-2425 | • DESC 80016CX<br>• Fast Acquisition Time: 3.2 μs to 0.01%<br>• Gain Bandwidth Product: 2.5 MHz<br>• Low Droop Rate: 5 μV/ms<br>• Differential Inputs<br>• Monolithic Construction |
|  | HA-5320 | • Ultra-fast Acquisition Time: 1μs to 0.01%<br>• Gain Bandwidth Product: 2.0 MHz<br>• Differential Inputs<br>• Completely Monolithic, Includes Hold Capacitor |
|  | HA-5330 | • Ultra-fast Acquisition Time: 0.5 μs to 0.01%<br>• Gain Bandwidth Product: 4.5 MHz<br>• Differential Inputs<br>• Completely Monolithic, Internal Hold Capacitor |

Connected for Voltage Gain = +1

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## Operational Amplifiers

| High Speed | | Precision | | Low Power | | General Purpose | | High Speed | Low Power Fixed Supply Current | | General Purpose | Precision |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bipolar | J-FET | Bipolar Programmable | Bipolar Fixed Supply Current | | | | | | | |
| **HA-2620:** 100 MHz<br>35 V/μs | **HA-2542:** 60 MHz<br>375 V/μs | **HA-5130:**<br>10μV $V_{IO}$<br>0.4 μV/°C | **HA-5147:**<br>3 nV/√Hz<br>10μV $V_{IO}$<br>35 V/μs<br>120 MHz | **HA-2720:**<br>±1.2 V/±18 V<br>15 μA | **HA-5141:**<br>Single Supply<br>+2V/+40 V<br>45 μA | **HA-2600:**<br>12 MHz<br>7 V/μs<br>3 mV $V_{IO}$ | Duals | **HA-5112:** 60 MHz<br>20 V/μs<br>Low Noise | **HA-5142:**<br>Single Supply<br>+2 V/+40 V<br>45 μA<br>**HA-5152:**<br>200 μA<br>4.5 V/μs<br>1.3 MHz | | **HA-5102:**<br>8 MHz<br>3 V/μs<br>Low Noise | |
| **HA-2520:** 20 MHz<br>120 V/μs<br>200 ns | | **HA-5127:**<br>3 nV/√Hz<br>10 μV $V_{IO}$<br>10 V/μs | | | | **HA-5101:**<br>10 MHz<br>10 V/μs<br>Low Noise<br>3.3 nV/√Hz | | **HA-5114:** 60 MHz<br>20 V/μs<br>Low Noise<br>**HA-2400 (PRAM):**<br>40 MHz<br>30 V/μs<br>4 channel<br>Addressable | **HA-5144:**<br>Single Supply<br>+2 V/+40 V<br>45 μA<br>**HA-5154:**<br>200 μA<br>4.5 V/μs<br>1.3 MHz | | **HA-4741:**<br>3.5 MHz<br>1.6 V/μs<br>1 mV $V_{IO}$<br>Low Noise<br>**HA-5104:**<br>8 MHz<br>3 V/μs<br>Low Noise | **HA-5134:**<br>4 MHz<br>1 V/μs<br>50 μV $V_{IO}$<br>Low Noise |
| **HA-5160:** 120 MHz<br>120 V/μs<br>J-FET | **HA-5147:** 120 MHz<br>35 V/μs<br>3 nV/√Hz | **HA-5137:**<br>3 nV/√Hz<br>10 μV $V_{IO}$<br>20 V/μs | | | | **HA-5111:**<br>100 MHz<br>50 V/μs<br>Low Noise<br>3.3 nV/√Hz | Quads | | | | | |
| **HA-5190:** 150 MHz<br>200 V/μs<br>70 ns | **HA-2544:** 33 MHz<br>10 μV $V_{IO}$<br>@$A_{CL}$ = 1<br>150 V/μs S.R.<br>$I_{CC}$ = 10 mA | | | | | | | | | | | |
| **HA-2540:** 400 MHz<br>400 V/μs | | | | | | | | | | | | |
| **HA-2539:** 600 MHz<br>600 V/μs | **HA-2529:** 20 MHz<br>160 V/μs<br>200 ns<br>30 mA $I_{out}$ | | | | | | | | | | | |
| **HA-2541:** 40 MHz<br>@$A_{CL}$ = 1<br>280 V/μs<br>90 ns | | | | | | | | | | | | |

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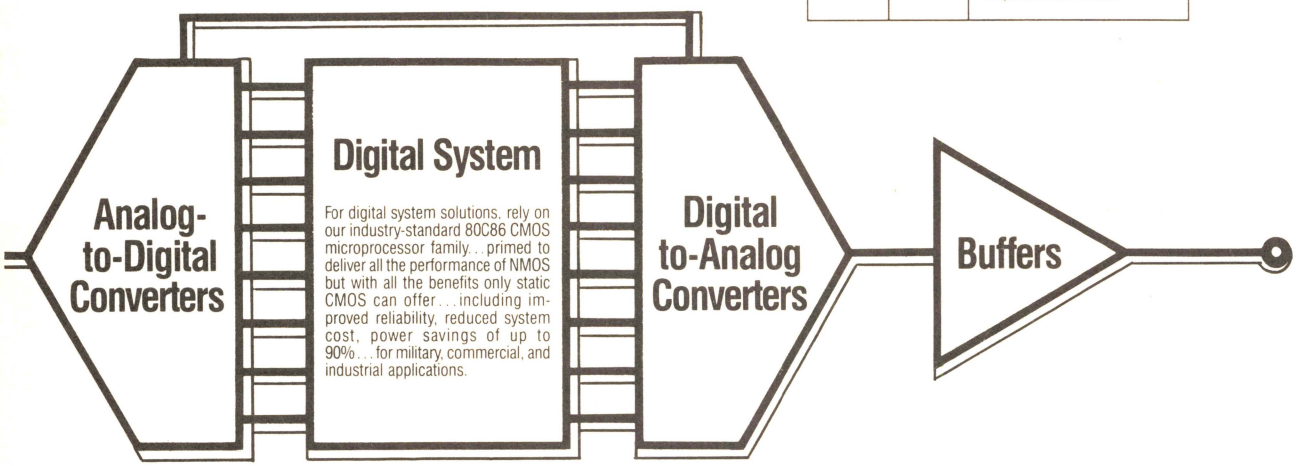
## Analog-to-Digital Converters

| Resolution (bits) | Part Number | Features |
|---|---|---|
| 12 | HI-574A | • DESC 8512704XC<br>• Complete A/D Converter with Clock and Reference<br>• µP Compatible<br>• ±12 V to ±15 V Operation<br>• Typical Conversion Time: 20 µs<br>• Bus Access Time: 150 ns<br>• Superior Alternate Source for AD574A |
| 12 | HI-674A | • Typical Conversion Time: 12 µs<br>• Same pinouts and operating characteristics as HI-574A |
| 12 | HI-774A | • Typical Conversion Time: 8 µs<br>• Same pinouts and operating characteristics as HI-574A and HI-674A<br>• Digital Error Correction |

## Buffers

| Classification | Part Number | Features |
|---|---|---|
| Current Buffers | HA-5002 | • Voltage Gain: 0.995V/V<br>• Output Current: ±100 mA<br>• High Slew Rate: 1300 V/µs<br>• Full Power Bandwidth: DC to 80 MHz<br>• Low Supply Current: 8.3 mA |
| | HA-5033 | • Output Current: ±100 mA<br>• Differential Gain (Phase): 0.1% (0.1°)<br>• High Slew Rate: 1000 V/µs<br>• Wide Power bandwidth: DC to 80 MHz<br>• Fast Rise Time: 3 ns |
| High-Voltage Operational Amplifier | HA-2640 | • Output Voltage Swing: ±35 V<br>• Supply Voltage: ±10 to ±40 V<br>• Bandwidth: 4 MHz<br>• Slew Rate: 5 V/µs<br>• Common Mode Input Voltage Swing: ±35 V<br>• Output Overload Protection |

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## CMOS Analog Multiplexers

| Classification | Number of Channels | Part Number | Typical Specifications (@ 25°C) Max Input Voltage | Typical Specifications (@ 25°C) $R_{ON}$ (ohms) | Military Part Number |
|---|---|---|---|---|---|
| Industry Standard | 16 Single-ended | HI-506 | | 180 | JAN 19001BXC |
| | 8 Differential | HI-507 | | 180 | JAN 19003BXC |
| | 8 Single-ended | HI-508 | | 180 | JAN 19007BEC |
| | 4 Differential | HI-509 | 30 V p-p | 180 | JAN 19008BEC |
| | 8 Single-ended, Low-power | HI-1818A | | 250 | |
| | 4 Differential Low-power | HI-1828A | | 250 | |
| Overvoltage Protected | 16 Single-ended | HI-546 | | 1.2K | JAN 19002BXC DESC 8513101XA, in LCC, 85131013A |
| | 8 Differential | HI-547 | 70 V p-p | 1.2K | JAN 19004BXC DESC 8513102XA, in LCC, 85131023A |
| | 8 Single-ended | HI-548 | | 1.2K | JAN 19005BEC DESC 77050202EA, in LCC, 770502022A |
| | 4 Differential | HI-549 | | 1.2K | JAN 19006BEC DESC 8513103EA, in LCC, 85131032A |
| High Speed, Mode Programmable | 16/Dual 8 100 ns | HI-516 | 30 V p-p | 620 | |
| | 8/Dual 4 80 ns | HI-518 | | 480 | |
| Video, Wideband Low Level | 4 Channel, 10 MHz | HI-524 | 30 V p-p | 700 | |
| | 4 Differential | HI-539 | | 4 (...$R_{ON}$) | |

## Digital-to-Analog Converters

| Classification | Resolution (bits) | Part Number | Output: Current | Output: Voltage | Settling Time (To ½ LSB @ 25°C) Typical |
|---|---|---|---|---|---|
| High Resolution, High Speed | 16 | HI-DAC16 | ✓ | | 1.0 µs to 0.003% |
| | 12 | HI-562A | ✓ | | 300 ns |
| | 12 | HI-5660 | ✓ | | 250 ns |
| (Includes Ref.) | 12 | HI-565A | ✓ | | 350 ns |
| (Includes Ref.) | 12 | HI-5680I | ✓ | | 300 ns |
| (Includes Ref.) | 12 | HI-5680V | | ✓ | 1.5 µs |
| (Includes Ref.) | 12 | HI-5685I | ✓ | | 300 ns |
| (Includes Ref.) | 12 | HI-5685V | | ✓ | 1.5 µs |
| (Includes Ref.) | 12 | HI-5687I | ✓ | | 300 ns |
| (Includes Ref.) | 12 | HI-5687V | | ✓ | 1.5 µs |
| (Includes Ref.) | 12 | HI-5690V | | ✓ | 750 ns |
| (Includes Ref.) | 12 | HI-5695V | | ✓ | 750 ns |
| (Includes Ref.) | 12 | HI-5697V | | ✓ | 750 ns |


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# HA-5033

June 1986

## Video Buffer

### FEATURES

- DIFFERENTIAL PHASE ERROR 0.1°
- DIFFERENTIAL GAIN ERROR 0.1%
- HIGH SLEW RATE (±15V) 1300V/μs
- WIDE BANDWIDTH (SMALL SIGNAL) 250MHz
- WIDE POWER BANDWIDTH DC to 65MHz
- FAST RISE TIME 3ns
- HIGH OUTPUT DRIVE ±10V WITH 100Ω LOAD
- WIDE POWER SUPPLY RANGE ±5V TO ±16V
- REPLACE COSTLY HYBRIDS

### APPLICATIONS

- VIDEO BUFFER
- HIGH FREQUENCY BUFFER
- ISOLATION BUFFER
- HIGH SPEED LINE DRIVER
- IMPEDANCE MATCHING
- CURRENT BOOSTERS
- HIGH SPEED A/D INPUT BUFFERS

### DESCRIPTION

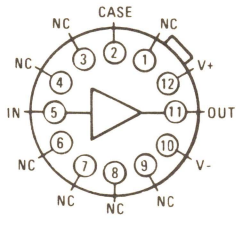
The HA-5033 is a unity gain monolithic I. C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outstanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/μs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce PNP transistors of lower frequency response, which results in a lower AC performance.

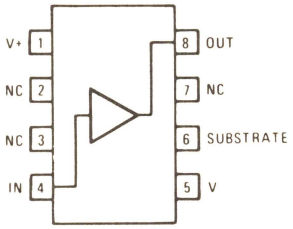
The HA-5033 is available in a 12 pin (TO-8) metal can or an 8 pin plastic mini-DIP. The HA-5033-2 is specified over temperature range of -55°C to +125°C. The HA-5033-5 is specified over temperature range of 0°C to +75°C.

### PINOUTS

TOP VIEWS

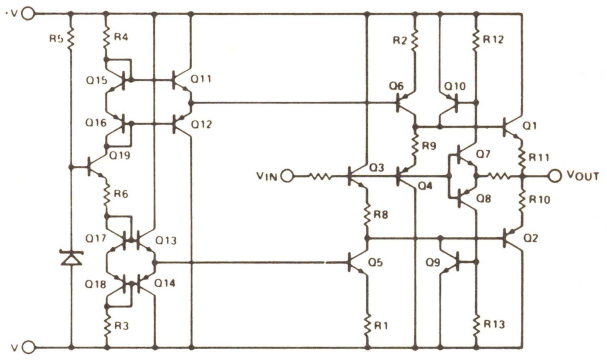



METAL CAN PACKAGE




MINI-DIP

### SCHEMATIC

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# HA-2542

## Wideband, High Slew Rate, High Output Current Operational Amplifier

September 1987

### Features

- Stable at Gains of 2 or Greater
- Gain Bandwidth.....70MHz
- High Slew Rate (Min.).....300V/$\mu$s
- High Output Current (Min.).....100mA
- Power Bandwidth (Typ.).....5.5MHz
- Output Voltage Swing (Min.).....$\pm$10V
- Monolithic Bipolar Dielectric Isolation Construction

### Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

### Description

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D. I. technology this amplifier offers 350V/$\mu$s slew rate, 70MHz gain bandwidth, and $\pm$100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

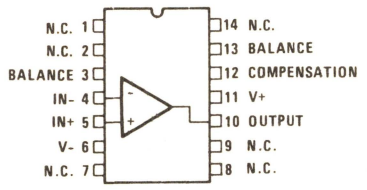
The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

The HA-2542 is available in ceramic or plastic 14 lead DIP packages, or a 12 lead metal can (TO-8) which is pin compatible with the HA-2541, HA-5190, LH0032 and HOS-050C. The HA-2542-2 is specified over the -55°C to +125°C temperature range and is also offered as a military part. The HA-2542-5 is specified over the commercial temperature range of 0°C to 75°C.

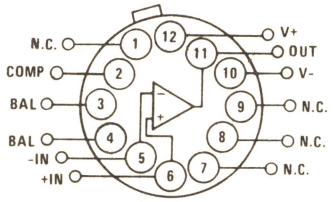
For more information on the HA-2542, please refer to Application Note 552 (Using The HA-2542), or Application Note 556 (Thermal Safe-Operating-Areas For High Current Op Amps).

### Pinouts

**HA1-2542 CERAMIC DIP**
**HA3-2542 PLASTIC DIP**
TOP VIEW

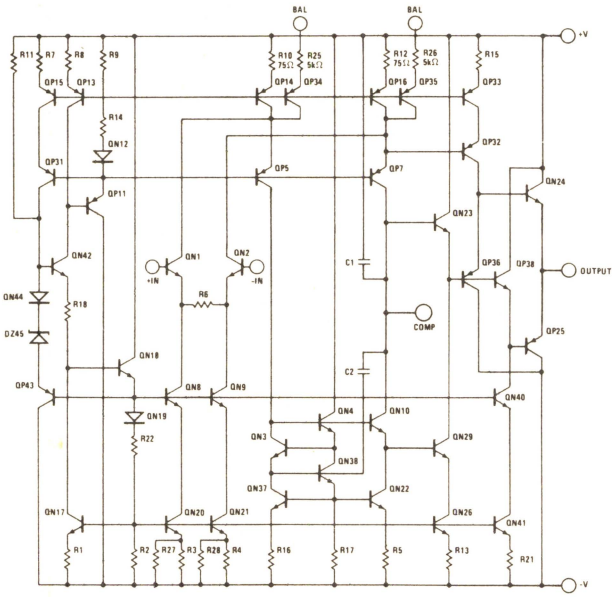



**HA2-2542 METAL CAN (TO-8)**
TOP VIEW




$V_{CASE}$ = V-

### Schematic

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# HA-2541

## Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

July 1987

### Features

- Unity Gain Bandwidth ..... 40MHz
- High Slew Rate ..... 250V/$\mu$s
- Low Offset Voltage ..... 0.8mV
- Fast Settling Time (0.1%) ..... 90ns
- Power Bandwidth ..... 4MHz
- Output Voltage Swing (Min) ..... $\pm$10V
- Unity Gain Stability
- Monolithic Bipolar Dielectric Isolation Construction

### Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

### Description

The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

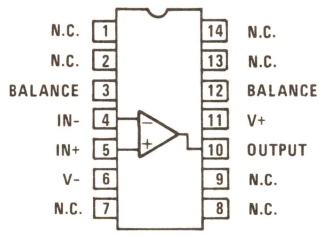
The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/$\mu$s slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with 90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

Packaged in a metal can (TO-8) or 14 pin ceramic DIP, the HA-2541 is pin compatible with the HA-2540 and HA-5190 op amps. The HA-2541-2 is specified over the temperature range of -55°C to +125°C. The HA-2541-5 is specified over the temperature range of 0°C to +75°C. For the military grade product, refer to the HA-2541 military data sheet.

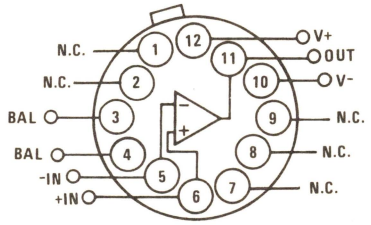
For further application suggestions on the HA-2541, please refer to Applicaton Note 550 (Using the HA-2541), and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers). Also see 'Applications' in this data sheet.

### Pinouts

**HA1-2541 CERAMIC DIP**
TOP VIEW

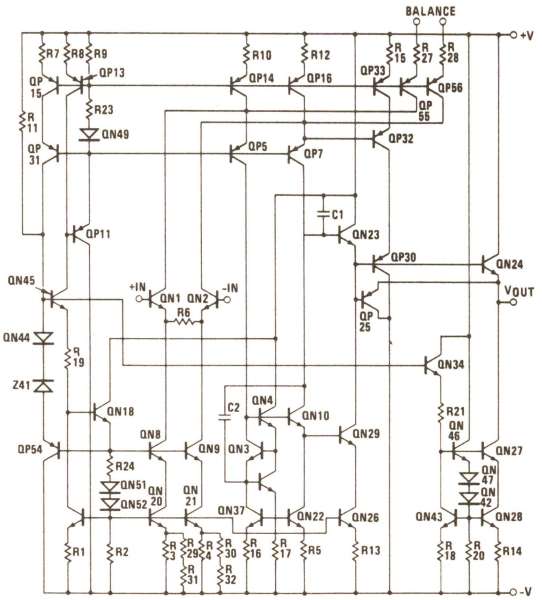



**HA2-2541 METAL CAN (TO-8)**
TOP VIEW




$V_{CASE}$ = V–

### Schematic

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# HA-2540

## Wideband, Fast Settling Operational Amplifier

May 1987

### Features

- Very High Slew Rate ..... 400V/$\mu$s
- Fast Settling Time ..... 200ns
- Wide Gain-Bandwidth ..... 400MHz
- Power Bandwidth ..... 6MHz
- Low Offset Voltage ..... 8mV
- Input Voltage Noise ..... 6nV/ Hz
- Output Voltage Swing ..... $\pm$10V
- Monolithic Bipolar Construction

### Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

### Description

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of $\pm$10V into a 1K$\Omega$ load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

A 400/$\mu$s slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 200ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

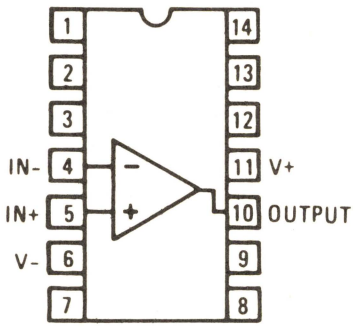
The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 is specified from 0°C to +75°C.

The HA-2540 is available in the 14 pin ceramic and epoxy DIP packages.

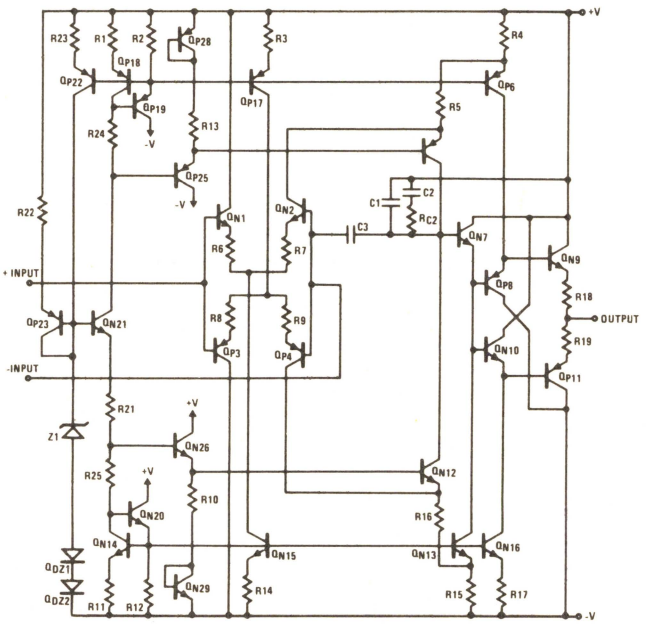
Refer to Application Note 541 for more information on High Speed Op-Amp applications. MIL-STD-883 data sheet is available on request.

### Pinout

CERAMIC/EPOXY DIP
TOP VIEW




### Schematic

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# HA-2539

## Very High Slew Rate Wideband Operational Amplifier

July 1987

### Features

- Very High Slew Rate ..... 600V/$\mu$s
- Open Loop Gain ..... 30kV/V
- Wide Gain-Bandwidth ($A_{VCL}$ = 10) ..... 600MHz
- Power Bandwidth ..... 9.5MHz
- Low Offset Voltage ..... 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... $\pm$10V
- Monolithic Bipolar Dielectric Isolation Construction

### Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

### Description

The Harris HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Harris High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/$\mu$s slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full $\pm$10V swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

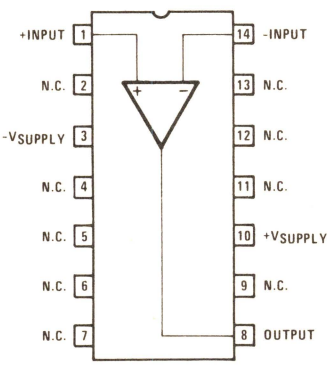
The HA-2539 is available in 14 pin ceramic and plastic DIP. The HA-2539-2 operates over -55°C to +125°C temperature range while the HA-2539-5 operates over the 0°C to +75°C range.

For further design assistance please refer to Application Note 541 (Using The HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers).

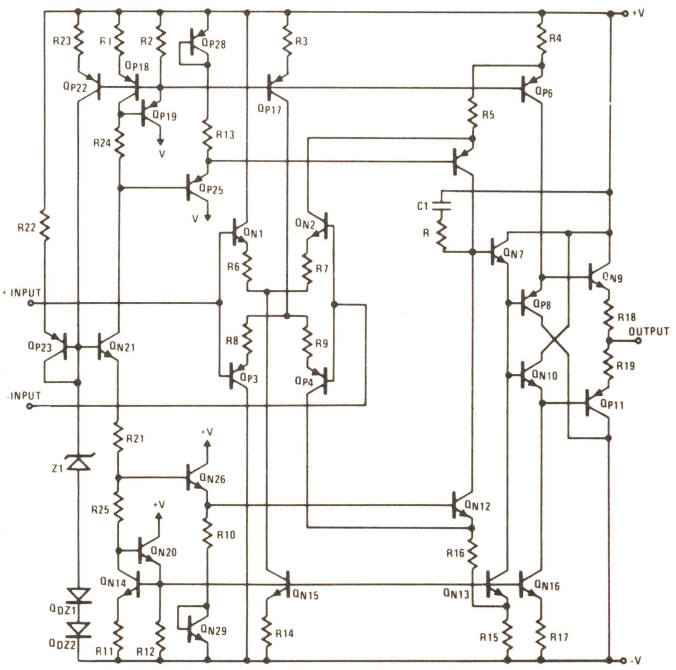
For the military grade products the HA-2539/883 data sheet is available upon request.

### Pinout

**HA1-2539 CERAMIC DIP**
**HA3-2539 PLASTIC DIP**
TOP VIEW




### Schematic

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# HA-2544

October 1987

## Video Operational Amplifier

### Features

- Unity Gain Bandwidth ..... 33MHz
- High Slew Rate ..... 150V/µs
- Low Supply Current ..... 10mA
- Differential Gain Error ..... <0.05dB
- Differential Phase Error ..... <0.1°
- Gain Tolerance at 5MHz ..... 0.1dB

### Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits
- Data Acquisition Systems

### Description

The HA-2544 is a Dielectrically Isolated, monolithic operational amplifier designed and constructed in the Harris High Frequency Process. It is another addition to the Harris series of high speed, wideband operational amplifiers and offers true video performance combined with the versatility of an operational amplifier.

The HA-2544 features 33MHz unity gain bandwidth and 150V/µs slew rate while offering video performance of <0.05dB differenital gain error, <0.1° differential phase error, and gain tolerance of just 0.1dB at 5MHz. These video parameters are tested and guaranteed at 5MHz. High performance and low power requirements are met with a supply current of only 10mA.

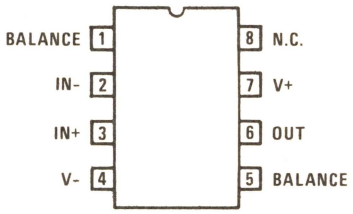
Uses of the HA-2544 range from video and video test equipment to radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 can also be used as a standard wideband, high speed, and fast settling operational amplifier in circuits such as pulse amplifiers and high speed data acquisition systems.

The HA-2544-2 is guaranteed over the military temperature range (-55°C to +125°C); the HA-2544-5/2544C-5 over the commercial temperature range (0°C to +75°C). The HA-2544 is available in TO-99 Metal Can, and both Plastic and Ceramic Mini-DIP packages. Military (/883) product and data sheets are available upon request.

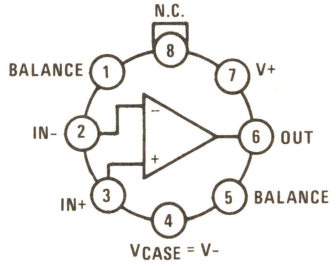
### Pinouts

TOP VIEWS

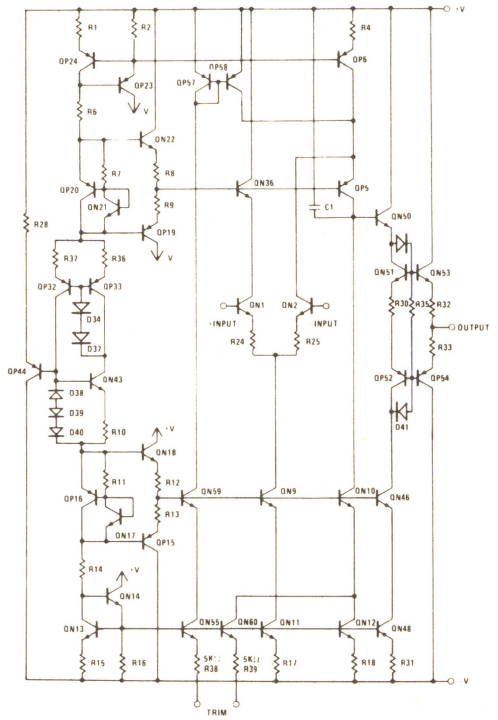
**HA1-2544 CERAMIC DIP**
**HA3-2544 PLASTIC DIP**




**HA2-2544 (TO-99) METAL CAN**




### Schematic



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# HA-5151/52/54

## Single/Dual/Quad Low Power Operational Amplifiers

August 1987

### Features

- Low Supply Current ..... < 200μA/Amplifier
- Dual Supply Voltage Range ..... ±1.5V to ±15V
- Single Supply Voltage Range ..... 3V to 30V
- High Slew Rate ..... 6V/μs
- Low $V_{OS}$ Drift ..... 3μV/°C
- Low Noise ..... 15nV/$\sqrt{Hz}$
- Dielectric Isolation

### Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Remote Sensor/Transmitter
- Battery Powered Equipment

### Description

The HA-5151/52/54 series is a group of dielectrically isolated bipolar amplifiers designed to provide excellent AC performance while drawing less than 200μA of supply current per amplifier. These unity gain stable amplifiers are especially well suited for portable and lightweight equipment where available power is limited.

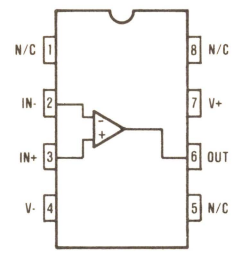
The HA-5151/52/54 series combines superior low power AC performance with DC precision not usually found in general purpose amplifiers. The DC performance is centered around low input offset voltage (0.5mV), low offset voltage drift (3μV/°C), and low input bias current (70nA). This is combined with a very low input noise voltage of 15nV/$\sqrt{Hz}$ at 1kHz.

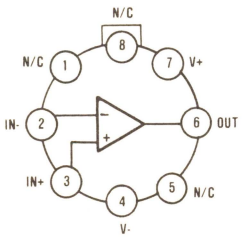
The AC performance of the HA-5151/52/54 series surpasses that of typical low power amplifiers with 6V/μs slew rate and a full power bandwidth of 95kHz. This makes the HA-5151/52/54 series an excellent choice for virtually all audio processing applications as well as remote sensor/transmitter designs requiring both low power and high speed. The suitability of the HA-5151/52/54 series for remote and low power operation is further enhanced by the wide range of supply voltages (±1.5V to ±15V) as well as single supply operation (3V to 30V).

These amplifiers are available in singles (HA-5151, Can or Mini-DIP), duals (HA-5152, Can or Mini-DIP) or quads (HA-5154, 14 pin DIP), as well as over both the commercial (0°C to +75°C) and military (-55°C to +125°C) temperature ranges. These amplifiers also carry industry standard pinouts which allow the HA-5151/52/54's to be interchangeable with most other operational amplifiers.

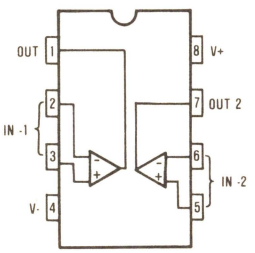
### Pinouts

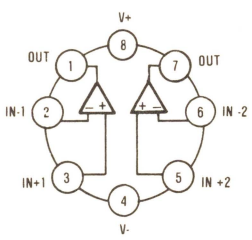
TOP VIEWS



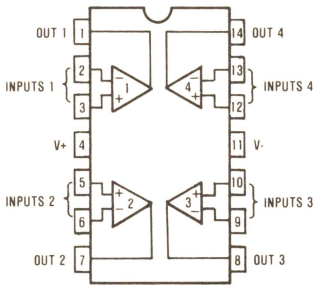




HA-5151




HA-5152




HA-5154

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# HA-5141/42/44

## Single/Dual/Quad Ultra-Low Power Operational Amplifiers

August 1987

### Features

- Low Supply Current ..... 45μA/Amp
- Wide Supply Voltage Range ..... Single 3V to 30V or Dual ±1.5V to ±15V
- High Slew Rate ..... 1.5V/μs
- High Gain ..... 100kV/V
- Unity Gain Stable
- Available in Singles, Duals and Quads

### Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation

### Description

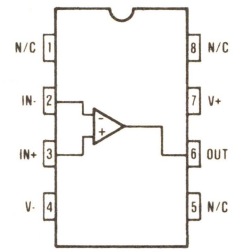
The HA-5141/42/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. These amplifiers are well suited to applications which require low power dissipation and good electrical characteristics.

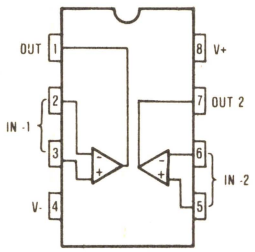
The HA-5141/42/44 provides accurate signal processing by virtue of their low input offset voltage (0.5mV), low input bias current (45nA), high open loop gain (100kV/V) and low noise, for low power operational amplifiers ($20nV/\sqrt{Hz}$). These characteristics coupled with a 1.5/μs slew rate and a 400kHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

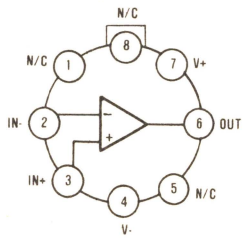
These amplifiers are available in singles (HA-5141, Can or Mini-DIP), duals (HA-5142, Can, Mini-DIP or 20 pin LCC) or quads (HA-5144, 14 pin DIP or 20 pin LCC) with industry standards pinouts which allow the HA-5141/5142/5144's to be interchangeable with most other operational amplifiers.

### Pinouts

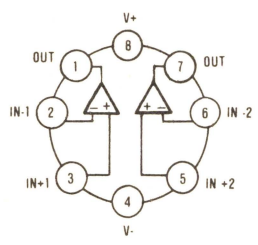
TOP VIEWS



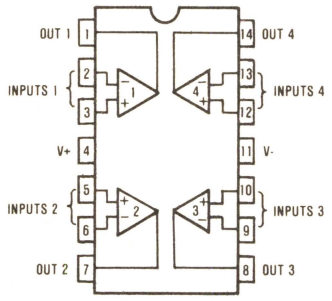




HA-5141




HA-5142




HA-5144

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# HA-5134

## Precision Quad Operational Amplifier

May 1987

### Features

- Low Offset Voltage.....Max 200$\mu$V
- Low Offset Voltage Drift..... Max 2$\mu$V/$^{o}$C
- Offset Voltage Match (5134A)... Full Temp. Max 250$\mu$V
- High Channel Separation.....120dB
- Low Noise ..... 7nV/$\sqrt{Hz}$
- Wide Bandwidth .....4MHz
- High CMRR/PSRR (Typ).....120dB
- Dielectric Isolation

### Applications

- Instrumentation Amplifiers
- State-Variable Filters
- Precision Integrators
- Threshold Detectors
- Precision Data Acquisition Systems
- Low-Level Transducer Amplifiers

### Description

The HA-5134 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741. Each amplifier features guaranteed maximum values for offset voltage of 200$\mu$V, offset voltage drift of 2$\mu$V/$^{o}$C, and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and $A_{VOL}$ is guaranteed above 750K V/V from -55$^{o}$C to +125$^{o}$C.

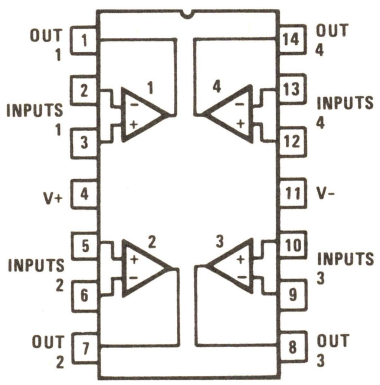
Precision performance of the HA-5134 is enhanced by a noise voltage density of 7nV/$\sqrt{Hz}$ at 1KHz, noise current density of 2pA/$\sqrt{Hz}$ at 1KHz and channel separation of 120dB. Each unity-gain stable quad amplifier is fabricated using the dielectric isolation process to assure performance in the most demanding applications.

The HA-5134 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

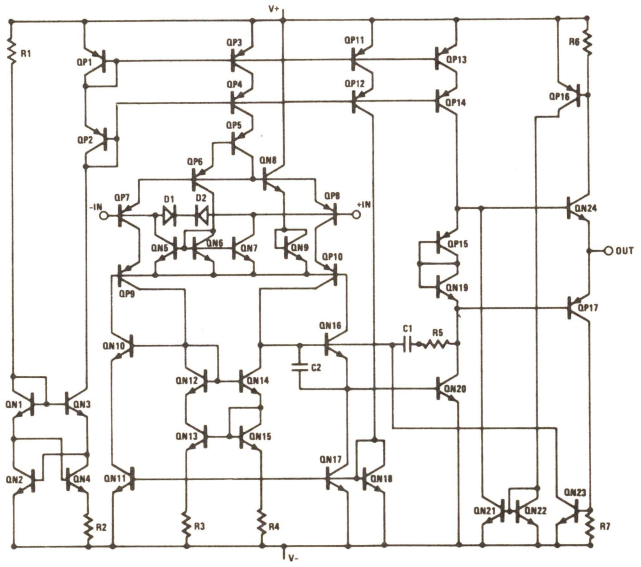
The HA-5134-2 has guaranteed operation from -55$^{o}$C to +125$^{o}$C and can be ordered as a military grade part. The HA-5134-5 is guaranteed from 0$^{o}$C to +75$^{o}$C and all devices are available in ceramic dual-in-line packages.

### Pinout

TOP VIEW




### Schematic (Each Amplifier)

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# HA-5101/5111

## Low Noise, High Performance Operational Amplifiers

October 1987

### Features

- Low Noise ..... 3.3nV/$\sqrt{Hz}$ at 1KHz
- Wide Bandwidth ..... 10MHz (Compensated)
  100MHz (Uncompensated)
- High Slew Rate ..... 10V/μs (Compensated)
  50V/μs (Uncompensated)
- Low Offset Voltage Drift ..... 3μV/°C
- High Gain ..... 1 x $10^6$V/V
- High CMRR/PSRR ..... 100dB
- High Output Drive Capability ..... 30mA

### Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators

### Description

The HA-5101/5111 are dielectrically isolated operational amplifiers featuring low noise and high performance. Both amplifiers have an excellent noise voltage density of 3.5nV/$\sqrt{Hz}$ at 1KHz. The uncompensated HA-5111 is stable at a minimum gain of 10 and has the same DC specifications as the unity gain stable HA-5101. The difference in compensation yields a 100MHz gain-bandwidth product and a 50V/μs slew rate for the HA-5111 versus a 10MHz unity gain bandwidth and a 10V/μs slew rate for the HA-5101.

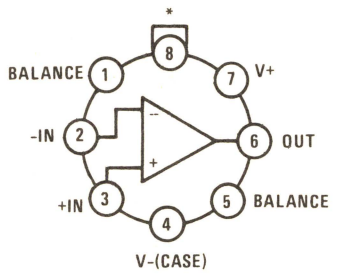
DC characteristics of the HA-5101/5111 assure accurate performance. The 1mV offset voltage is externally adjustable and offset voltage drift is just 3μV/°C. An offset current of only 30nA reduces input current errors and an open loop voltage gain of 1 x $10^6$V/V increases loop gain for low distortion amplification.

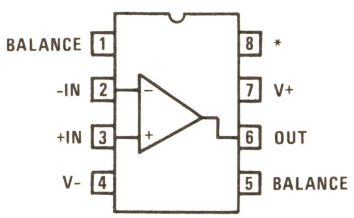
The HA-5101/5111 are ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head and phono cartridge preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators and high Q filters.

The HA-5101/5111-2 has guaranteed operation from -55°C to +125°C and can be ordered as a military grade part. The HA-5101/5111-5 has guaranteed operation from 0°C to +75°C. All devices are available in Ceramic Mini-DIP and TO-99 Can packages. Additionally, the HA-5101/5111-5 is available in a Plastic Mini-DIP package.

### Pinouts

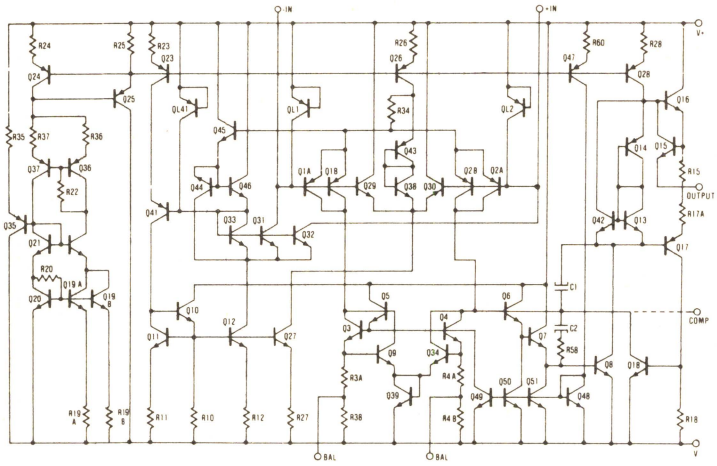
TOP VIEWS




*HA-5101 No Connect
HA-5111 Compensation

### Schematic



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# HA-5147

## Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifier

January 1987

### Features

- High Speed ..... 35V/$\mu$s
- Wide Gain Bandwidth ..... 120 MHz
- Low Noise ..... 3 nV/$\sqrt{\text{Hz}}$ at 1 KHz
- Low $V_{OS}$ ..... 10$\mu$V
- High CMRR ..... 126 dB
- High Gain ..... 1800V/mV

### Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

### Description

The HA-5147 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3 nV/$\sqrt{\text{Hz}}$) precision instrumentation performance with high speed (35V/$\mu$s) wideband capability.

This amplifier's impressive list of features include low $V_{OS}$ (10 $\mu$V), wide gain-bandwidth (120 MHz), high open loop gain (1800V/mV), and high CMRR (126dB) Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140 mW of power.

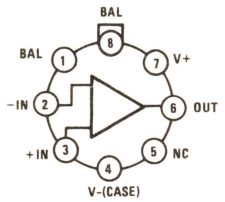
Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

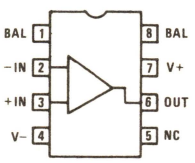
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten. The HA-5147 is available in TO-99 metal can, both epoxy and ceramic 8 pin mini-DIPs, as well as 20 pin LCC packages.

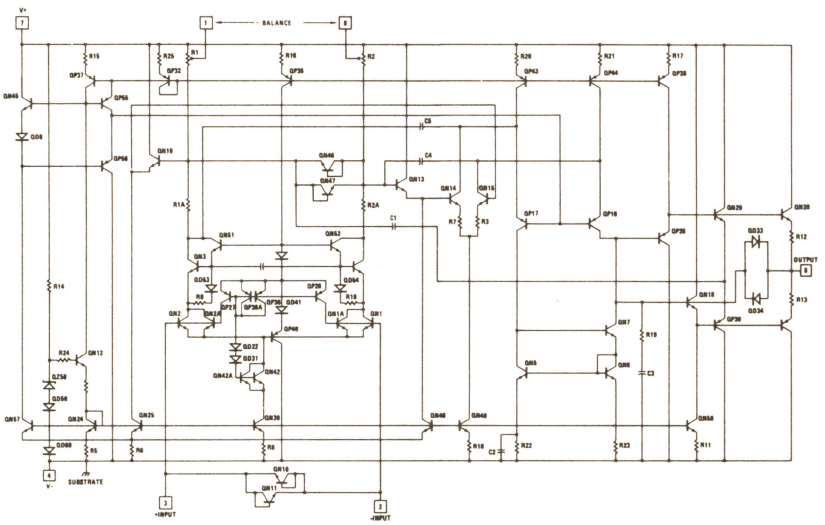
### Pinouts

TOP VIEW




### Schematic

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# HA-5002

PRELIMINARY

## Monolithic, Wideband, High Slew Rate, High Output Current Buffer

### Features

- Voltage Gain ..... 0.995
- High Input Impedance ..... 3000 KΩ
- Low Output Impedance ..... 3Ω
- Very High Slew Rate ..... 1300V/μsec
- Very Wide Bandwidth ..... 110MHz
- High Output Current ..... ±200mA
- Pulsed Output Current ..... 400mA
- Monolithic Construction

### Applications

- Line Driver
- Data Acquisition
- 110MHz Buffer
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Radar Cable Driver
- Video Products

### Description

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris D.I. technologies, the HA-5002 current buffer offers 1300V/μsec slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3 ohm output impedance.

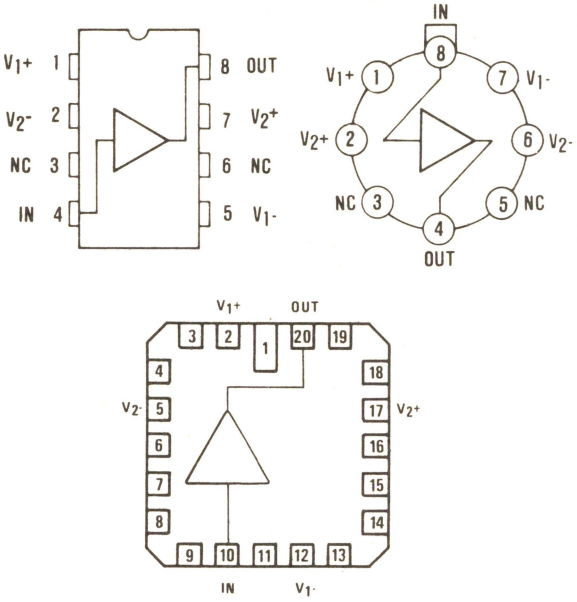
The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000K ohm input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

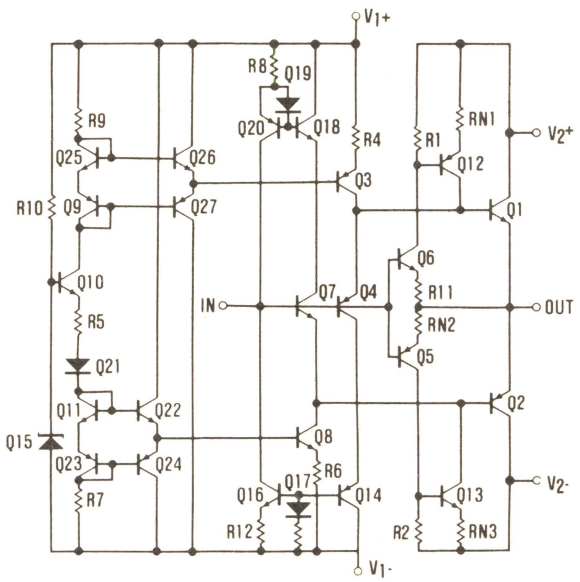
The HA-5002 is available in 8-pin can, 8-pin mini-dip, and 20-pin LCC packages.

### Pinout

TOP VIEWS




### Schematic

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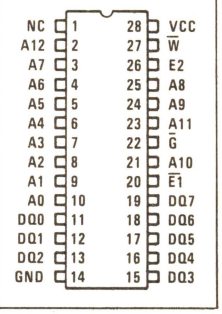
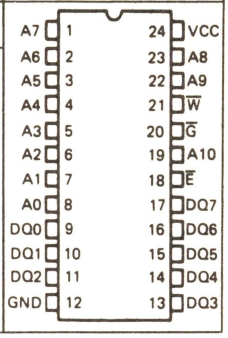
## CMOS STATIC RAMs 64K

| 8192 x 8 — 64K Asynchronous | | | | | Pinout |
|---|---|---|---|---|---|
| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin | |
| | | Operating | Standby | | |
| HM-65642 | 150 ns | 20 mA | 250 μA | AM99C88<br>NMC6164<br>MB8464<br>CDM6264 | |
| HM-65642B | 150 ns | 20 mA | 100 μA | | |

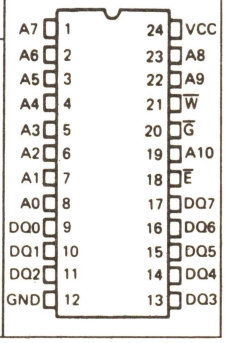



## CMOS STATIC RAMs — 16K

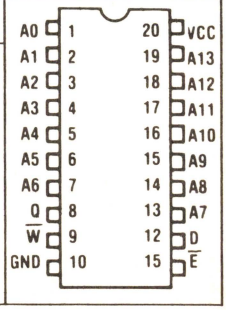
| 2048 x 8 — 16K Synchronous | | | | | Pinout |
|---|---|---|---|---|---|
| Part Number | Access Time | Power Supply Current | | Similar To | |
| | | Operating | Standby | | |
| HM-6516B | 120 ns | 10 mA/MHz | 50 μA | Hitachi 6116<br>Toshiba 5517<br>National 6516 | |
| HM-6516 | 200 ns | 10 mA/MHz | 100 μA | | |




| 2048 x 8 — 16K Asynchronous | | | | | Pinout |
|---|---|---|---|---|---|
| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin | |
| | | Operating | Standby | | |
| HM-65162S | 55 ns | 70 mA | 100 μA | Fujitsu 8416<br>Hitachi 6116<br>NEC 446<br>Toshiba 5517<br>National 6116<br>IDT 6116 | |
| HM-65162B | 70 ns | 70 mA | 50 μA | | |
| HM-65162 | 90 ns | 70 mA | 100 μA | | |
| HM-65162C | 90 ns | 70 mA | 900 μA | | |




| 16384 x 1 — 16K Asynchronous | | | | | Pinout |
|---|---|---|---|---|---|
| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin | |
| | | Operating | Standby | | |
| HM-65262S | 55 ns | 50 mA | 50 μA | Hitachi 6167<br>IDT 6167 | |
| HM-65262B | 70 ns | 50 mA | 50 μA | | |
| HM-65262 | 85 ns | 50 mA | 50 μA | | |

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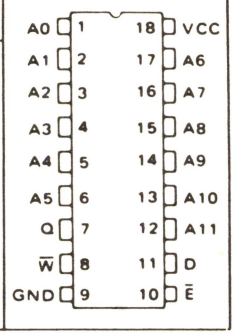
# CMOS STATIC RAMs — 4K & 1K

## 4096 x 1 — 4K Synchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-6504S | 120 ns | 7 mA/MHz | 25 μA | Fujitsu 8404 |
| HM-6504B | 200 ns | 7 mA/MHz | 25 μA | Oki 5104 |
| HM-6504 | 300 ns | 7 mA/MHz | 25 μA | National 6504 |

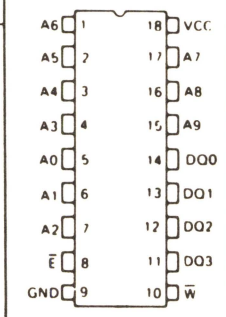
Pinout




## 1024 x 4 — 4K Synchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-6514S | 120 ns | 7 mA/MHz | 25 μA | Fujitsu 6514<br>Hitachi 4334<br>Nec 444 |
| HM-6514B | 200 ns | 7 mA/MHz | 25 μA | RCA 5114<br>Toshiba 5514 |
| HM-6514 | 300 ns | 7 mA/MHz | 25 μA | National 6514 |

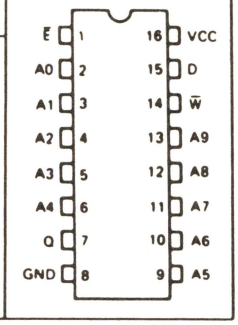
Pinout




## 1024 x 1 — 1K Synchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-6508B | 180 ns | 4 mA/MHz | 10 μA | National 74C929<br>Intersil 6508 |
| HM-6508 | 250 ns | 4 mA/MHz | 10 μA | AMI 56508 |

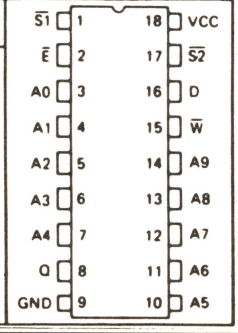
Pinout




## 1024 x 1 — 1K Synchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-6518B | 180 ns | 4 mA/MHz | 10 μA | National 74C930<br>Intersil 6518 |
| HM-6518 | 250 ns | 4 mA/MHz | 10 μA | |

Pinout

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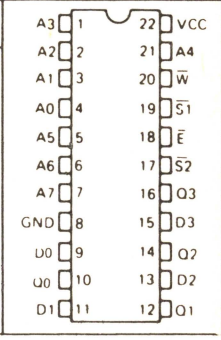
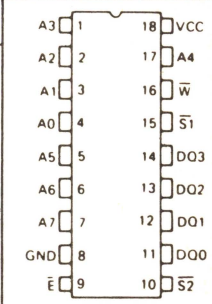
# CMOS STATIC RAMS — 1K

| 256 x 4 — 1K Synchronous | | | | | Pinout |
|---|---|---|---|---|---|
| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin | |
| | | Operating | Standby | | |
| HM-6551B | 220 ns | 4 mA/MHz | 10 μA | Intersil 6551 |  |
| HM-6551 | 300 ns | 4 mA/MHz | 10 μA | | |



| 256 x 4 — 1K Synchronous | | | | | Pinout |
|---|---|---|---|---|---|
| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin | |
| | | Operating | Standby | | |
| HM-6561B | 220 ns | 4 mA/MHz | 10 μA | Intersil 6561 |  |
| HM-6561 | 300 ns | 4 mA/MHz | 10 μA | | |



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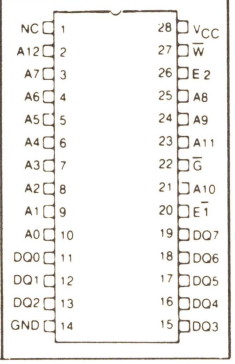
# CMOS STATIC RAM MODULES

## LCC RAM Module — 8K x 8 — 64K Asynchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-8808AS | 100 ns | 70 mA | 250 μA | EDH8808A |
| HM-8808AB | 120 ns | 70 mA | 250 μA | IDT7M864 |
| HM-8808A | 150 ns | 70 mA | 900 μA | HM6264 |

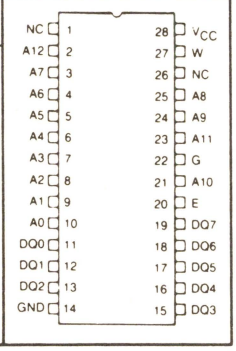
**Pinout**




## LCC RAM Module — 8K x 8 — 64K Asynchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-8808S | 100 ns | 70 mA | 250 μA | EDH8808 |
| HM-8808B | 120 ns | 70 mA | 250 μA | IDT8M864 |
| HM-8808A | 150 ns | 70 mA | 900 μA | |

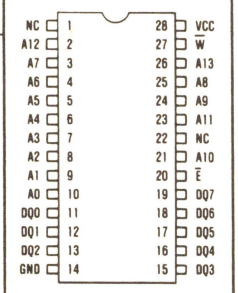
**Pinout**




## LCC RAM Module — 16K x 8 — 128K Asynchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-8816H | 85 ns | 400 mA | 800 μA | — |
| HM-8816HB | 70 ns | 400 mA | 800 μA | — |

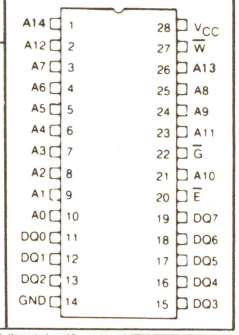
**Pinout**




## LCC RAM Module — 32768 x 8 — 256K Asynchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-8832 | 180 ns | 20 mA | 900 μA | EDH8832<br>IDT7M856<br>HM62256<br>MSM5256<br>μPD43256<br>TC55256 |

**Pinout**

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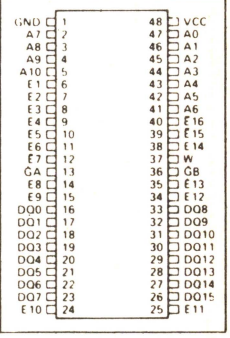
# CMOS STATIC RAM MODULES

## LCC RAM Module — 16384 x 16 / 32768 x 8 — 256K Synchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-92560 | 150 ns | 30/15 mA | 500 µA | — |
| HM-92560-5 | 250 ns | 35/20 mA | 3.5 mA | — |

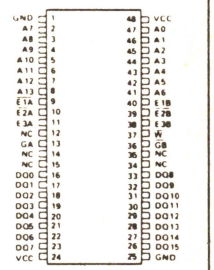
Pinout




## LCC Buffered Ram Module—16384 x 16 / 32768 x 8—256K Synchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-92570 | 250 ns | 30/15 mA | 600 µA | |
| | 300 ns | 35/20 mA | 3.5 mA | EDH892570 |

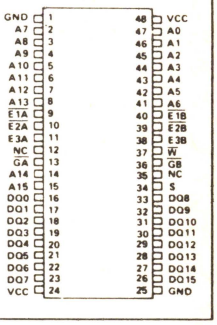
Pinout



## LCC Buffered Ram Module—65536 x 16 / 131072 x 8—1M Asynchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM-91M2 | 180 ns | 30 mA | 2 mA | EDH891M2 |

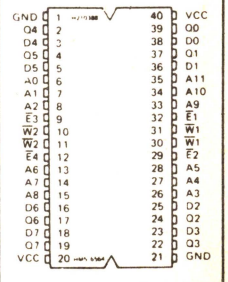
Pinout




## LCC RAM Module — 16384 x 4 / 8192 x 8 — 64K Synchronous

| Part Number | Access Time | Power Supply Current | | Replaces Pin for Pin |
|---|---|---|---|---|
| | | Operating | Standby | |
| HM5-6564 | 350 ns | 56/28 mA | 800 µA | — |
| HM5-6564-5 | 450 ns | 60/30 mA | 5.6 mA | — |

Pinout

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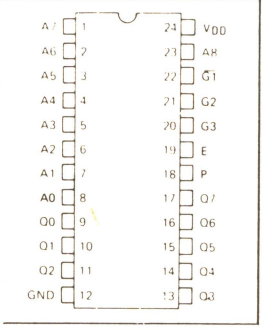
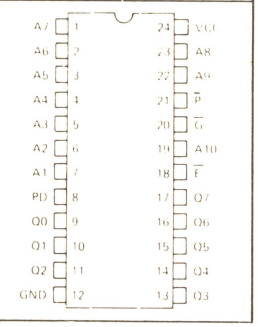
# CMOS PROMs — 4K & 16K

| 512 x 8 — 4K Synchronous | | | | | | Pinout |
|---|---|---|---|---|---|---|
| Part Number | Fuse Element | Access Time | Power Supply Current | | Replaces Pin for Pin | |
| | | | Operating | Standby | | |
| HM-6642 | NiCr | 200 ns | 20 mA/MHz | 100 μA | Harris 7641<br>Signetics 82S141 |  |



| 2048 x 8 — 16K Synchronous | | | | | | Pinout |
|---|---|---|---|---|---|---|
| Part Number | Fuse Element | Access Time | Power Supply Current | | Replaces Pin for Pin | |
| | | | Operating | Standby | | |
| HM-6617B<br>HM-6617 | NiCr<br>NiCr | 90 ns<br>120 ns | 20 mA/MHz<br>20 mA/MHz | 100 μA<br>100 μA | NMOS 2716<br>National 27C16<br>National 6716<br>Intersil 6716<br>Harris 6616 |  |







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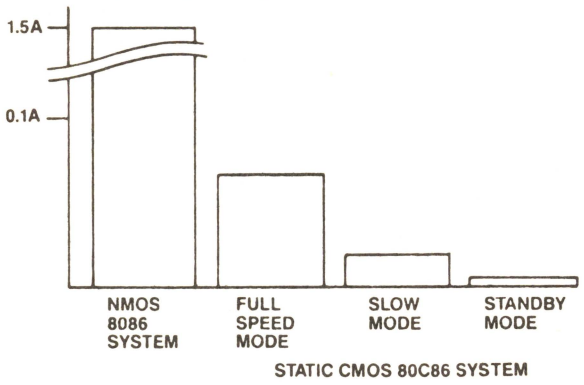
# Harris Chip Carriers: Your Competitive Edge

## CMOS and Surface Mount

Harris static CMOS circuits — the best combination of low power and performance — now give you the best choice in packaging. The 80C86 16-bit and 80C88 8/16-bit CPUs, along with the entire 80C86 family of support and peripheral circuits, are available in surface mount packages — ceramic Leadless Chip Carriers (LCCs) and Plastic Leaded Chip Carriers (PLCCs).

CMOS and surface mount — the right combination for low power system design. The low power of CMOS lets you throw out large, bulky power supplies, shrink enclosure size and increase system packing density.




STATIC CMOS LOW POWER

In many cases, dual-in-line packaging becomes the limiting factor. No longer. LCCs and PLCCs show a typical package space savings of 40-80% when compared to dual-in-line packages (see Table 1). Package weight is also reduced nearly 80%.

Harris LCCs and PLCCs conform to industry and JEDEC standards for pinout and physical dimensions — making your design and manufacturing transition to surface mount simple.

Maximize the Harris CMOS system packing density advantage with surface mount packaging. In addition to the 80C86/88 Family, take a look at the wide selection of Harris CMOS RAMs and programmable logic devices, along with linear data acquisition and telecom products, in LCCs and PLCCs.

## Ceramic Leadless Chip Carriers (LCCs)

For military and extended temperature range applications which demand unwavering performance in harsh environments, ceramic leadless chip carriers (LCCs) are the answer.

LCCs are constructed in the same manner as time-proven, side-brazed ceramic packages. Hermetically sealed and temperature-resistant, devices packaged in ceramic LCCs can be processed to MIL-STD-883 for high-reliability military applications.

## Plastic Leaded Chip Carriers (PLCCs)

Plastic leaded chip carriers (PLCCs) provide the cost-effective avenue for meeting new goals in commercial and industrial system size and weight reductions. From personal computers to biomedical instrumentation to remote data acquisition systems, portability and performance are key to their success. Harris products in PLCC packages can meet these design goals — and provide the low-cost, high-density answer for your system.

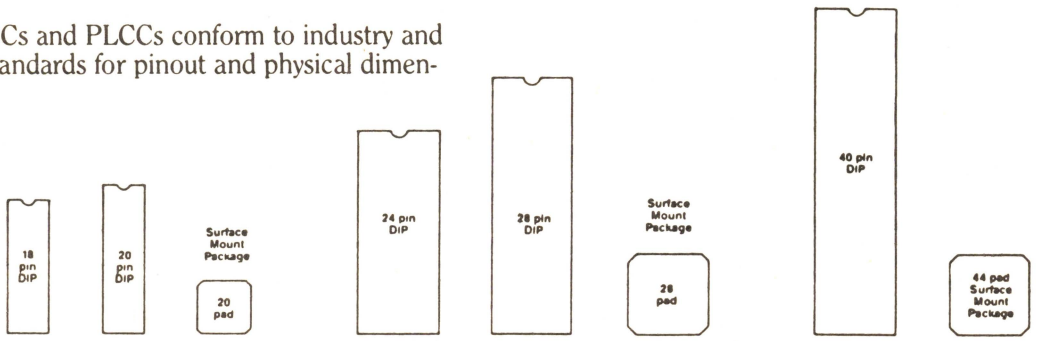



**TABLE 1**
**PACKAGE AREA COMPARISON DIP vs. SURFACE MOUNT**

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# HARRIS PRODUCTS AVAILABLE IN SURFACE MOUNT PACKAGING

Products listed below are available in surface mount packaging. Contact your local Harris sales representative for package options and availability.

| Product | Description | Product | Description |
|---|---|---|---|
| HA-2400 | 4 CHANNEL PROG. OP AMP | HI-516 | 16 CHAN/DIFF 8 CHAN CMOS HI SPEED MUX |
| HA-2420 | FAST SAMPLE/HOLD AMP | | |
| HA-2512 | HIGH SLEW RATE OP AMP | HI-518 | 8 CHAN/DIFF 4 CHAN CMOS HI SPEED MUX |
| HA-2522 | HIGH SLEW RATE OP AMP | | |
| HA-2622 | WIDE BANDWIDTH OP AMP | HI-524 | 4 CHANNEL WIDEBAND AND VIDEO MUX |
| HA-4741 | QUAD OP AMP | HI-539 | LOW LEVEL MUX |
| HA-4902 | QUAD COMPARATOR | HI-562A | 12-BIT D/A CONVERTER |
| HA-5127 | PRECISION OP AMP | HI-1818A | 8 CHANNEL MUX |
| HA-5137 | PRECISION OP AMP | HI-1828A | DIFF 4 CHANNEL MUX |
| HA-5141 | LOW POWER OP AMP | HI-5043 | DUAL SPDT ANALOG SWITCH |
| HA-5142 | LOW POWER PRECISION DUAL OP AMP | HI-5045 | DUAL DPST ANALOG SWITCH |
| HA-5144 | LOW POWER PRECISION QUAD OP AMP | HM-6504 | 4096 X 1 STATIC CMOS RAM |
| HA-5147 | PRECISION OP AMP | HM-6514 | 1024 X 4 STATIC CMOS RAM |
| HA-5151 | LOW POWER OP AMP | HM-6516 | 2048 X 8 STATIC CMOS RAM |
| HA-5152 | DUAL LOW POWER OP AMP | HM-65162 | 2048 X 8 STATIC CMOS RAM |
| HA-5154 | QUAD LOW POWER OP AMP | HM-65262 | 16K X 1 CMOS STATIC RAM |
| HC-5502A | PBX SLIC | HM-6616 | 2048 X 8 CMOS PROM |
| HC-5504 | PBX SLIC | HM-6641 | 512 X 8 CMOS PROM |
| HC-5512D | PCM FILTER | HPL-16LC8 | PROGRAMMABLE LOGIC ARRAY |
| HC-55564 | CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR (CVSD) | HPL-16RC4 | PROGRAMMABLE LOGIC ARRAY |
| | | HPL-16RC6 | PROGRAMMABLE LOGIC ARRAY |
| HD-15530 | MANCHESTER ENCODER-DECODER 24 PIN | HPL-16RC8 | PROGRAMMABLE LOGIC ARRAY |
| HD-4702 | PROG. BIT RATE GENERATOR | 80C86 | CMOS 16 BIT CPU |
| HD-6406 | PROG. ASYNC. COMM. INTERFACE | 80C88 | 8 BIT CMOS MICROPROCESSOR |
| HD-6409 | MANCHESTER ENCODER-DECODER | 82C37A | CMOS DMA CONTROLLER 8 MHZ |
| HF-10 | CMOS UNIVERSAL ACTIVE FILTER | 82C50A | CMOS ASYNC. COMM. ELEMENT |
| HI-201 | QUAD SPST CMOS ANALOG SWITCH | 82C52 | CMOS SERIAL COMM. INTERFACE |
| HI-201HS | HIGH SPEED QUAD SPST SWITCH | 82C54 | CMOS PROGRAMMABLE TIMER 8 MHZ |
| HI-506 | 16 CHAN CMOS ANALOG MUX | 82C55A | CMOS PROG. PERIPH. INT. 8 MHZ |
| HI-506A | 16 CHAN OVERVOLTAGE PROTECTED MUX | 82C59A | CMOS INT. CONT. 8 MHZ |
| | | 82C82 | CMOS OCTAL LATCH |
| HI-507 | 8 CHAN CMOS ANALOG MUX | 82C83H | CMOS INV. OCTAL LATCH |
| HI-507A | 8 CHAN OVERVOLTAGE PROTECTED CMOS MUX | 82C84A | CMOS CLK. GEN. |
| | | 82C85 | CLOCK GEN. W. STOP CLOCK |
| HI-508 | 8 CHAN CMOS ANALOG MUX | 82C86H | CMOS OCTAL BUS TRANSCEIVER |
| HI-508A | 8 CHAN OVERVOLTAGE PROTECTED MUX | 82C87H | CMOS OCTAL BUS TRANSCEIVER |
| HI-509 | 4 CHAN CMOS ANALOG MUX | 82C88 | CMOS BUS CONTROLLER |
| HI-509A | 4 CHAN OVERVOLTAGE PROTECTED CMOS MUX | 82C89 | BUS ARBITER |





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# STANDARD PRODUCT HIGHLIGHTS

## HI-8010/8011/8012

HIGH VOLTAGE DISPLAY DRIVER

- The HI-8010/8011/8012 devices are 35volt High Voltage dichroic display drivers with internally generated backplane driver. These device allow easy interface to 5 volt logic systems .The chip can drive up to 30-38 segments of LCD and require minimal display-to-data source interfacing. Data is loaded serially and held in internal latches until new data is received. The backplane is controlled either by an external RC network or by an external squarewave. The devices are easily cascadable and run at 2 MHz. We offer a large selection of packages for both military and industrial applications. This product is pin-for-pin compatable with the AMI 4520 series display drivers.

## HI-8030/8031

HIGH VOLTAGE DISPLAY DRIVER WITH INDEPENDENT COUNTER/TIMER

- The HI-8030/8031 drives either conventional twisted neumatic or high voltage dichroic displays. The devices drive 3/4 digit 7 segment displays with 3/4 annunciators respectively. Additionally, these devices include a multi-function counter/timer that can be used in conjunction with the display driver or independently for other unrelated system tasks. The counter/timer blocks are under software control and can be programmed to count in 5 separate modes, (hex, decimal, min./sec., hours/min., and sec./.1sec.). The displays can be up to 35volts. The HI-8030/31 boasts 10MHz operation , on chip backplane driver with oscillator circuitry, fully cascadable architecture, easy microprocessor interface and 2mA/segment drive capability for vacuum fluorescent displays.

## HI-8000

REAL TIME LOW-POWER MICROPROCESSOR COMPATIBLE CLOCK / TIMER / ALARM / CALENDAR / STOPWATCH / EVENT COUNTER

- The HI-8000 is a microprocessor compatible real-time clock that uses a multiplexed address/data bus similar to 6805,8085,and 8086. The timebase can be supplied by a crystal or by an externally available clock. The maximum count is 128 years with a resolution of 15.3 us. It features automatic leap year compensation. Programmable prescalers allow 4 independent clock rates to be generated by the chip. A standby mode is provided that leaves the clock running while disabling all other functions. In addition to the real time clock the HI-8000 also provides a timer and an alarm. The timer may have its own independent timebase, is 16 bits wide, and has independent interrupt and square wave outputs. The alarm is individually programmable for all clock registers. The alarm can be used to wake the HI-8000 out of the standby (or sleep) mode.

## HI-8024

REAL TIME CLOCK WITH INDEPENDENT COUNTER/TIMER

- The HI-8024 performs essentially the same function as the HI-8000 . The advantage of the 8024 is that it contains fewer pins, saving board space. The 8024 eliminates the 3 programmable output clock drivers and removes the crystal driver for the independent timer oscillator. The on-chip timer is still available but it must now be driven by an external timebase signal. The 8024 still provides the 3 independent programmable counters, thus providing latitude in the choice of crystal used.

## HI-8573/8575/8575

GENERAL PURPOSE OP AMP/COMPARATOR

- The HI-8573/8574/8575 series devices are pin-for-pin compatible with the Motorola MC14573/ MC14574/ MC14575 op amp/comparator chips. These devices provide selectable bias currents for trading off power consumption against slew rate. The CMOS technology enables extremely high input resistance and picoamp range input bias currents. These devices are internally compensated and are compatable with CMOS or TTL inputs.

## FOUNDRY SERVICES:

- Holt Integrated Circuits is dedicated to providing the best possible wafer foundry services to our customers and to providing lightning fast turnaround. Holt offers 3-um double poly silicon gate and 4-um metal gate CMOS technology. We will accept P.G. tapes, CALMA data base tapes, masks, CIF, and support full custom or semi-custom designs. Spice parameters are provided for simulation. We invite you to visit our 50,000 sq.ft. facility. Being onshore reduces the cost and expensive delays associated with offshore communications, shipping, and customs requirements. Our California based, class-100, 4" wafer processing facility brings you close to the process and people who can help you meet your production goals.


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**9351 Jeronimo Road, Irvine, CA 92718**

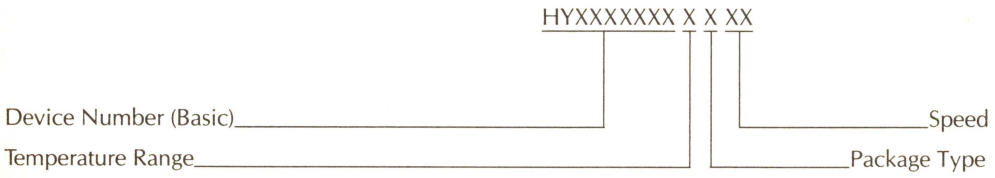
**Contact : Roger Smith or Joyce Bohlman at (714) 859-8800 or (800) 222-HOLT**

HYUNDAI SEMICONDUCTOR

# PRODUCT SELECTION GUIDE

| DEVICE | PART NO. | DESCRIPTION | PACKAGE TYPE | | | | | ACCESS TIME (ns) |
|---|---|---|---|---|---|---|---|---|
| | | | S | P | J | D | X | |
| | HY51C64X-12/15 | 64K×1 CMOS | • | | | | • | 120/150 |
| | HY51C64LX-12/15 | 64K×1 CMOS LOW POWER | • | | | | • | 120/150 |
| DRAM | HY5164X-12/15 | 64K×1 | • | | | | • | 120/150 |
| | HY51C256X-12/15/20 | 256K×1 CMOS | • | | | | • | 120/150/200 |
| | HY51C256LX-12/15/20 | 256K×1 CMOS LOW POWER | • | | | | • | 120/150/200 |
| | HY6116AX-10/12/15 | 2K×8 | | • | | | • | 100/120/150 |
| | HY6116ALX-10/12/15 | 2K×8 LOW POWER | | • | | | • | 100/120/150 |
| | HY61C16AX-35/45/55/70 | 2K×8 HIGH SPEED | • | • | | | • | 35/45/55/70 |
| | HY61C16ALX-35/45/55/70 | 2K×8 HIGH SPEED/LOW POWER | • | • | | | • | 35/45/55/70 |
| | HY61C67X-35/45/55/70 | 16K×1 HIGH SPEED | • | | | | • | 35/45/55/70 |
| | HY61C67LX-35/45/55/70 | 16K×1 HIGH SPEED/LOW POWER | • | | | | • | 35/45/55/70 |
| SRAM | HY61C68X-35/45/55/70 | 4K×4 HIGH SPEED | • | | | | • | 35/45/55/70 |
| | HY61C68LX-35/45/55/70 | 4K×4 HIGH SPEED/LOW POWER | • | | | | • | 35/45/55/70 |
| | HY62C64X-45/55/70 | 8K×8 HIGH SPEED | | • | | | • | 45/55/70 |
| | HY62C64LX-45/55/70 | 8K×8 HIGH SPEED/LOW POWER | | • | | | • | 45/55/70 |
| | HY6264X-10/12/15 | 8K×8 | | • | | | • | 100/120/150 |
| | HY6264LX-10/12/15 | 8K×8 LOW POWER | | • | | | • | 100/120/150 |
| | HY62C87X-35/45/55/70 | 64K×1 HIGH SPEED | • | | | | • | 35/45/55/70 |
| | HY62C87LX-35/45/55/70 | 64K×1 HIGH SPEED/LOW POWER | • | | | | • | 35/45/55/70 |
| | HY62C88X-35/45/55/70 | 16K×4 HIGH SPEED | • | | | | • | 35/45/55/70 |
| | HY62C88LX-35/45/55/70 | 16K×4 HIGH SPEED/LOW POWER | • | | | | • | 35/45/55/70 |
| EPROM | HY2764AX-15/20/30 | 8K×8 CMOS (12.5 VOLT VPP) | | • | | • | • | 150/200/300 |
| | HY2764AX-15/20/30 | 8K×8 (12.5 VOLT VPP) | | • | | • | • | 150/200/300 |
| EEPROM | HY93C46X | 64×16 CMOS (SERIAL ACCESS) | • | | • | | • | |
| | HY93C46EX | 64×16 CMOS (SERIAL ACCESS) | • | | • | | • | |
| | HY9346X | 64×16 (SERIAL ACCESS) | • | | • | | • | |
| | HY9346EX | 64×16 (SERIAL ACCESS) | • | | • | | • | |
| PEEL | HY18CV8X | 20 PIN PLD REPLACEMENT | • | | | | • | |

NOTES
1. X is package type
2. If you want any package type other than listed above, contact our sales office or representatives nearest you.




## *Temperature Range-Operation

NO MARK: 0°C to +70° C
E : −40° to +85° C

## *Package Type

Plastic DIP 300 MIL S
600 MIL P
SOIC J
CERDIP 600 MIL D
DIE FORM X

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# IMS C004 programmable link switch

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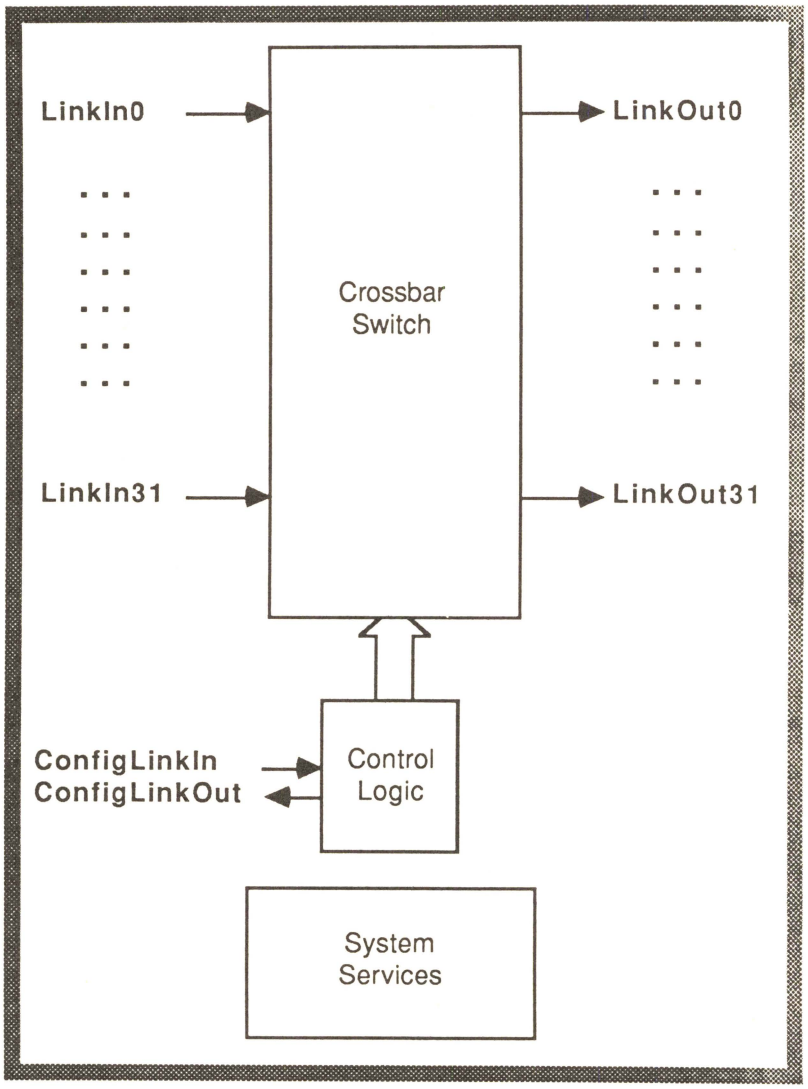
**Product Data**

## FEATURES

Standard INMOS links
32 way crossbar switch
Regenerates input signal
Cascadable to any depth
No loss of signal integrity
10 or 20 Mbits/sec operating speed
Separate INMOS configuration link
Single +5V ±10% power supply
TTL and CMOS compatibility
1W power dissipation
Standard 84 pin ceramic PGA




## APPLICATIONS

Programmable crossbar switch
Component of larger switch
Reconfigurable supercomputers
Message routing systems
High speed multiprocessor systems
Telecommunications
Robotics
Fault tolerant systems
Additional links for transputers

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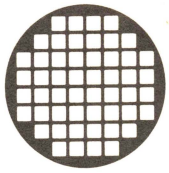


# IMSC011 link adaptor

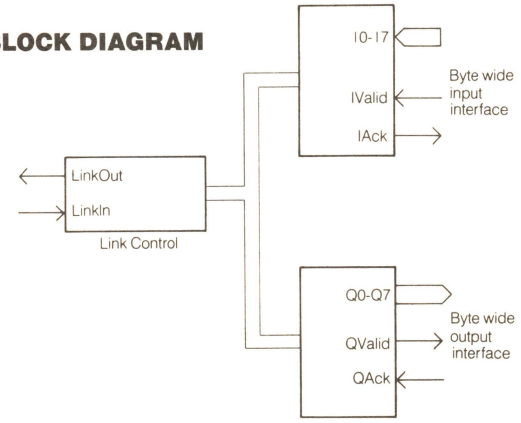
## FEATURES

- High performance system interconnect
- Bi-directional handshaken byte-wide interface
- INMOS serial link
- 10 or 20 Mbits/sec data rate
- Interrupt control for microprocessor buses
- Two configuration options
- Advanced 1.5 micron CMOS technology
- Standard 600 mil 28 pin DIP

## APPLICATIONS

- Programmable I/O pins for a transputer
- Link between transputers running at different clock frequencies
- Interface between transputers and industry standard peripherals
- High performance handshaken link between standard microprocessor buses

## BLOCK DIAGRAM




# IMSC012 link adaptor

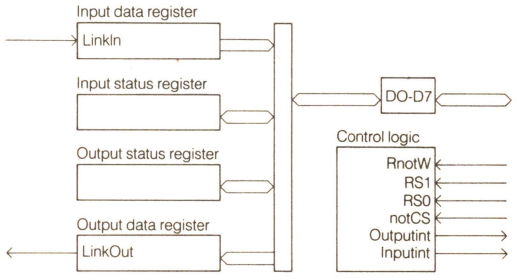
## FEATURES

- High performance system interconnect
- Bi-directional handshaken byte-wide interface
- INMOS serial link
- 10 or 20 Mbits/sec data rate
- Interrupt control for microprocessor buses
- Advanced 1.5 micron CMOS technology
- Standard 300 mil 24 pin DIP

## APPLICATIONS

- Interface between transputers and industry standard peripherals
- High performance handshaken link between standard microprocessor buses

## BLOCK DIAGRAM

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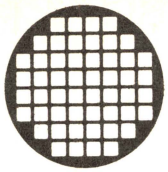


# IMS T212 transputer

**IMS T212:** The IMS T212 integrates a 16-bit microprocessor, four standard transputer communications links, 2K bytes of on-chip RAM, a memory interface and peripheral interfacing on a single 1.5 micron CMOS chip.

**Processor:** The design of the T212 achieves compact programs, efficient high level language implementation and provides direct support for the occam model of concurrency. Procedure calls, process switching and interrupt latency are all sub-microsecond. The T212 provides high performance arithmetic and direct support for floating point operations.

The processor shares its time between any number of concurrent processes. A process which is waiting for communication or a timeout does not consume any processor time. Two levels of process priority enable fast interrupt response to be acheived.

**Links:** The T212 uses a DMA block transfer mechanism to transfer messages between its memory and other transputer products via INMOS links (full duplex, serial links, capable of data rates up to 20Mbits/sec). Transputers can communicate with each other through links, or to a byte-wide bus through INMOS link adaptors. The link interfaces and the processor all operate concurrently, allowing the processing to continue while the data is being transferred on all of the links.

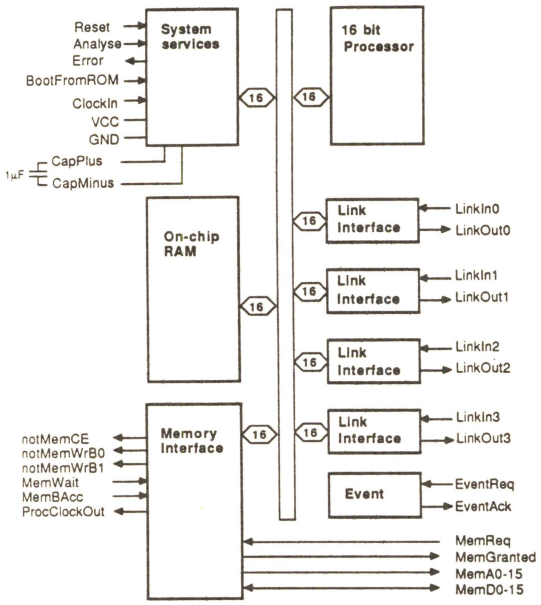
**Memory:** The 2K bytes of RAM provide a maximum data rate of 40 Mbytes/s with multiport access for the processor and links.

**Memory interface:** Provides 64K bytes of direct address space with a maximum data rate of 20 Mbytes/s. 16 bits data and 16 bits address non-multiplexed. Optimized for fast static RAM, word or byte organized.

**Peripheral interface:** The memory controller supports memory mapped peripherals, which may use DMA. Links may be interfaced to peripherals via an INMOS link adaptor. A peripheral can request attention via the event pin.

**Time:** The processor includes timers for both high and low priority processes.

**IMS T212 block diagram**




**Error handling:** High-level language execution is made secure with array bounds checking, arithmetic overflow detection, etc. A flag is set when an error is detected. The error can be handled internally by software or externally by sensing the error pin. System state is preserved for subsequent analysis.

**Programming:** Programming in occam provides maximum performance and allows exploitation of concurrency. Occam is the lowest level language available for programming transputers; industry standard languages such as C, Fortran and Pascal are also available.

**Other Products:** IMS T414 32 bit transputer; IMS IM212 16 bit transputer disk controller; IMS T800 floating point transputer; IMS C004 programmable link switch; IMS C011, IMS C012 link adaptors; evaluation software and hardware.

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# IMS T414 transputer

**IMS T414:** The IMS T414 integrates a 32-bit microprocessor, four standard transputer communications links, 2K bytes of on-chip RAM, a memory interface and peripheral interfacing on a single 1.5 micron CMOS chip.

**Processor:** The design of the T414 achieves compact programs, efficient high level language implementation and provides direct support for the occam model of concurrency. Procedure calls, process switching and interrupt latency are all sub-microsecond. The T414 provides high performance arithmetic and direct support for floating point operations.

The processor shares its time between any number of concurrent processes. A process which is waiting for communication or a timeout does not consume any processor time. Two levels of process priority enable fast interrupt response to be acheived.

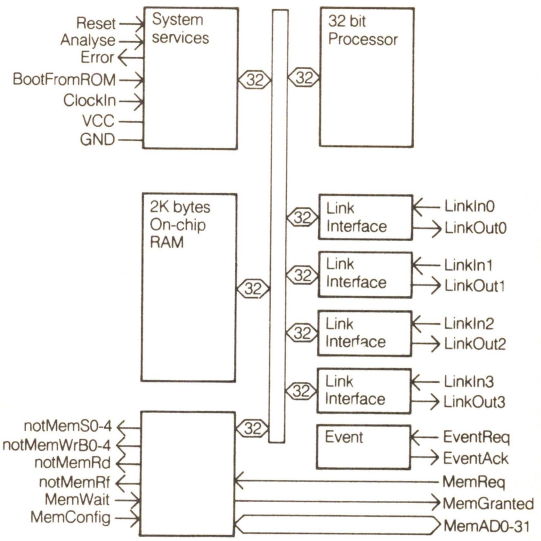
**Links:** The T414 uses a DMA block transfer mechanism to transfer messages between its memory and other transputer products via INMOS links (full duplex, serial links, capable of data rates up to 20Mbits/sec). Transputers can communicate with each other through links, or to a byte-wide bus through INMOS link adaptors. The link interfaces and the processor all operate concurrently, allowing the processing to continue while the data is being transferred on all of the links.

**Memory:** The 2K bytes of RAM provide a maximum data rate of 80 Mbytes/s with multiport access for the processor and links.

**Memory interface:** The T414 can directly access a linear address space up to 4 Gbytes. The 32 bit wide memory interface uses multiplexed data and address lines and provides a data rate of up to 25 MBytes/s. A configurable memory controller provides all timing, control and DRAM refresh signals for a wide variety of mixed memory systems.

**Peripheral interface:** The memory controller supports memory mapped peripherals, which may use DMA. Links may be interfaced to peripherals via an INMOS link adaptor. A peripheral can request attention via the event pin.

## T414 block diagram




**Time:** The processor includes timers for both high and low priority processes.

**Error handling:** High-level language execution is made secure with array bounds checking, arithmetic overflow detection, etc. A flag is set when an error is detected. The error can be handled internally by software or externally by sensing the error pin. System state is preserved for subsequent analysis.

**Programming:** Programming in occam provides maximum performance and allows exploitation of concurrency. Occam is the lowest level language available for programming transputers; industry standard languages such as C, Fortran and Pascal are also available.

**Other Products:** IMS T212 16 bit transputer, IMS T800 floating point transputer, IMS M212 16 bit transputer disk controller; IMS C004 programmable link switch, IMS C011, IMS C012 link adaptors; evaluation software and hardware.

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# IMS T800 transputer

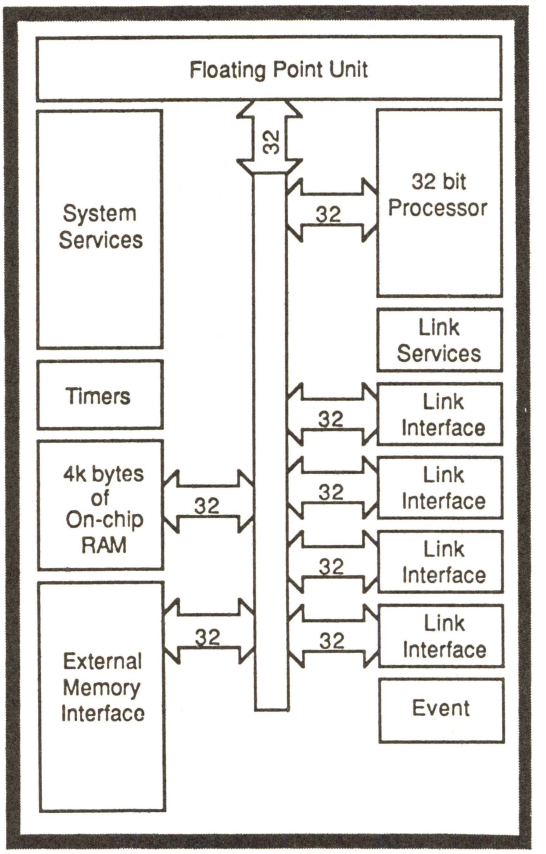
## Product Data

### FEATURES

Integral hardware 64 bit floating point unit
ANSI-IEEE 754-1985 floating point representation
Sustained 1.5(2.25†) Mflops
32 bit architecture with 15 MIPS† performance
Hardware and pin compatible with IMS T414-20
4 Kbytes on chip RAM for 120 Mbytes/sec† data rate
32 bit configurable memory interface
Directly addresses 4 Gbytes at 40 Mbytes/sec†
High performance graphics support
Sub-microsecond context switch & interrupt latency
Four 5/10/20 Mbits/sec INMOS serial links
Hardware scheduler for concurrent programs
Internal timers for real time processing
External event interrupt
Support for run-time error diagnostics
Boots from communication link or ROM
On-chip DRAM controller
Internal program continues during DMA
Optional external memory wait states
Single 5 MHz clock input
Single +5V ±10% power supply

### APPLICATIONS

Scientific and mathematical applications
High speed multi processor systems
High performance graphics processing
Supercomputers
Workstations and workstation clusters
Digital signal processing
Accelerator processors
Distributed databases
System simulation
Telecommunications
Robotics
Fault tolerant systems
Image processing
Molecular modelling
Pattern recognition
Artificial intelligence




Note: † indicates a reference to a 30 MHz device.

**Other Products:** IMS T414 32 bit transputer; IMS IM212 16 bit transputer disk controller; IMS C004 programmable link switch; IMS C011, IMS C012 link adaptors; evaluation software and hardware.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# IMS M212 disk processor

**IMS M212:** The IMS M212 integrates a 16-bit microprocessor, two standard transputer communications links, 2K bytes of fast on-chip RAM, 4K bytes of preprogrammed ROM, a bytewide external memory interface and a full four channel floppy and soft-sectored Winchester disk controller on a single 1.5 micron CMOS chip.

**Processor:** The M212 processor is identical to that of the IMS T212 and is therefore fully compatible with the T414 and other members of the transputer family. It is designed to achieve efficient implementation of high level language programs and to provide direct support for the occam model of concurrency. Procedure calls, process switching and interrupt latency are all sub-microsecond.

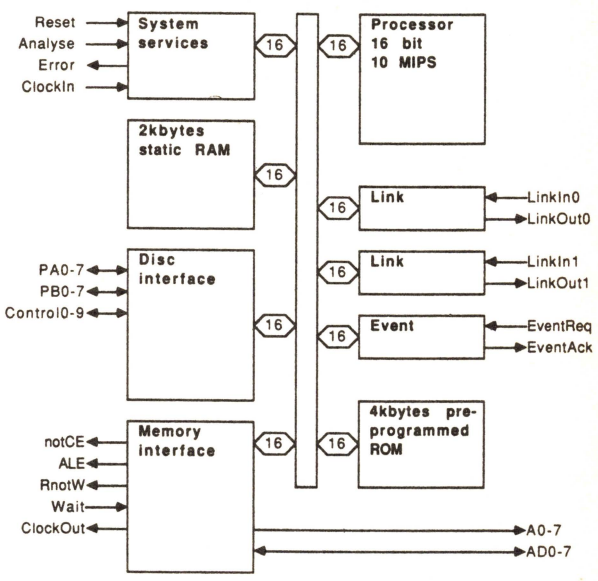
The processor shares its time between any number of concurrent processes. A process which is waiting for communication or a timeout does not consume any processor time. Two levels of process priority enable fast interrupt response to be acheived.

**Time:** The processor includes timers for both high and low priority processes.

**Links:** The M212 uses a DMA block transfer mechanism to pass messages between its memory and other transputer products via serial links. The links are full duplex, two wire, zero glue, bidirectional connections capable of data rates of up to 20Mbits/sec each way. The links can communicate directly to other transputers, or via link adaptors to I/O ports or other microprocessor busses. The DMA engines and the processor all operate concurrently, allowing processing to continue while data is being transferred both ways on all of the links.

**Disk Controller:** The disk interface consists of two bi-directional, 8-bit wide programmable ports to control the time insensitive functions of the disk, such as drive/head selection, track stepping, ready, etc. Time critical and interface signals are controlled by a dedicated 10-bit wide port. These ten signals are Vin, PhaseUp/Dn, Early/Late, Read/WriteData, WriteGate/Clock and Index.

**IMS M212 block diagram**




Data rates between 125kHz and 10MHz are possible.

The disk interface provides simple connection to ST506/412 and SA450 compatible drives. The hardware contains facilities for address mark detection, FM and MFM encoding and decoding, error detection and syndrome generation and ID field recognition in addition to data separation and precompensation. All of these facilities are fully programmable.

**Memory:** The M212 can access a linear address space of up to 64kbytes. 16 address and 8 data bits are multiplexed for the simplest interface to bytewide memory. A wait pin is provided.

**Peripheral interface:** Links may be connnected to peripherals via link adaptors. Peripherals may be memory mapped and request attention using the event input pin. Alternatively the disk control ports may be programmed to provide a dedicated peripheral interface.

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# IMS A100

## Cascadable Signal Processor

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### FEATURES

- Full 16 bit, 32 stage, transversal filter
- Fully cascadable with no speed degradation or reduction in dynamic range.
- Coefficients selectable as 4, 8, 12, or 16 bits wide
- Data throughput to 10 MHz
- High speed microprocessor compatible interface.
- Data input and output through dedicated ports or via the microprocessor interface
- Fully static high speed CMOS implementation
- TTL compatible
- Single +5V ±10 % power supply
- Power dissipation < 1.5 Watts
- Standard 84-pin ceramic PGA

### APPLICATIONS

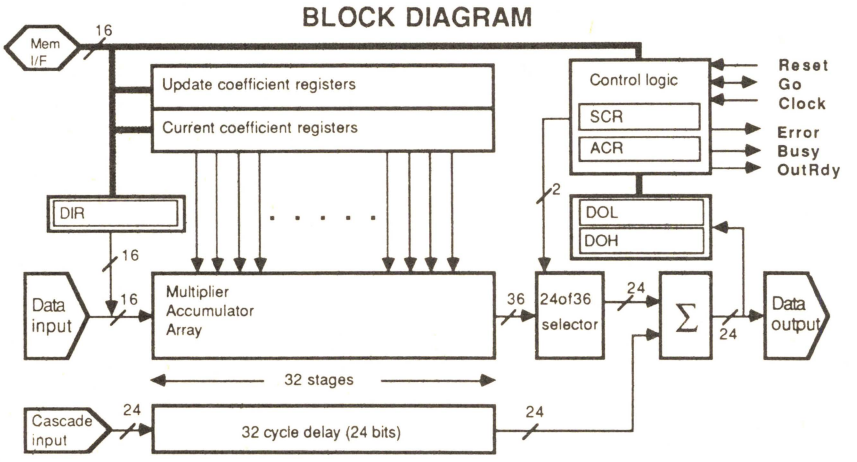
- Digital FIR filtering
- High speed adaptive filtering
- Correlation and Convolution
- Discrete Fourier Transform
- Speech processing using Linear Predictive Coding
- Image processing
- Waveform synthesis
- Adaptive and fixed equalizers and echo cancellers
- Spread spectrum communication
- Beamforming and beamscanning in sonar and radar
- Pulse compression
- High speed fixed point matrix multiplication

### DESCRIPTION

The IMS A100 is a high speed, high accuracy 32 stage digital transversal filter. It's flexible architecture allows it to be used as a "building block" in a wide range of Digital Signal Processing (DSP) applications. The part is capable of performing high speed DFTs, convolution, and correlation, as well as many filtering functions.

The input data word length is 16 bits, and coefficients are programmable to be 4, 8, 12, or 16 bits wide; two's complement numerical formats are used for both data and coefficients. The coefficients can be updated asynchronously to the system clock during normal operation, allowing the chip to be used in a variety of adaptive systems. The IMS A100 can also be cascaded to construct longer transversal filters with no additional logic or degradation in speed, whilst preserving a high degree of accuracy. The device is controlled through a standard memory interface, allowing use with any general purpose microprocessor. Data communications can be either through the memory interface, or through dedicated data ports.

### BLOCK DIAGRAM





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# IMS1830
# IMS1830L
## CMOS
## High Performance
## 32K x 8 Static RAM

**MIL-STD-883C Versions Available**

### FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Low Power Standby and Operation; Standby 3mW (typ.), Operation 300mW (typ.)
- 45, 55, 70, and 85 nsec Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- 28 Pin, 600-mil DIP, 32 pin LCC
- Fast Write Cycle when Outputs Disabled
- Battery Backup Operation - 2V Data Retention (L version only)

### DESCRIPTION

The IMS1830 is a high speed CMOS 32K x 8 Static RAM having access times of 45, 55, 70, and 85ns.

The IMS1830 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1830 provides a Chip Enable function (/E) to place the circuit into a reduced power standby mode.

The IMS1830L is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1830M and IMS1830LM are MIL-STD-883 versions intended for military applications that demand superior reliability and performance.

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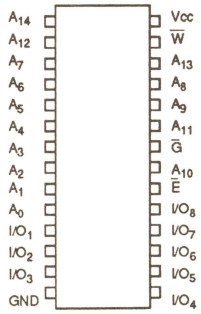
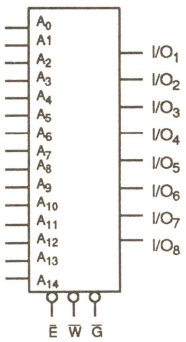
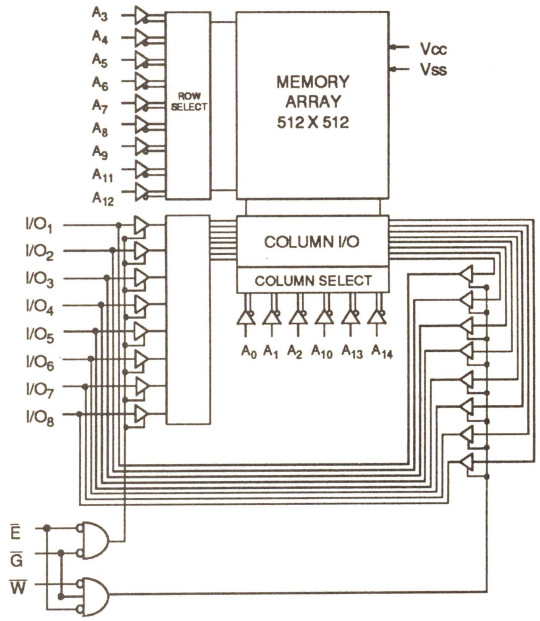
### PIN CONFIGURATION




### LOGIC SYMBOL




### BLOCK DIAGRAM




### PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$-$A_{14}$ | ADDRESS INPUTS | Vcc | POWER |
| $\overline{W}$ | WRITE ENABLE | Vss | GROUND |
| $I/O_1$-$I/O_8$ | DATA IN/OUT | | |
| $\overline{E}$ | CHIP ENABLE | | |
| $\overline{G}$ | OUTPUT ENABLE | | |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# IMS1203

# CMOS High Performance 4K x 1 Static RAM

**MIL-STD-883C Versions Available**

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## FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 1 Bit Organization
- 20, 25, 35 and 45 nsec Address Access Times
- 20, 25, 35 and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 18-Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

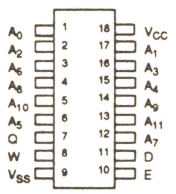
## DESCRIPTION

The INMOS IMS1203 is a high performance 4K x 1 CMOS static RAM. The IMS1203 allows speed enhancements to existing 4K X 1 applications with the additional benefit of reduced power consumption.

The IMS1203 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1203 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

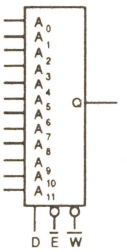
The IMS1203M is a MIL-STD-883 version intended for military applications that demand superior reliability and performance.

## PIN CONFIGURATION

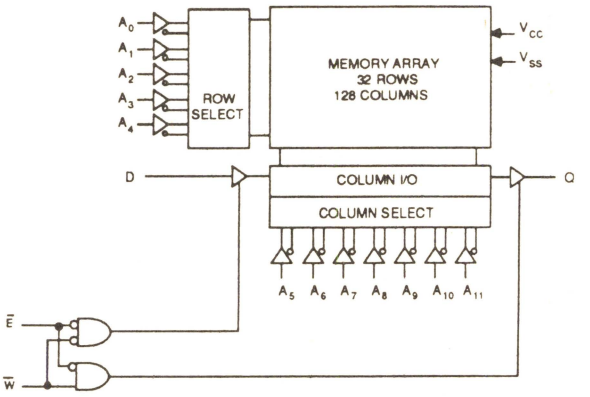



DIP

## LOGIC SYMBOL




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0 - A_{11}$ | ADDRESS INPUTS | $V_{CC}$ | POWER (+5V) |
| $\overline{W}$ | WRITE ENABLE | $V_{ss}$ | GROUND |
| D | DATA IN | | |
| $\overline{E}$ | CHIP ENABLE | | |
| Q | DATA OUTPUT | | |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# IMS1223

# CMOS High Performance 1K x 4 Static RAM

**MIL-STD-883C Versions Available**

## FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 1K x 4 Bit Organization
- 20, 25, 35 and 45 nsec Address Access Times
- 20, 25, 35 and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- 18-Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

## DESCRIPTION

The INMOS IMS1223 is a high performance 1K x 4 CMOS static RAM. The IMS1223 allows speed enhancements to existing 1K X 4 applications with the additional benefit of reduced power consumption.

The IMS1223 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1223 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1223M is a MIL-STD-883 version intended for military applications that demand superior reliability and performance.

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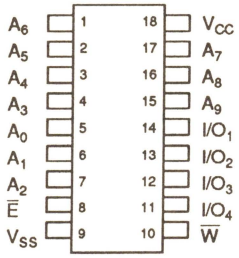
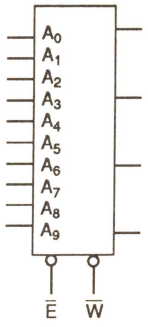
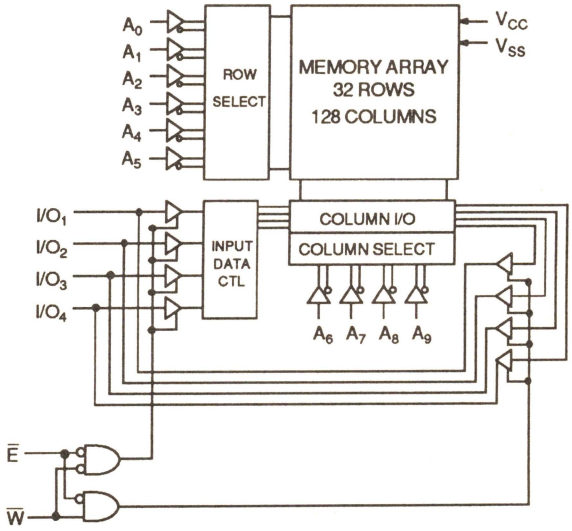
## PIN CONFIGURATION




## LOGIC SYMBOL




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_9$ | ADDRESS INPUTS | $V_{CC}$ | POWER |
| $\overline{W}$ | WRITE ENABLE | $V_{SS}$ | GROUND |
| $\overline{E}$ | CHIP ENABLE | | |
| I/O | DATA IN/OUT | | |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# IMS1403
# IMS1403L
# CMOS
# High Performance
# 16K x 1 Static RAM

**MIL-STD-883C Versions Available**

## FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 1 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)
- Single +5V ± 10% Operation
- Power Down Function
- Pin Compatible with IMS1400
- Battery Backup Operation - 2V Data Retention (L version only)

## DESCRIPTION

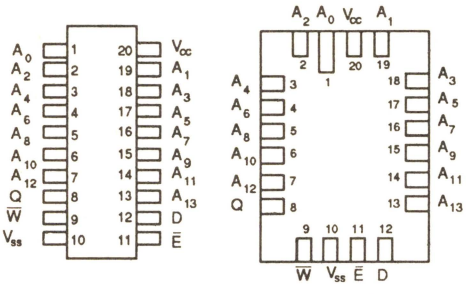
The INMOS IMS1403 is a high performance 16K x 1 CMOS static RAM. The IMS1403 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1403 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1403L is a low power version offering battery backup data retention operating from a 2 volt supply.

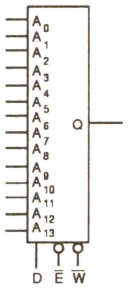
The IMS1403M and IMS1403LM are extended temperature versions for military applications.

## PIN CONFIGURATION

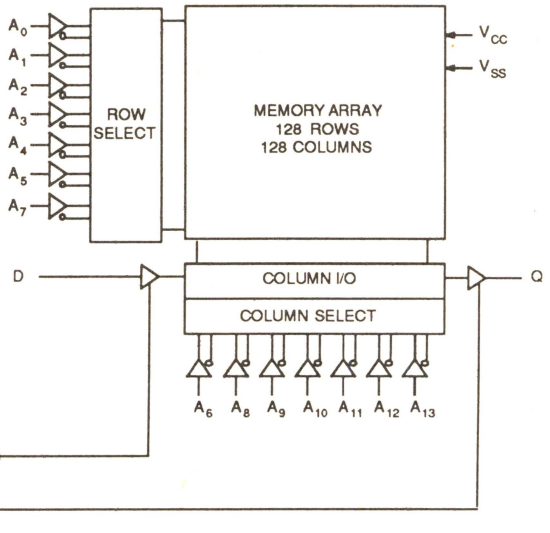



DIP CHIP CARRIER

## LOGIC SYMBOL




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_{13}$ | ADDRESS INPUTS | Q | DATA OUTPUT |
| $\overline{W}$ | WRITE ENABLE | $V_{CC}$ | POWER |
| $\overline{E}$ | CHIP ENABLE | $V_{SS}$ | GROUND |
| D | DATA INPUT | | |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# IMS1423
# CMOS
# High Performance
# 4K x 4 Static RAM

**MIL-STD-883C Versions Available**

## FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 4 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Pin Compatible with IMS1420

## DESCRIPTION

The INMOS IMS1423 is a high performance 4K x 4 CMOS static RAM. The IMS1423 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1423 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1423 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1423M is a MIL-STD-883 version intended for military applications that demand superior performance and reliability.

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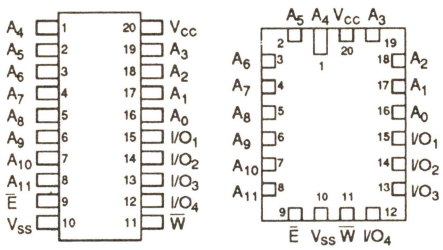
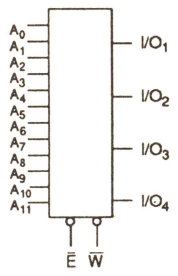
## PIN CONFIGURATION

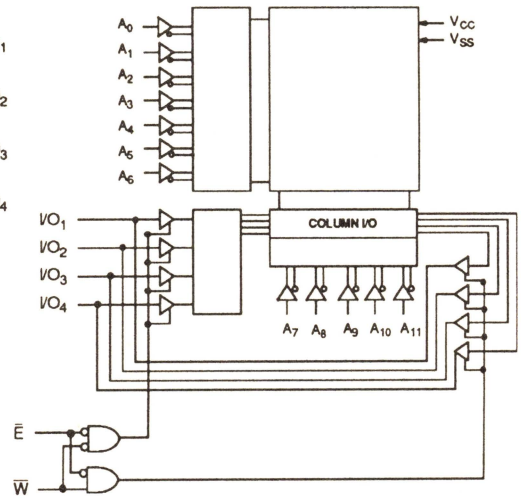



DIP CHIP CARRIER

## LOGIC SYMBOL




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_{11}$ | ADDRESS INPUTS | $V_{CC}$ | POWER |
| $\overline{W}$ | WRITE ENABLE | $V_{SS}$ | GROUND |
| $\overline{E}$ | CHIP ENABLE | | |
| I/O | DATA IN/OUT | | |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# IMS1433
## CMOS

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# High Performance 2K x 8 Static RAM

**MIL-STD-883C Versions Available**

### FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 2K x 8 Bit Organization
- 30, 35, 45, and 55 nsec Address Access Times
- 30, 35, 45, and 55 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- 24 Pin, 300-mil DIP
- Fast Write Cycle when Outputs Disabled

### DESCRIPTION

The IMS1433 is a high speed CMOS 2K x 8 Static RAM having access times of 30, 35, 45, and 55ns.

The IMS1433 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1433 provides a Chip Enable function (/E) to place the circuit into a reduced power standby mode.

The IMS1433M is a MIL-STD-883 version intended for military applications that demand superior performance and reliability.

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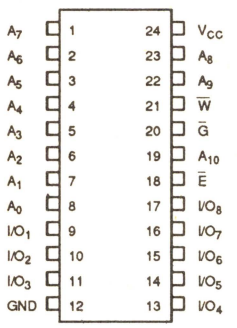
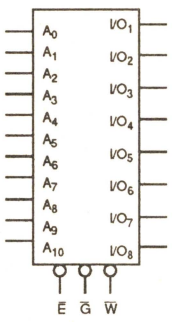
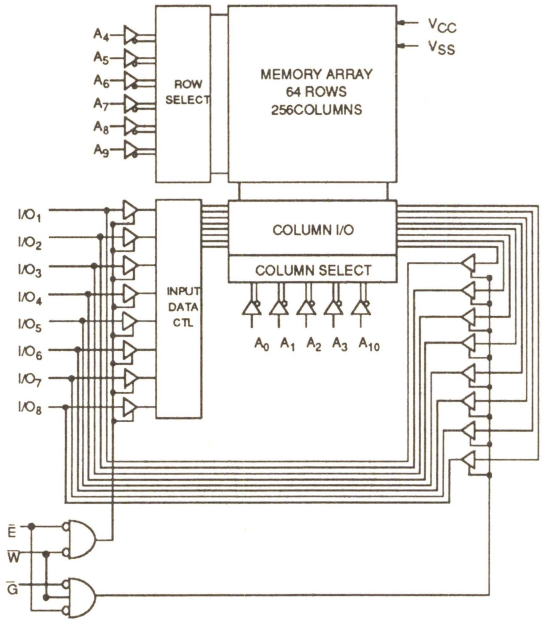
### PIN CONFIGURATION




### LOGIC SYMBOL




### BLOCK DIAGRAM




### PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$-$A_{10}$ | ADDRESS INPUTS | $V_{CC}$ | POWER (+5V) |
| $\overline{W}$ | WRITE ENABLE | $V_{SS}$ | GROUND |
| $I/O_1$-$I/O_8$ | DATA IN/OUT | | |
| $\overline{E}$ | CHIP ENABLE | | |
| $\overline{G}$ | OUTPUT ENABLE | | |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# IMS1600

## High Performance 64K x 1 CMOS Static RAM

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**MIL-STD-883C Versions Available**

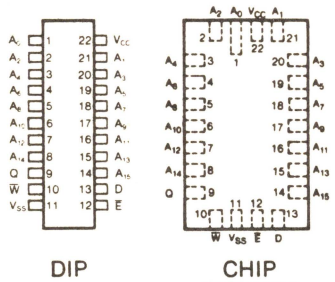
### FEATURES

- INMOS Very High Speed CMOS Advanced Process—1.6 Micron Design Rules
- 64K x 1 Bit Organization
- 35, 45, 55 and 70nsec Address Access Times
- 35, 45, 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 22-Pin, 300-mil DIP (JEDEC Standard Pinout)
- Single +5V ± 10% Operation
- Power Down Function

### DESCRIPTION

The IMS1600 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power. By using stable CMOS levels, the standby power may be reduced to an even lower level.

### PIN CONFIGURATION

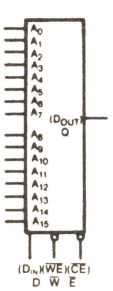



DIP

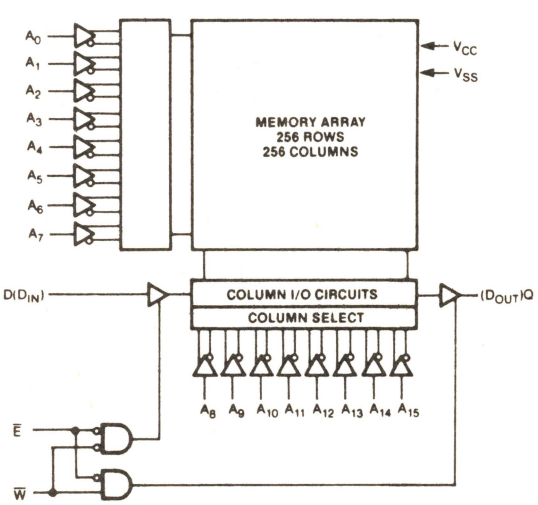



CHIP CARRIER

### LOGIC SYMBOL




### BLOCK DIAGRAM




### PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{15}$ | ADDRESS INPUTS |
| $\overline{W}$ | WRITE ENABLE |
| $\overline{E}$ | CHIP ENABLE |
| D | DATA INPUT |
| Q | DATA OUTPUT |
| $V_{CC}$ | POWER (+5V) |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# IMS1601L
# CMOS Commercial Battery Backed 64K x 1 Static RAM

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**MIL-STD-883C Versions Available**

## FEATURES

- INMOS Very High Speed CMOS
- Advanced Process—1.6 Micron Design Rules
- 64K x 1 Bit Organization
- 35, 45, 55 and 70nsec Address Access Times
- 35, 45, 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 22 Pin, 300-mil DIP (JEDEC Standard Pinout)
- 22 Pin LCC (JEDEC Standard Pinout)
- Single +5V ± 10% Operation
- Power Down Function
- Data Retention to 2 volts

## DESCRIPTION

The IMS1601L is a high performance 64K x 1 CMOS static RAM.

The IMS1601L features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1601L provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode.

The IMS1601L also provides battery backup capability offering data retention from a 2 volt supply.

The IMS1601L extended temperature version is available for military applications.

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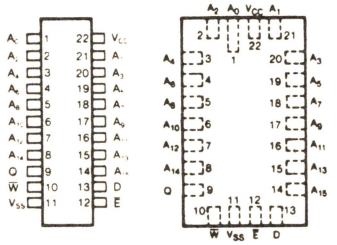
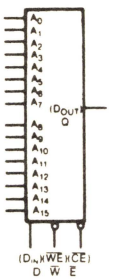
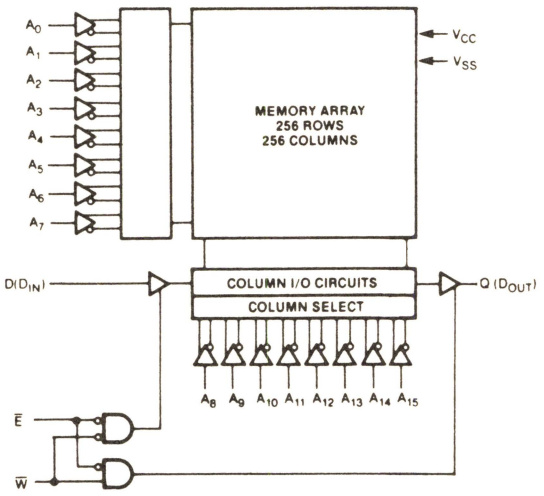
## PIN CONFIGURATION




## LOGIC SYMBOL



## BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{15}$ | ADDRESS INPUTS |
| $\overline{W}$ | WRITE ENABLE |
| $\overline{E}$ | CHIP ENABLE |
| D | DATA INPUT |
| Q | DATA OUTPUT |
| $V_{CC}$ | POWER (+5V) |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# IMS1620
# IMS1620L
# IMS1620A
# CMOS
# High Performance
# 16K x 4 Static RAM

**MIL-STD-883C Versions Available**

## FEATURES

- INMOS Very High Speed CMOS
  - 1620A -1.2 Micron Design Rules
  - 1620/20L - 1.6 Micron Design Rules
- 16K x 4 Bit Organization
- 25, 35, 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V ± 10% Operation
- Power Down Function
- 22-Pin, 300-mil DIP
- 22 Pin LCC
- Battery Backup Operation 2V Data Retention (L Version Only)

## DESCRIPTION

The IMS1620 is a high speed CMOS 16K x 4 Static RAM having access times of 25, 35, 45, 55 and 70ns. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary CMOS technology.

The IMS1620 features fully static operation requiring no external clocks or timing strobes. The IMS1620 is optimized for high speed system operation as well as providing increased reliability due to the CMOS process.

The low power version (IMS1620L) offers a battery backup data retention capability operating from a 2 volt battery.

The IMS1620 is available in JEDEC Standard 22-pin Plastic and Ceramic 300-mil DIP, and a JEDEC Standard 22-pin Ceramic Leadless Chip Carrier. INMOS also provides a Military version, the IMS1620M, as well as a 16K x 4 Static RAM with an Output Enable function $\overline{G}$, the IMS1624 and IMS1624M.

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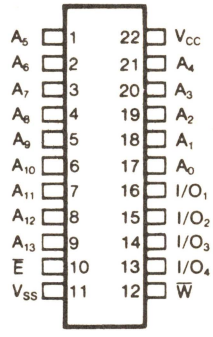
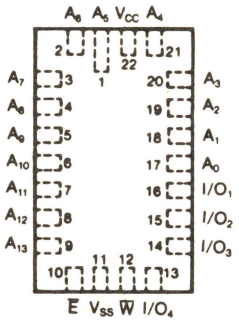
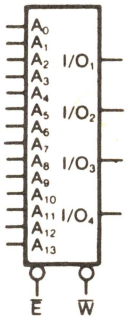
## PIN CONFIGURATION




CHIP CARRIER

## LOGIC SYMBOL




## PIN NAMES

| | |
|---|---|
| $A_0$-$A_{13}$ ADDRESS INPUTS | $V_{CC}$ POWER (+5V) |
| $\overline{W}$ WRITE ENABLE | $V_{SS}$ GROUND |
| I/O DATA IN/OUT | |
| $\overline{E}$ CHIP ENABLE | |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# IMS1624
# IMS1624L
# IMS1624A
## CMOS
## High Performance
## 16K x 4 Static RAM

**MIL- STD-883 Versions Available**

### FEATURES

- INMOS Very High Speed CMOS
  - 1620A - 1.2 Micron Design Rules
  - 1620/1620L - 1.6 Micron Design Rules
- 16K x 4 Bit Organization
- 25, 35, 45, 55 and 70nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Single +5V ± 10% Operation
- Power Down Function
- 24-Pin, 300-mil DIP
- 28- Pin LCC
- Output Enable to Control Bus Contention
- Battery Backup Operation 2V Data Retention (L Version Only)

### DESCRIPTION

The IMS1624 is a high performance 16K x 4 CMOS static RAM.

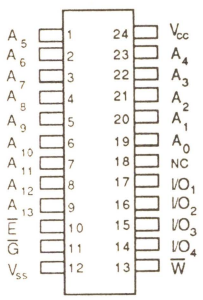
The IMS1624 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode. The IMS1624 also includes an Output Enable ($\overline{G}$) function to improve system performance and to control bus contention. The IMS1624 is functionally equivalent to the IMS1620, with the addition of the $\overline{G}$ control function.

The IMS1624 is available in a 24 Pin Ceramic and Plastic DIP and a 28 Pin Ceramic Leadless Chip Carrier.

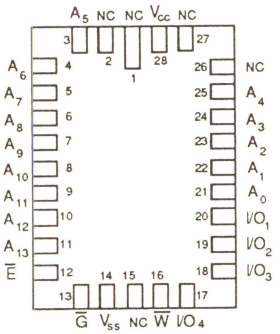
The IMS1624L is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1624M and IMS1624LM are MIL-STD-883 versions intended for military applications that demand superior performance and reliability.

### PIN CONFIGURATION

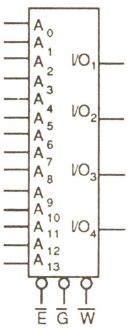



DIP




CHIP CARRIER

### LOGIC SYMBOL




### PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$–$A_{13}$ | ADDRESS INPUTS | $V_{CC}$ | POWER (+5V) |
| $\overline{W}$ | WRITE ENABLE | $V_{SS}$ | GROUND |
| I/O | DATA IN/OUT | | |
| $\overline{E}$ | CHIP ENABLE | | |
| $\overline{G}$ | OUTPUT ENABLE | | |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# IMS1630
# IMS1630L
# CMOS
# High Performance
# 8K x 8 Static RAM

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**MIL-STD-883C Versions Available**

## FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 8K x 8 Bit Organization
- 45, 55 and 70 nsec Address Access Times
- 45, 55 and 70 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- 28 Pin, 600-mil DIP (JEDEC Standard)
- Fast Write Cycle when Outputs Disabled
- Battery Backup Operation - 2V data retention (L version only)

## DESCRIPTION

The IMS1630 is a high speed CMOS 8K x 8 Static RAM having access times of 45, 55 and 70ns.

The IMS1630 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1630 provides two Chip Enable functions (/E1, E2) to place the circuit in a reduced power standby mode.

The IMS1630L is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1630M and IMS1630LM are available in extended temperature versions for military operating applications.

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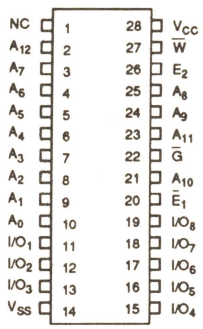
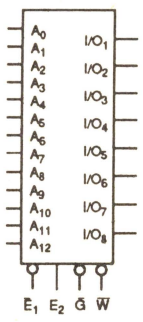
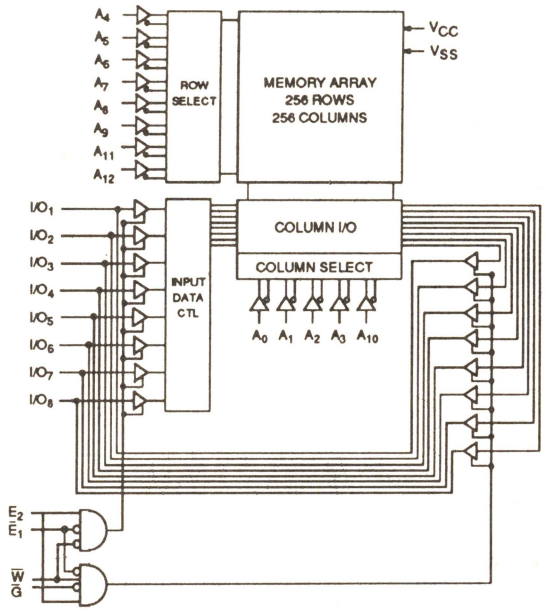
## PIN CONFIGURATION




## LOGIC SYMBOL




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$-$A_{12}$ | ADDRESS INPUTS | $V_{CC}$ | POWER (+5V) |
| $\overline{W}$ | WRITE ENABLE | $V_{SS}$ | GROUND |
| $I/O_1$-$I/O_8$ | DATA IN/OUT | | |
| $E_1$, $E_2$ | CHIP ENABLE | | |
| $\overline{G}$ | OUTPUT ENABLE | | |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# IMS1800
# IMS1800L
# CMOS
# High Performance
# 256K x 1 Static RAM

Preliminary

**MIL-STD-883C Versions Available**

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## FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 256K x 1 Bit Organization
- 25, 30, 35 and 45 nsec Address Access Times
- 25, 30, 35 and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 24-Pin, 300-mil DIP
- 28 Pin LCC
- Single +5V ± 10% Operation
- Battery Backup Operation 2V Data Retention (L version only)

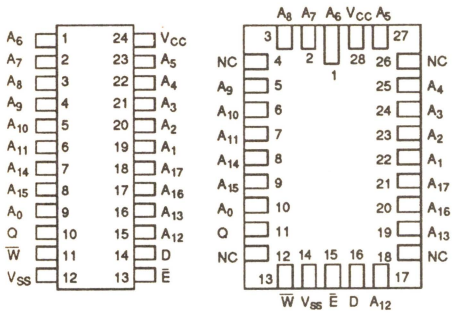
## DESCRIPTION

The INMOS IMS1800 is a high performance 256K x 1 CMOS static RAM. The IMS1800 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1800 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1800 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

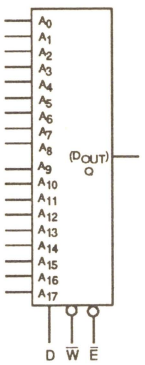
The IMS1800M and IMS1800LM are MIL-STD-883 versions intended for military applications that demand superior reliability and performance.

## PIN CONFIGURATION

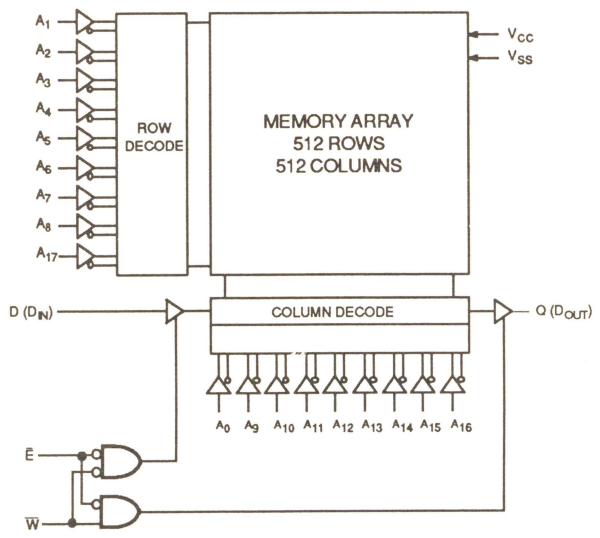



DIP CHIP CARRIER

## LOGIC SYMBOL




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_{17}$ | ADDRESS INPUTS | Q | DATA OUTPUT |
| $\overline{W}$ | WRITE ENABLE | $V_{CC}$ | POWER |
| $\overline{E}$ | CHIP ENABLE | $V_{SS}$ | GROUND |
| D | DATA INPUT | | |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# IMS1820
# IMS1820L
# CMOS
# High Performance 64K x 4 Static RAM

**MIL-STD-883C Versions Available**

inmos®

## FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 64K x 4 Bit Organization
- 25, 30, 35 and 45 nsec Address Access Times
- 25, 30, 35 and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- 24-Pin, 300-mil DIP
- 28 Pin LCC
- Single +5V ± 10% Operation
- Battery Backup Operation 2V Data Retention (L version only)

## DESCRIPTION

The INMOS IMS1820 is a high performance 64K x 4 CMOS static RAM. The IMS1820 offers maximum density and performance enhancements with the additional advantages of reduced power consumption and superior reliability.

The IMS1820 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1820 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1820M and IMS1820LM are MIL-STD-883 versions intended for military applications that demand superior reliability and performance.

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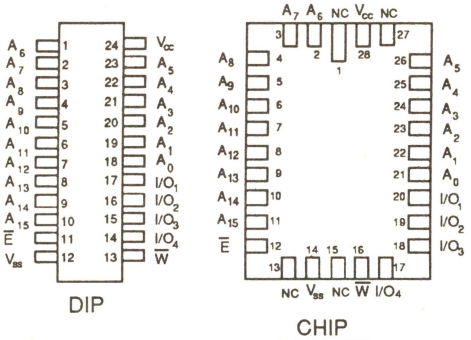
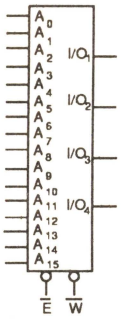
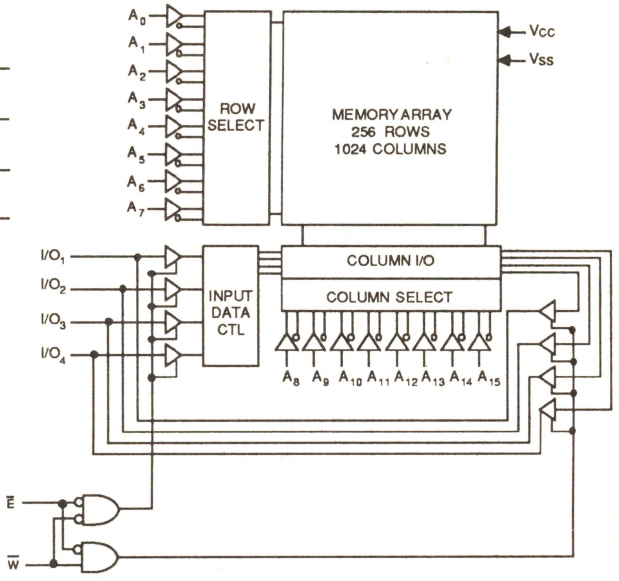
## PIN CONFIGURATION




## LOGIC SYMBOL



## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$–$A_{15}$ | ADDRESS INPUTS | $V_{CC}$ | POWER (+5V) |
| $\overline{W}$ | WRITE ENABLE | $V_{SS}$ | GROUND |
| I/O | DATA IN/OUT | | |
| $\overline{E}$ | CHIP ENABLE | | |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# IMSM624

# CMOS 64K x 16 Static RAM Module

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## FEATURES

- INMOS' Very High Speed CMOS RAMs
- Customer Configured Memory:
  -64K by 16, 128K by 8 or 256K by 4
- 1024K-bit density
- 35, 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Includes Decoupling Capacitors
- Common Data Input & Output
- Three-state Output
- 40-Pin, 900-mil DIP
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Battery Back-up Operation- 2V Data Retention (L version only)

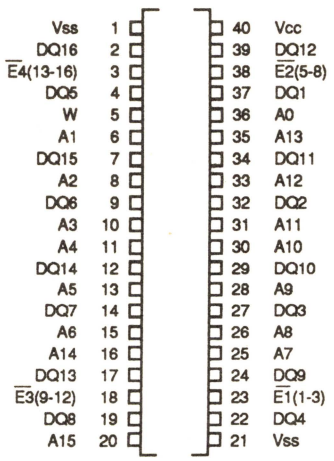
## DESCRIPTION

The INMOS IMSM624 is a high speed 1024K-bit CMOS memory in a single, compact package. The IMSM624 is comprised of sixteen IMS1600 high performance CMOS static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate. Four chip select signals are provided (one for each 64K x 4 array) allowing the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4.

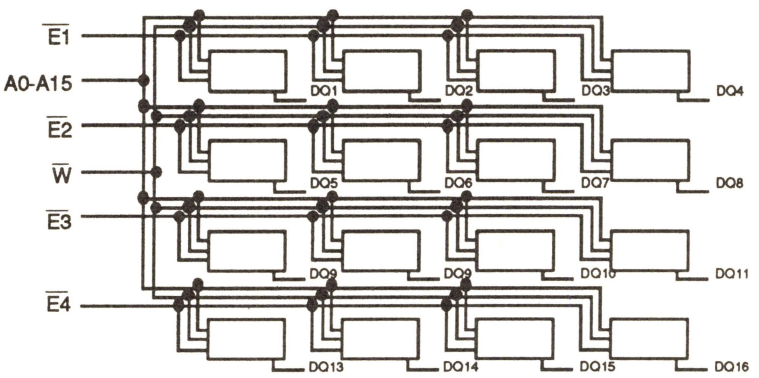
The IMSM624 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times.The IMSM624 is offered in a high density 40-pin, 900 mil center, sidebrazed DIP. Dual ground pins are provided for maximum noise immunity.

All INMOS Military Memory Modules are 100% processed to MIL-STD-883C, method 5004, Class B.

## PIN CONFIGURATION




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| A0 - A15 | ADDRESS INPUTS | Vcc | POWER |
| W | WRITE ENABLE | Vss | GROUND |
| E1-4 | CHIP ENABLE | | |
| DQ1-16 | DATA IN/OUT | | |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# IMSM820

# CMOS 64K x 4 Static RAM Module

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## FEATURES

- INMOS' Very High Speed CMOS RAMs
- Advanced Process - 1.6 Micron Design Rules
- 64K x 4 Bit Organization
- 35, 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Includes Decoupling Capacitors
- Common Data Input & Output
- Three-state Output
- 24-Pin, 300-mil DIP (JEDEC Std.)
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Battery Back-up Operation- 2V Data Retention (L version only)

## DESCRIPTION

The INMOS IMSM820 is a high performance 64K x 4 CMOS memory in a single, compact package. The IMSM820 is comprised of four IMS1600 high performance CMOS static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

The IMSM280 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMSM820 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

All Inmos Military Memory Modules are 100% processed to MIL-STD-883C, method 5004, Class B.

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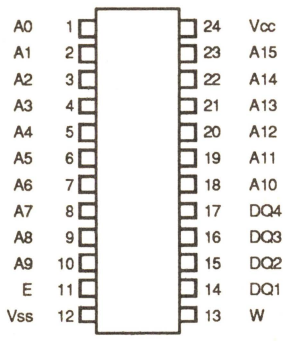
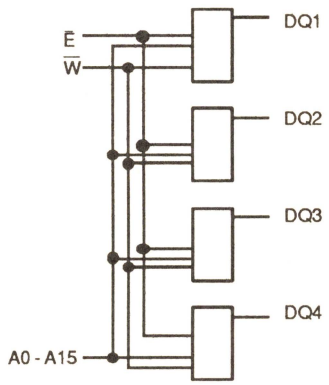
## PIN CONFIGURATION




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0 - A_{15}$ | ADDRESS INPUTS | $V_{CC}$ | POWER |
| $\overline{W}$ | WRITE ENABLE | $V_{SS}$ | GROUND |
| $\overline{E}$ | CHIP ENABLE | | |
| $DQ_{1-4}$ | DATA IN/OUT | | |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# IMSM830

# CMOS 32K x 8 Static RAM Module

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## FEATURES

- INMOS' Very High Speed CMOS RAMs
- Advanced Process - 1.6 Micron Design Rules
- 32K x 8 Bit Organization
- 45, 55, 70 and 85 nsec Access Times
- Fully TTL Compatible
- Includes Decoupling Capacitors
- Common Data Input & Output
- Output Enable Function
- Three-state Output
- 28-Pin, 600-mil DIP (JEDEC Std.)
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Battery Back-up Operation- 2V Data Retention (L version only)

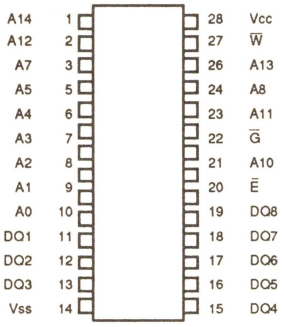
## DESCRIPTION

The INMOS IMSM830 is a high performance 32K x 8 CMOS memory in a single, compact package. The IMSM830 is comprised of four IMS1624 high performance CMOS static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate. Functional equivalence to a monolithic 256K device is accomplished by an on-board decoder that interprets the high order address to select two of four RAMs.

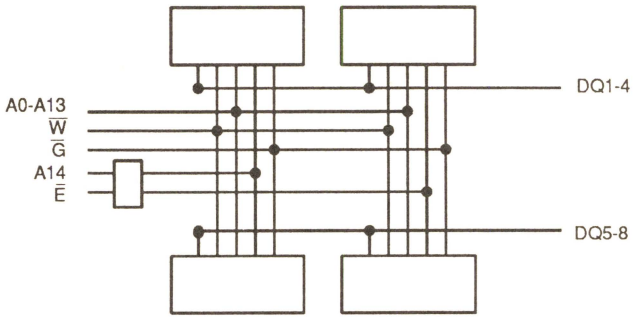
The IMSM830 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMSM830 provides a Chip Enable (/E) function that can place the device into a low-power standby mode and an Output Enable (/G) function to eliminate bus contention.

All Inmos Military Memory Modules are 100% processed to MIL-STD-883C, method 5004, Class B.

## PIN CONFIGURATION




## BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_{14}$ | ADDRESS INPUTS | $DQ_{1-8}$ | DATA IN/OUT |
| $\overline{W}$ | WRITE ENABLE | | |
| $\overline{E}$ | CHIP ENABLE | $V_{CC}$ | POWER |
| $\overline{G}$ | OUTPUT ENABLE | $V_{SS}$ | GROUND |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# IMS G171

# High performance CMOS Colour look-up table

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## FEATURES

- Compatible with the RS170 video standard.
- Pixel Rates up to 50 MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Up to 8 bits per pixel.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun, composite blank.
- Low DAC glitch energy.
- Video signal output into 37.5 Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single + 5 V ± 10% power supply.
- Low power dissipation, 880 mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL package.

## DESCRIPTION

The IMS G171 integrates the function of a colour look-up table (or colour palette), digital to analogue converters (designed to drive into a doubly terminated 75 Ω line) and bi-directional microprocessor interface into a single 28 pin package.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G171 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

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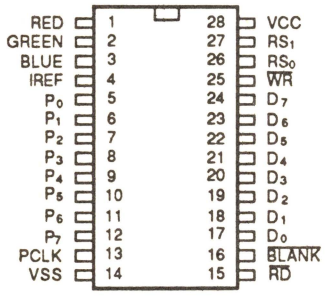
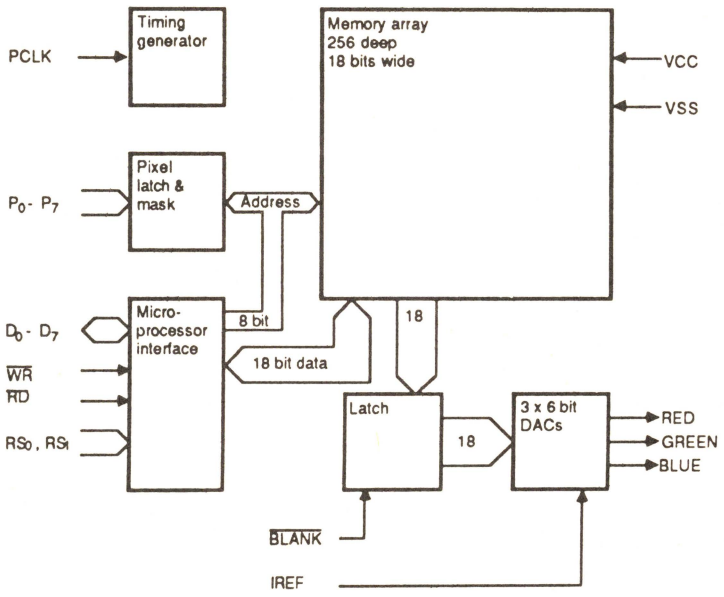
### PIN CONFIGURATION




| PIN NAMES | |
|---|---|
| $P_0$ - $P_7$ | Pixel address inputs |
| $D_0$ - $D_7$ | Program data inputs |
| $RS_0$, $RS_1$ | Register select |
| RED, GREEN, BLUE | Analogue video outputs |
| PCLK | Pixel clock |
| $\overline{WR}$ | Write enable |
| $\overline{RD}$ | Read enable |
| $\overline{BLANK}$ | Video blanking input |
| IREF | Reference current |
| VCC | +5 volt supply input |
| VSS | Ground |

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# IMS G176

# High performance CMOS Colour look-up table

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## FEATURES

- Compatible with the RS170 video standard.
- Pixel Rates up to 65 MHz.
- Single monolithic, high performance CMOS.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun, composite blank.
- Low DAC glitch energy.
- Video signal output into 37.5 Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single + 5 V power supply.
- Low power dissipation, typically 1W at maximum pixel rate.
- Standard 600 mil 28 pin DIL package.

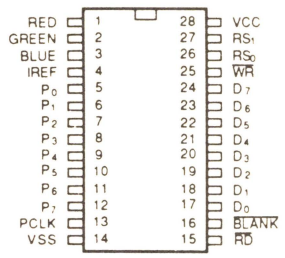
## DESCRIPTION

The IMS G176 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters (designed to drive into a double terminated 75 Ω line) and bi-directional microprocessor interface into a single 28 pin package.

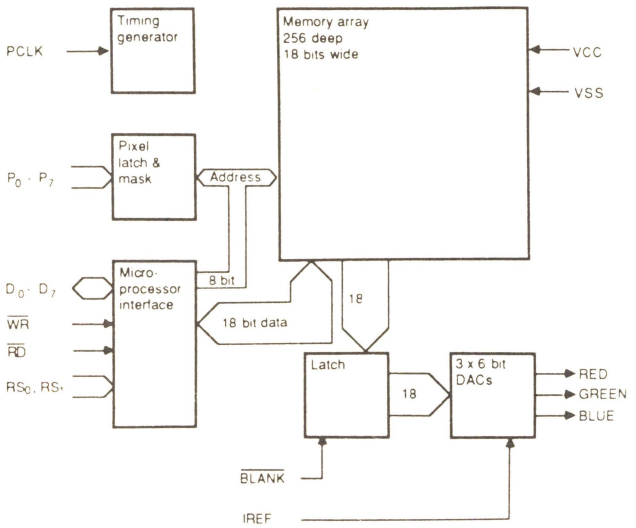
The IMS G176 is capable of displaying 256 colours, choosing from a total of 262,144 colours. This component replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

PIN CONFIGURATION




| PIN NAMES | |
|---|---|
| $P_0$ - $P_7$ | Pixel address inputs |
| $D_0$ - $D_7$ | Program data i/o's |
| $RS_0$, $RS_1$ | Register select |
| RED, GREEN, BLUE | Analogue video outputs |
| PCLK | Pixel clock |
| $\overline{WR}$ | Write enable |
| $\overline{RD}$ | Read enable |
| $\overline{BLANK}$ | Video blanking input |
| IREF | Reference current |
| VCC | +5 volt supply input |
| VSS | Ground |

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**INOVA Microelectronics Corporation**
2220 Martin Avenue • Santa Carla, CA 95050
(408) 980-0730 / FAX: (408) 980-1805 / TELEX: 510-601-8887

# S64K16

*64K × 16 SRAM*
*Advance Information*

# S32K8

*32K × 8 SRAM*
*Advance Information*

# S128K8

*128K × 8 SRAM*
*Advance Information*



| *Parameter* | *Unit* | *S128K8-45* | *S128K8-55* | *S128K8-70* | *S128K8-100* |
|---|---|---|---|---|---|
| Access Time | ns | 45 | 55 | 70 | 100 |
| Cycle Time | ns | 45 | 55 | 70 | 100 |
| Operating Current | mA | 125 | 100 | 70 | 70 |
| CMOS Standby Current | mA | 0.2 | 0.2 | 0.2 | 0.2 |

- **Fully static 128K × 8 SRAM**
- **Advanced 4-T CMOS technology**
- **JEDEC standard pinout**
- **2-volt data retention**
- **Military, industrial and commercial temperature ranges**
- **Processed in conformance to MIL-STD-883C**
- **Available in ceramic dip**

The INOVA S128K8 is a high performance 1M-bit Static Random Access Memory (SRAM), organized as 128K 8-bit bytes. This device is constructed by employing INROUTE™, INOVA's routing technology, an advance that turns VLSI devices into ULSI macrocircuits. Higher density means lower weight and higher reliability as compared to multiple lower density devices.

The INOVA S128K8 is manufactured using a high reliability 4-transistor cell CMOS process, which has low active and standby power characteristics. All inputs and outputs are fully TTL compatible. Operation is fully static; there is no need for extra control logic to generate clocks and timing strobes.

The package outline and pinout are JEDEC standard.

Every military grade device is processed and screened to the demanding requirements of MIL-STD-883C. INOVA's industrial and commercial grade devices differ from military grade only in burn-in time and electrical test temperature. All speed ranges except the 45ns speed are available in military grade.

INOVA offers a true packaging alternative to the larger capacity hybrid solutions by offering a monolithic device in a JEDEC standard pinout.

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## Absolute Maximum Ratings

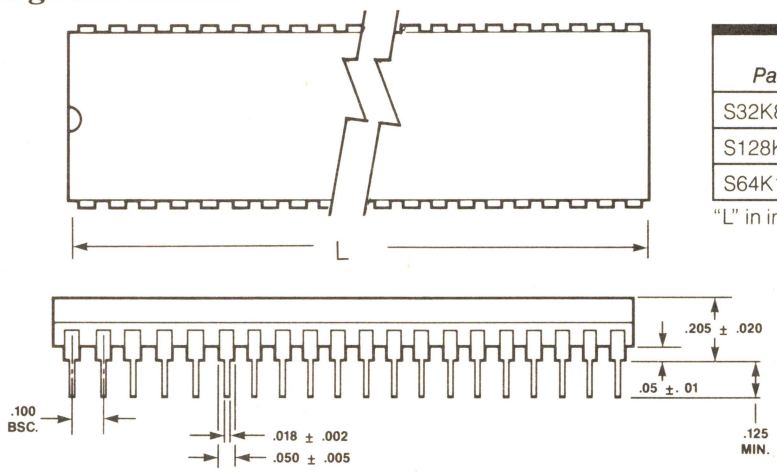
| | |
|---|---|
| Temperature under bias | −55°C to 125°C |
| Storage temperature | −65° to 150°C |
| Supply voltage(1) | −0.5V to 7.0V |
| Signal voltage on any pin | −0.5V to 7.0V |
| Power dissipation | 1 Watt |
| D.C. continuous output current per output | 20mA |

## Recommended Operating Conditions

| *Parameter* | *Symbol* | *Min.* | *Max.* | *Unit* |
|---|---|---|---|---|
| Supply Voltage (1) | $V_{CC}$ | 4.5 | 5.5 | V |
| Input HIGH Voltage | $V_{IH}$ | 2.2 | $V_{CC}$ + .5 | V |
| Input LOW Voltage | $V_{IL}$ | −0.5 | 0.8 | V |
| Operating temp. military | $T_A$ | −55 | 125 | °C |
| Operating temp. industrial | $T_A$ | −40 | 85 | °C |
| Operating temp. commercial | $T_A$ | 0 | 70 | °C |

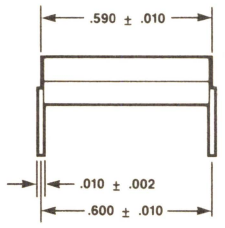
**Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Dimensions




| *Part* | *No. Pins* | *"L" Dimension* |
|---|---|---|
| S32K8 | 28 | 1.40 |
| S128K8 | 32 | 1.60 |
| S64K16 | 40 | 2.00 |

"L" in inches +/− .02 in.

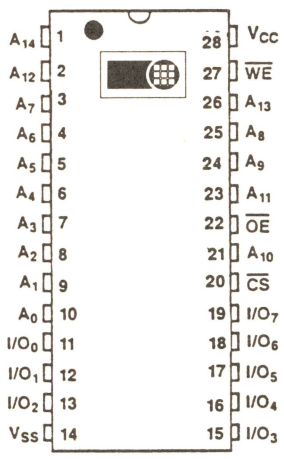



## Pinout Compatibility

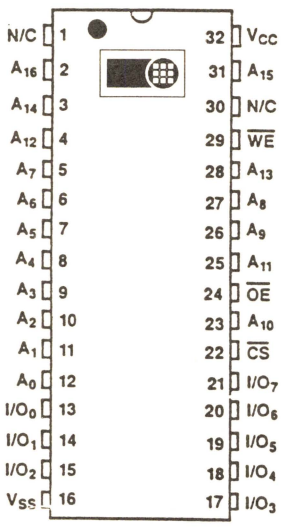
Inova has carefully configured their RAMs to conform to JEDEC standards, providing smooth upgrade paths to the next level of memory density. By following a few simple conventions the user can design one socket which accommodates both 32K × 8 and 128K × 8 devices.

The 28 pin JEDEC DIP and the 32 pin JEDEC DIP pinouts are closely aligned. In fact 27 of 28 pins are a perfect match and VCC can be connected between pin 30 (No connection) and pin 32 of the 32 pin package to supply power when the smaller 28 pin version is installed.

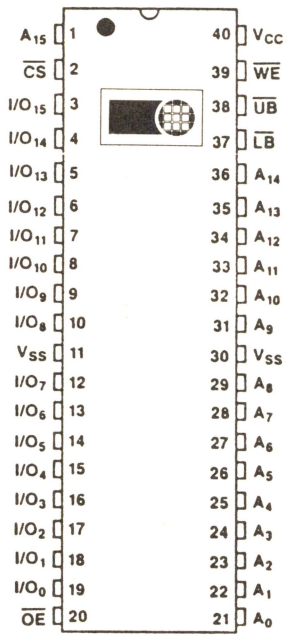
## Pinout




S32K8




S128K8




S64K16

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### A/D Converters

| Res. | P/N | (μsec) Conv.Time |
|---|---|---|
| 8* | ADC5120/30/40 | 2.5-6 |
| 12* | ADC574/674 | 12 & 20 |
| 12* | ADC5200 Series | 13-50 |
| 12* | ADC5610 Series | 13 |
| 12* | ADC5245/6 | 0.9 |
| 12* | ADC6002 | 0.5 |
| 12* | ADC84/85/87 | 8-10 |
| 12* | ADC6010 | 4 |
| 12 | ADC9003 | 1.0 (w/S/H) |
| 14 | ADC2735 | 6.8 |
| 14 | ADC2714 | 6.5-10 |
| 16 | ADC1140 | 35 |
| 16 | ADC1600-2 | 2 |
| 16 | ADC6001 | 35 |
| 16 | A8016 | 8-16 |
| 16* | ADC5290/1 | 35 |

### Video DACs

| Res. | P/N | Type |
|---|---|---|
| 4 | VDAC0405H/R | Video Freq. |
| 4 | VDAC3400S | Triple Output |
| 4 | RGBDAC3404A | w/LUT |
| 4 | RGBDAC3405S* | w/LUT |
| 4 | RGBDAC3408 | w/LUT |
| 4 | RGBDAC4E | w/LUT |
| 6 | VDAC0605H/R | Video Freq. |
| 8 | VDAC0805H/R | Video Freq. |
| 8 | VDAC8308TH | Video Freq. |
| 8 | VDAC1840/1842 | Video Freq. |
| 8 | VDAC1850/1852* | Video Freq. |
| 8 | RGBDAC3800* | Triple Output |
| 8 | VDAC888E | Triple Output |
| 8 | RGBDAC3808* | w/LUT |
| 8 | RGBDAC8E* | w/LUT |

### Data Acquisition System

| Res. | P/N | Type |
|---|---|---|
| 12 | DAS5712 | 40kHz |
| 14 | DAS5714 | 10kHz |
| 16 | DAC5716 | 2.5kHz |

### DC/DC Converters

| P/N | Output Pwr | Input Voltage | % Eff |
|---|---|---|---|
| PS2805* | 3.5W | +24±33 | 70 |
| PS2815* | 7.5W | +24±33 | 70 |
| PS6008* | 25W | +36±23 | 75 |
| PS6009* | 70W | +28±40 | 70 |
| PS9002 | 20W | +12±10 | 75 |
| A970* | 1W | +12±10 | 50 |
| A971* | 10W | +12±10 | 50 |
| A972* | 5W | +28±10 | 55 |

### Sample/Hold Amplifiers

| P/N | (μsec) Acq Time | (ns) Aperture |
|---|---|---|
| A880 | 1.4 | 100 |
| A882 | 6 | 25 |
| SH343/344* | 20 | 60 |
| SH346/347* | 2 | .4 |
| SH376* | 0.2 | 0.5 |
| SH377* | 0.1 | 0.5 |

### D/A Converters

| Res | P/N | Sett. Time Iout | Vout |
|---|---|---|---|
| 10 | DAC3003 | - | 2.5 |
| 10 | MDAC6003 | - | 30 |
| 12 | DACHK | 2 | 3 |
| 12 | DAC88 | - | 6 |
| 12 | DAC390 | - | 4 |
| 14 | 414-BIN | 2 | 100 |
| 16 | 416-BIN | 2 | 100 |
| 18 | 418-BCD | 2 | 100 |

### Voltage/Frequency Converters

| P/N | Freq. Range |
|---|---|
| A-8400 | 0 to 100K |
| A-8402 | 0 to 500K |
| A-8404 | 0 to 1M |
| VFC3802 | 20 to 2M |
| VFC3805 | 50 to 5M |
| VFC3810 | 100 to 10M |

* Military versions available.

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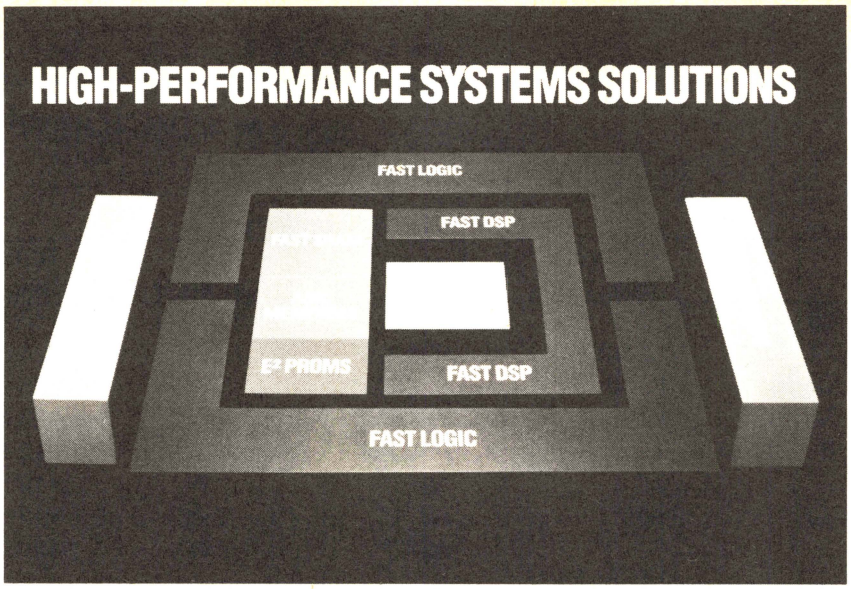


# IDT Products

A major revolution is taking place in the semiconductor industry. High-speed CMOS technology is rapidly displacing older NMOS and bipolar processes as the workhorse of the 80's and beyond. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Over the past five years, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest products of their type available in the industry today. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, our product strategy has been to apply the advantages of our CEMOS technology to produce integrated circuit elements required to implement high-performance digital systems. Many of our innovative product designs offer high levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards.

IDT is the leading U.S. supplier of high-speed CMOS static RAMs. High-performance logic, digital signal processing (DSP) circuits, MICROSLICE™ bit-slice microprocessor products, data conversion devices and modular subsystem assemblies complement these RAMs to provide high-speed CMOS solutions to a broad range of applications and systems.

Equal to developing state-of-the art technology and advanced, superior quality products, is IDT's commitment to providing the highest level of customer satisfaction in the industry. Our company is recognized for quick delivery and responsive, courteous service.

IDT's goal is to provide cost-effective circuits to create systems which are far superior to previous generations in performance, reliability, weight and size. We are dedicated to maintaining our leadership position as a state-of-the-art IC manufacturer, and will continue to hone our technological edge as well as develop an ever broader range of high-yield, high-performance products. Through these superior products and creative solutions to customer needs, IDT will play an increasingly important role as a major manufacturer in the era of high-speed CMOS.

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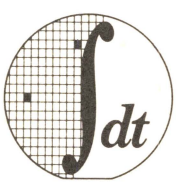


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# High-Speed CMOS MICROSLICE™ Products

- CMOS microprogrammable bit-slice microprocessor family
- CMOS Error Detection and Correction product family
- IDT49C000 products offer dramatically improved system performance through new innovative architectures
- IDT39C000 products are pin-compatible, performance-enhanced 2900 family replacements
- Meets or exceeds bipolar speeds and output drive at a small fraction of the power consumption
- Sequential letter suffix designates 20%-40% speed upgrade
- Instruction set/operation codes functionally identical to 2900 family

| | Part Number | Description | Replaces | Oper. Power (max) (mW) Com'l. | Mil. |
|---|---|---|---|---|---|
| MICROPROCESSORS | IDT39C01C<br>IDT39C01D<br>IDT39C01E | 4-Bit μP Slice | Am2901B,C; Am29C01C; CY7C901 | 157<br>184<br>210 | 192<br>220<br>247 |
| | IDT39C03A<br>IDT39C03B | 4-Bit μP Slice | Am2903 | 265 | 330 |
| | IDT39C203<br>IDT39C203A | 4-Bit μP Slice | Am29203 | 265 | 330 |
| | IDT49C401<br>IDT49C401A | 16-Bit μP Slice | IMI4X2901B | 660 | 825 |
| | IDT49C402<br>IDT49C402A | 16-Bit μP Slice, Quad 2901 with 8 additional destination functions and a 64 × 16 dual-port memory capacity | Four 2901s & One 2902; Am29C101; CY7C9101; WSI59016 | 945 | 1180 |
| | IDT49C403<br>IDT49C403A | 16-Bit μP Slice, Quad 2903/29203 with 64 × 16 register file, 4 Q-registers, word/BYTE control, BYTE swap, cascadable | Four 2903/29203s & One 2902 | 1180 | 1375 |
| | IDT49C404<br>**IDT49C404A** | 32-Bit μP Slice, 3-port device with 32-Bit ALU, 64 × 32 register file, cascadable funnel shifter, priority encoder, merge logic and mask generator | Two Am29334s & One Am29332 | **1600** | **2200** |
| SEQUENCERS | IDT39C09A<br>IDT39C09B | 4-Bit Sequencer | Am2909A; CY7C909 | 236 | 302 |
| | IDT39C10B<br>IDT39C10C | 12-Bit Sequencer with 33-Deep Stack | Am2910A; CY7C910 | 395 | 495 |
| | IDT39C11A<br>IDT39C11B | 4-Bit Sequencer | Am2911A; CY7C911 | 236 | 302 |
| | IDT49C410<br>IDT49C410A | 16-Bit Sequencer with 33-Deep Stack | Am2910; Am29C10; CY7C910 | 395 | 495 |
| | IDT49C411 | 20-Bit Interruptable Sequencer | Am29331; TI74AS8838 | TBD | TBD |
| REG. FILES | IDT39C705A<br>IDT39C705B | 16 × 4 Register File Extension | Am29705A | 210 | 275 |
| | IDT39C707<br>IDT39C707A | 16 × 4 Register File Extension | Am29707 | 210 | 275 |
| EDC | IDT39C60<br>IDT39C60-1<br>IDT39C60A | 16-Bit Cascadable Error Detection Correction Unit | Am2960,-1,A; N2960; MC74F2960,-1,A | 446 | 550 |
| | IDT49C460<br>IDT49C460A<br>**IDT49C460B** | 32-Bit Cascadable Error Detection Correction Unit | DP8402; 74AS632; ALS632 | 500 | 690 |
| OTHER | IDT39C02A | Carry Lookahead Generator | Am2902A | 30 | 30 |
| | IDT49C25 | Clock Generator | Am2925 | 30 | 30 |

Shaded area indicates new product. **Boldface** indicates improved feature.

# High-Speed CMOS Static RAMs

- Extremely fast access times
- Low power consumption
- 2V data retention battery backup on all low-power devices
- Three-state outputs
- 'M' type ceramic RAM modules are built with monolithic RAMs in LCC packages surface mounted onto multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process
- 'MP' type commercial plastic modules are built using IDT monolithic RAMs in SMD plastic packages, surface mounted onto epoxy laminate (FR4) substrates

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (typical) Oper. (mW) | Power (typical) Standby ($\mu$W) |
|---|---|---|---|---|---|
| IDT100490 | 64K (64K × 1) with ECL 100K compatible I/O | — | 15 | 320 | — |
| IDT6116 | 16K (2K × 8) | 35 | 25 | **160** | **20** |
| IDT6120 | 16K (2K × 8) with high-speed chip select | 22 (chip select access time) | 18 | **160** | — |
| IDT61298 | 256K (64K × 4) with output enable $\overline{(OE)}$ for added system flexibility | 35 | 25 | 350 | 100 |
| IDT6167 | 16K (16K × 1) | **15** | **12** | **150** | 10 |
| IDT6168 | 16K (4K × 4) | **15** | 15 | 225 | 10 |
| IDT6169 | 16K (4K × 4) with high-speed chip select | 15 (chip select access time) | 12 | 225 | — |
| IDT6198 | 64K (16K × 4) with output enable $\overline{(OE)}$ for added system flexibility | 20 | 15 | 300 | 30 |
| IDT71256 | 256K (32K × 8) | 45 | 35 | **250** | **15** |
| IDT71257 | 256K (256K × 1) | **35** | **25** | 350 | 100 |
| IDT71258 | 256K (64K × 4) | **35** | **25** | 350 | 100 |
| IDT71281 | 256K (64K × 4) with separate data inputs and outputs; outputs track inputs during write mode | 35 | 25 | 350 | 100 |
| IDT71282 | 256K (64K × 4) with separate data inputs and outputs; outputs in high impedance state during write mode | 35 | 25 | 350 | 100 |
| IDT71501 | 64K (64K × 1) synchronous RAM; all inputs and outputs latched | 45 | 35 | 385 | — |
| IDT71502 | 64K (4K × 16) registered RAM for writable control store use; has on-board serial load, parity, breakpoint and trace logic | 45 | 35 | 350 | 30 |
| IDT7164 | 64K (8K × 8) | 35 | 30 | **250** | 30 |
| IDT7165 | 64K (8K × 8) with asynchronous clear and high-speed chip select | 45 | 30 | **250** | 30 |
| IDT71C65 | 64K (8K × 8) with CMOS compatible I/O | 35 | 30 | 250 | 30 |
| IDT71681 | 16K (4K × 4) with separate data inputs and outputs; outputs track inputs during write mode | 25 | 20 | 225 | 10 |
| IDT71682 | 16K (4K × 4) with separate data inputs and outputs; outputs in high impedance state during write mode | 25 | 20 | 225 | 10 |
| IDT7174 | 64K (8K × 8) with cache address comparator, asynchronous clear and high-speed chip select | 45 | 35 | **250** | — |
| IDT7186 | 64K (4K × 16) | 55 | 45 | 300 | 30 |
| IDT7187 | 64K (64K × 1) | **25** | **15** | 250 | 30 |
| IDT7188 | 64K (16K × 4) | **20** | **15** | 300 | 30 |
| IDT7198 | 64K (16K × 4) output enable $\overline{(OE)}$ and second chip select $\overline{(CS_2)}$ for added system flexibility and memory control | **20** | **15** | 300 | 30 |
| IDT71981 | 64K (16K × 4) with separate data inputs and outputs; outputs track inputs during write mode | **20** | **15** | 300 | 30 |

Shaded area indicates new product. **Boldface** indicates improved feature.

*CONTINUED*



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# High-Speed CMOS Static RAMs (continued)

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (max) Oper. (mW) | Power (max) Standby (mW) |
|---|---|---|---|---|---|
| IDT71982 | 64K (16K × 4) with separate data inputs and outputs; outputs in high impedance state during write mode | **20** | **15** | 300 | 30 |
| IDT7MB6042 | 8K × 112 high-speed writable control store with SPC™ | — | TBD | TBD | TBD |
| IDT7MB624 | 1 Megabit (64K × 16, 128K × 8, 256K × 4) plastic RAM module – customer configurable organization | — | 30 | 10725 | 1320 |
| IDT7MC156 | 256K (256K × 1) static RAM module (ceramic SIP) | — | 30 | 1485 | 330 |
| IDT7MC4001 | 1 Megabit (1024K × 1) static RAM module (ceramic SIP) | — | TBD | 1348 | 330 |
| IDT7MC4032 | 512K (16K × 32) RAM module with separate I/O (ceramic dual SIP) | — | 30 | 5940 | 660 |
| IDT7MP156 | 256K (256K × 1) plastic SIP RAM module | — | 30 | 1375 | 330 |
| IDT7MP4008 | 4 Megabit (512K × 8) static RAM module (plastic SIP) | — | 45 | 2585 | 380 |
| IDT7MP456 | 256K (64K × 4) plastic SIP RAM module | — | 30 | 1705 | 330 |
| IDT7MP6025 | 512K (64K × 8) registered static RAM module | — | 25MHz | TBD | TBD |
| IDT7M4016 | 4 Megabit (256K × 16) RAM module | — | 45 | TBD | TBD |
| IDT7M4017 | 2 Megabit (64K × 32) RAM module | 60 | 45 | TBD | TBD |
| IDT7M6001 | 32K × 20 double buffered RAM module with registered, multiplexed address | 20MHz | 25MHz | TBD | TBD |
| IDT7M6026 | 2 Megabit (64K × 32) registered and buffered RAM module | 60 | 45 | TBD | TBD |
| IDT7M6032 | 16K × 32 high-speed writable control store with SPC™ | TBD | TBD | TBD | TBD |
| IDT7M624 | 1 Megabit (64K × 16, 128K × 8, 256K × 4) RAM module – customer configurable organization | 35 | 30 | 10725 | 1320 |
| IDT7M656 | 256K (16K × 16, 32K × 8, 64K × 4) RAM module – customer configurable organization | **30** | **20** | 7040 | 85 |
| IDT7M812 | 512K (64K × 8) RAM module offering maximum addressable memory required by 8-bit MPs | 35 | 30 | 5280 | 880 |
| IDT7M824 | 1 Megabit (128K × 8) RAM module with registered buffered/latched addresses and I/Os | 60 | **45** | 2640 | 935 |
| IDT7M856 | 256K (32K × 8) RAM module with monolithic pinout | 50 | 40 | 2090 | 440 |
| IDT7M912 | 512K (64K × 9) RAM module offering maximum addressable memory required by 8-bit MPs | 35 | 30 | 5940 | 990 |
| IDT8MP612 | 512K (32K × 16) plastic SIP RAM module | — | **45** | 1650 | 165 |
| IDT8MP624 | 1 Megabit (64K × 16) plastic SIP RAM module | — | **45** | 1925 | 440 |
| IDT8MP628 | 128K (8K × 16) plastic SIP RAM module | — | 35 | 1650 | 165 |
| IDT8MP656 | 256K (16K × 16) plastic SIP RAM module | — | **40** | 1870 | 330 |
| IDT8MP824 | 1 Megabit (128K × 8) plastic SIP RAM module | — | **45** | 1210 | 440 |
| IDT8M612 | 512K (32K × 16) RAM module with monolithic pinout | 60 | **45** | 1650 | 275 |
| IDT8M624 | 1 Megabit (64K × 16) RAM module with monolithic pinout | **60** | **45** | 1925 | 495 |
| IDT8M628 | 128K (8K × 16) RAM module with monolithic pinout | 50 | 35 | 1650 | 220 |
| IDT8M656 | 256K (16K × 16) RAM module with monolithic pinout | 60 | **40** | 1870 | 440 |
| IDT8M824 | 1 Megabit (128K × 8) RAM module with monolithic pinout | 60 | **45** | 1210 | 550 |
| IDT8M856 | 256K (32K × 8) RAM module with monolithic pinout (low-power) | 55 | 45 | 880 | 66 |

Shaded area indicates new product. **Boldface** indicates improved feature.

# High-Speed CMOS Dual-Port RAMs

- High-speed, low-power
- Independent read or write access to any memory location from either port
- Each port has separate controls, address and I/O
- On-chip port arbitration logic
- Fully asynchronous operation from either port
- $\overline{INT}$ and $\overline{BUSY}$ flags ($\overline{BUSY}$ only in IDT7132/7142)
- Automatic power-down feature controlled by $\overline{CE}$
- 2V data retention battery back-up on all low-power devices
- Dual-port RAM modules built with IDT monolithic dual-port RAMs in LCC packages, surface mounted to multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process

| Part Number | Description | Max. Speed (ns) Mil. | Com'l. | Power (typical) Oper. (mW) | Standby (mW) |
|---|---|---|---|---|---|
| IDT7130 | 8K (1K × 8) replaces Synertek SY2130 | **45** | **35** | 325 | 1 |
| IDT7132 | 16K (2K × 8) fastest available speeds in this industry standard product; now multiple sourced | 45 | 35 | 325 | 1 |
| IDT71321 | 16K (2K × 8) high-speed dual-port with interrupt output (MASTER) | 45 | 35 | 325 | 1 |
| IDT71322 | 16K (2K × 8) with Semaphore | **45** | 45 | 500 | 1 |
| IDT7133 | 32K (2K × 16) | 70 | 55 | 375 | 1 |
| IDT7134 | 32K (4K × 8) high-speed operation in system where on-chip arbitration is not needed | **45** | 45 | 500 | 1 |
| IDT71342 | 32K (4K × 8) with Semaphore | **45** | 45 | 500 | 1 |
| IDT7140 | 8K (1K × 8) functions as slave with IDT7130 to provide 16-bit words or wider; pin compatible with IDT7130 | **45** | **35** | 325 | 1 |
| IDT7142 | 16K (2K × 8) functions as slave with IDT7132 to provide 16-bit words or wider; pin compatible with IDT7132 | 45 | 35 | 325 | 1 |
| IDT71421 | 16K (2K × 8) functions as slave with IDT71321 to provide 16-bit words or wider; pin compatible with IDT71321 | 45 | 35 | 325 | 1 |
| IDT7143 | 32K (2K × 16) functions as slave with IDT7133 to provide 32-bit words or wider | 70 | 55 | 375 | 1 |
| IDT7M134 | 64K (8K × 8) dual-port RAM module | **60** | **45** | 950 | 20 |
| IDT7M135 | 128K (16K × 8) dual-port RAM module | **60** | **45** | 1600 | 50 |
| IDT7M137 | 256K (32K × 8) dual-port RAM module where on-chip arbitration is not needed | **60** | **55** | 1800 | 60 |
| IDT7M144 | 64K (8K × 8) functions as slave with IDT7M134 to provide 16-bit words or wider; pin compatible with IDT7M134 | **60** | **45** | 950 | 20 |
| IDT7M145 | 128K (16K × 8) functions as slave with IDT7M135 to provide 16-bit words or wider; pin compatible with IDT7M135 | **60** | **45** | 1600 | 50 |

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# High-Speed CMOS FIFOs

- Extremely fast access and cycle times
- Low-power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Single read/write line operation
- Empty, full and half-full flags indicate status
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Auto retransmit capability
- FIFO modules are built with IDT monolithic FIFOs in LCC packages, surface mounted to multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (typical) Oper. (mW) | Power (typical) Standby (mW) |
|---|---|---|---|---|---|
| IDT7200 | 256 × 9 | 30 | 25 | 250 | 25 |
| IDT7201 | 512 × 9 replaces Mostek MK4501 | 40 | 35 | 250 | 25 |
| IDT7201A | 512 × 9 Half-Full Flag | **30** | **25** | 250 | 25 |
| IDT7202 | 1024 × 9 | 40 | 35 | 250 | 25 |
| IDT7202A | 1024 × 9 Half-Full Flag | 40 | 35 | 250 | 25 |
| IDT7203 | 2K × 9 Half-Full Flag | 40 | 35 | 375 | 50 |
| IDT7204 | 4K × 9 Half-Full Flag, largest monolithic FIFO available | 40 | 35 | 375 | 40 |
| IDT72103 | 2K × 9 parallel input/output, serial input/output – 40MHz | 50 | 50 | 375 | 40 |
| IDT72104 | 4K × 9 parallel input/output, serial input/output – 40MHz | 50 | 50 | 375 | 40 |
| IDT72401 | 64 × 4 replaces MMI 67401 | **35MHz** | **45MHz** | 200 | 20 |
| IDT72402 | 64 × 5 replaces MMI 67402 | **35MHz** | **45MHz** | 200 | 20 |
| IDT72403 | 64 × 4 output enable | **35MHz** | **45MHz** | 200 | 20 |
| IDT72404 | 64 × 5 output enable | **35MHz** | **45MHz** | 200 | 20 |
| IDT72413 | 64 × 5 replaces MMI 67413 output enable, Half-Full, Almost-Full/ Empty Flags | **35MHz** | **45MHz** | 200 | 20 |
| IDT7M203 | 2K × 9 FIFO module using four IDT7201s | 50 | 40 | 630 | 100 |
| IDT7M204 | 4K × 9 FIFO module using four IDT7202s | 50 | 40 | 630 | 100 |
| IDT7M205 | 8K × 9 FIFO module using four IDT7203s | 60 | 55 | 1400 | 400 |
| IDT7M206 | 16K × 9 FIFO module using four IDT7204s | 60 | 55 | 1400 | 400 |

Integrated Device Technology

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# High-Speed CMOS Parallel Multiplier-Accumulators

- High speed, low power
- Parallel multiplier-accumulators with selectable accumulation, rounding and preloading
- Extended product output for multiple accumulations
- Preload function allows output register to be preset
- All devices perform subtraction and double precision addition and multiplication
- Inputs and outputs directly TTL-compatible

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (typical) Oper. (mW) | Power (typical) Standby (μW) |
|---|---|---|---|---|---|
| IDT7209 | 12 × 12–pin and functionally compatible with TRW TDC1009J | 40 | 35 | 200 | 500 |
| IDT7210 | 16 × 16–with 35-bit output; pin and functionally compatible with TRW TDC1010J | 30 | 25 | 220 | 550 |
| IDT7243 | 16 × 16–with 19-bit output; pin and functionally compatible with TRW TDC1043 | 55 | 45 | 200 | 500 |

# High-Speed CMOS Parallel Multipliers

- High-speed, low-power
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Inputs and outputs directly TTL-compatible
- Three-state output controls and separate register enables

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (typical) Oper. (mW) | Power (typical) Standby (μW) |
|---|---|---|---|---|---|
| IDT7212 | 12 × 12–pin and functionally compatible with TRW MPY012H | 40 | 30 | 150 | 500 |
| IDT7213 | 12 × 12–with single clock architecture | 40 | 30 | 150 | 500 |
| IDT7216 | 16 × 16–pin and functionally compatible with TRW MPY016H/K and AMD Am29516 | 25 | 20 | 220 | 500 |
| IDT7217 | 16 × 16–with single clock architecture; pin and functionally compatible with AMD Am29517 | 25 | 20 | 220 | 500 |

# High-Speed CMOS Floating-Point Products

- Advanced CEMOS technology
- Full IEEE standard 754 conformance
- Single 5V supply
- Full 32-bit and 64-bit multiply and ALU operations
- 144-Pin Grid Array
- Low-power – 500mW per device

| Part Number | Description | Max. Speed | Operating Power typical (mW) |
|---|---|---|---|
| IDT721264 | 32-/64-Bit Multiplier–pin and functionally compatible withWeitek WTL1264 | Single precision 16.7 MFLOPs (60ns) Double precision 8 MFLOPs (120ns) | 500 |
| IDT721265 | 32-/64-Bit ALU–pin and functionally compatible with Weitek WTL1265 | Single precision 16.7 MFLOPs (60ns) Double precision 16.7 MFLOPs (60ns) | 500 |

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# High-Speed CMOS Data Conversion Products

- High speed, low power
- Available in military and commercial temperature ranges
- Produced with advanced CEMOS high-performance technology

**VIDEO DACs**

- IDT75C18 is pin and function compatible with TRW 1018 with half the power consumption
- IDT75C19 is world's first CMOS 9-bit Video DAC
- IDT75C458 PaletteDAC™ is pin and function compatible with Brooktree BT458
- IDT7MB5038 is a triple 8-bit, 125MHz module with on-board voltage reference

**FLASH A/D CONVERTERS**

- IDT75C48 is pin and function compatible with TRW 1048 with half the power consumption, on-chip Error Detection and Correction, extended analog input range and improved output characteristics
- IDT75C58 has enhanced features such as overflow output and three-state control which allows stacking two devices for 9-bit resolution
- IDT7M5048 is a complete Flash ADC module product with input buffer amplifier, reference voltage generator and optimized layout and decoupling
- IDT7M5049 is a complete 9-bit ADC module using two IDT75C58 devices

| Part Number | Description | Replaces | Power Oper. (mW) |
|---|---|---|---|
| IDT75C18 | 8-bit, 125MHz Video DAC with ECL inputs | TDC1018 | 400 |
| IDT75C19 | World's first 9-bit, 125MHz Video DAC | — | 400 |
| IDT75C458 | Triple 8-bit, 125MHz PaletteDAC™ | BT458 | 1000 |
| IDT75C48 | 8-bit, 20MHz Flash ADC | TDC1048 | 500 |
| IDT75C58 | 8-bit, 20MHz Flash ADC with Overflow output | — | 500 |
| IDT7MB5038 | Triple 8-bit, 125MHz Video DAC Module | — | 1500 |
| IDT7M5048 | Complete Flash Module using IDT75C48 | — | 800 |
| IDT7M5049 | 9-bit Flash Module using two IDT75C58s | — | 1200 |

# High-Speed CMOS E² PROMs

- Fast access times
- Internal address and data input latches
- Serial access versions with SPC™ (IDT78C18A, IDT78C68A, IDT78C258A)
- On-chip timer, latches, charge pump
- Write protection circuitry
- 5 volt operation
- $\overline{\text{DATA}}$ polling

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (typical) Oper. (mW) | Power (typical) Standby (mW) |
|---|---|---|---|---|---|
| IDT78C16A | 2K × 8 E²PROM | 90 | 70 | 500 | 4.5 |
| IDT78C18A | 2K × 8 E²PROM with Serial Protocol Channel (SPC™) | 90 | 70 | 500 | 4.5 |
| IDT78C256A | 32K × 8 E²PROM | 70 | 55 | — | — |
| IDT78C258A | 32K × 8 E²PROM with Serial Protocol Channel (SPC™) | 70 | 55 | — | — |
| IDT78C64A | 8K × 8 E²PROM | 55 | 45 | — | — |
| IDT78C68A | 8K × 8 E²PROM with Serial Protocol Channel (SPC™) | 55 | 45 | — | — |
| IDT7M7864 | 8K × 8 E²PROM module with JEDEC E²PROM pinout | 85 | 70 | — | — |

Shaded area indicates new product. **Boldface** indicates improved feature.

# High-Speed CMOS Logic Products (continued)

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (typical) Oper. (mW) | Power (typical) Standby (μW) |
|---|---|---|---|---|---|
| IDT54/74FCT640A | Octal Bidirectional Transceiver | 5.3 | 5.0 | 10.0 | 5.0 |
| IDT54/74FCT645A | Octal Bidirectional Transceiver | 4.9 | 4.6 | 10.0 | 5.0 |
| IDT54/74FCT646A | Octal Non-inverting Registered Transceiver | 7.7 | 6.3 | 10.0 | 5.0 |
| IDT54/74FCT648A | Octal Inverting Registered Transceiver | 7.7 | 6.3 | 10.0 | 5.0 |
| IDT54/74FCT651A | Octal Non-inverting Registered Transceiver | 7.7 | 6.3 | 10.0 | 5.0 |
| IDT54/74FCT652A | Octal Inverting Registered Transceiver | 7.7 | 6.3 | 10.0 | 5.0 |
| IDT54/74FCT821A | 10-Bit Non-inverting Register | 12.0 | 12.0 | 10.0 | 5.0 |
| IDT54/74FCT822A | 10-Bit Inverting Register | 12.0 | 12.0 | 10.0 | 5.0 |
| IDT54/74FCT823A | 9-Bit Non-inverting Register | 12.0 | 12.0 | 10.0 | 5.0 |
| IDT54/74FCT824A | 9-Bit Inverting Register | 12.0 | 12.0 | 10.0 | 5.0 |
| IDT54/74FCT825A | 8-Bit Non-inverting Register | 12.0 | 12.0 | 10.0 | 5.0 |
| IDT54/74FCT826A | 8-Bit Inverting Register | 12.0 | 12.0 | 10.0 | 5.0 |
| IDT54/74FCT827A | 10-Bit Non-inverting Buffer | 10.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT828A | 10-Bit Inverting Buffer | 9.5 | 7.5 | 10.0 | 5.0 |
| IDT54/74FCT833A | 8-Bit Transceiver w/Parity | 14.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT834A | 8-Bit Transceiver w/Parity | 14.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT841A | 10-Bit Non-inverting Latch | 11.0 | 9.5 | 10.0 | 5.0 |
| IDT54/74FCT842A | 10-Bit Inverting Latch | 11.0 | 9.5 | 10.0 | 5.0 |
| IDT54/74FCT843A | 9-Bit Non-inverting Latch | 11.0 | 9.5 | 10.0 | 5.0 |
| IDT54/74FCT844A | 9-Bit Inverting Latch | 11.0 | 9.5 | 10.0 | 5.0 |
| IDT54/74FCT845A | 8-Bit Non-inverting Latch | 11.0 | 9.5 | 10.0 | 5.0 |
| IDT54/74FCT846A | 8-Bit Inverting Latch | 11.0 | 9.5 | 10.0 | 5.0 |
| IDT54/74FCT853A | 8-Bit Transceiver w/Parity | 14.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT854A | 8-Bit Transceiver w/Parity | 14.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT861A | 10-Bit Non-inverting Transceiver | 10.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT862A | 10-Bit Inverting Transceiver | 10.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT863A | 9-Bit Non-inverting Transceiver | 10.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT864A | 9-Bit Inverting Transceiver | 10.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT138 | 1-of-8 Decoder | 12.0 | 9.0 | 10.0 | 5.0 |
| IDT54/74FCT139 | Dual 1-of-4 Decoder | 12.0 | 9.0 | 10.0 | 5.0 |
| IDT54/74FCT161 | Synchronous Binary Counter | 11.5 | 11.0 | 10.0 | 5.0 |
| IDT54/74FCT163 | Synchronous Binary Counter | 11.5 | 11.0 | 10.0 | 5.0 |
| IDT54/74FCT182 | Carry Lookahead Generator | 11.5 | 9.0 | 10.0 | 5.0 |
| IDT54/74FCT191 | Up/Down Binary Counter | 16.0 | 12.0 | 10.0 | 5.0 |
| IDT54/74FCT193 | Up/Down Binary Counter | 10.5 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT240 | Octal Buffer | 9.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT244 | Octal Buffer | 7.0 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT245 | Octal Bidirectional Transceiver | 7.5 | 7.0 | 10.0 | 5.0 |
| IDT54/74FCT273 | Octal D Flip-Flop | 15.0 | 13.0 | 10.0 | 5.0 |
| IDT54/74FCT299 | Octal Universal Shift Register | 16.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT373 | Octal Transparent Latch | 8.5 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT374 | Octal D Flip-Flop | 11.0 | 10.0 | 10.0 | 5.0 |

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# High-Speed CMOS Logic Products

- FCTXXXA devices 35%-50% faster than FAST™ with equivalent output drive but at dramatically lower CMOS power over full temperature and voltage supply extremes
- FCT devices same speed and output drive as FAST™, but at dramatically lower CMOS power
- 54/74FCT8XXA devices same speed and output drive as 29800, but at dramatically lower CMOS power
- 54/74FCT8XXB devices 32%-38% faster than 29800 with equivalent output drive, but at dramatically lower CMOS power
- Both CMOS and TTL output compatible (eliminates need for pull-up resistors when driving CMOS static RAMs)
- Substantially lower input current levels than FAST™ or ALS (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Pin-compatible with industry standard MSI logic
- Devices formerly designated 39C8XX are now designated 54/74FCT8XXA or 29FCTXX

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (typical) Oper. (mW) | Power (typical) Standby (μW) |
|---|---|---|---|---|---|
| IDT29FCT52A | Octal Registered Transceiver | 7.2 | 6.5 | 10.0 | 5.0 |
| IDT29FCT53A | Octal Registered Transceiver | 7.2 | 6.5 | 10.0 | 5.0 |
| IDT29FCT52 | Octal Registered Transceiver | 11.0 | 10.0 | 10.0 | 5.0 |
| IDT29FCT53 | Octal Registered Transceiver | 11.0 | 10.0 | 10.0 | 5.0 |
| IDT29FCT520A | Multilevel Pipeline Register | 16.0 | 14.0 | 10.0 | 5.0 |
| IDT29FCT521A | Multilevel Pipeline Register | 16.0 | 14.0 | 10.0 | 5.0 |
| IDT49FCT601 | 16-Bit Bidirectional Latch w/Byte-Swap | — | — | 20.0 | 10.0 |
| IDT49FCT618 | 16-Bit Register with SPC™ | 11.0 | 10.0 | 20.0 | 5.0 |
| IDT49FCT661 | 16-Bit Synchronous Binary Counter | — | — | 20.0 | 10.0 |
| IDT49FCT818 | Octal Register with SPC™ | 11.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT138A | 1-of-8 Decoder | 7.8 | 5.8 | 10.0 | 5.0 |
| IDT54/74FCT139A | Dual 1-of-4 Decoder | 7.8 | 5.9 | 10.0 | 5.0 |
| IDT54/74FCT161A | Synchronous Binary Counter | 7.5 | 7.2 | 10.0 | 5.0 |
| IDT54/74FCT163A | Synchronous Binary Counter | 7.5 | 7.2 | 10.0 | 5.0 |
| IDT54/74FCT182A | Carry Lookahead Generator | — | — | 10.0 | 5.0 |
| IDT54/74FCT191A | Up/Down Binary Counter | 10.5 | 7.8 | 10.0 | 5.0 |
| IDT54/74FCT193A | Up/Down Binary Counter | 6.9 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT240A | Octal Buffer | 5.1 | 4.8 | 10.0 | 5.0 |
| IDT54/74FCT244A | Octal Buffer | 4.6 | 4.3 | 10.0 | 5.0 |
| IDT54/74FCT245A | Octal Bidirectional Transceiver | 4.9 | 4.6 | 10.0 | 5.0 |
| IDT54/74FCT273A | Octal D Flip-Flop | 8.3 | 7.2 | 10.0 | 5.0 |
| IDT54/74FCT299A | Octal Universal Shift Register | 9.5 | 7.2 | 10.0 | 5.0 |
| IDT54/74FCT373A | Octal Transparent Latch | 5.6 | 5.2 | 10.0 | 5.0 |
| IDT54/74FCT374A | Octal D Flip-Flop | 7.2 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT377A | Octal D Flip-Flop | 8.3 | 7.2 | 10.0 | 5.0 |
| IDT54/74FCT399A | Quad Dual-Port Register | 7.2 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT521A | 8-Bit Comparator | 9.5 | 7.2 | 10.0 | 5.0 |
| IDT54/74FCT533A | Octal Transparent Latch | 5.6 | 5.2 | 10.0 | 5.0 |
| IDT54/74FCT534A | Octal D Flip-Flop | 7.2 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT540A | Octal Inverting Buffer | — | — | 10.0 | 5.0 |
| IDT54/74FCT541A | Octal Non-inverting Buffer | — | — | 10.0 | 5.0 |
| IDT54/74FCT543A | Octal Non-inverting Latched Transceiver | 7.7 | 6.3 | 10.0 | 5.0 |
| IDT54/74FCT573A | Octal Transparent Latch | 5.6 | 5.2 | 10.0 | 5.0 |
| IDT54/74FCT574A | Octal D Register | 7.2 | 6.5 | 10.0 | 5.0 |

Shaded area indicates new product. **Boldface** indicates improved feature.

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# High-Speed CMOS Logic Products (continued)

| Part Number | Description | Max. Speed (ns) Mil. | Max. Speed (ns) Com'l. | Power (typical) Oper. (mW) | Power (typical) Standby (μW) |
|---|---|---|---|---|---|
| IDT54/74FCT377 | Octal D Flip-Flop | 15.0 | 13.0 | 10.0 | 5.0 |
| IDT54/74FCT399 | Quad Dual-Port Register | 11.5 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT521 | 8-Bit Comparator | 15.0 | 11.0 | 10.0 | 5.0 |
| IDT54/74FCT533 | Octal Transparent Latch | 12.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT534 | Octal D Flip-Flop | 11.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT540 | Octal Inverting Buffer | 9.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT541 | Octal Non-inverting Buffer | 9.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT543 | Octal Non-inverting Latched Transceiver | 9.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT573 | Octal Transparent Latch | 8.5 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT574 | Octal D Register | 11.0 | 10.0 | 10.0 | 5.0 |
| IDT54/74FCT640 | Octal Bidirectional Transceiver | 8.0 | 7.0 | 10.0 | 5.0 |
| IDT54/74FCT645 | Octal Bidirectional Transceiver | 11.0 | 9.5 | 10.0 | 5.0 |
| IDT54/74FCT646 | Octal Non-inverting Registered Transceiver | 11.0 | 9.0 | 10.0 | 5.0 |
| IDT54/74FCT648 | Octal Inverting Registered Transceiver | 9.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT651 | Octal Non-inverting Registered Transceiver | 11.0 | 9.0 | 10.0 | 5.0 |
| IDT54/74FCT652 | Octal Inverting Registered Transceiver | 9.0 | 8.0 | 10.0 | 5.0 |
| IDT54/74FCT827 | 10-Bit Non-inverting Buffer | 5.0 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT828 | 10-Bit Inverting Buffer | 6.5 | 5.5 | 10.0 | 5.0 |
| IDT54/74FCT821B | 10-Bit Non-inverting Register | 8.5 | 7.5 | 10.0 | 5.0 |
| IDT54/74FCT822B | 10-Bit Inverting Register | 8.5 | 7.5 | 10.0 | 5.0 |
| IDT54/74FCT823B | 9-Bit Non-inverting Register | 8.5 | 7.5 | 10.0 | 5.0 |
| IDT54/74FCT824B | 9-Bit Inverting Register | 8.5 | 7.5 | 10.0 | 5.0 |
| IDT54/74FCT825B | 8-Bit Non-inverting Register | 8.5 | 7.5 | 10.0 | 5.0 |
| IDT54/74FCT826B | 8-Bit Inverting Register | 8.5 | 7.5 | 10.0 | 5.0 |
| IDT54/74FCT827B | 10-Bit Non-inverting Buffer | 6.5 | 5.0 | 10.0 | 5.0 |
| IDT54/74FCT828B | 10-Bit Inverting Buffer | 6.5 | 5.0 | 10.0 | 5.0 |
| IDT54/74FCT833B | 8-Bit Transceiver w/Parity | 10.0 | 7.0 | 10.0 | 5.0 |
| IDT54/74FCT834B | 8-Bit Transceiver w/Parity | 10.0 | 7.0 | 10.0 | 5.0 |
| IDT54/74FCT841B | 10-Bit Non-inverting Latch | 7.5 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT842B | 10-Bit Inverting Latch | 7.5 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT843B | 9-Bit Non-inverting Latch | 7.5 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT844B | 9-Bit Inverting Latch | 7.5 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT845B | 8-Bit Non-inverting Latch | 7.5 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT846B | 8-Bit Inverting Latch | 7.5 | 6.5 | 10.0 | 5.0 |
| IDT54/74FCT853B | 8-Bit Transceiver w/Parity | 10.0 | 7.0 | 10.0 | 5.0 |
| IDT54/74FCT854B | 8-Bit Transceiver w/Parity | 10.0 | 7.0 | 10.0 | 5.0 |
| IDT54/74FCT861B | 10-Bit Non-inverting Transceiver | 6.5 | 5.0 | 10.0 | 5.0 |
| IDT54/74FCT862B | 10-Bit Inverting Transceiver | 6.5 | 5.0 | 10.0 | 5.0 |
| IDT54/74FCT863B | 9-Bit Non-inverting Transceiver | 6.5 | 5.0 | 10.0 | 5.0 |
| IDT54/74FCT864B | 9-Bit Inverting Transceiver | 6.5 | 5.0 | 10.0 | 5.0 |
| IDT54AHCT138 | 1-of-8 Decoder | 27.0 | — | 3.5 | 5.0 |
| IDT54AHCT139 | Dual 1-of-4 Decoder | 25.0 | — | 3.5 | 5.0 |

Shaded area indicates new product. **Boldface** indicates improved feature.

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# High-Speed CMOS Logic Products (continued)

| Part Number | Description | Max. Speed (ns) Mil. | Com'l. | Power (typical) Oper. (mW) | Standby (μW) |
|---|---|---|---|---|---|
| IDT54AHCT161 | Synchronous Binary Counter | 20.0 | — | 3.5 | 5.0 |
| IDT54AHCT163 | Synchronous Binary Counter | 20.0 | — | 3.5 | 5.0 |
| IDT54AHCT182 | Carry Lookahead Generator | 15.0 | — | 3.5 | 5.0 |
| IDT54AHCT191 | Up/Down Binary Counter | 22.0 | — | 3.5 | 5.0 |
| IDT54AHCT193 | Up/Down Binary Counter | 19.0 | — | 3.5 | 5.0 |
| IDT54AHCT240 | Octal Buffer | 12.0 | — | 3.5 | 5.0 |
| IDT54AHCT244 | Octal Buffer | 13.0 | — | 3.5 | 5.0 |
| IDT54AHCT245 | Octal Bidirectional Transceiver | 15.0 | — | 3.5 | 5.0 |
| IDT54AHCT273 | Octal D Flip-Flop | 17.0 | — | 3.5 | 5.0 |
| IDT54AHCT299 | Universal Shift Register | 20.0 | — | 3.5 | 5.0 |
| IDT54AHCT373 | Octal Transparent Latch | 19.0 | — | 3.5 | 5.0 |
| IDT54AHCT374 | Octal D Flip-Flop | 18.0 | — | 3.5 | 5.0 |
| IDT54AHCT377 | Octal D Flip-Flop | 18.0 | — | 3.5 | 5.0 |
| IDT54AHCT399 | Quad Dual-Port Register | 18.0 | — | 3.5 | 5.0 |
| IDT54AHCT521 | 8-Bit Comparator | 18.0 | — | 3.5 | 5.0 |
| IDT54AHCT533 | Octal Transparent Latch | 24.0 | — | 3.5 | 5.0 |
| IDT54AHCT534 | Octal D Flip-Flop | 18.0 | — | 3.5 | 5.0 |
| IDT54AHCT573 | Octal Transparent Latch | 15.0 | — | 3.5 | 5.0 |
| IDT54AHCT574 | Octal D Register | 15.0 | — | 3.5 | 5.0 |
| IDT54AHCT640 | Octal Bidirectional Transceiver | 14.0 | — | 3.5 | 5.0 |
| IDT54AHCT645 | Octal Bidirectional Transceiver | 15.0 | — | 3.5 | 5.0 |



Shaded area indicates new product. **Boldface** indicates improved feature.

Integrated Device Technology, Inc.

# HIGH SPEED BI-CMOS ECL STATIC RAM 64K (64K x 1-BIT)

**PRELIMINARY**
**IDT100490**

## FEATURES:

- 65,536-words x 1-bit organization
- Low power dissipation: 320mW (typ.)
- Fully compatible with 100K logic level
- Address access time: 15ns (max.)
- Write pulse width: 10ns (min.)
- Open emitter output for ease of memory expansion
- Static operation: no clocks or refresh required
- Separate data input and output
- JEDEC standard high-density 22-pin plastic and sidebraze DIP and 24-pin Small Outline IC

## DESCRIPTION:

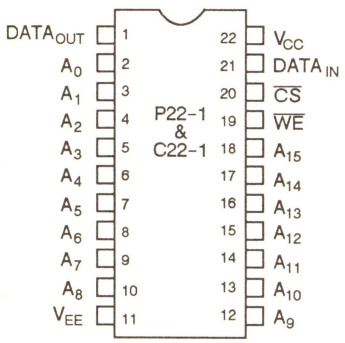
The IDT 100490 is a 100K compatible 65,536-bit high-speed BiCMOS™ ECL™ static RAM organized as 64K x 1.

The IDT100490 is available with address access times as fast as 15ns with a typical power consumption of only 320mW. This product offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

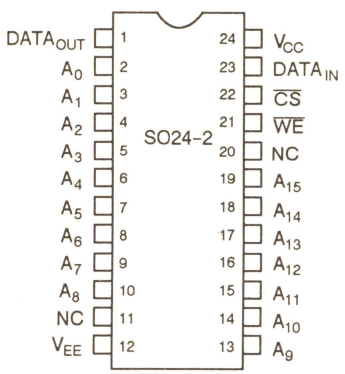
Designed for very high-speed applications, the IDT100490 is fully compatible with standard ECL 100K logic levels and offers extremely fast access times. The address access time of 15ns and write pulse width of 10ns assure that operation of this BiCEMOS part will be as fast as those available with less dense parts requiring external address decoding.

The IDT100490 is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

## PIN CONFIGURATIONS

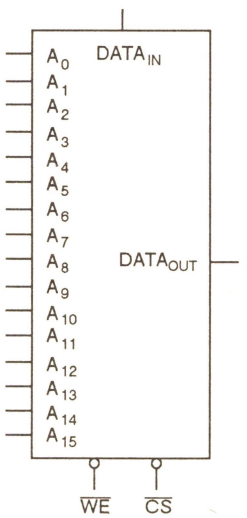



DIP, TOP VIEW

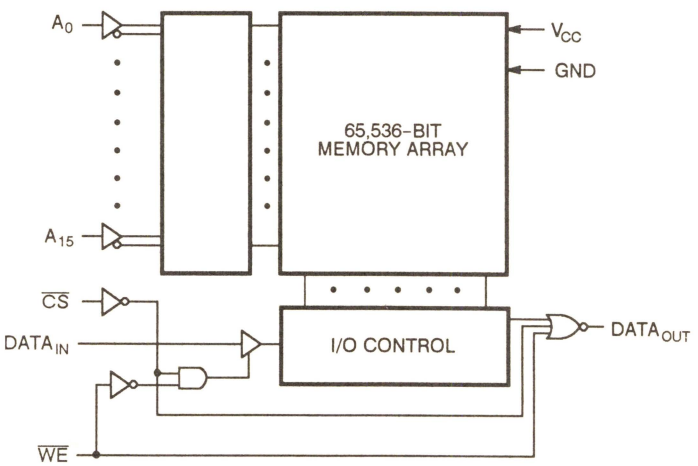



SOIC, TOP VIEW

## LOGIC SYMBOL




## FUNCTIONAL BLOCK DIAGRAM

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**COMMERCIAL TEMPERATURE RANGE** **OCTOBER 1987**

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# 16-BIT CMOS MICROPROCESSOR SLICE

**IDT49C402**
**IDT49C402A**

MICROSLICE™ PRODUCT

## FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402A 45% faster than four 2901s and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Clamp diodes on all inputs provide noise suppression
- Fully cascadable
- 68-pin PGA, Shrink DIP (600 mil, 70 mil centers) and LCC (25 and 50 mil centers)
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

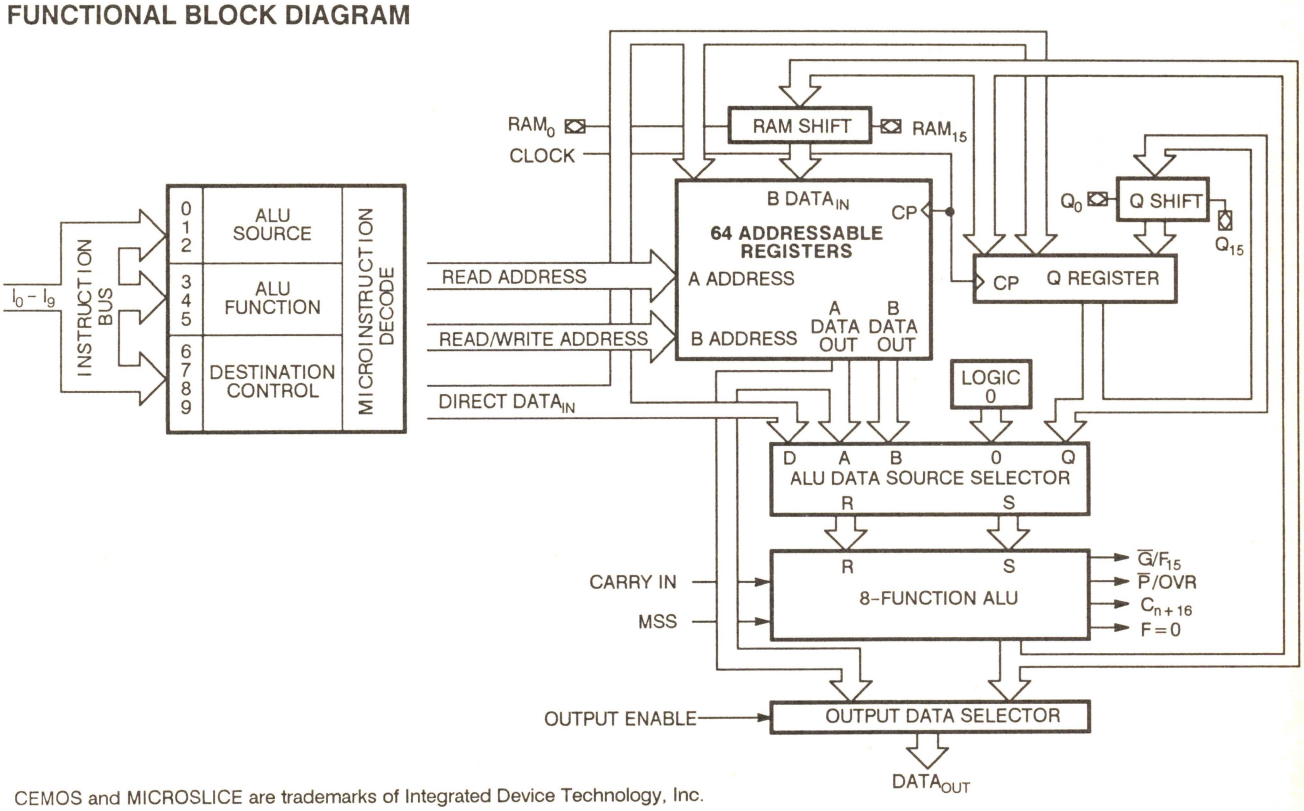
The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: (a) a 3-bit instruction field ($I_0$, $I_1$, $I_2$) which controls the source operand selection for the ALU; (b) a 3-bit microinstruction field ($I_3$, $I_4$, $I_5$) used to control the eight possible functions of the ALU; (c) eight destination control functions which are selected by the microcode inputs ($I_6$, $I_7$, $I_8$); and (d) a tenth microinstruction input, $I_9$, offering eight additional destination control functions. This $I_9$ input, in conjunction with $I_6$, $I_7$, and $I_8$, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU and new combinations of destination functions with the RAM A port output available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64 words by 16 bits—four times the number of working registers in a 2901.

The IDT49C402s are fabricated using CEMOS CMOS technology designed for high performance and high reliability. These performance enhanced devices feature both bipolar speed and bipolar output drive capabilities while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

## FUNCTIONAL BLOCK DIAGRAM

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Integrated Device Technology, Inc.

# 16-BIT CMOS MICROPROCESSOR SLICE

**IDT49C403**
**IDT49C403A**

## FEATURES:

- Monolithic 16-bit CMOS µP Slice
- Replaces four 2903As/29203s and a 2902A
- Fast
  - 50% faster than four 2903As/29203s and a 2902
- Low power CMOS
  - Commercial: 225mA (max.)
  - Military: 250mA (max.)
- Performs binary and BCD Arithmetic
- Expanded two-address architecture with independent, simultaneous access to two, expandable 64 x 16 register files
- Word/Byte Control
- Expanded 4 x 16 Q Register
- Performs BYTE Swap and Word/Byte Operation
- Fully cascadable without the need for additional carry lookahead
- Incorporates three 16-bit Bidirectional Busses
- Includes Serial Protocol Channel ™
  - Flexible on-chip diagnostics
  - Serially monitors all pin states
  - Reads and Writes to Register File
- High Output Drive
  - Commercial: 16mA (max.)
  - Military: 12mA (max.)
- Available in 108-pin PGA
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT49C403 is a high-speed, fully cascadable 16-bit CMOS microprocessor slice. It combines the standard function of four 2903s/29203s and one 2902 with additional control features aimed at enhancing the performance of all bit-slice microprocessor designs.

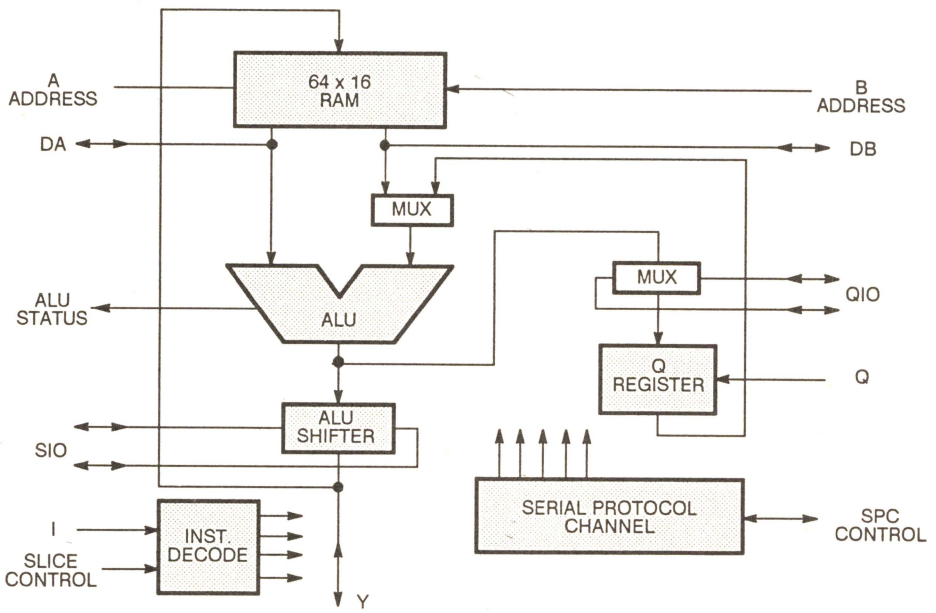
Included in this extremely low power, yet fast IDT49C403 device are: 3 bidirectional data busses, 64 word x 16-bit two-port expandable RAM, 4 word x 16-bit Q Register, parity generation, sign extension, multiplication/division and normalization logic. Additionally, the IDT49C403 offers the special feature of enhanced byte support through both Word/BYTE control and BYTE swap control.

The IDT49C403 easily supports fast 100ns microcycles and will enhance the speed of all existing quad 2903A/29203 systems by 50%. Being specified at an extremely low 225mA, the IDT device offers an immediate system power savings and improved reliability.

Also featured on the IDT49C403 is an innovative diagnostics capability known as Serial Protocol Channel (SPC). This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, along with system testing during manufacturing.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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Integrated Device Technology, Inc.

# 32-BIT CMOS MICROPROCESSOR SYSTEM-SLICE™

**IDT49C404**
**IDT49C404A**

MICROSLICE™ PRODUCT

## FEATURES:

- High speed CMOS
  - Microcycle Time: 80ns
- Three bidirectional 32-bit data I/O ports
  - DA, DB, Y
- 64-word x 32-bit expandable 7-port register file
  - 3 input ports and 4 output ports
  - Writes 3 operands and reads 4 operands in one cycle
- 64-bit in, 32-bit out cascadable funnel shifter
  - Fast alignment to any bit boundary
- 32-bit high-speed ALU cascadable to 64 bits
  - Selects status flags from any bit boundary
- Flexible mask generator and merge logic
  - Selects bit-fields on any width, on any boundary
- Priority encoder
- Powerful orthogonal instruction set
- Built-in multiplication/division support
- Counter function
  Includes Serial Protocol Channel (SPC™)
  - Flexible on-chip diagnostics
  - Serially monitors all pin states
  - Reads and writes to Register File
- Single 5V supply
- Available in 208-pin PGA
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT49C404 "SYSTEM-SLICE™" is an expandable, microprogrammable, high-speed CMOS 32-bit microprocessor slice. This monolithic, highly parallel, 3-port device consists of a 7-port 64-word by 32-bit working RAM, 64 bits in/32 bits out cascadable funnel shifter, high-speed multi-function 32-bit ALU and 32-bit mask generation and merge logic.

The IDT49C404 uniquely incorporates shift, ALU and merge functions into a single cycle and utilizes an orthogonal instruction set to create a highly parallel architecture that achieves added performance.

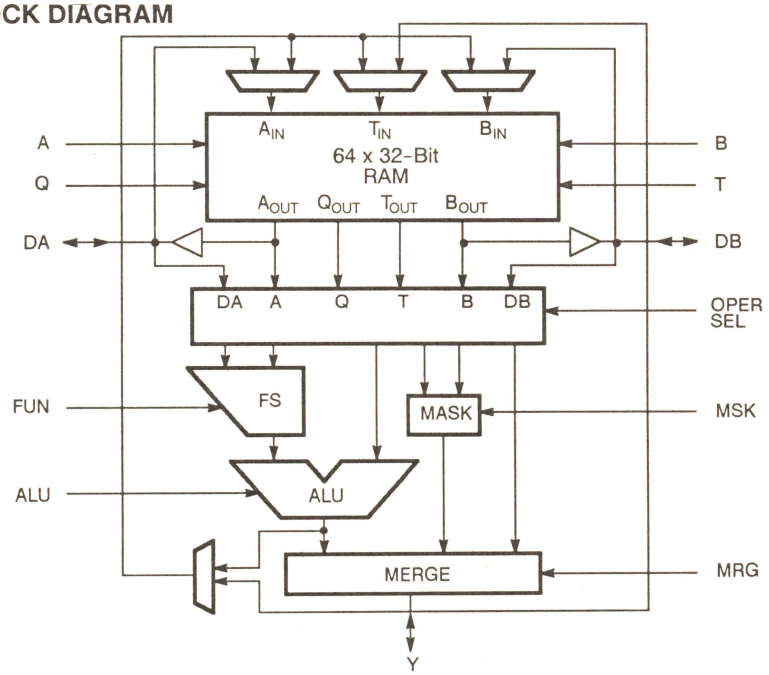
Supporting ultra-fast cycle times, the IDT49C404 offers a very-low-power CMOS alternative to existing bipolar counterparts.

This 32-bit device has been optimized, both architecturally and instruction set-wise, for use in all types of dedicated intelligent controllers such as high-speed graphics engines, array processors, fast disk and communication controllers, robotics, data base manipulation, design automation and AI.

Also featured on the IDT49C404 is an innovative diagnostics capability known as Serial Protocol Channel (SPC). This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, along with system testing during manufacturing.

The IDT49C404 is fabricated using CEMOS™, IDT's advanced CMOS technology designed for high-performance and high-reliability. The device is packaged in a 208-lead pin grid array. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# 16-BIT CMOS MICROPROGRAM SEQUENCER

**IDT49C410**
**IDT49C410A**

MICROSLICE™ PRODUCT

## FEATURES:

- 16-bit wide address path
  - Address up to 65,536 words of microprogram memory
- 16-bit loop counter
  - Pre-settable down-counter for counting loop iterations and repeating instructions
- Low-power CEMOS™
  - $I_{CC}$ (max.)
    Military: 90mA
    Commercial: 75mA
- Fast
  - IDT49C410 meets 2901A speeds
  - IDT49C410A 30% speed upgrade
- 33-deep stack
  - Accommodates highly nested microcode
- 16 powerful microinstructions
  - Executes 16 sequence control instructions
- Available in 48-pin 600 mil plastic and sidebraze, 48-pin 400 mil SHRINK-DIP, 48-pin LCC, 52-pin PLCC and 48-pin Flatpack
- Three enables control branch address sources
- Four address sources
- 2901A instruction compatibility
- Military product available compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT49C410s are architecture and function code compatible to the 2901A with an expanded 16-bit address path, thus allowing for programs up to 65,536 words in length. They are microprogram address sequencers intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, they provide conditional branching to any microinstruction within their 65,536 microword range.

The 33-deep stack provides microsubroutine return linkage and looping capability. The deep stack can be used for highly nested microcode applications. Microinstruction loop count control is provided with a count capacity of 65,536.

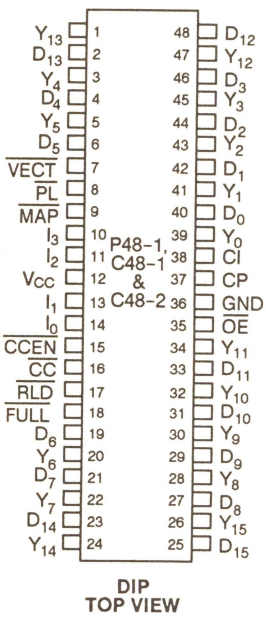
During each microinstruction, the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (µPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a last-in/ first-out stack (F).

The IDT49C410s are fabricated using CEMOS, a CMOS technology designed for high performance and high reliability.

The IDT49C410s are pin-compatible, performance-enhanced, easily upgradable versions of the 2901A.

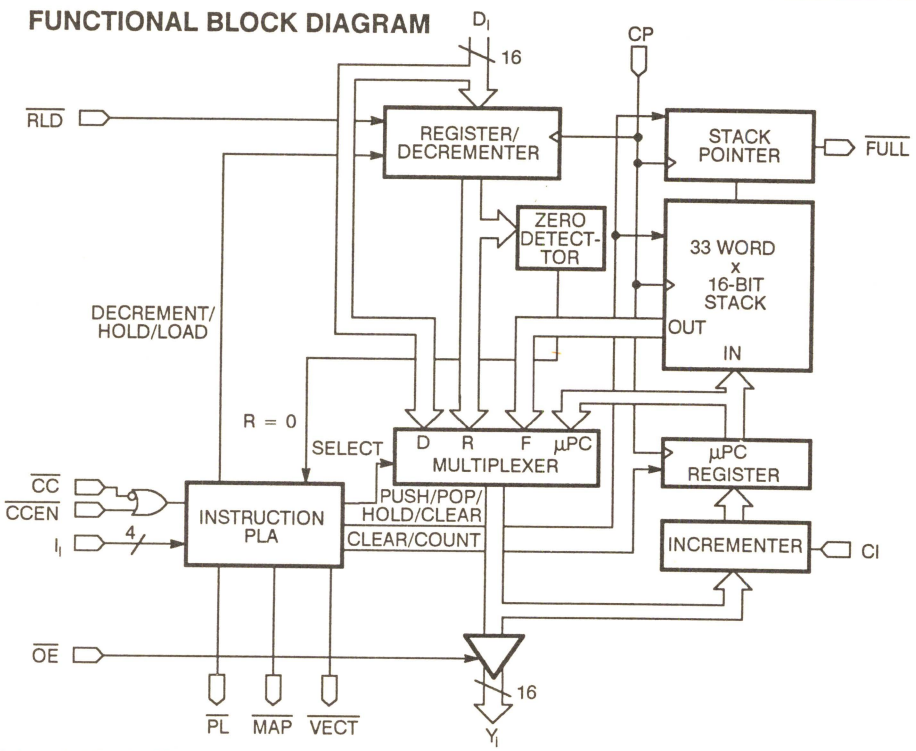
The IDT49C410s are available in 48-pin DIPs (600 mil x 100 mil centers or space-saving 400 mil x 70 mil centers), 48-pin LCC, 52-pin PLCC and 48-pin flatpacks.

## PIN CONFIGURATION




DIP
TOP VIEW

## FUNCTIONAL BLOCK DIAGRAM

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# 32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

**IDT49C460**
**IDT49C460A**
**IDT49C460B**

## FEATURES:

- Fast

| | Detect | Correct |
|---|---|---|
| – IDT49C460B | 25ns (max.) | 30ns (max.) |
| – IDT49C460A | 30ns (max.) | 36ns (max.) |
| – IDT49C460 | 40ns (max.) | 49ns (max.) |

- Low-power CMOS
  - – Commercial: 95mA (max.)
  - – Military: 125mA (max.)
- Improves system memory reliability
  - – Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - – Data words up to 64-bits
- Built-in diagnostics
  - – Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - – Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the 2960
- Available in PGA, Sidebraze DIP, LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors and will detect all double bit errors and some triple bit errors.

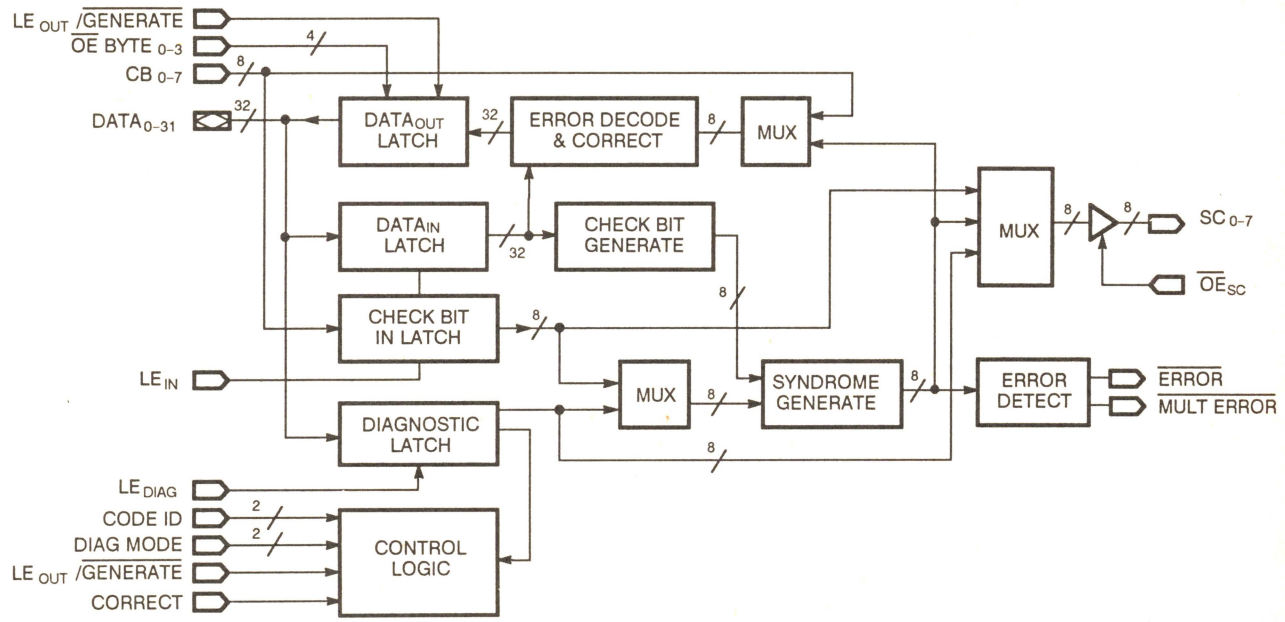
The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

They are fabricated using CEMOS™, a single poly, double metal CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin PGA, sidebraze DIP (600 mil, 70 mil centers), LCC (25 mil and 50 mil centers) and PLCC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS STATIC RAM 256K (32K x 8-BIT)

**PRELIMINARY**
**IDT71256S**
**IDT71256L**

## FEATURES:

- High-speed address/chip select time
  - Military: 45/55/70/85ns (max.)
  - Commercial: 35/45/55/70ns (max.)
- Low-power operation
  - IDT71256S
    Active: 300mW (typ.)
    Standby: 200μW (typ.)
  - IDT71256L
    Active: 250mW (typ.)
    Standby: 15μW (typ.)
- Battery Backup operation—2V data retention
- Produced with advanced high-performance CEMOS™ technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 28-pin CERDIP and plastic DIP (600 mil), 28-pin SOIC and 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

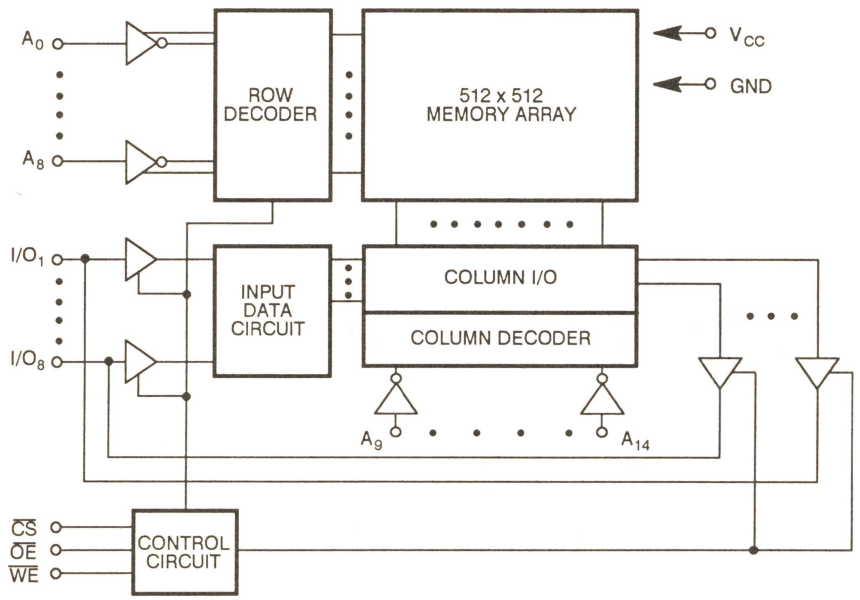
Address access times as fast as 35ns are available with power consumption of only 300mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 15μW, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5μW when operating off a 2V battery.

All inputs and outputs of the IDT71256 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71256 is packaged in a 28-pin SOIC, a 28-pin 600 mil CERDIP or plastic DIP and 32-pin leadless chip carrier and PLCC, providing high board-level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS STATIC RAMS 256K (64K x 4-BIT)

## Separate Data Inputs And Outputs

**PRELIMINARY**
**IDT71281S/L**
**IDT71282S/L**

## FEATURES:

- Separate data inputs and outputs
- IDT71281S/L: outputs track inputs during write mode
- IDT71282S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low power consumption
  - IDT71281/2S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - IDT71281/2L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin DIP
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT71281/IDT71282 are 262,144-bit high-speed static RAMs organized as 64K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

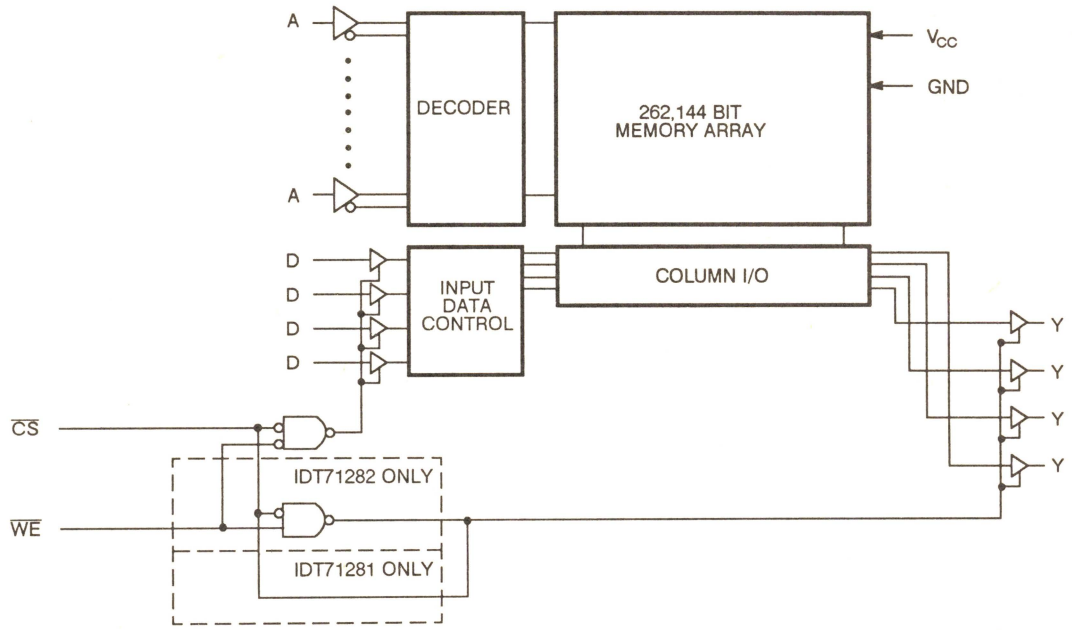
Access times as fast as 25ns are available with typical power consumption of only 350mW. These circuits also offer a reduced power standby mode ($I_{SB}$). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode. The ultra-low-power standby mode capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 100µW operating off a 2V battery.

All inputs and outputs of the IDT71281/IDT71282 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71281/IDT71282 are packaged in 28-pin sidebraze DIPs, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH SEMAPHORE

**PRELIMINARY**
**IDT71322S**
**IDT71322L**

## FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low-power operation
  - IDT71322S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71322L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible, single 5V(±10%) power supply
- Available in a variety of plastic and hermetic packages for both through hole and surface mount applications
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

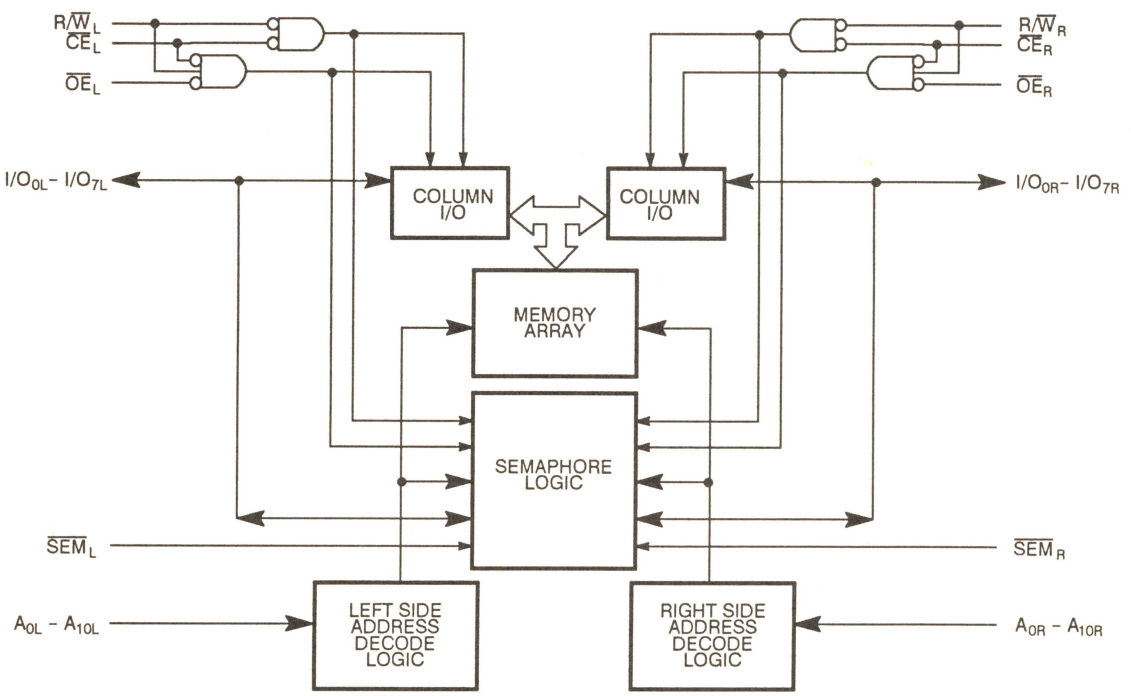
The IDT71322 is an extremely high-speed 2K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71322 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200μW from a 2V battery.

The IDT71322 is packaged in a 48-pin sidebraze or plastic DIP or 52-pin LCC and PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

**PRELIMINARY**
**IDT7133S/L**
**IDT7143S/L**

## FEATURES:

- High-speed access
  - Military: 70/90ns (max.)
  - Commercial: 55/70/90ns (max.)
- Low-power operation
  - IDT7133/43S
    Active: 375mW (typ.)
    Standby: 5mW (typ.)
  - IDT7133/43L
    Active: 375mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, DIP (600 mil, 70 mil centers), LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT7133/7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

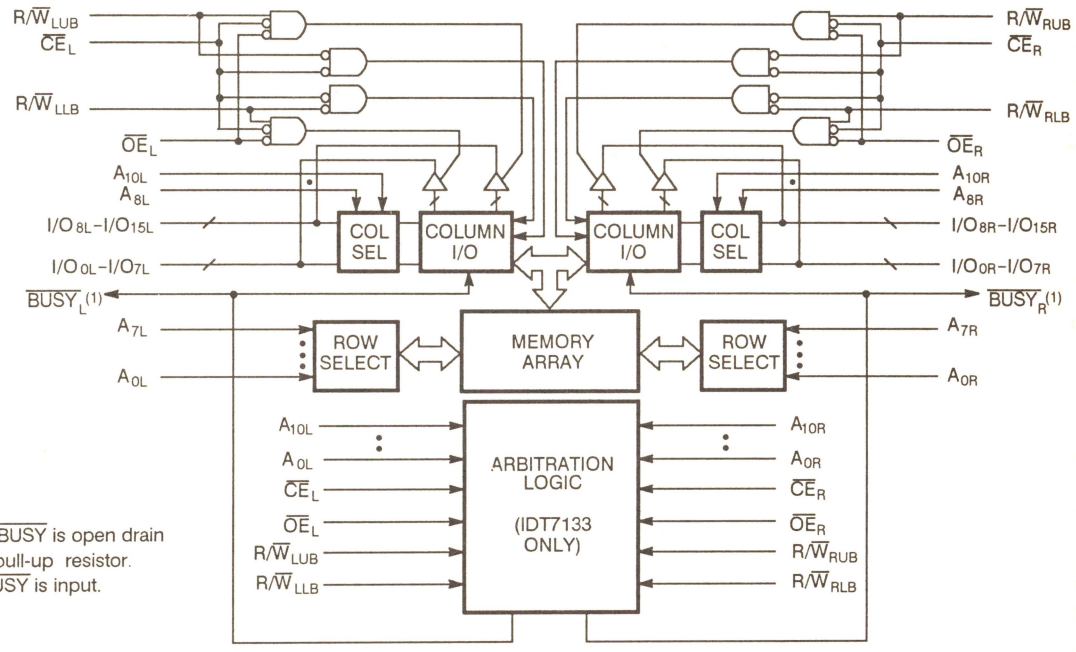
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 375mW of power at maximum access times as fast as 55ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 1mW from a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packaged in a 68-pin PGA, 68-pin LCC, and 70 mil center DIPs.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM




**NOTES:**

1. IDT7133 (MASTER): $\overline{BUSY}$ is open drain output and requires pull-up resistor.
   IDT7143 (SLAVE): $\overline{BUSY}$ is input.
2. LB = LOWER BYTE
   UB = UPPER BYTE

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# CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

**PRELIMINARY**
**IDT71342S**
**IDT71342L**

## FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low-power operation
  - IDT71342S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71342L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible; single +5V(±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

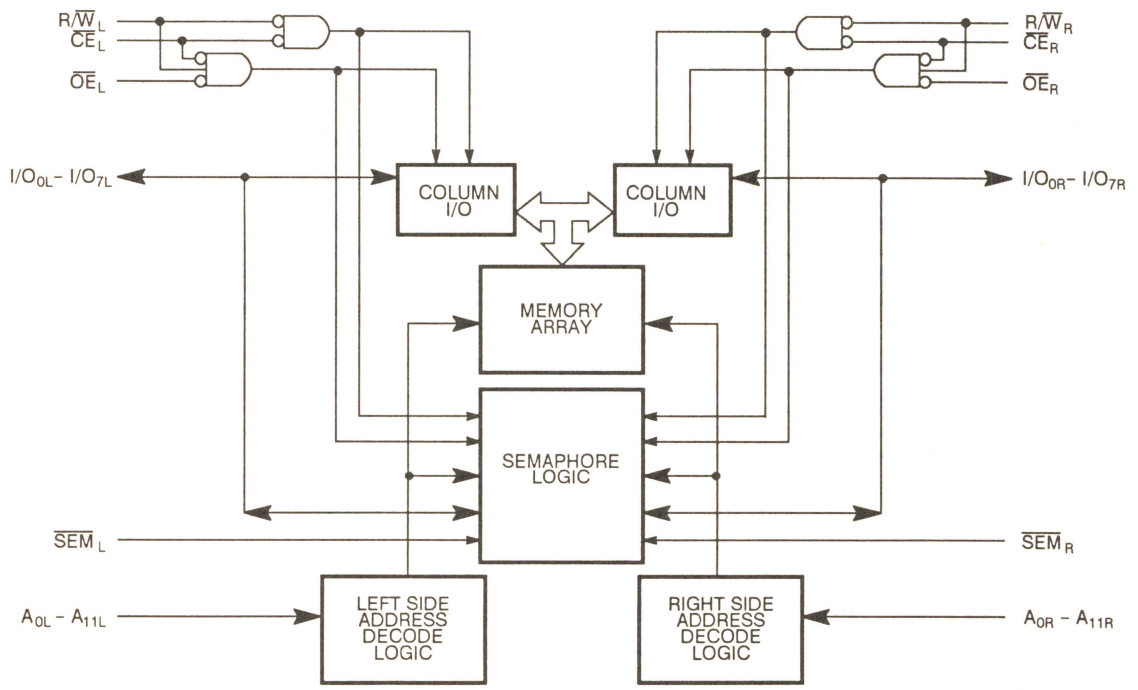
The IDT71342 is an extremely high-speed 4K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71342 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

Fabricated using IDT's CEMOS™ high-performance technology this device typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200μW from a 2V battery. The device is packaged in either a hermetic 52-pin leadless chip carrier or a 52-pin PLCC.

The IDT71342 military devices are manufactured in compliance with the latest revision of MIL-STD-883, Class B.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS SYNCHRONOUS RAM 64K (64K x 1-BIT)

**PRELIMINARY**
**IDT71501S**

## FEATURES:

- Internal pipeline registers on Address, Data and control lines
- High-speed (equal access and cycle time)
  - Military: 35/45ns (max.)
  - Commercial: 35/45ns (max.)
- Low power consumption: 385mW (typ.)
- All inputs/outputs TTL-compatible ($V_{OL}$ = 0.4V @ $I_{OL}$ = 8mA)
- Separate, latched data input and output
- Three-state output
- Available in JEDEC standard 24-pin, 300 mil CERDIP and Plastic DIP, 24-pin, 300 mil SOIC and 28-pin LCC
- Produced with advanced CEMOS™ high-performance technology
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

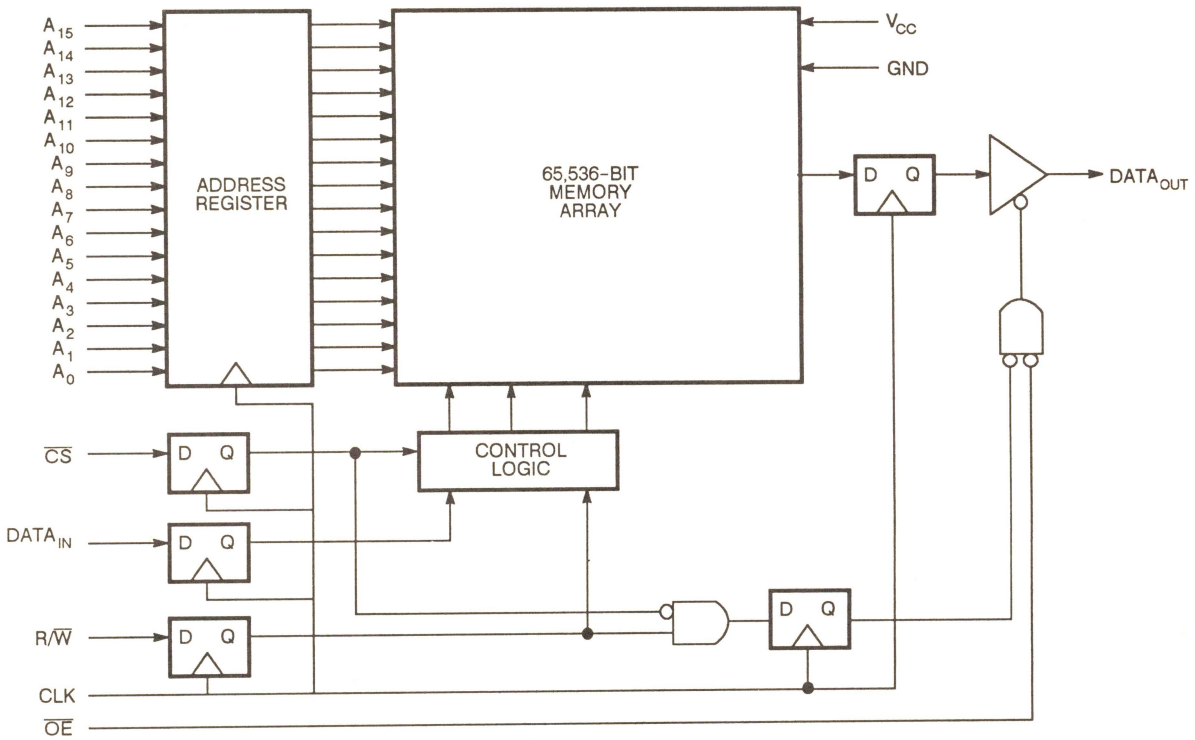
The IDT71501 is a high-speed 64K x 1 static RAM synchronized with pipeline registers on the Address, Data, Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) pins. This product is designed to assist in the design of pipelined processing systems by removing the need for external pipeline registers. The internal registers offer speed improvements through higher integration of system functions.

Access times are as fast as 35ns, with higher speed Output Enable ($\overline{OE}$) and Clock to Valid Data Output functions to enable the high-speed system designer the maximum throughput possible in an efficient large-memory pipelined system. Fabricated using IDT's CEMOS high-performance technology, these devices operate on only 385mW of power.

The IDT71501 is packaged in industry standard 24-pin, 300 mil plastic and ceramic DIPs, as well as a 28-pin leadless chip carrier (LCC) and a 24-lead, 300 mil gullwing SOIC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS STATIC RAM 64K (4K x 16-BIT) REGISTERED RAM w/SPC™

**ADVANCE INFORMATION**
**IDT71502S**
**IDT71502L**

Integrated Device Technology

## FEATURES:

- 4K x 16-bit RAM with register at output, serial load and readback
- Designed for microprogram writable control store
- Serial Protocol Channel (SPC) allows load and readout of RAM over a 4-wire channel
- RAM address counter speeds RAM load, readout
- Outputs may be programmed to be registered or non-registered in groups of 8 bits
- Initialize register allows initial microword selection
- Synchronous and asynchronous output enables allow for depth expansion and bus driving
- Breakpoint comparator supports system diagnostics
- Parity check on outputs for high-reliability designs
- High-speed (address set-up before clock)
  - Military: 45/55/70ns (max.)
  - Commercial: 30/35/45/55ns (max.)
- Built in CMOS for low power consumption
- Inputs and outputs directly TTL-compatible
- Standard 48-pin DIP
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT71502 Registered RAM is designed expressly for efficient use in writable control stores. This 65,536-bit high-speed static RAM is organized as 4K x 16 bits with a high-speed register at the RAM outputs and serial load and readback capability using the IDT Serial Protocol Channel (SPC). Its architecture is optimized for microprogram writable control store use. Hardware is provided for software test and debug, parity checking and serial microcode load at initialization.

The IDT71502 is available with address set-up before clock times as fast as 30ns with a maximum power consumption of only 900mW.

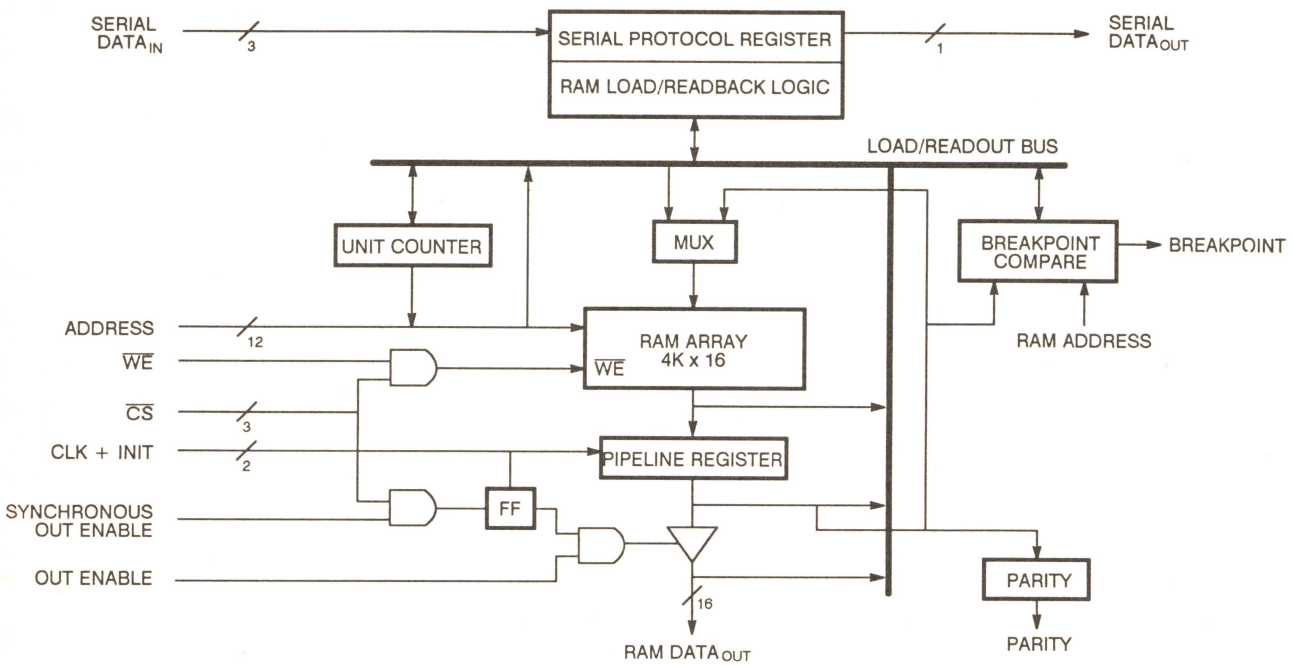
All inputs and outputs of the IDT71502 are TTL-compatible and the device operates from a single 5V supply. Fully static, asynchronous circuitry is used, requiring no clocks (with the exception of the register clock) or refreshing for operation.

The IDT71502 is fabricated using IDT's high-performance, high-reliability technology – CEMOS ™. This technology gives the IDT71502 the combination of low power, high speed and high density that makes it a cost-effective alternative to bipolar and NMOS devices such as registered PROMs.

The IDT71502 is packaged in a 48-pin, 600 mil DIP, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS STATIC RAM 64K (8K x 8-BIT) RESETTABLE RAM

**IDT7165S**
**IDT7165L**

## FEATURES:

- High-speed asynchronous RAM clear on Pin 1 (clears all RAM bits to 0, reset cycle time = 2 x $t_{AA}$)
- High-speed address access time
  - Military: 35/45/55ns (max.)
  - Commercial: 30/35/45/55ns (max.)
- High-speed chip select ($\overline{CS}_1$) time
  - Military: 20/25/30/35ns (max.)
  - Commercial: 15/20/25/30ns (max.)
- Low-power operation
  - IDT7165S
    Active: 300mW (typ.)
    Standby: 100µW (typ.)
  - IDT7165L
    Active:250mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation—2V data retention voltage (IDT7165L only)
- Produced with CEMOS™ high-performance technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin, 600 mil DIP, 300 mil plastic DIP, 28-pin SOIC, 32-pin LCC and PLCC
- Military product is compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT7165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. The $\overline{RESET}$ pin provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset, or for a fast clear to be available to graphics, histogramming and other designs where a byte-by-byte RAM clear would cause noticeable system speed degradation.

This product is fabricated using IDT's high-performance, high-reliability CEMOS technology. Address access time of 30ns and chip select ($\overline{CS}_1$) time of 15ns are available with maximum power consumption of only 770mW. This circuit also offers a reduced power standby mode. When $CS_2$ goes low, the circuit will automatically go to and remain in a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating from a 2V battery.

All inputs and outputs of the IDT7165 are TTL-compatible and the device operates from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, so no clocks or refreshing operation is required.

The IDT7165 is packaged in a 28-pin 300 or 600 mil DIP, 28-pin SOIC, and 32-pin LCC and PLCC, providing high board level densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to the military temperature applications which require instant destruction of sensitive RAM data and demand the highest level of performance and reliability.

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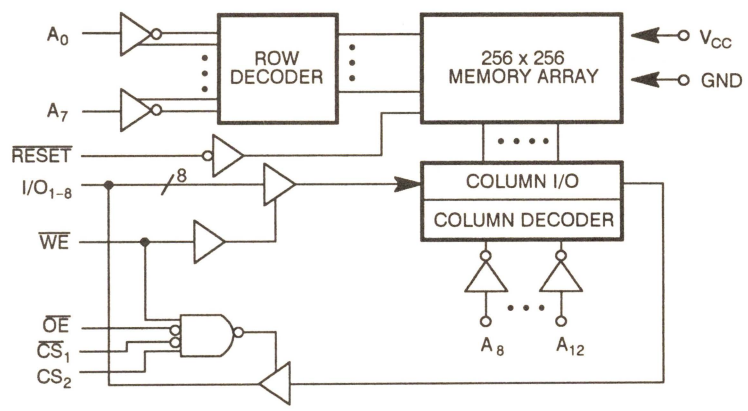
## FUNCTIONAL BLOCK DIAGRAM

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# CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 256 x 9-BIT & 512 x 9-BIT

**IDT7200S/L**
**IDT7201SA/LA**

Integrated Device Technology

## FEATURES:

- First-In/First-Out dual-port memory
- 256 X 9 organization (IDT7200)
- 512 x 9 organization (IDT7201A)
- Low power consumption
- Ultra high speed—35ns cycle time (28.5MHz)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT7200 and IDT7201A pin and functionally compatible with Mostek MK4501, but with Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in Plastic DIP, CERDIP, LCC, PLCC, 300 mil sidebraze DIP and Flatpack
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT7200/7201A are dual-port memories that utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

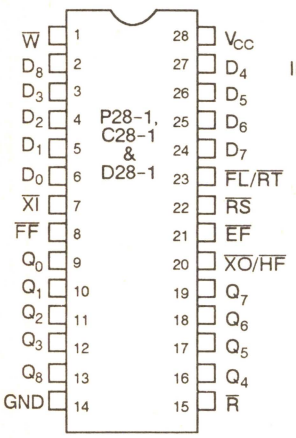
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 35ns (28.5MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

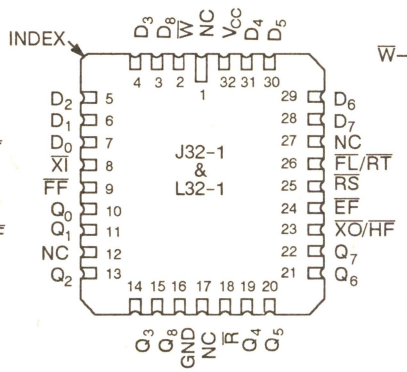
The IDT7200/1A are fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

## PIN CONFIGURATIONS

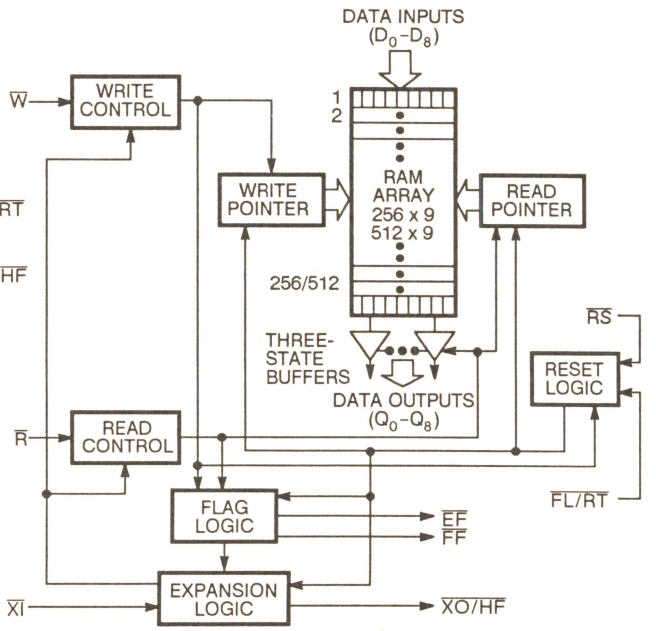



DIP
TOP VIEW




PLCC/LCC
TOP VIEW

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 1024 x 9-BIT

**IDT7202SA/LA**

## FEATURES:

- First-In/First-Out dual-port memory
- 1024 x 9 organization (IDT7202A)
- Low power consumption
- Ultra high speed—35ns cycle time (28.5MHz)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin compatible with Mostek MK4501, but with Half-Full Flag capability
- IDT7202A allows for deep word structure (1024) without expansion
- Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance CEMOS ™ technology
- Available in Plastic DIP, CERDIP, LCC, PLCC, 300 mil sidebraze DIP and Flatpack
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT7202A is a dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

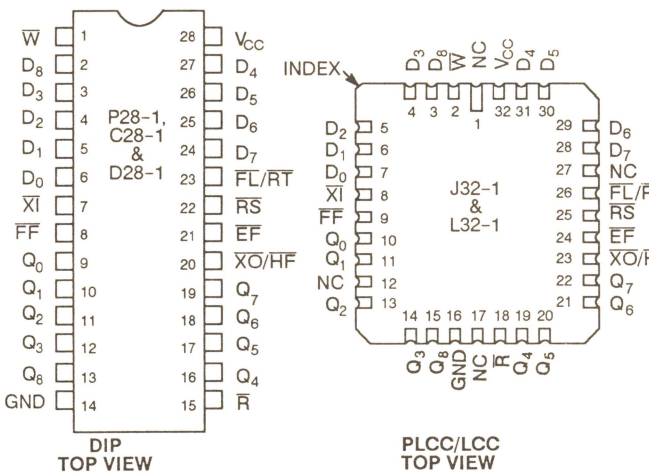
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 35ns (28.5MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

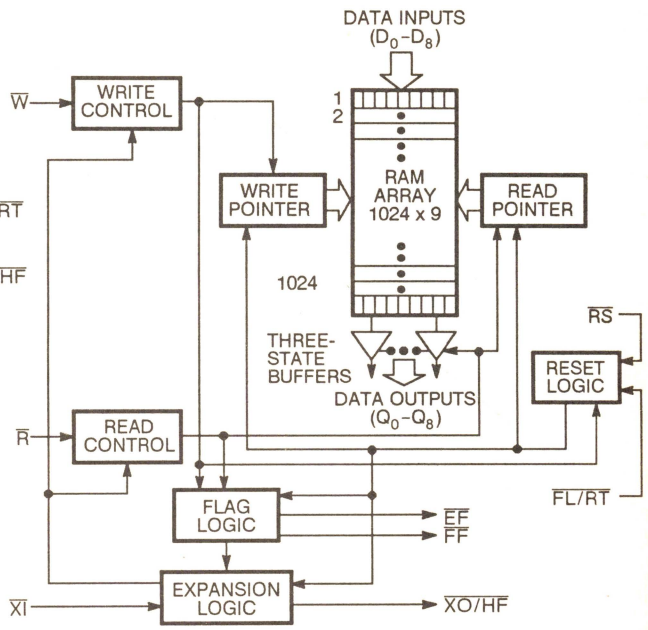
The IDT7202A is fabricated using IDT's high-speed CEMOS technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 1024 x 9 organization of the IDT7202A allows a 1024 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

## PIN CONFIGURATIONS




## FUNCTIONAL BLOCK DIAGRAM

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# CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT & 4096 x 9-BIT

**IDT7203S/L**
**IDT7204S/L**

## FEATURES:

- First-In/First-Out dual-port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- Low power consumption
  - Active: 660mW (max.)
  - Power down: 66mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT7201/7202
- IDT7204 allows 4096 word structure without expansion
- Half-full flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in CERDIP, Plastic DIP, PLCC and LCC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT7203/7204 is dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty Flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

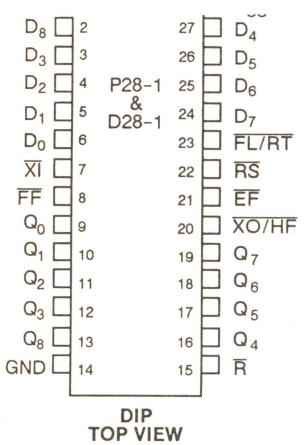
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz).

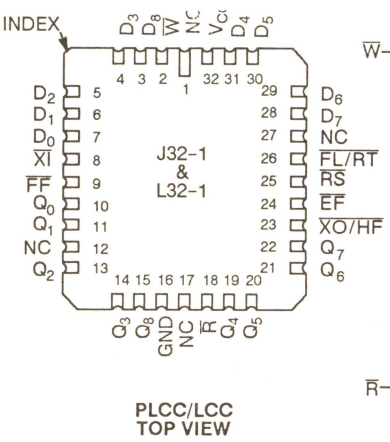
The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7203/7204 is fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 4096 x 9 organization for the IDT7204 allows a 4096 deep word structure without the need for expansion.

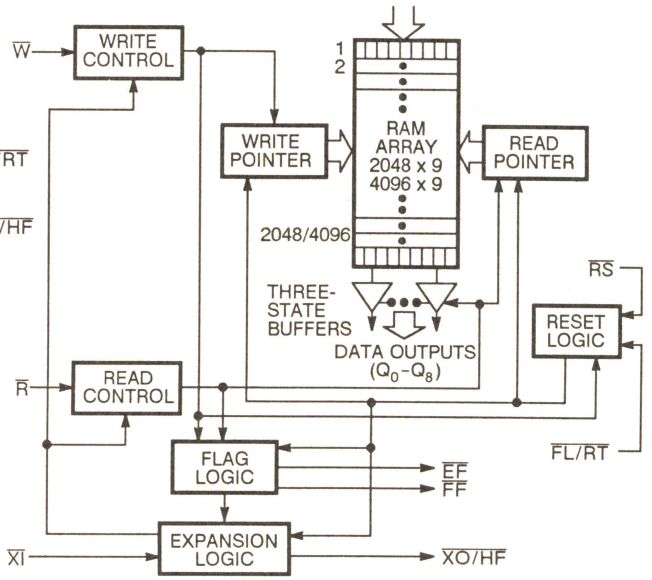
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

## PIN CONFIGURATIONS




## FUNCTIONAL BLOCK DIAGRAM

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# 16 x 16-BIT PARALLEL CMOS MULTIPLIER-ACCUMULATOR

**IDT7210L**
**IDT7243L**

## FEATURES:

- 16 x 16-bit parallel multiplier-accumulator with selectable accumulation and subtraction
- High-speed: 20ns multiply-accumulate time
- IDT7210 features selectable accumulation, subtraction, rounding and preloading with 35-bit result
- IDT7243 features selectable accumulation, subtraction and rounding with 19-bit result
- IDT7210 is pin and functionally compatible with the TRW TDC1010J
- IDT7243 is pin and functionally compatible with the TRW TDC1043
- Both devices perform subtraction and double precision addition and multiplication
- Produced using advanced CEMOS™ high-performance technology
- Low power consumption (less than 250mW typical) – less than 1/10 the power of compatible bipolar and 1/7 the power of NMOS designs
- Input and output directly TTL-compatible
- Single 5V supply
- Available in plastic and topbraze DIP, SHRINK-DIP, LCC, Fine-Pitch LCC, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

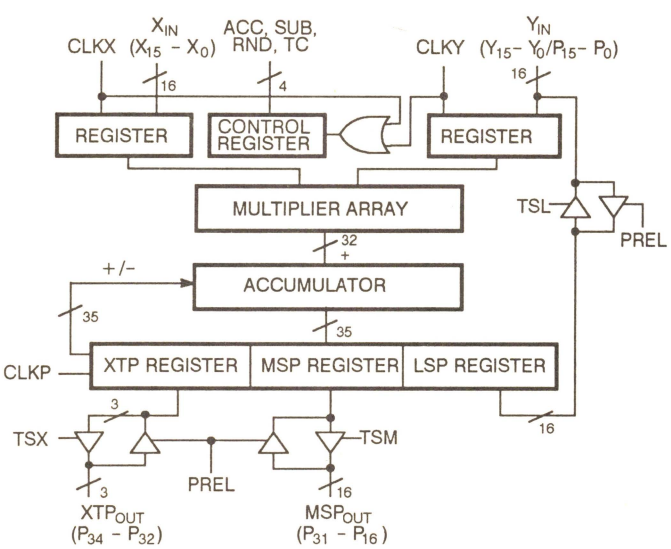
The IDT7210/7243 are high-speed, low-power 16 x 16-bit parallel multiplier-accumulators that are ideally suited for real-time digital signal processing applications. Fabricated using CEMOS silicon gate technology, these devices offer a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/7 to 1/10 the power dissipation and exceptional speed (20ns maximum) performance.

Pin and functional replacements for TRW's TDC1010J/TDC1043, the IDT7210/7243 operate from a single 5 volt supply and are compatible with standard TTL logic levels. The architecture of the IDT7210/7243 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flops, a preload capability (IDT7210 only) which enables input data to be preloaded into the output registers, individual three-state output ports for the Extended Product (XTP) and Most Significant Product (MSP) and a Least Significant Product output (LSP) which is multiplexed with the Y input. Unlike the IDT7210, the IDT7243 does not have either a preload capability or a Least Significant Product (LSP) output accessible externally.

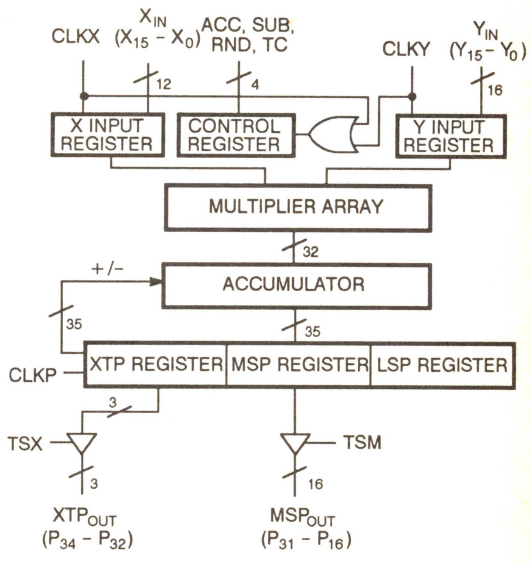
The $X_{IN}$ and $Y_{IN}$ data input registers may be specified through the use of the Two's Complement input (TC) as either a two's complement or an unsigned magnitude, yielding a full-precision 32-bit result that may be accumulated to a full 35-bit result. The three output registers – Extended Product (XTP), Most Significant Product (MSP) and Least Significant Product (LSP) – are controlled by the respective TSX, TSM and TSL input lines. The LSP output can be routed through $Y_{IN}$ ports in the IDT7210.

Continued on Page 2

## FUNCTIONAL BLOCK DIAGRAM




IDT7210




IDT7243

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# CMOS PARALLEL-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

**IDT72103**
**IDT72104**

## FEATURES:

- 35ns parallel port access time
- 50MHz serial input/output port frequency
- Serial-to-Parallel, Parallel-to-Serial, Serial-to-Serial and Parallel-to-Parallel operations
- Easily expandable in depth and width
- Programmable wordlengths from 4 bits to any bit width using Flexishift™ for serial operations without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Full-Minus-One, Empty, Almost-Empty (1/8 from empty), Empty-Plus-One and Half-Full
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture
- Output enable control provided for parallel port
- Retransmit capability in single device mode
- High-performance CEMOS™ technology
- Available in 40-pin ceramic and plastic DIP, 44-pin LCC and J-Leaded PLCC
- Military product compliant to MIL-STD-883, Class B

## APPLICATIONS:

- High-Speed Data Acquisition Systems
- Local Area Network Buffers
- Remote Telemetry Buffers
- Serial Link Buffers
- High-Speed Parallel Bus-to-Bus Serial Communications
- Magnetic Media Controllers
- Single Chip Video Frame Buffers
- FAX/Printer Buffers

## DESCRIPTION:

The IDT72103/72104 are high-speed Parallel-Serial FIFOs that are ideally suited for serial communications, high-density media storage and local area networks.

The devices have four ports: two 9-bit parallel ports and the other two for serial input and serial output. A variety of operations can be performed: Serial-to-Parallel, Parallel-to-Serial, Serial-to-Serial and Parallel-to-Parallel. The Parallel-Serial FIFOs can expand in depth or width for any of these modes.

A unique feature that enhances the bandwidth is the handling of serial wordlengths that are not a multiple of 9. The IDT72103/72104 can be configured to handle serial wordlengths of 4 to 9 bits, up to words of any length, using multiple devices. This feature is provided without using any additional ICs. For example, a used can configure a 4K x 24 FIFO by using three devices to generate internal increments to the read/write pointers every 24 cycles rather than every 27 cycles, thereby maintaining a high bandwidth.

A number of flags are provided to monitor the status of the FIFO. These include Full, Almost-Full (when the FIFO is more than 7/8 full), Full-Minus-One (when the FIFO has one or zero locations left), Empty, Almost-Empty (when the FIFO is less than 1/8 full), Empty-Plus-One (when there is only one or zero samples left in the FIFO) and Half-Full.

Read and Write controls are provided to permit asynchronous and simultaneous operations. An Output Enable control is provided on the parallel port and this is an additional control to the Read input that also controls the parallel port. Expansion controls $\overline{XO}$ and $\overline{XI}$ are provided to allow cascading for deeper FIFOs.

The IDT72103/72104 are manufactured using IDT's CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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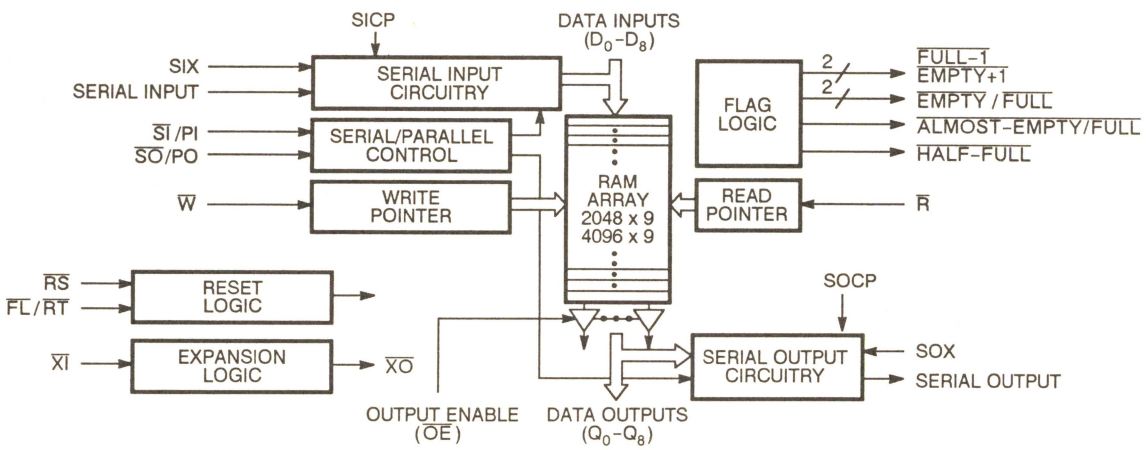
## FUNCTIONAL BLOCK DIAGRAM

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# 32-BIT AND 64-BIT IEEE FLOATING-POINT MULTIPLIER AND ALU

**IDT721264**
**IDT721265**

## FEATURES

- Conforms to the requirements of IEEE Standard 754, 1985 version, for full 32-bit and 64-bit multiply and arithmetic operations
- Very high-speed operation
  - 16.7 megaflops (60ns) pipelined ALU operation (Add/Subtract/Convert/Compare)
  - 16.7 megaflops (60ns) pipelined 32-bit (single precision) multiplications
  - 8.0 megaflops (120ns) pipelined 64-bit (double precision) multiplications
- Full floating-point function arithmetic logic unit including:
  - Add
  - Subtract
  - Absolute value
  - Compare
  - Conversion to and from two's complement integer
  - Performs 2-A to support Newton-Raphson division
- Low-power (500mW typical per device) operation
- Single 5 volt supply—no need for two supplies
- Advanced CEMOS™ technology
- Flexible system design
  - Three 32-bit ports allow two data inputs and one result output every clock cycle
  - One, two or three port architectures supported
  - Single phase, edge-triggered clock interface, with fully registered TTL compatible inputs and outputs
- Full commercial and military ranges available
- Standard 144-pin grid array package
  - Pin and functionally compatible with Weitek 1264/1265

## DESCRIPTION

The IDT721264 floating-point multiplier and the IDT721265 floating-point ALU provide high-speed 32-bit and 64-bit floating-point processing capability.

The IDT721264/65 are fabricated using IDT's advanced CEMOS technology and are capable of a total flow-through multiply latency (time required from the input of the operand until the result can be used by another device) of 180ns for single precision and 270ns for double precision multiplications. This ultra-high-speed performance is achieved by combining both state-of-the-art CEMOS technology and advanced circuit design techniques.

For signal processing applications, where higher throughput speeds are required, operations including the function specification can be pipelined. For single precision multiplications, new operands can be loaded and a product unloaded every 80ns, while double precision multiplies can be accomplished at a 160ns rating. The IDT721265 ALU executes all operations at an 80ns pipelined throughput. All operations, including the function specification, are pipelined so there is no penalty for interleaving various functions. The on-chip pipeline is automatically advanced, using internal timers, so explicit pipeline flushing is not required.

This flexible two-chip set operates in full conformance with the requirements of IEEE standard 754, 1985 version. It performs operations on single (32-bit) and double (64-bit) precision operands, as well as conversion to 32-bit two's complement integers (IDT721265 only). The IDT721264/65 accommodates all rounding modes, infinity and reserved operand representations and the treatment of exceptions such as overflow, underflow, invalid and inexact operations. Exact conformance to the standards ensures complete software portability between prototype development and final application. A "FAST" mode eliminates the time penalty for denormalized numbers by substituting zero for a denormalized number.

The flexible input/output architecture of these devices allows them to be used in systems with one, two or three 32-bit buses, or one 64-bit bus. Fully registered inputs and outputs, separately controlled, are loaded on each rising edge of the clock.

A 64-bit function control determines the arithmetic function to be performed while a 4-bit status output flags arithmetic exceptions and conditions. Both the function inputs and status outputs propagate along with the data to ease system design timing.

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# 16 x 16-BIT PARALLEL CMOS MULTIPLIERS

**IDT7216L**
**IDT7217L**

## FEATURES:

- 16 x 16 parallel multiplier with double precision product
- 20ns clocked multiply time
- Low power consumption: 120mA
- Produced with advanced submicron CEMOS™ high-performance technology
- IDT7216L is pin- and functionally-compatible with TRW MPY016H/K and AMD Am29516
- IDT7217L requires only single clock with register enables making it pin- and functionally-compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL- compatible
- Three-state output
- Available in Plastic DIP, Shrink-DIP, Top Braze DIP, PLCC, Fine-Pitch LCC, LCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT7216/IDT7217 are high-speed, low-power 16 x 16 multipliers, ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, submicron CEMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10th the power consumption.

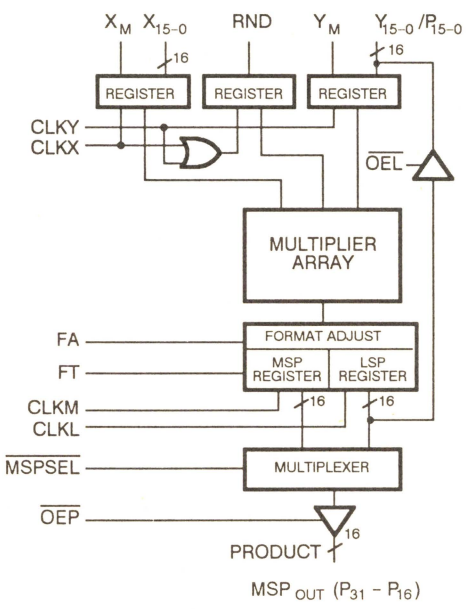
The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplications such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition, and in any system requirement where multiplication speeds of a mini/micro computer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

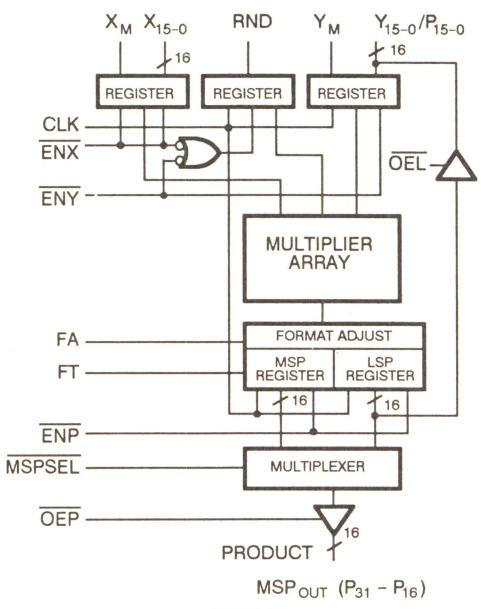
The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The $\overline{MSPSEL}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

The IDT7216/IDT7217 multipliers are 100% compliant to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAMS




**IDT7216**




**IDT7217**

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# CMOS PARALLEL FIFO 64 x 4-BIT AND 64 x 5-BIT

**IDT72401**
**IDT72402**
**IDT72403**
**IDT72404**

## FEATURES:

- First-In/First-Out dual-port memory
- 64 x 4 organization (IDT72401/403)
- 64 x 5 organization (IDT72402/404)
- IDT72401/402 pin and functionally compatible with MMI67401/02
- RAM-based FIFO with low fall-through time
- Low power consumption
  - Active: 200mW (typ.)
- Maximum shift-rate – 45MHz
- High data output drive capability
- Asynchronous and simultaneous read and write
- Fully expandable by bit width
- Fully expandable by word depth at 35MHz
- IDT72403/404 have Output Enable pin to enable output data
- High-speed data communications applications
- High-performance CEMOS™ technology
- Available in CERDIP, Plastic DIP, LCC and SOIC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT72401 and IDT72403 are asynchronous, high-performance First-In/First-Out memories organized 64-words-by-4-bits. The IDT72402 and IDT72404 are asynchronous, high-performance First-In/First-Out memories organized as 64-words-by-5-bits. The IDT72403 and IDT72404 also have an Output Enable ($\overline{OE}$) pin. The FIFOs accept 4-bit or 5-bit data at the data input ($D_0$ - $D_{3,4}$). The stored data stack up on a first-in/first-out basis.

A Shift Out (SO) signal causes the data at the next to last word to be shifted to the output while all other data shifts down one location in the stack. The Input Ready (IR) signal acts like a flag to indicate when the input is ready for new data (IR = HIGH), or to signal when the FIFO is full (IR = LOW). The Input Ready signal can also be used to cascade multiple devices together. The Output Ready (OR) signal is a flag to indicate that the output contains valid data (OR = HIGH), or to indicate that the FIFO is empty (OR = LOW). The Output Ready signal can also be used to cascade multiple devices together.

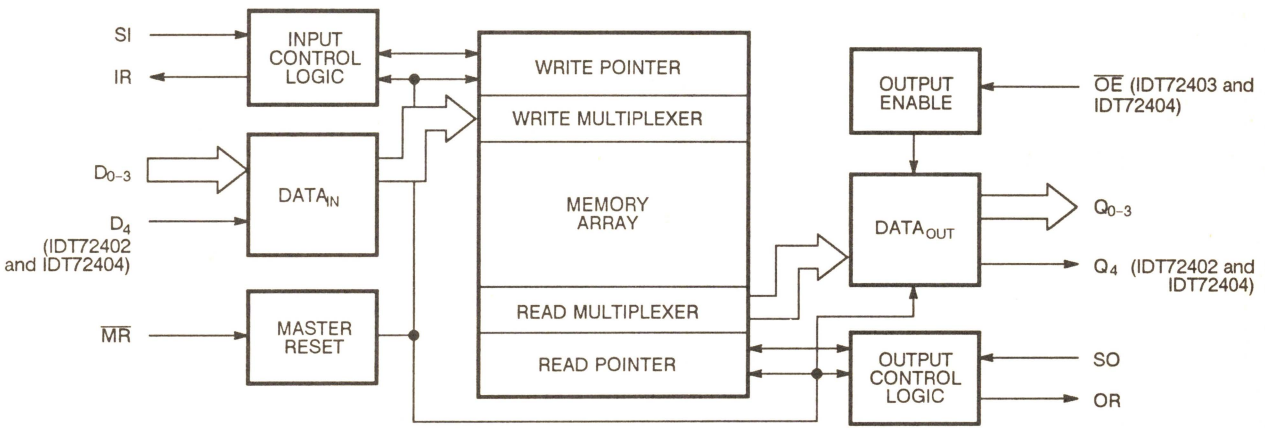
Width expansion is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready pin of the receiving device is connected to the Shift Out pin of the sending device, and the Output Ready pin of the sending device is connected to the Shift In pin of the receiving device.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The45MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

## FUNCTIONAL BLOCK DIAGRAM

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# 8-BIT CMOS VIDEO DAC

**IDT75C18**

Integrated Device Technology

## FEATURES:

- Graphics-ready
- Pin- and function-compatible with TRW TDC1018
- 8 bits, 1/2 LSB linearity
- 70, 100, 125MHz models available
- ECL-compatible inputs
- Low power dissipation < 400mW
- Power supply noise rejection > 50dB
- Registered data and video controls
- Differential current outputs
- Flexible video controls
- Inherently low glitch energy
- Multiplying mode capability
- Single 5V power supply
- Available in 24-pin hermetic DIP, 24-pin plastic DIP and 28-pin LCC
- Military product is compliant to MIL-STD-883, Class B

## DESCRIPTION:

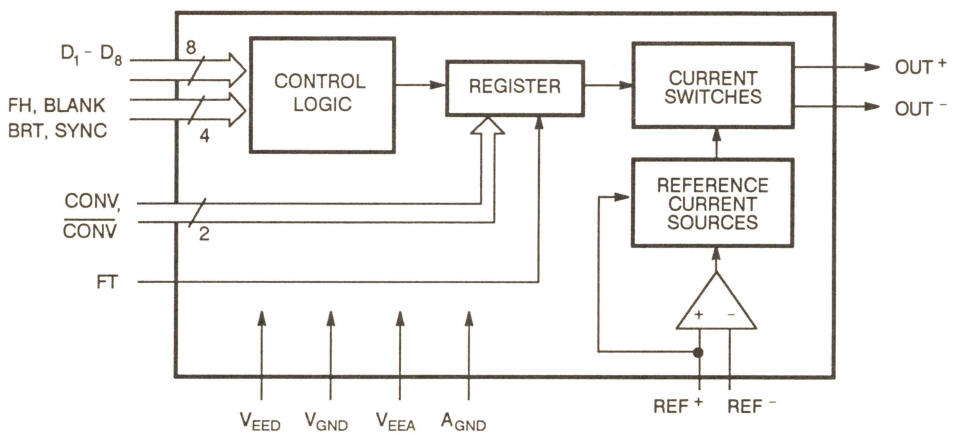
The IDT75C18 is a 70/100/125 MegaSample per Second (MSPS), 8-bit Digital to Analog Converter. It can directly drive a doubly terminated 75Ω load to levels compatible with RS-343A. Four special controls for blanking, synchronization and highlighting allow the device to be used in typical video applications with no extra components

The IDT75C18 is built using IDT's high-performance CEMOS ™ process. Innovative design methods, which include on-chip data registers and precise matching of propagation delays, as well as an improved segmenting/decoding architecture, significantly reduce glitch energy. The IDT75C18 offers high-performance and low power in a 24-pin hermetic DIP, 24-pin plastic DIP or 28-pin LCC.

The IDT75C18 is pin- and function-compatible with the TRW TDC1018, with the advantage of low power due to CMOS processing. Besides providing higher reliability by running cooler, power supply requirements are reduced. Another advantage of the lower power dissipation is that this part may be packaged in a space-saving, cost-effective, 0.3-inch plastic package.

The IDT75C18 military DAC is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS TRIPLE 8-BIT PALETTE DAC™

**PRELIMINARY**
**IDT75C458**

## FEATURES:

- 125/100/75MHz operating speed
- Fixed pipeline delay: 8 clock cycles
- Pin- and function-compatible with Brooktree BT458
- Triple 8-bit DACs
- Integral and differential linearity < 1/2LSB
- 256 x 24 Dual-Ported Color Palette RAM
- 4 x 24 Dual-Ported Overlay Palette RAM
- Multiplexed TTL pixel and overlay inputs
- RS-343A compatible RGB outputs
- Universal 8-bit MPU interface
- CEMOS ™ monolithic construction
- Single 5V power supply
- 84-pin ceramic and plastic PGA package
- Typical power dissipation: 1000mW
- Military product is compliant to MIL-STD-883, Class B

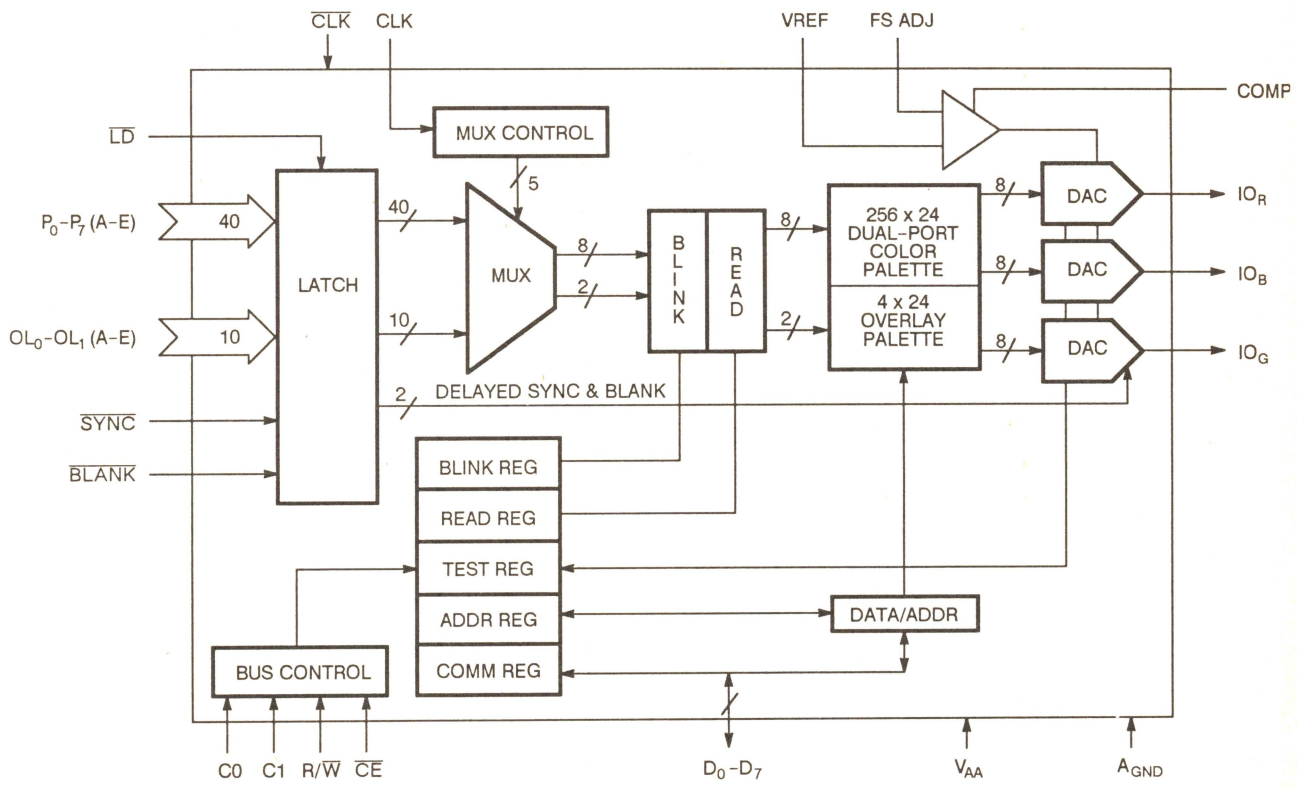
## DESCRIPTION:

The IDT75C458 is a triple 8-bit video DAC with on-chip, dual-ported color palette memory. This chip is specifically designed for the display of high resolution color graphics. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on-chip.

The IDT75C458 supports up to 259 simultaneous colors from a palette of 16.8 million. Other features included on-chip are programmable blink rates, bit plane masking and blinking as well as a color overlay capability. The IDT75C458 generates RS-343A compatible red, green, and blue video outputs which are capable of directly driving a doubly terminated 75Ω coaxial cable.

The IDT75C458 military DACs are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS FLASH A/D CONVERTER

**IDT75C48**

## FEATURES:

- 8-bit resolution
- 20 MSPS conversion rate
- Pin- and function-compatible with TRW 1048
- Low power consumption: 500mW
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase < 1 Degree
- Differential Gain < 2%
- 1/2 LSB linearity
- Selectable output formats
- TTL-compatible
- Available in 28-pin Plastic DIP, CERDIP and LCC
- Military product is compliant to MIL-STD-883, Class B

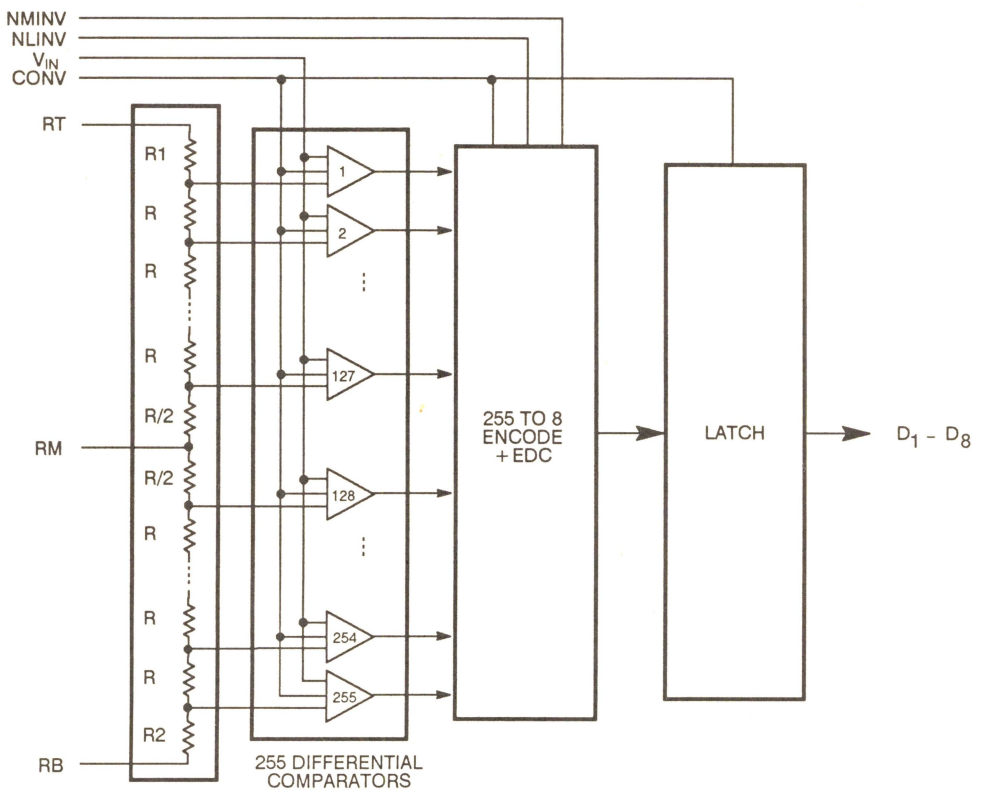
## DESCRIPTION:

The IDT75C48 is a 20 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 7MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption, due to CEMOS™ processing, virtually eliminates thermal considerations. The IDT75C48 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C48 consists of a reference voltage generator, 255 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. Two control inputs allow the output coding format to be programmed for straight binary or offset two's complement in either the true or inverted form.

The IDT75C48 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# CMOS FLASH A/D CONVERTER

**PRELIMINARY IDT75C58**

## FEATURES:

- 8-bit resolution
- 20 MSPS conversion rate
- Overflow Output
- Low power consumption: 500mW
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Tri-state outputs
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase = 1 Degree
- Differential Gain = 2%
- 1/2 LSB linearity
- TTL-compatible
- Available in 28-pin CERDIP and Plastic DIP or LCC
- Military product is compliant to MIL-STD-883, Class B

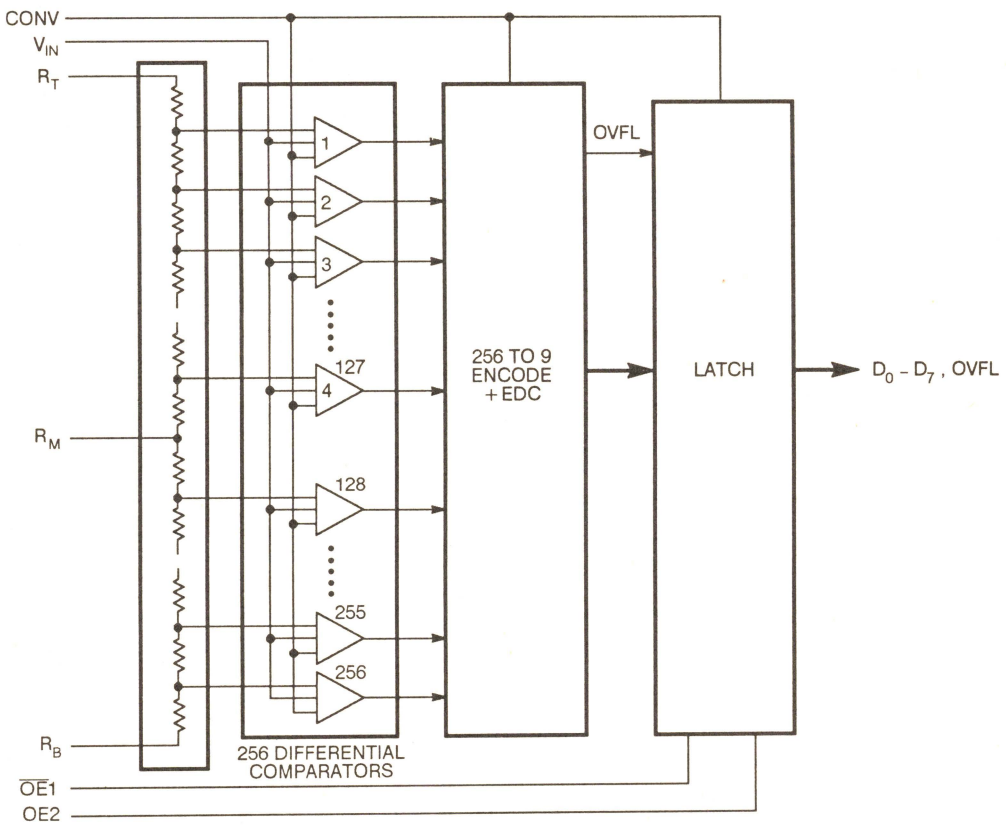
## DESCRIPTION:

The IDT75C58 is a 20 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 7MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption due to CEMOS™ processing virtually eliminates thermal considerations. The IDT75C58 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C58 consists of a reference voltage generator, 255 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. An additional comparator detects an Overflow condition ($V_{IN}$ more positive than Full-Scale – 1LSB) and activates the OVFL output. This output, together with two output enable inputs ($\overline{OE1}$ and OE2), allow the stacking of two IDT75C58s for 9-bit resolution with no external components.

The IDT75C58 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# FAST CMOS EEPROM 16K (2K x 8-BIT)

**PRELIMINARY IDT78C16A**

## FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 70ns (max.)
  - Commercial: 55ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{DATA}$ Polling—detection of write cycle completion
- Low-power CEMOS™ technology
  - 125mA active current
  - 0.9mA standby current (full CMOS)
- Data protection circuitry ($V_{CC}$ lockout for $V_{CC}$ < 4.0V) provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- JEDEC approved byte-wide pinout
- 24-pin THINDIP (300 mil.), 24-pin DIP (600 mil.) and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

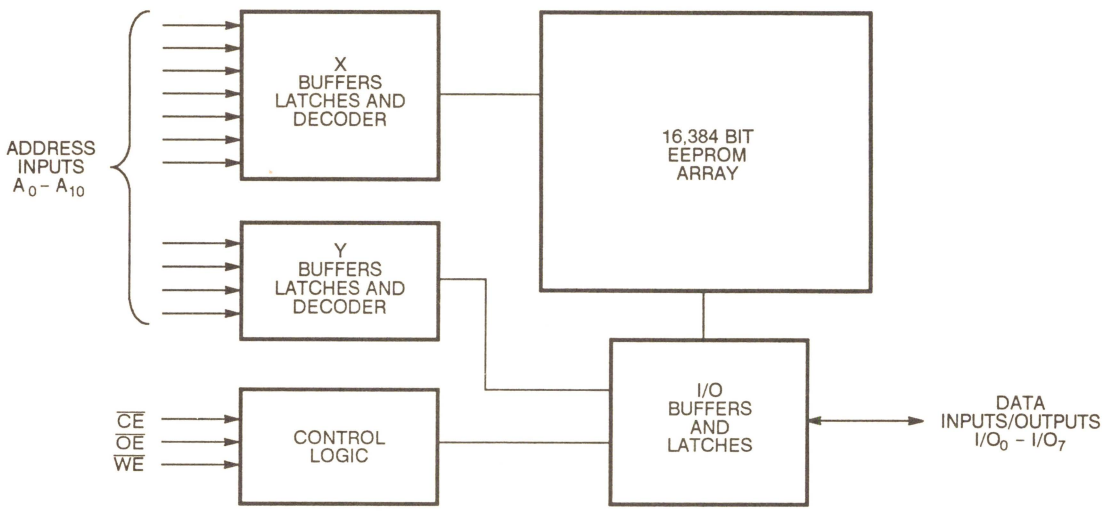
The IDT78C16A is a 5 volt only 2K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM). This high-speed CEMOS™ EEPROM is written on a byte basis and provides 16,384 bits of non-volatile data storage (data retention in excess of 100 years). Its fast read access time allows zero wait state read cycles with high-performance microprocessors.

Writing is simplified by an internal charge-pump and timer circuit which eliminates the need for special external programming voltage and write pulse shaping circuits. Byte erase before write occurs automatically and input buffers, latches and internal timer free the host system for other tasks during the write cycle. A $\overline{DATA}$ Polling mode provides a method for determining write cycle completion. The IDT78C16A also contains a dual voltage detection logic circuit which allows the device to be used in older applications which incorporate external programming circuits.

The IDT78C16A is function- and pinout-compatible with the IDT6116, 2K x 8 static RAM. It is ideal for systems requiring non-volatility and in-system data modifications.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# FAST CMOS EEPROM WITH SERIAL PROTOCOL CHANNEL (SPC™) 16K (2K x 8-BIT)

**IDT78C18A**

## FEATURES:

- 2K x 8 EEPROM with serial write and readback
- 5 volt only operation
- Fast access times
  - Military: 70/90/100/120ns
  - Commercial: 55/70/90/100ns
- Low-power CEMOS™ technology
  - Active Current: 100mA
  - Standby Current (full CMOS): 0.9mA
- Serial Protocol Channel (SPC) allows load and readout of the nonvolatile memory array over a 4-wire channel
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- Data protection circuitry ($V_{CC}$ lockout for $V_{CC}$ < 4.0V) provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Available in 28-pin THINDIP and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

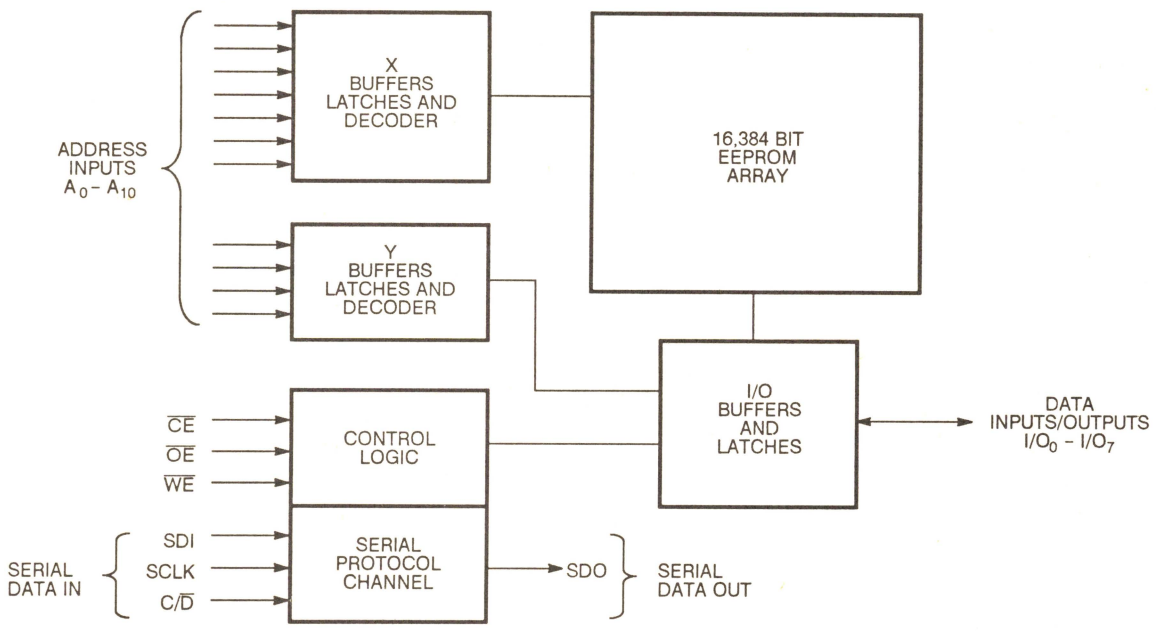
The IDT78C18A is a 5 volt only 2K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM) with Serial Protocol Channel (SPC). SPC complements the EEPROM's parallel information path by providing a serial link (4 additional pins) by which its nonvolatile array can be loaded or read. The IDT78C18A is written on a byte basis and provides 16,384 bits of nonvolatile data storage (data retention in excess of 100 years). Fast read access times allow zero wait state cycles with high-performance microprocessors.

Writing is simplified by an internal charge-pump and timer circuit which eliminates the need for external programming voltage and write pulse shaping circuits. Internal latches free the host system for other tasks during a write cycle. Byte erase before write occurs automatically. A $\overline{\text{DATA}}$ Polling mode is provided for determining write cycle completion.

The IDT78C18A is ideal for systems requiring nonvolatility and in-system data modifications. With SPC, a serial link can be established during board layout for easy field updates of code changes.

The IDT78C18A military EEPROM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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# 256K (256K x 1-BIT) CMOS STATIC RAM SIP MODULE

**IDT7MC156**

## FEATURES:

- High-density 256K (256K x 1) CMOS static RAM module
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 28-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 600mW (typ.)
  - Full standby: less than 30mW (typ.)
- Utilizes IDT7187s high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

## DESCRIPTION:

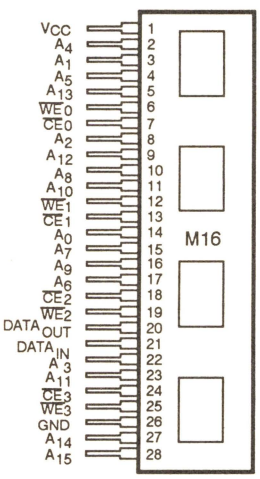
The IDT7MC156 is a 256K (256K x 1-bit) high-speed static RAM module constructed on a co-fired ceramic substrate using four IDT7187 64K x 1 static RAMs in surface mount packages.

The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC156 is offered in a 28-pin ceramic SIP (single in-line package). At only 350 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing greater than three IDT7MC156 modules to be stacked per inch of board space.

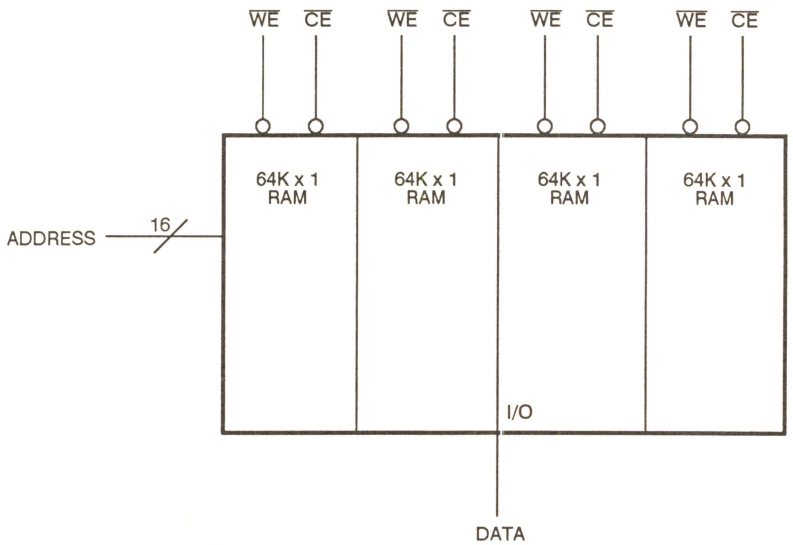
The IDT7MC4156 is available with maximum access times as fast as 25ns with maximum power consumption of 1.35 watts. The module also offers a full standby mode of 330mW (max.).

All inputs and outputs of the IDT7MC156 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

## PIN CONFIGURATION




## FUNCTIONAL BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| $A_0$–$A_{15}$ | Address Lines |
| $D_{IN}$ | Data Input |
| $D_{OUT}$ | Data Output |
| $\overline{CS}_{0-3}$ | Chip Enable |
| $\overline{WE}_{0-3}$ | Write Enable |
| $V_{CC}$ | Power |
| GND | Ground |

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# 256K (256K x 1-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

**IDT7MP156**

## FEATURES:

- High-density 256K (256K x 1) CMOS static RAM module
- Cost- effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 28-pin SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 600mW (typ.)
  - Full standby: less than 30mW (typ.)
- Utilizes IDT7187 high-performance 64K static RAMs produced with advanced CEMOS technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

## DESCRIPTION

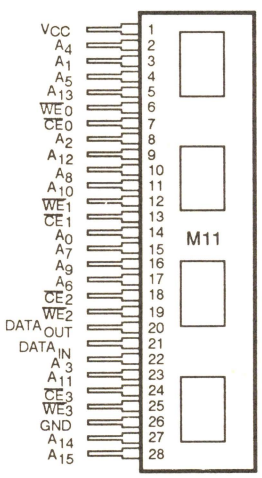
The IDT7MP156 is a 256K (256K x 1-bit) high-speed static RAM module constructed on an epoxy lamintae surface using four IDT7187 64K x 1 static RAMs in surface mount packages. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology.

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP156 is offered in a 28-pin SIP (single in-line package). The IDT7MP156 can be mounted on 200 mil centers, yielding 1.25 megabits of memory in less than 3 square inches of board space.

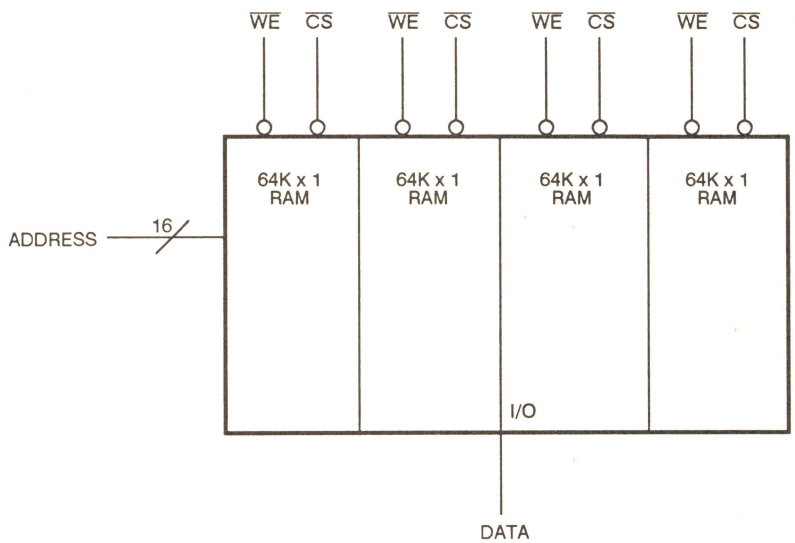
The IDT7MP156 is available with maximum access times as fast as 25ns with maximum power consumption of 1.35 watts. The module also offers a full standby mode of 330mW (max.).

All inputs and outputs of the IDT7MP156 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

## PIN CONFIGURATION




## FUNCTIONAL BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| $A_0$-$A_{15}$ | Address Lines |
| $D_{IN}$ | Data Input |
| $D_{OUT}$ | Data Output |
| $\overline{CE}_{0-3}$ | Chip Enable |
| $\overline{WE}_{0-3}$ | Write Enable |
| $V_{CC}$ | Power |
| GND | Ground |

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# 1 MEGABIT CMOS STATIC RAM MODULE

**IDT7M624S**

Integrated Device Technology

## FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 4.8W (typ. in 64K x 16 organization)
  - Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Pin-compatible with IDT7M656 (256K RAM module)
- Single 5V(±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

## DESCRIPTION:

The IDT7M624 is a 1024K-bit high-speed CMOS static RAM constructed on a multi-layered ceramic substrate using 16 IDT7187 64K x 1 static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

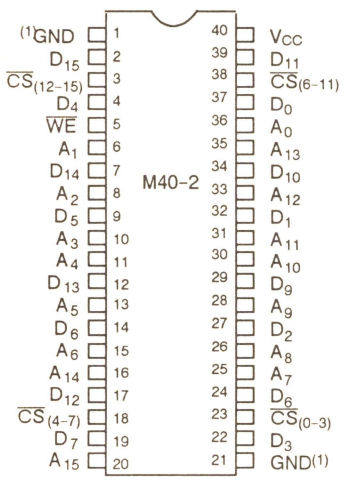
The IDT7M624 is available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 10.7W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 4.5W (max.) and a full standby mode of 1.7W (max.).

The IDT7M624 is offered in a 40-pin, 900 mil center sidebraze DIP to take advantage of the compact IDT7187s in leadless chip carriers.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

All IDT military module semiconductor components are compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

## PIN CONFIGURATION

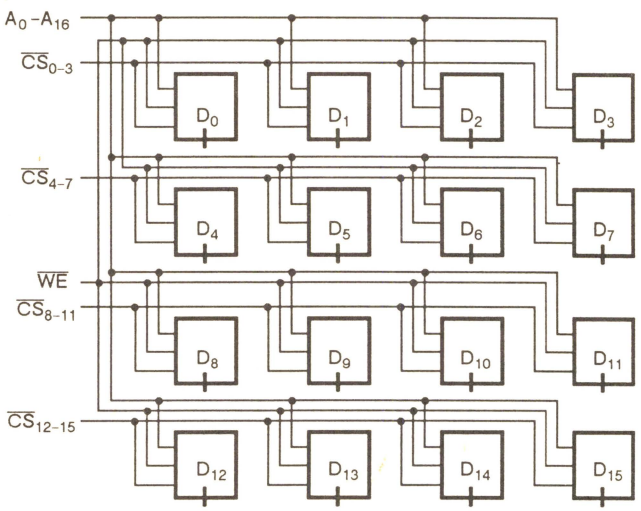



DIP
TOP VIEW

## PIN NAMES

| | |
|---|---|
| $A_{0-16}$ | Address |
| $I/O_{0-8}$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | Power |
| GND | Ground |

## FUNCTIONAL BLOCK DIAGRAM




**NOTES:**

1. Both GND pins need to be grounded for proper operation.

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# 64K (8K x 8-BIT) CMOS EEPROM MODULE

**IDT7M7864**

## FEATURES:

- Equivalent to JEDEC standard 8K x 8 monolithic EEPROM
- 8,192 x 8 CMOS EEPROM module complete with decoder and decoupling capacitor
- Fast access times
  - Military: 85/105/115/135ns
  - Commercial: 65/80/100/110ns
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ns max.
- $\overline{DATA}$ Polling—detection of write cycle completion
- Utilizes IDT78C16As—high-performance 16K EPROMs
- Single 5V (±10%) power supply
- Data protection circuitry ($V_{CC}$ lockout for $V_{CC}$ < 4.0V)
- Provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Available in 28-pin, 600 mil DIP
- Military modules available with semiconductor components compliant to the latest revision of MIL-STD-883, Class B

## DESCRIPTION:

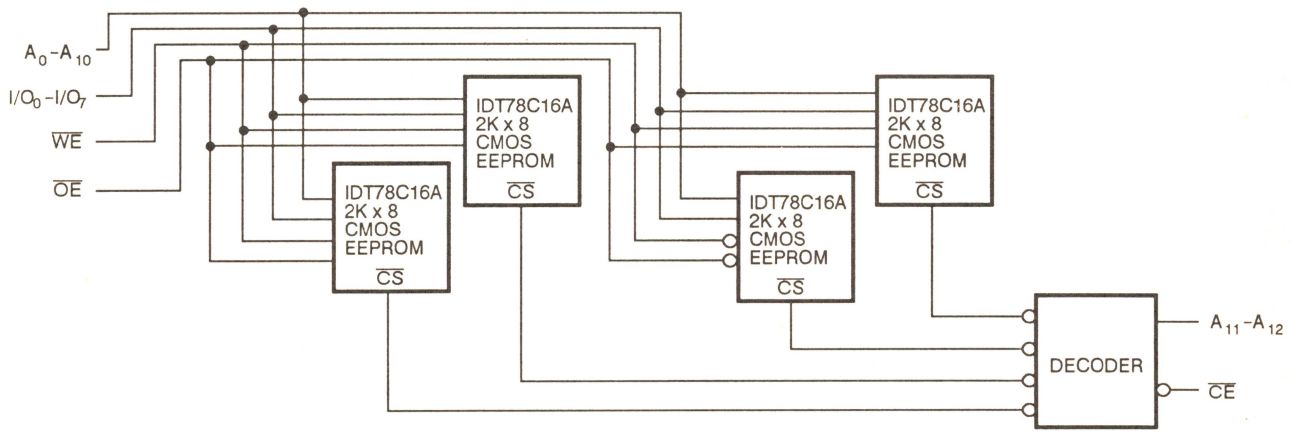
The IDT7M7864 is a 5 volt only 8K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM) constructed on a co-fired ceramic substrate using four IDT78C16A (2K x 8) EEPROMs in leadless chip carriers. Functional equivalence to monolithic 64K EEPROMs is achieved by utilization of an on-board decoder circuit that interprets the higher order address A11 and A12 to select one of the four 2K x 8 EEPROMs.

The IDT7M7864 offers a reduced power standby mode. When $\overline{CE}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as these conditions are held. In standby mode, the module consumes less than 440mW. Substantially lower power levels can be achieved in the $1_{SB1}$ mode (less than 20mW max.).

The pinout of the IDT7M7864 is equivalent to monolithic 64K EEPROMs. Its fast read access time allows zero wait state read cycles with high-performance microprocessors.

All IDT module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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Integrated Device Technology, Inc.

# 512K (64K x 8-BIT or 64K x 9-BIT) CMOS STATIC RAM MODULE

**IDT7M812**
**IDT7M912**

## FEATURES:

- High-density 512K-bit CMOS static RAM module
- 64K x 8 (IDT7M812) or 64K x 9 (IDT7M912) configuration
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 2.4W (typ. in 64K x 8 organization)
  - Standby: 240μW (typ. in 64K x 8 organization)
- Utilizes 8 (IDT7M812) or 9 (IDT7M912) IDT187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 40-pin, 600 mil center sidebraze DIP, achieving very high memory density
- Single 5V(±10%) power supply
- Dual $V_{CC}$ and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

## DESCRIPTION:

The IDT7M812/IDT7M912 are 512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using 8 IDT7187 64K x 1 static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

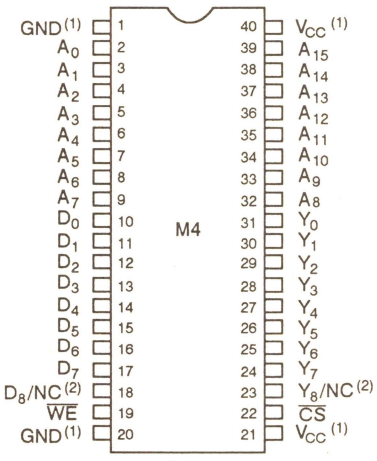
The IDT7M812/IDT7M912 are available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 5.9W (IDT7M912, 64K x 9 option). The Module also offers a standby power mode of less than 2.5W (max.) and a full standby mode of 1W (max.).

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64K x 9) option can provide more flexibility in system application for error detection, parity bit, etc.

All inputs and outputs of the IDT7M812/IDT7M912 are TTL-compatible and operate from a single 5V supply. (NOTE: Both $V_{CC}$ pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing access and cycles times for ease of use.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

## PIN CONFIGURATION

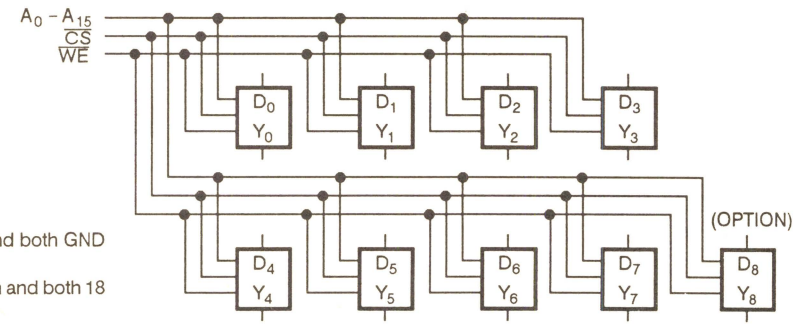



DIP
TOP VIEW

## PIN NAMES

| | |
|---|---|
| $A_0$–$A_{15}$ | Address |
| $D_0$–$D_8$ | Data Input |
| $Y_0$–$Y_8$ | Data Output |
| $\overline{CS}$ | Chip Select |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | Power |
| GND | Ground |

## FUNCTIONAL BLOCK DIAGRAM




**NOTES:**

1. Both $V_{CC}$ pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. Pin 18 is $D_8$ and pin 23 is $Y_8$ in 64K x 9 (IDT7M912) option and both 18 and 23 are NC in 64K x 8 (IDT7M812) option.

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# 1 MEGABIT (64K x 16-BIT) & 512K (32K x 16-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

**IDT8MP624S**
**IDT8MP612S**

## FEATURES:

- High-density 1024K/512K-bit CMOS static RAM module
- 64K x 16 organization (IDT8MP624) with 32K x 16 option (IDT8MP612)
- Upper byte ($I/O_{9-16}$) and lower byte ($I/O_{1-8}$) separated control
  – Allows flexibility in application
- Fast access time: 40ns (max.)
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Offered in a SIP (single in-line) package for maximum space-savings
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

## DESCRIPTION:

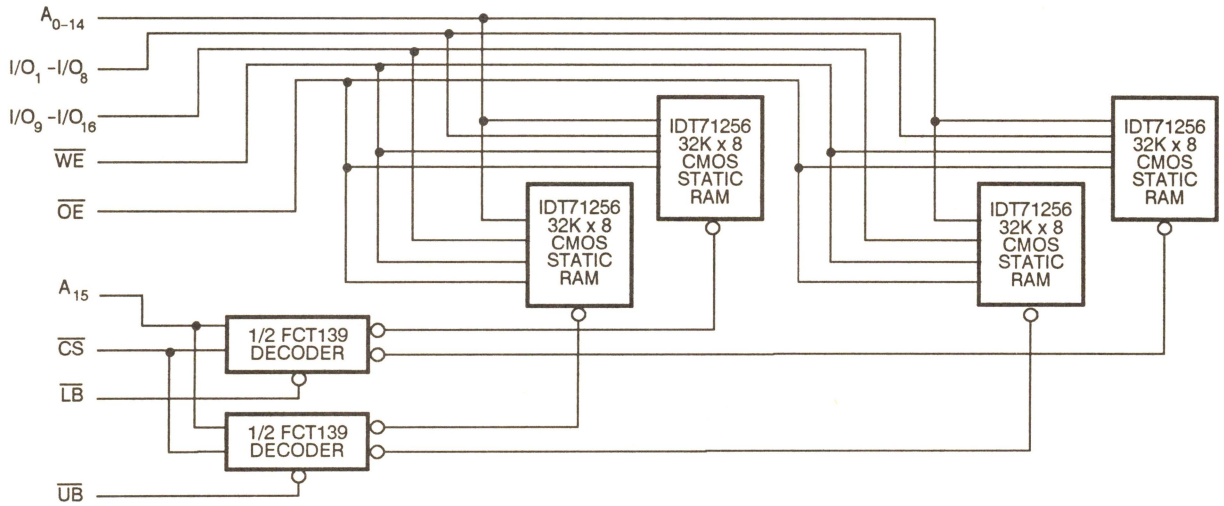
The IDT8MP624S/IDT8MP612S are 1024K/512K high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT71256 32K x 8 static RAMs (IDT8MP624S) or two IDT71256 static RAMs (IDT8MP612S) in plastic surface-mount packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address $A_{15}$ to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte ($I/O_{1-8}$) and upper byte ($I/O_{9-16}$) control, respectively. (On the IDT8MP612S 32K x 16 option, $A_{15}$ needs to be externally grounded for proper operation.) Extremely high speeds are achieved by the use of IDT71256s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 1024K/512K static RAMs available.

The IDT8MP624S/IDT8MP612S are available with access times as fast as 40ns over the commercial temperature range, with maximum operating power consumption of only 1.8W (64K x 16 option). The module also offers a full standby mode of 330mW (max.)

The IDT8MP624S/IDT8MP612S are offered in a 40-pin plastic SIP package. For the 40-pin JEDEC standard DIP, refer to the IDT8M624S/IDT8M612S.

All inputs and outputs of the IDT8MP624S/IDT8MP612S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

## FUNCTIONAL BLOCK DIAGRAM

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# 1 MEGABIT (64K x 16-BIT) & 512K (32K x 16-BIT) CMOS STATIC RAM MODULE

**IDT8M624L**
**IDT8M612L**

Integrated Device Technology

## FEATURES:

- High-density 1024K/512K-bit CMOS static RAM module
- 64K x 16 organization (IDT8M624L) with 32K x 16 option (IDT8M612L)
- Upper byte ($I/O_{9-16}$) and lower byte ($I/O_{1-8}$) separated control
  – Allows flexibility in application
- Equivalent to JEDEC standard for future monolithic 64K x 16/ 32K x 16 static RAMs
- High-speed – 85ns (max.) commercial temperature range
- Low power consumption
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (± 10%) power supply
- Inputs and outputs directly TTL-compatible

## DESCRIPTION:

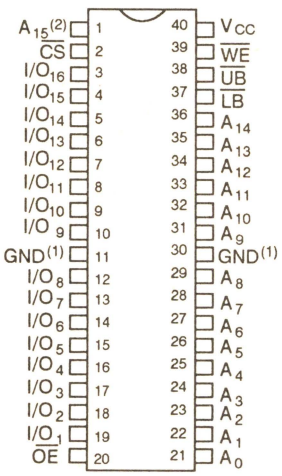
The IDT8M624L/IDT8M612L are 1024K/512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using four 32K x 8 static RAMs (IDT8M624L) or two 32K x8 static RAMs (IDT8M612L) in leadless chip carriers. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address $A_{15}$ to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte ($I/O_{1-8}$) and upper byte ($I/O_{9-16}$) control, respectively. (On the IDT8M612L 32K x 16 option, $A_{15}$ needs to be externally grounded for proper operation.)

The IDT8M624L/IDT8M612L are available with access times as fast as 85ns commercial, with maximum operating power consumption of only 825mW (max. – IDT8M624L 64K x 16 option). The module also offers a full standby mode of 2.2mW (max.).

The IDT8M624L/IDT8M612L are offered in a high-density 40-pin, 600 mil center sidebraze DIP.

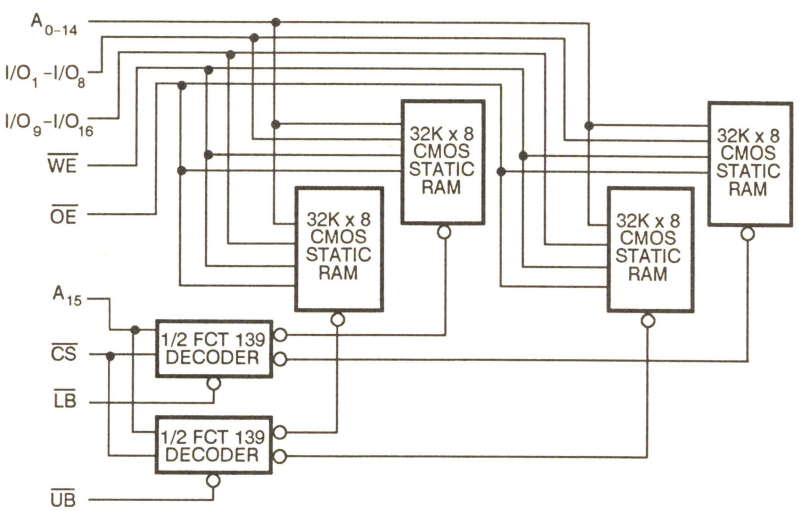
All inputs and outputs of the IDT8M624L/IDT8M612L are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

## PIN CONFIGURATION




DIP
TOP VIEW

## FUNCTIONAL BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| $A_{0-15}$ | Addresses |
| $I/O_{1-16}$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | Power |

| | |
|---|---|
| GND | Ground |
| $\overline{OE}$ | Output Enable |
| $\overline{UB}$ | Upper Byte Control |
| $\overline{LB}$ | Lower Byte Control |

**NOTES:**

1. Both GND pins need to be grounded for proper operation.
2. On IDT8M612L, 512K (32K x 16-bit) option, $A_{15}$ (pin 1) requires external grounding for proper operation.

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# 1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

**IDT8MP824S**

## FEATURES:

- High-density 1024K (128K x 8) CMOS static RAM module
- Fast access time
  - 50ns (max.) over commercial temperature range
- Low power consumption
  - Active: less than 500mW (typ.)
  - Standby: less than 8.8mW (typ.)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in a SIP (single in-line) package for maximum space-saving
- Utilizes IDT71256s—high-performance 256K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

## DESCRIPTION:

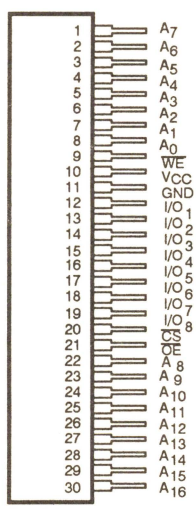
The IDT8MP824S is a1024K (131, 072 x 8-bit) high-speed static RAM constructed on an epoxy laminate substrate using four IDT71256 32K x 8 static RAMs in plastic surface mount packages. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address $A_{15}$ and $A_{16}$ to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

The IDT8MP824S is available with maximum access times as fast as 50ns over the commercial temperature range, with maximum operating power consumption of 825mW. The module also offers a full standby mode of 330mW (max.).

The IDT8MP824S is offered in a 30-pin SIP (single in-line) package. For the 32-pin JEDEC standard DIP, refer to the IDT8M824S.

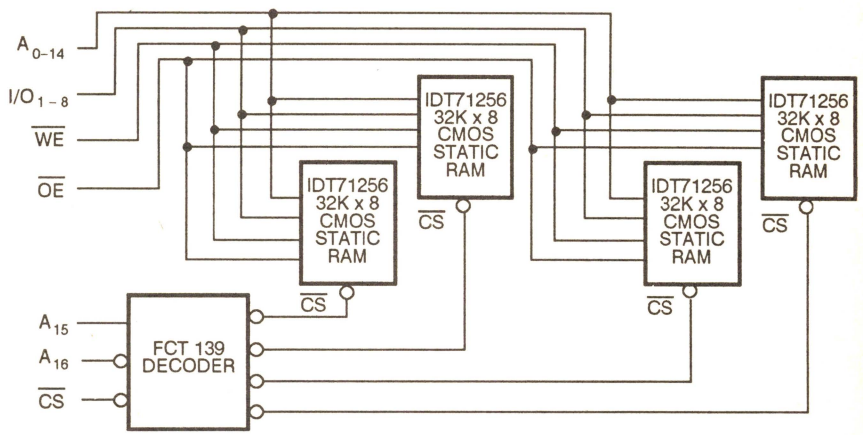
All inputs and outputs of the IDT8MP824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

## PIN CONFIGURATION




SIP
SIDE VIEW

## FUNCTIONAL BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| $A_{0-16}$ | Addresses |
| $I/O_{1-8}$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $V_{CC}$ | Power |

| | |
|---|---|
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| GND | Ground |

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Integrated Device Technology, Inc.

# 1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM MODULE

**PRELIMINARY**
**IDT8M824S**

## FEATURES:

- High-density 1024K (128K x 8) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 128K x 8 static RAMs
- High-speed
  - Commercial: 40ns (max.)
  - Military:60ns (max.)
- Low power consumption
  - Active: less than 550mW (typ.)
  - Standby: less than 20mW (typ.)
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 32-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

## DESCRIPTION:

The IDT8M824S is a1024K (131,072 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT71256 32K x 8 static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address $A_{15}$ and $A_{16}$ to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

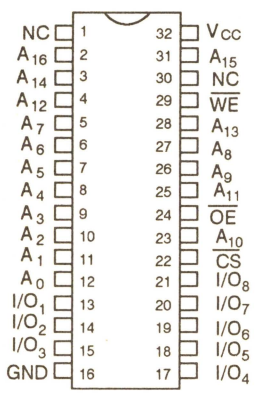
The IDT8M824S is available with maximum access times as fast as 40ns for commercial temperature range, with maximum power consumption of 1.2 watts. The module offers a full standby mode of 440mW (max.).

The IDT8M824S is offered in a 32-pin, 600 mil center sidebraze DIP, adhering to JEDEC standards for one megabit monolithic pinouts, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT8M824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

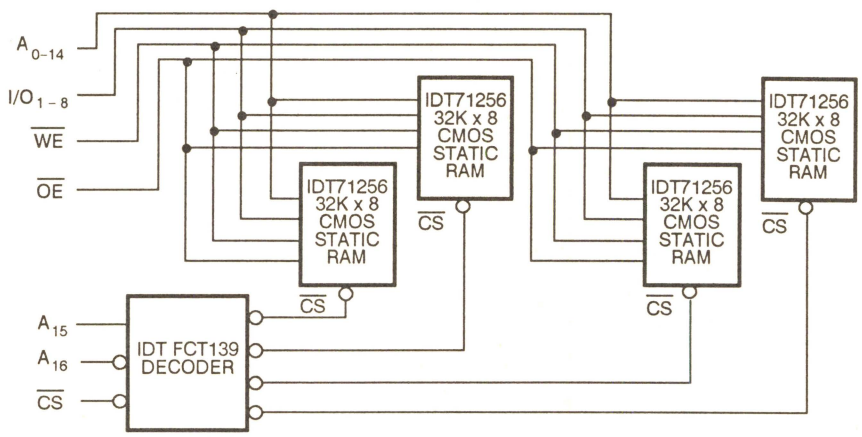
All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

## PIN CONFIGURATION




DIP
TOP VIEW

## FUNCTIONAL BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| $A_{0-16}$ | Addresses |
| $I/O_{0-8}$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $V_{CC}$ | Power |

| | |
|---|---|
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| GND | Ground |

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# 256K (16K x 16-BIT) & 128K (8K x 16-BIT) CMOS STATIC RAM PLASTIC SIP MODULES

**IDT8MP656S**
**IDT8MP628S**

## FEATURES:

- High-density 256K/128K CMOS static RAM modules
- 16K x 16 organization (IDT8MP656S) with 8K x 16 option (IDT8MP628)
- Upper byte ($I/O_{9-16}$) and lower byte ($I/O_{1-8}$) separated control
  - Flexibility in application
- Fast access times
  - 50ns (max.): IDT8MP656S over commercial temperature range
  - 35ns (max.): IDT8MP628S over commercial temperature range
- Low power consumption
  - Active: less than 1W (typ. in 16K x 16 organization)
  - Standby: less than 1mW (typ.)
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in an SIP (single in-line) package for maximum space-savings
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

## DESCRIPTION:

The IDT8MP656S/IDT8MP628S are 256K/128K-bit high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT7164 8K x 8 static RAMs (IDT8MP656S) or two IDT7164 static RAMs (IDT8MP628S) in plastic surface mount packages.

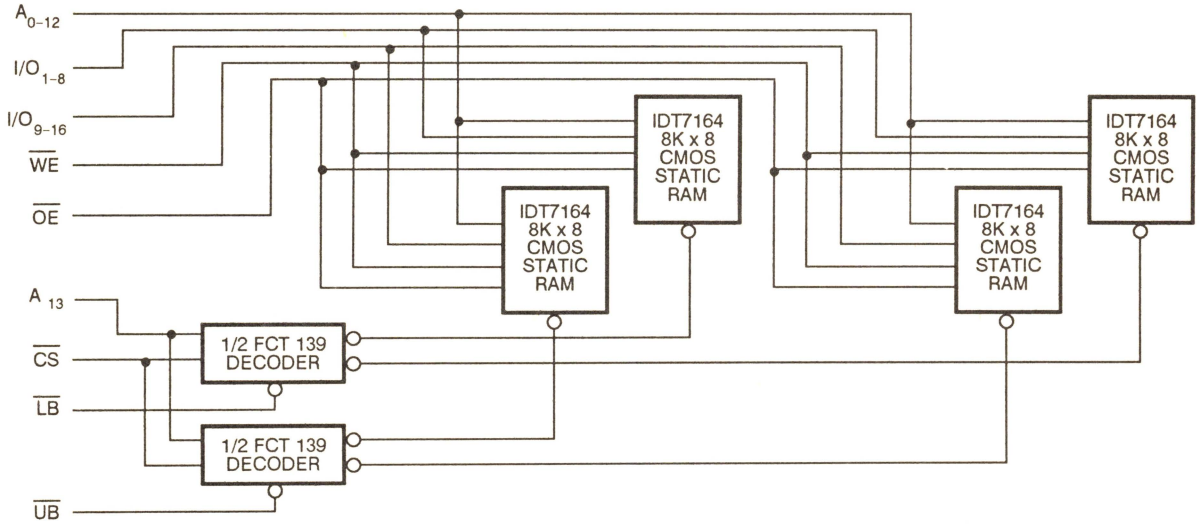
Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address $A_{13}$ to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte ($I/O_{1-8}$) and upper byte $I/O_{9-16}$) control, respectively. (On the IDT8MP628S 8K x 16 option, $A_{13}$ needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s, fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

The IDT8MP656S/IDT8MP628S are available with maximum operating power consumption of only 1.8W (IDT8MP656S 16K x 16 option). The modules also offer a full standby mode of 330mW (max.).

The IDT8MP656S/IDT8MP628S are offered in a 40-pin plastic SIP. For the JEDEC standard 40-pin DIP, refer to the IDT8M656S/IDT8M628S.

All inputs and outputs of the IDT8MP656S/IDT8MP628S are TTL-compatible and operate from a single 5V supply. (NOTE: Both $V_{CC}$ pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

## FUNCTIONAL BLOCK DIAGRAM

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# 256K (16K x 16-BIT) & 128K (8K x 16-BIT) CMOS STATIC RAM MODULE

**IDT8M656S**
**IDT8M628S**

Integrated Device Technology

## FEATURES:

- High-density 256K/128K-bit CMOS static RAM modules
- 16K x 16 organization (IDT8M656) with 8K x 16 option (IDT8M628)
- Upper byte ($I/O_{9-16}$) and lower byte ($I/O_{1-8}$) separated control
  - Flexibility in application
- Equivalent to JEDEC standard for future monolithic 16K x 16/8K x 16 static RAMs
- High-speed
  - Military: 50ns (max.)
  - Commercial: 40ns (max.) – IDT8M656S
    : 35ns (max.) – IDT8M628S
- Low power consumption: typically less than 825mW operating (IDT8M656), less than 40mW in standby
- Utilizes IDT7164s – high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

## DESCRIPTION:

The IDT8M656S/IDT8M628S are 256K/128K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using four IDT7164 8K x 8 static RAMs (IDT8M656S) or two IDT7164 static RAMs (IDT8M628S) in leadless chip carriers.

Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address $A_{13}$ to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte ($I/O_{1-8}$) and upper byte ($I/O_{9-16}$) control, respectively. (On the IDT8M628S 8K x 16 option, $A_{13}$ needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

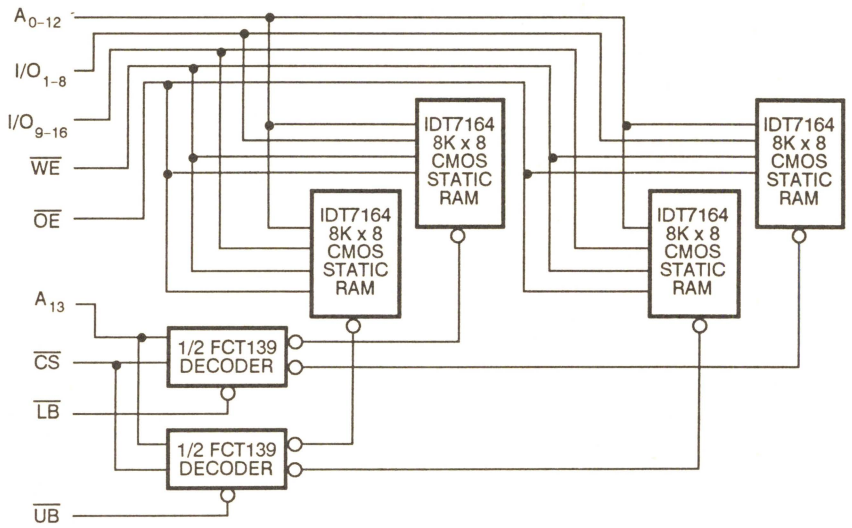
The IDT8M656S/IDT8M628S are available with access times as fast as 40ns (IDT8M656S) and 35ns (IDT8M628S) over the commercial temperature range, with maximum operating power consumption of only 1.98W (IDT8M656S 16K x 16 option). The module also offers a full standby mode of 440mW (max.).

The IDT8M656S/IDT8M628S are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7164s in leadless chip carriers.

All inputs and outputs of the IDT8M656S/IDT8M628S are TTL-compatible and operate from a single 5V supply. (NOTE: Both $V_{CC}$ pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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**MILITARY AND COMMERCIAL TEMPERATURE RANGES** **OCTOBER 1987**


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# 256K (32K x 8-BIT) CMOS STATIC RAM MODULE (Low-Power Version)

**IDT8M856L**

## FEATURES:

- High-density 256K (32K x 8-bit) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 32K x 8 static RAMs
- High-speed—45ns (max.) commercial; 55ns (max.) military
- Low power consumption; typically less than 225mW operating, less than 500μW in full standby
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Pin-compatible with IDT7M864 (8K x 8 SRAM module)
- Offered in the JEDEC standard 28-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V ( ±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

## DESCRIPTION:

The IDT8M856 is a 256K (32,768 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT7164 (8,192 x 8) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 256K static RAMs is achieved by utilization of an on-board decoder circuit that interprets the higher order address $A_{13}$ and $A_{14}$ to select one of the four 8K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

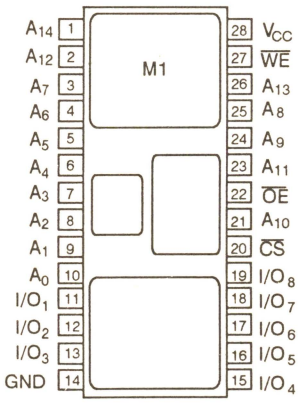
The IDT8M856 is available with maximum access times as fast as 45ns for commercial and 55ns for military temperature ranges, with maximum power consumption of only 825mW. The circuit also offers a substantially low-power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a standby mode with power consumption of only 83mW (max.).

The IDT8M856 is offered in a 28-pin, 600 mil center sidebraze DIP. This provides four times the density of the IDT7M864 (8K x 8 module) in the same socket, with only minor pin assignment changes. In addition, the JEDEC standard for 256K monolithic pinouts has been adhered to, allowing for compatibility with 256K monolithics.

All inputs and outputs of the IDT8M856 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

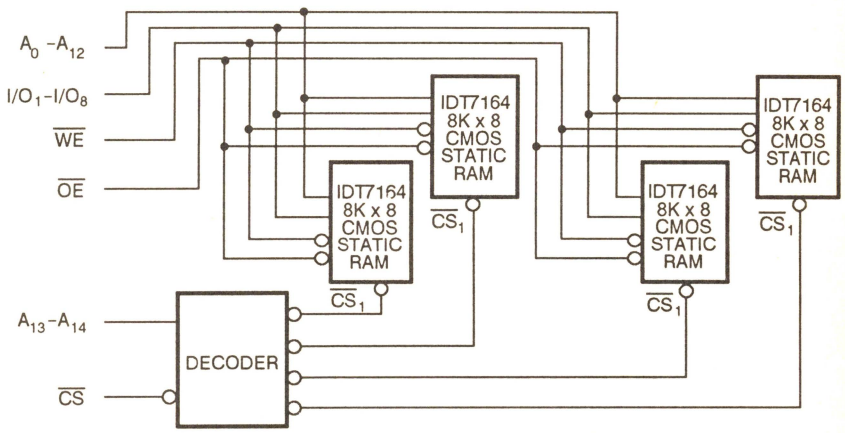
All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

## PIN CONFIGURATION




DIP, TOP VIEW

## FUNCTIONAL BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0 - A_{14}$ | Addresses | $\overline{WE}$ | Write Enable |
| $I/O_1 - I/O_8$ | Data Input/Output | $\overline{OE}$ | Output Enable |
| $\overline{CS}$ | Chip Select | GND | Ground |
| $V_{CC}$ | Power | | |

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## FEATURES:

- FCT equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- **"A" Version approximately 35% faster than FAST**
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The "FCT" series is a family of industry standard memory interface circuits that are pin compatible, functional equivalent replacements to the Fairchild FAST series, but at CMOS power levels (1/10 operation, 1/100 standby).

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
$V_{LC}$ = 0.2V; $V_{HC}$ = -0.2V
Commercial: $T_A$ = 0°C to +70°C; $V_{CC}$ = 5.0V ±5%
Military: $T_A$ = -55°C to +125°C; $V_{CC}$ = 5.0V ±10%

| SYMBOL | PARAMETER | TEST CONDITIONS [1] | | MIN. | TYP.[2] | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic High Level | | 2.0 | – | – | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic Low Level | | – | – | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., | $V_I$ = $V_{CC}$ | – | – | 5 | μA |
| | | | $V_I$ = 2.7V | – | – | 5 | |
| $I_{IL}$ | Input LOW Current | | $V_I$ = 0.4V | – | – | -5 | |
| | | | $V_I$ = GND | – | – | -5 | |
| $I_{OZ}$ | Off State (High Impedance) Output Current | $V_{CC}$ = Max., | $V_O$ = $V_{CC}$ | – | – | 10 | μA |
| | | | $V_O$ = 2.7V | – | – | 10 | |
| | | | $V_O$ = 0.4V | – | – | -10 | |
| | | | $V_O$ = GND | – | – | -10 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_N$ = -18mA | | – | -0.7 | -1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max.,[3] $V_O$ = GND | | -60 | -120 | – | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 3V, $V_{IN}$ = $V_{LC}$ or $V_{HC}$, $I_{OH}$ = -32μA | | $V_{HC}$ | $V_{CC}$ | – | V |
| | | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -300μA | $V_{HC}$ | $V_{CC}$ | – | |
| | | | $I_{OH}$ = -12mA MIL. | 2.4 | 4.3 | – | |
| | | | $I_{OH}$ = -15mA COM'L. | 2.4 | 4.3 | – | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 3V, $V_{IN}$ = $V_{LC}$ or $V_{HC}$, $I_{OL}$ = 300μA | | – | GND | $V_{LC}$ | |
| | | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 300μA | – | GND | $V_{LC}$ | |
| | | | $I_{OL}$ = 32mA MIL. | – | 0.3 | 0.5 | |
| | | | $I_{OL}$ = 48mA COM'L. | – | 0.3 | 0.5 | |
| $V_{OL}$ | Output LOW Voltage (Buffers and Transceivers) | $V_{CC}$ = 3V, $V_{IN}$ = $V_{LC}$ or $V_{HC}$, $I_{OL}$ = 300μA | | – | GND | $V_{LC}$ | |
| | | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 300μA | – | GND | $V_{LC}$ | |
| | | | $I_{OL}$ = 48mA MIL. | – | 0.3 | 0.55 | |
| | | | $I_{OL}$ = 64mA COM'L. | – | 0.3 | 0.55 | |
| $I_{CCQ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max. $V_{IN}$ ≥ $V_{HC}$ ; $V_{IN}$ ≤ $V_{LC}$ $f_{CP}$ = $f_I$ = 0 | | – | 0.001 | 1.5 | mA |
| $I_{CCT}$ | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC}$ = Max. $V_{IN}$ = 3.4V[4] | | – | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current | $V_{CC}$ = Max. Outputs Open One Bit Toggling 50% Duty Cycle | $V_{IN}$ ≥ $V_{HC}$ $V_{IN}$ ≤ $V_{LC}$ | – | 0.15 | 0.25 | mA/ MHz |

**NOTES:**

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.

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## HIGH-PERFORMANCE SYSTEMS SOLUTIONS

| | 16 | 18 | 20 | 22 | 24 | 28 | 32 | 40 | 44 | 48 | 52 | 64 | 68 | 84 | 108 | 144 | 208 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **THROUGH HOLE TECHNOLOGY** | | | | | | | | | | | | | | | | | |
| Plastic DIP (300 mil) | ● | ● | ● | ● | ● | ● | | | | | | | | | | | |
| Plastic DIP (600 mil) | | | | | ● | ● | | ● | | ● | | | | | | | |
| Plastic DIP (900 mil) | | | | | | | | | | | | ● | | | | | |
| CERDIP (300 mil) | ● | ● | ● | | ● | | | | | | | | | | | | |
| CERDIP (600 mil) | | | | | ● | ● | | ● | | | | | | | | | |
| Sidebraze DIP (300 mil) | | | ● | ● | ● | ● | | | | | | | | | | | |
| Sidebraze DIP (400 mil) | | | | | | ● | | | | | | | | | | | |
| Sidebraze DIP (400 mil Fine Pitch) | | | | | | | | | | ● | | | | | | | |
| Sidebraze DIP (600 mil) | | | | | ● | ● | | ● | | ● | | | | | | | |
| Sidebraze DIP (600 mil Fine Pitch) | | | | | | | | | | | | | ● | | | | |
| Sidebraze DIP (900 mil) | | | | | | | | | | | | ● | | | | | |
| Topbraze DIP (900 mil) | | | | | | | | | | | | ● | | | | | |
| Pin Grid Array (Cavity Up) | | | | | | | | | | | | | ● | | ● | | ● |
| Pin Grid Array (Cavity Down) | | | | | | | | | | | | | ● | | | ● | |
| **SURFACE MOUNT TECHNOLOGY** | | | | | | | | | | | | | | | | | |
| Plastic Small Outline (SOIC) | ● | ● | ● | | ● | ● | | | | | | | | | | | |
| Leadless Chip Carrier (Sq.) | | | ● | | | ● | | | ● | ● | ● | | ● | | | | |
| Leadless Chip Carrier (Rect.) | | | ● | ● | ● | ● | ● | | | | | | | | | | |
| Leadless Chip Carrier (Fine Pitch) | | | | | | | | | | ● | | | ● | | | | |
| Plastic Leaded Chip Carrier (Sq.) | | | ● | | | ● | | | ● | | ● | | ● | ● | | | |
| Plastic Leaded Chip Carrier (Rect.) | | | | | | | ● | | | | | | | | | | |
| CERPACK | ● | | ● | | ● | | | | | | | | | | | | |
| Flatpack | | | ● | | ● | ● | | | | | | | | | | | |
| Ceramic Quad Flatpack | | | | | | | | | | ● | | ● | | | | | |
| Plastic Quad Flatpack | | | | | | | | | | | | | | | ● | | |
| Plastic Pin Grid Array (Cavity Up) | | | | | | | | | | | | | ● | | | | ● |
| Plastic Pin Grid Array (Cavity Dwn) | | | | | | | | | | | | | ● | ● | | | |



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**INTEGRATED POWER SEMICONDUCTORS, LTD.**

## Motor Driver Selection Guide

| Function | Part Number | Volts | Amps | Logic | Internal Clamp Diodes |
|---|---|---|---|---|---|
| H Bridge | IP3D03 | 50 | 4.0 | Yes | Yes |
| | IP3D03A | 80 | 4.0 | Yes | Yes |
| | IP3M02 | 15 | .25 | Yes | Yes |
| Dual Bridge | IP1M10 | 36 | 0.2 | Yes | Yes |
| | IP1M20 | 36 | 0.2 | Yes | Yes |
| | IP293 | 36 | 1.0 | Yes | |
| | IP293D | 36 | 0.6 | Yes | Yes |
| | IP293DA | 36 | 1.0 | Yes | Yes |
| | IP293E | 36 | 1.0 | Yes | |
| | IP293ED | 36 | 1.0 | Yes | Yes |
| | IP293C | 36 | 1.0 | Yes | |
| | IP293CD | 36 | 1.0 | Yes | Yes |
| | IP293L | 15 | 0.5 | Yes | |
| | IP293LD | 15 | 0.5 | Yes | Yes |
| Stepper Motor Control/ Driver | IP3717 | 40 | 0.8 | Yes | Yes |
| | IP3717A | 40 | 0.8 (Lower Sat) | Yes | Yes |
| | IP3770 | 40 | 1.2 (Lower Sat.) | Yes | |
| 3-Phase Brushless DC Motor Controller/ Driver | IP3M05* | 15 | 2.5 | Yes | Yes |
| | IP3M06* | 15 | 1.5 | Yes | Yes |
| | IP3M13* | 15 | 4.0 | Yes | Yes |
| Universal Quad Driver | IP2D08 | 50 | 2.0 | Yes | Yes |
| | IP2D08A* | 80 | 2.0 | Yes | Yes |
| | IP2D09 | 50 | 2.0 | Yes | Yes |
| | IP2D09A* | 80 | 2.0 | Yes | Yes |

## PWM Circuit Selection Guide

| Part Number | Outputs | Output Type | Output Transistor Rating | Under Voltage Lockout | Soft Start | Double Pulse Suppression | Dead Time Adjust |
|---|---|---|---|---|---|---|---|
| IP1P00/IP3P00 | 1 | Totem Pole | 18V/200mA | Yes | Yes | N/A | Yes |
| IP1P01/IP3P01 | 1 | N/A | N/A | N/A | N/A | N/A | No |
| IP1P125/IP3P125 | 2 | Totem Pole | 35V/100mA | Yes | Yes | Yes | No |
| IP494A/IP494AC | 2 | Uncommitted | 40V/200mA | Yes | Ext. | N/A | Yes |
| IP1524/IP3524 | 2 | Uncommitted | 40V/50mA | No | Ext. | No | No |
| IP1524B/IP3524B | 2 | Uncommitted | 60V/200mA | Yes | Ext. | Yes | No |
| IP1525A/IP3525A | 2 | Totem Pole | 35V/100mA | Yes | Yes | Yes | Yes |
| IP1526/IP3526 | 2 | Totem Pole | 35V/100mA | Yes | Yes | Yes | Yes |
| IP1526A/IP3526A | 2 | Totem Pole | 35V/100mA | Yes | Yes | Yes | Yes |
| IP1527A/IP3527A | 2 | Totem Pole | 35V/100mA | Yes | Yes | Yes | Yes |
| IP1842/IP3842 | 1 | Totem Pole | 30V/200mA | Yes | Yes | N/A | Yes |
| IP1843/IP3843 | 1 | Totem Pole | 30V/200mA | Yes | Yes | N/A | Yes |
| IP1844/IP3844 | 1 | Totem Pole | 30V/200mA | Yes | Yes | N/A | Yes |
| IP1845/IP3845 | 1 | Totem Pole | 30V/200mA | Yes | Yes | N/A | Yes |
| IP5560/IP1060 | 1 | Uncommitted | 18V/40mA | Yes | Ext. | N/A | Yes |
| IP5561/IP5561C | 1 | Open Collector | 18V/40mA | Yes | Ext. | N/A | No |
| IP5568/IP5568C | 1 | Open Collector | 18V/40mA | Yes | Ext. | N/A | No |
| IP35060A/IP34060A | 1 | Uncommitted | 40V/200mA | Yes | Ext. | N/A | Yes |
| IP35063/IP34063 | 1 | Uncommitted | 40V/1.5A | N/A | Ext. | N/A | No |

## Voltage Regulator Selection Guide

| Output Current | Output Voltage | 1% Output Tolerance | | | | | 4% Output Tolerance | | | | | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.5A | Fixed +5V | IP78M05A | IP78M05AC | | | | IP78M05 | IP78M05C | | | | TO-39 |
| | Fixed +12V | IP78M12A | IP78M12AC | | | | IP78M12 | IP78M12C | | | | |
| | Fixed +15V | IP78M15A | IP78M15AC | | | | IP78M15 | IP78M15C | | | | TO-220 |
| | Fixed -5V | IP79M05A | IP79M05AC | | | | IP79M05 | IP79M05C | | | | |
| | Fixed -12V | IP79M12A | IP79M12AC | | | | IP79M12 | IP79M12C | | | | TO-220 |
| | Fixed -15V | IP79M15A | IP79M15AC | | | | IP79M15 | IP79M15C | | | | (Hermetic) |
| 1.5A | Fixed +5V | IP7805A | IP7805AC | IP140A-5 | IP240A-5 | IP340A-5 | IP7805 | IP7805C | LM140-5 | LM240-5 | LM340-5 | TO-3 |
| | Fixed +12V | IP7812A | IP7812AC | IP140A-12 | IP240A-12 | IP340A-12 | IP7812 | IP7812C | IP140-12 | IP240-12 | IP340-12 | |
| | Fixed +15V | IP7815A | IP7815AC | IP140A-15 | IP240A-15 | IP340A-15 | IP7815 | IP7815C | IP140-15 | IP240-15 | IP340-15 | TO-66 |
| | Adj. +1.2V to +37V | IP117A | IP217A | IP317A | | | IP117 | IP217 | IP317 | | | |
| | Adj. +1.2V to +57V | IP117AHV | IP217AHV | IP317AHV | | | IP117HV | IP217HV | IP317HV | | | TO-220 |
| | Fixed -5V | IP7905A | IP7905AC | IP120A-5 | IP220A-5 | IP320A-5 | IP7905 | IP7905C | IP120-5 | IP220-5 | IP320-5 | |
| | Fixed -12V | IP7912A | IP7912AC | IP120A-12 | IP220A-12 | IP320A-12 | IP7912 | IP7912C | IP120-12 | IP220-12 | IP320-12 | TO-39 |
| | Fixed -15V | IP7915A | IP7915AC | IP120A-15 | IP220A-15 | IP320A-15 | IP7915 | IP7915C | IP120-15 | IP220-15 | IP320-15 | |
| | Adj. -1.2V to -37V | IP137A | IP237A | IP337A | | | IP137 | IP237 | IP337 | | | TO-220 |
| | Adj. -1.2V to -57V | IP137AHV | IP237AHV | IP337AHV | | | IP137HV | IP237HV | IP337HV | | | (Hermetic) |
| 3.0A | Fixed +5V | IP123A-5 | IP223A-5 | IP323A-5 | | | IP123-5 | IP223-5 | IP323-5 | | | TO-3 |
| | Fixed +12V | IP123A-12 | IP223A-12 | IP323A-12 | | | IP123-12 | IP223-12 | IP323-12 | | | |
| | Fixed +15V | IP123A-15 | IP223A-15 | IP323A-15 | | | IP123-15 | IP223-15 | IP323-15 | | | TO-218 |
| | Adj. +1.2V to +37V | IP150A | IP250A | IP350A | | | IP150 | IP250 | IP350 | | | |
| | Adj. +1.2V to +37V (Low Dropout) | IP1R07A | IP2R07A | IP3R07A | | | IP1R07 | IP2R07 | IP3R07 | | | TO-220 |
| | Fixed –5V | IP1R17A-05 | IP2R17A-05 | IP3R17A-05 | | | IP1R17-05 | IP2R17-05 | IP3R17-05 | | | |
| | Fixed –5.2V | IP1R17A-5.2 | IP2R17A-5.2 | IP3R17A-5.2 | | | IP1R17-5.2 | IP2R17-5.2 | IP3R17-5.2 | | | |
| | Fixed –12V | IP1R17A-12 | IP2R17A-12 | IP3R17A-12 | | | IP1R17-12 | IP2R17-12 | IP3R17-12 | | | |
| | Fixed –15V | IP1R17A-15 | IP2R17A-15 | IP3R17A-15 | | | IP1R17-15 | IP2R17-15 | IP3R17-15 | | | |
| 5.0A | Fixed +5V | IP1R18A-05 | IP2R18A-05 | IP3R18A-05 | | | IP1R18-05 | IP2R18-05 | IP3R18-05 | | | TO-3 |
| | Fixed +12V | IP1R18A-12 | IP2R18A-12 | IP3R18A-12 | | | IP1R18-12 | IP2R18-12 | IP3R18-12 | | | |
| | Fixed +15V | IP1R18A-15 | IP2R18A-15 | IP3R18A-15 | | | IP1R18-15 | IP2R18-15 | IP3R18-15 | | | TO-218 |
| | Adj. +1.2V to +37V | IP138A | IP238A | IP338A | | | IP138 | IP238 | IP338 | | | |
| | Fixed –5V | IP1R19A-05 | IP2R19A-05 | IP3R19A-05 | | | IP1R19-05 | IP2R19-05 | IP3R19-05 | | | |
| | Fixed –5.2V | IP1R19A-5.2 | IP2R19A-5.2 | IP3R19A-5.2 | | | IP1R19-5.2 | IP2R19-5.2 | IP3R19-5.2 | | | |
| | Fixed –12V | IP1R19A-12 | IP2R19A-12 | IP3R19A-12 | | | IP1R19-12 | IP2R19-12 | IP3R19-12 | | | |
| | Fixed –15V | IP1R19A-15 | IP2R19A-15 | IP3R19A-15 | | | IP1R19-15 | IP2R19-15 | IP3R19-15 | | | |





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## IP3M05, IP3M06, IP3M13
## 3-Phase DC Brushless Motor Control/Drive Circuits

### Features

STANDARD

- Internal current sensing
- Short circuit protection
- Thermal shutdown
- Single pin loop filter
- Minimum external components
- Reference inputs to 2.5 mHz

CONFIGURABLE

- Divider ratios
- Open collector/differential hall input
- Under voltage sensing (5V/12V)
- Forward/reverse
- Start/stop run/brake
- Other logic functions

## IP1M10, IP2M10, IP3M10, IP1M20, IP2M20, IP3M20
## Dual Full-bridge Driver

### Features

- 200mA continuous output current per bridge
- Internal output clamp diodes
- Hysteretical logic inputs for noise immunity
- Thermal shutdown protection
- Peak current limit protection
- Crossover current blanking
- Separate +5V logic supply for minimum power dissipation (1M10 series only)
- Separate +7V to +36V logic supply (1M20 series only)

## IP3M11, IP3M21
## Voice Coil Driver

### Features

- 3A max output current (1.2A 3M21)
- H-bridge output
- Typical transconductance 1A/V (.4A/V 3M21)
- Single-ended or differential input
- 3% accuracy and linearity
- Compact 15-pin power SIP package
- Disable function
- Pin-controlled retract
- Separate retract supply pin
- Thermal shutdown protection
- Undervoltage sensing

## IP2D08, IP2D08A, P2D09, IP2D09A, IP3DO8, IP3D08A, IP3D09, IP3D09A
## Universal Quad Driver

### Features

- Output currents to 2 amps
- Current sense on D09/D09A
- 50/80 volt output breakdown
- Low output saturation voltage
- Low diode forward voltage
- Split supply operation
- Clamp diodes for transient suppression
- Compatible with standard logic families
- Improved noise immunity and parasitic suppression
- 50 volt output sustaining voltage

## IP1D03, IP2D03, IP3D03
## 5-amp Full Bridge Power Driver

### Features

- 5A maximum continuous output current
- 50V maximum supply voltage
- External current sense capability
- Internal crosover-current protection
- Thermal shutdown protection with hysteresis
- TTL compatible inputs with hysteresis
- MODSIP power package
- Hermetic 8-pin TO-3 package
- Parasitic protection from inductive transients

INTEGRATED POWER SEMICONDUCTORS, LTD.

Integrated Power Semiconductor

## IP1526A, IP2526A, IP3526A

## Advanced Regulating Pulse Width Modulators

### Features

- Low drain current
- 8 to 35 volt operation
- High performance 5V ±1% reference
- Low t.c. 1Hz to 400kHz oscillator
- Dual 100 mA source/sink outputs
- Digital current limiting
- Double pulse suppression
- Programmable deadtime
- Accurate current limit sense voltage
- Undervoltage lockout
- Single pulse metering
- Programmable soft-start
- Wide current limit common mode range
- TTL/CMOS compatible logic ports
- Symmetry correction capability
- Guaranteed 6 unit synchronization

## IP1P00, IP2P00, IP3P00, P1P01, IP2P01, IP3P01

## Switched Mode Power Supply Control Chip Set

### Features

IP1P00 series

- Undervoltage lockout with hysteresis
- Cycle by cycle current limit
- PWM with maximum duty cycle limit
- Soft start
- External synchronization

IP1P01 series

- 1% trimmed internal reference
- Error amp
- DC current limit
- PWM

## IP1842, IP2842, IP3842, IP1843, IP2843, IP3843, IP1844, IP2844, IP3844, IP1845, IP2845, IP3845

## Regulating Pulse Width Modulators

### Features

- Guaranteed ±1% reference voltage tolerance
- Guaranteed ±10% frequency tolerance
- Low start-up current (<500 μA)
- Under voltage lockout with hysteresis
- Output state completely defined for all supply and input conditions
- Interchangeable with UC1842, UC1843, UC1844 and UC1845 series for improved operation
- 500 kHz operation

## IP1P125, IP2P125, IP3P125 Regulating Pulse Width Modulators

### Features

- Pin compatible with 1525A series
- Low output crossover current
- Fixed 100ns deadtime
- 100ns response latched shutdown
- 50Hz to 500KHz operating frequency
- 5.1 volt ±1% reference
- Oscillator sync. terminal
- Soft-start
- Undervoltage lockout
- Latching PWM

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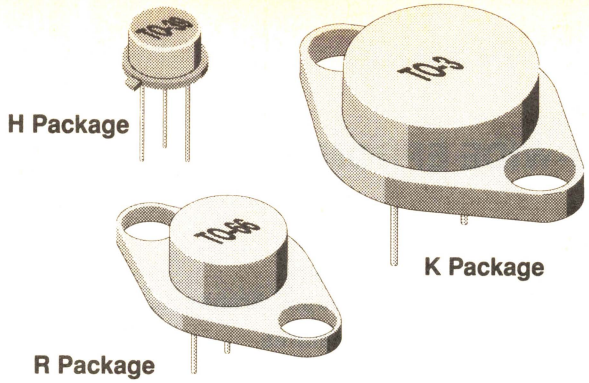


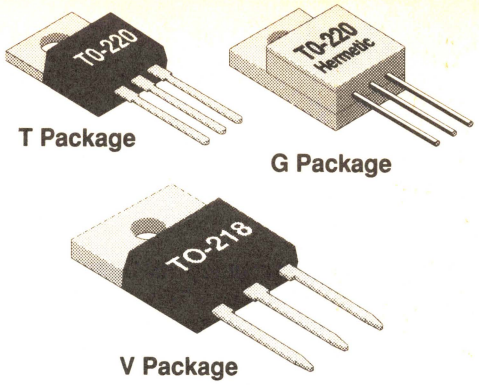


## *IP1R17, IP2R17, IP3R17, IP1R17A, IP2R17A, IP3R17A*

## *3-Amp, 3-Terminal, Fixed Negative Voltage Regulators*

### *Features*

- 3 Amp output current capability
- ±1% Output tolerence at room temperature (A suffix)
- 0.01%/V Line regulation
- o.5%/V Load regulation
- -5, -5.2, -12, -15 Volt fixed output voltages available
- Short circuit current limit protection
- Safe operating area protection
- Thermal shutdown protection
- Available in convenient, low-cost plastic TO-218 package
- Improved version of LM145

## *IP1R19, IP2R19, IP3R19, IP1R19A, IP2R19A, IP3R19A*

## *5-Amp, 3-Terminal, Fixed Negative Voltage Regulators*

### *Features*

- 5 Amp output current capability
- ±1% Output tolerence at room temperature (A suffix)
- 0.01%/V Line regulation
- o.5%/V Load regulation
- -5, -5.2, -12, -15 Volt fixed output voltages available
- Short circuit current limit protection
- Safe operating area protection
- Thermal shutdown protection
- Available in convenient, low-cost plastic TO-218 package

## *IP1R18, IP2R18 IP3R18, IP1R18A, IP2R18A, IP3R18A*

## *5-Amp, 3-Terminal, Fixed Positive Voltage Regulators*

### *Features*

- 5 Amp output current capability
- ±1% Output tolerence at room temperature (A suffix)
- 0.01%/V Line regulation
- o.5%/V Load regulation
- -5, -12, -15 Volt fixed output voltages available
- Short circuit current limit protection
- Safe operating area protection
- Thermal shutdown protection
- Available in convenient, low-cost plastic TO-218 package

## *IP3R07A, IP3R07*

## *Low Dropout, 3 Amp Positive Adjustable Voltage Regulator*

### *Features*

- 0.8V dropout voltage at 3A
- Guaranteed 1% output voltage tolerance
- Guaranteed 0.3% load regulation
- Guaranteed 0.01%/V line regulation
- 100% thermal limit burn-in
- Available in TO-218 and TO-220 packages

**INTEGRATED POWER SEMICONDUCTORS, LTD.**

Integrated Power Semiconductor

# 27210
# 1M (64K x 16) WORD-WIDE EPROM

- **High-Performance HMOS* II-E**
  - **— 150 ns Access Time**
  - **— Low 150 mA Active Power**
- **Complete Upgrade Capability**
  - **— PGM "Don't Care" Status Allows Wiring in Higher Order Addresses**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm—8 Seconds Typical**
- **New Word-Wide Pinout**
  - **— Clean, "Flow-Through" Architecture**
- **Standard EPROM Features**
  - **— TTL Compatibility**
  - **— Two Line Control**
  - **— int$_e$ligent Identifier™ For Automated Programming**
- **40-Pin DIP**

The Intel 27210 is a 5V only, 1,048,576-bit, Erasable Programmable Read Only Memory. It is organized as 64K-words of 16 bits each. It defines a new-clean memory architecture, oriented toward high-performance 16-bit and 32-bit CPUs, which simplifies circuit layout and offers a pin-compatible growth path to higher densities.

The 27210's unique circuit design provides for no-hardware-change upgrades to 4M-bits in the future. Since the $\overline{PGM}$ pin is a "don't care" state during read mode, direct connections to higher order addresses, A16 and A17, can be made without affecting the device's read operation.

The 27210 provides the highest density and performance available to 16-bit and 32-bit microprocessors. Its by-16 organization makes it an ideal single-chip firmware solution in most microprocessor applications. The 27210's large capacity is sufficient for storage of operating system kernels in addition to standard bootstrap and diagnostic code. Direct execution of operating system software is made possible by the 27210's fast 150 ns access time, which yields no-WAIT-state operation in such high-performance CPUs as the 10 MHz 80286.

The 27210 is part of a three-product megabit EPROM family. Other family members are the 27010 and 27011. These two products have byte-wide organizations geared toward simple upgrades from lower densities. The 27010 is organized as 128K x 8 in a 32-pin DIP package which is pin-compatible with JEDEC-standard 28-pin 512K EPROMs. The 8 x 16K x 8 27011 utilizes page addressing, allowing "drop in" replacement of the 512 K-bit 27513 and continued no-hardware-change upgrades to 32 M-bits in the same JEDEC-compatible 28-pin site.

The 27210 shares several features with standard JEDEC EPROMs, including two-line output control for simplified interfacing and the int$_e$ligent Identifier™ feature for automated programming. It can also be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 8 seconds.

The 27210 is manufactured using a scaled version of Intel's advanced HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

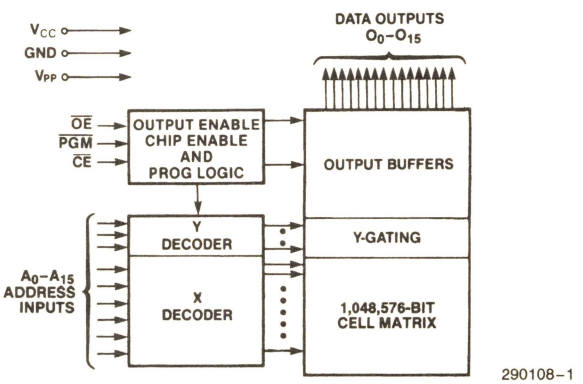


**Figure 1. Block Diagram**

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Intel Corp.

intel

# 27010
# 1M (128K x 8) BYTE-WIDE EPROM

- **Compatible with 28-Pin JEDEC EPROMs: 27256, 27512**
- **Complete Upgrade Capability**
  - **— $V_{PP}$, PGM "Don't Care" Status Allows Wiring in Higher Order Addresses**
- **Standard EPROM Features**
  - **— TTL Compatibility**
  - **— Two Line Control**
  - **— int$_e$ligent Identifier™ for Automated Programming**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm—15 Seconds Typical**
- **High-Performance HMOS* II-E**
  - **— 200 ns Access Time**
  - **— Low 150 mA Active Power**
- **Compact Packaging**
  - **— Smallest Standard-Addressed Footprint**
  - **— 32-Pin Cerdip**

The Intel 27010 is a 5V-only, 1,048,576-bit Erasable Programmable Read Only Memory. It is organized as 128 K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs allows upgrades from 16K through 512K EPROMs. In addition, unique circuit designs provide for no-hardware-change upgrades to 8M-bits in the future.

When a 32-pin DIP socket is configured for 27256 or 27512 EPROMs, it is easily upgraded for the 27010. By adding an A16 address line and $V_{CC}$ jumper, the 27010 can directly replace lower density 28-pin EPROMs. Upgrades through 8M-bits are accommodated without subsequent hardware changes. Since the $V_{PP}$ and PGM pins are in a "don't care" state during read mode, direct connections to higher order addresses, A17 through A19, can be made without affecting the device's read operation.

The 27010 provides the highest capacity available to microprocessors with 8-bit bus organizations for storage of large portions of operating system and application software. Its 200 ns access time provides no-WAIT-state operation with high-performance CPUs such as the 10 MHz 80188. The 27010 offers a minimal chip solution for code storage needs of 100% firmware-based equipment. And for reprogrammable systems, popular application programs can be made much more "user friendly." Often-used software is silently and quickly executed from reliable EPROM storage, greatly enhancing system utility. When two or more EPROM sockets are used in 16-bit or 32-bit systems, the compact 32-pin DIP package requires the smallest board space of any high density memory without utilizing paged or multiplexed addressing schemes.

The 27010 is part of a three-product megabit EPROM family. Other family members are the 27011 and 27210. The 8 x 16K x 8 27011 utilizes page-addressing, allowing "drop-in" replacement of the 512 K-bit 27513 and continued no-hardware-change upgrades to 32 M-bits in the same JEDEC-compatible 28-pin site. The 40-pin packaged 27210 is organized as 64K x 16, for systems in which word-wide memories are preferred.

The 27010 shares several features with standard JEDEC EPROMs, including two-line output control for simplified interfacing and the int$_e$ligent Identifier™ feature for automated programming. It can also be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 15 seconds.

The 27010 is manufactured using an advanced version of Intel's HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

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Intel Corp.

# 27011
# PAGE-ADDRESSED 1M (8 x 16K x 8) EPROM

- **Paged Organization**
  - **— Reduced Physical Address Requirement**
- **Compatible with 28-Pin JEDEC EPROMs**
  - **— Single-Trace Modification for Retrofitting 27128-Based Designs**
- **No-Hardware-Change Upgrades**
  - **-- Drop-In 27513 Replacement**
  - **— Direct Pin Compatibility through 32 M-Bit Density**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm—15 Seconds Typical**
- **Automatic Page Clear**
  - **— Resets to Page 0 on Power-Up**
- **High-Performance HMOS* II-E**
  - **— 200 ns Access Time**
  - **— Low 150 mA Active Power**
- **Standard EPROM Features**
  - **— TTL Compatibility**
  - **— Two Line Control**
  - **— int$_e$ligent Identifier™ for Automated Programming**
- **Smallest Megabit Package**
  - **— 28-Pin DIP, Minimal Footprint without Address/Data Multiplexing**

The Intel 27011 is a 5V-only, 1,048,576-bit Erasable Programmable Read Only Memory. It is organized as 8 pages of 16K 8-bit words. Its pin-compatibility with byte-wide JEDEC EPROMs allows retrofitting existing designs to the greater storage capacity afforded by the page-addressed organization. Its 16 K-byte physical address space requirement allows the 27011 to be utilized in address-constrained system designs.

When a 28-pin DIP socket is configured for 2764 or 27128 EPROMs, it is easily retrofitted to the 27011. By adding a WRITE ENABLE signal to pin 27 (DIP) or pin 31 (PLCC) (unused on 2764 and 27128), the 27011 can be used in an existing design. Thus, the 27011 enables product enhancements via additional feature sets and firmware-intensive performance upgrades. For sockets specifically configured for page-addressed EPROM, no hardware changes are required for upgrades through 32 M-bits in density!

The page-addressed organization allows the use of 28-pin DIP packages, the smallest megabit EPROM footprint with applicability to all microprocessors. This provides very efficient circuit board layouts.

The 27011 is part of a three-product megabit EPROM family. The other two members are standard-addressed byte-wide and word-wide versions, the 27010 and 27210, respectively. The 27010 is organized as 128K x 8 in a 32-pin DIP package which is pin-compatible with JEDEC-standard 28-pin 512K EPROMs. The 27210 is packaged in a 40-pin DIP with a 64K x 16 organization.

The 27011 has an automatic page clear circuit for ease of use of its paged organization. The page-select latch is automatically cleared to the lowest order page upon system power-up. The 27011 also contains many industry-standard features such as two-line output control for simple interfacing and the int$_e$ligent Identifier™ feature for automated programming. It also can be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 15 seconds.

The 27011 is manufactured using an advanced version of Intel's HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

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Intel Corp.

PRELIMINARY

# 27C256
# 256K (32K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

- **High Speed***
  - **— 120 ns Access Time**
- **Low Power Consumption***
  - **— 50 μA Standby, 20 mA Active Current Available**
- **Fast Programming**
  - **— 4 Second Programming for High Throughput**
- **EPI Processing**
  - **— Maximum Latch-up Immunity**
- **Simple Interfacing**
  - **— Two Line Control**
  - **— CMOS and TTL Compatible**
- **Versatile JEDEC-Approved Packaging**
  - **— Standard 28 Pin CERDIP**
  - **— Compact 32-Lead PLCC**
  - **— Cost Effective Plastic DIP**

(See Packaging Spec., Order #231369)

Intel's 27C256 EPROM is a 256K-bit 5V-only memory, organized as 32,768 words of 8 bits. The 27C256 is ideal in embedded control applications based on advanced 16-bit CPUs. Fast 120 ns access times allow no-Wait-state operation with 12 MHz 80286. The 27C256 also excels in reprogrammable environments where the system designer must strike an optimal density/performance balance. For example, bootstrap and diagnostic routines run fast with 1 Wait-state on a 16 MHz 80386.

The 27C256 is offered in Ceramic Dual In-Line Package (DIP or CERDIP), Plastic DIP (PDIP), and Plastic Leaded Chip Carrier (PLCC) packages. Cerdip packages provide flexibility in prototyping and R&D environments while PDIP and PLCC are most cost effective in production environments. The Quick-Pulse Programming™ Algorithm improves programming speed by as much as 100 times over older programming algorithms, further reducing cost for system manufacturers.

Intel's unique Epitaxial (EPI) processing provides excellent latch-up immunity. Prevention of latch-up guarantees for stresses up to 100 mA from $-1V$ to $V_{CC} + 1V$ on address and data pins and for $V_{PP}$ voltage overshoot up to 14V.

*These specifications are advance information for the new CMOS III-E version.

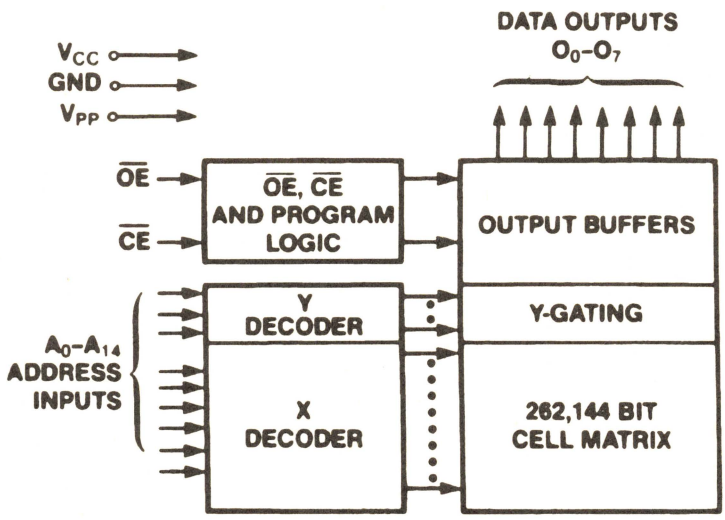


**Figure 1. Block Diagram**

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Intel Corp.

# 27512
# 512K (64K x 8) PRODUCTION AND UV ERASABLE PROM

- **Software Carrier Capability**
- **170 ns Maximum Access Time**
- **Two-Line Control**
- **int$_e$ligent Identifier™ Mode**
  **— Automated Programming Operations**
- **TTL Compatible**
- **Low Power**
  **— 125 mA max. Active**
  **— 40 mA max. Standby**
- **New Quick-Pulse Programming™ Algorithm**
  **— 8 Second Programming**
  **— int$_e$ligent Programming™ Algorithm Compatible**
- **Available in 28-pin Cerdip, Plastic DIP and PLCC Packages**
  (See packaging spec order #231369)

The Intel 27512 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). Organized as 64K words by 8 bits, individual bytes are accessed in under 170 ns. This ensures compatibility with high-performance microprocessors, such as the Intel 8 MHz iAPX 286, allowing full speed operation without the addition of performance-degrading WAIT states. The 27512 is also directly compatible with Intel's 8051 family of microcontrollers.

The 27512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the 27512's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabyte addressing capability provides designers with opportunities to engineer user-friendly, high-reliability, high-performance systems.

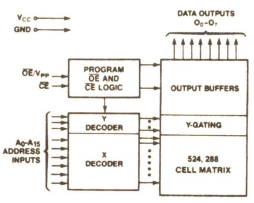
The 27512's large storage capability of 64 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27512 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The Plastic P27512 and PLCC N27512 are ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27512 and the N27512 to be programmed within eight seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27512 is manufactured using Intel's advanced HMOS *II-E technology.

*HMOS is a patented process of Intel Corporation.



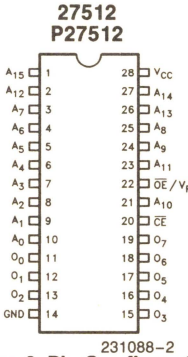

231088-1

**Figure 1. Block Diagram**

**Pin Names**

| | |
|---|---|
| $A_0$–$A_{15}$ | Addresses |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}/V_{PP}$ | Outputs Enable/$V_{PP}$ |
| $O_0$–$O_7$ | Outputs |
| D.U. | Don't Use |

| 27513 | 27256<br>27C256<br>87C256 | 27128<br>27128A | 2764<br>2764A<br>27C64<br>87C64 |
|---|---|---|---|
| D.U. | $V_{PP}$ | $V_{PP}$ | $V_{PP}$ |
| $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ |
| $A_7$ | $A_7$ | $A_7$ | $A_7$ |
| $A_6$ | $A_6$ | $A_6$ | $A_6$ |
| $A_5$ | $A_5$ | $A_5$ | $A_5$ |
| $A_4$ | $A_4$ | $A_4$ | $A_4$ |
| $A_3$ | $A_3$ | $A_3$ | $A_3$ |
| $A_2$ | $A_2$ | $A_2$ | $A_2$ |
| $A_1$ | $A_1$ | $A_1$ | $A_1$ |
| $A_0$ | $A_0$ | $A_0$ | $A_0$ |
| $D_0/O_0$ | $O_0$ | $O_0$ | $O_0$ |
| $D_1/O_1$ | $O_1$ | $O_1$ | $O_1$ |
| $O_2$ | $O_2$ | $O_2$ | $O_2$ |
| Gnd | Gnd | Gnd | Gnd |




231088-2

| 2764<br>2764A<br>27C64<br>87C64 | 27128<br>27128A | 27256<br>27C256<br>87C256 | 27513 |
|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $\overline{PGM}$ | $\overline{PGM}$ | $A_{14}$ | $\overline{WE}$ |
| N.C. | $A_{13}$ | $A_{13}$ | $A_{13}$ |
| $A_8$ | $A_8$ | $A_8$ | $A_8$ |
| $A_9$ | $A_9$ | $A_9$ | $A_9$ |
| $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ |
| $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}/V_{PP}$ |
| $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ |
| $\overline{CE}$ ALE/$\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ ALE/$\overline{CE}$ | $\overline{CE}$ |
| $O_7$ | $O_7$ | $O_7$ | $O_7$ |
| $O_6$ | $O_6$ | $O_6$ | $O_6$ |
| $O_5$ | $O_5$ | $O_5$ | $O_5$ |
| $O_4$ | $O_4$ | $O_4$ | $O_4$ |
| $O_3$ | $O_3$ | $O_3$ | $O_3$ |

**Figure 2. Pin Configurations**

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**October 1986**
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**Order Number: 231088-005**

**For more information: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051 (800) 548-4725**

Intel Corp.


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# 27513
# PAGE-ADDRESSED 512K (4 x 16K x 8) PRODUCTION AND UV ERASABLE PROM

- **Paged Organization**
  - **— Reduced Physical Address Requirement**
  - **— No Bank Switching Logic Needed**
- **Software Carrier Capacity**
- **Automatic Page Clear**
  - **— Resets to Page 0 on Power Up and On Demand with $\overline{RST}$ Signal**
- **TTL and CMOS Compatible**
- **170 ns Access Time**
- **Two Line Control**
- **Low Power**
  - **— 125 mA max. Active**
  - **— 40 mA max. Standby**
- **New Quick-Pulse Programming™ Algorithm**
  - **— 8 Second Programming**
  - **— int$_e$ligent Programming™ Algorithm Compatible**
- **Compatible with Industry Standard EPROM Pinouts**
  - **— Direct 27128A Compatibility**
  - **— 28-Pin Cerdip and Plastic Packages**

  (See Packaging Spec, Order #231369)

The Intel 27513 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory. It is organized as 4 pages of 16K 8-bit words. The 27513's paged organization brings 64 K-byte storage capacity to existing 128K EPROM-based designs and to popular 8-bit microprocessor or microcontroller systems that have 64 K-byte total addressing capability. The 27513 provides an ideal means of quadrupling current 16 K-byte code space.

The 27513's large storage capability of 64 K-bytes and 170 ns access time enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27513 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The P27513 and PLCC N27512 are ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. The P27513 and the N27512 enable implementation of new, advanced systems with firmware-intensive architectures. The combination of the P27513's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The 27513 enables firmware-intensive performance upgrades for systems based on microprocessors with 64K physical addressing capability like the 8085AH.

The 27513 has an automatic page clear circuit for ease of use of the page-addressed organization. The page-select latch is automatically cleared to the lowest order page upon system power up.

The 27513 has a fast access time. Individual bytes are accessed in under 170 ns. Intel's new Quick-Pulse Programming Algorithm enables the 27513 to be programmed within eight seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

Two-line control and industry standard 28-pin packaging are features common to all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27513 is manufactured using Intel's compacted HMOS* II technology.

* HMOS is a patented process of Intel Corporation

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Intel Corp.

# 27CX641/27CX642
# 8192 X 8 CMOS High-Speed UV-Erasable PROM

## Features

- **Advanced CMOS EPROM Technology**
- **High Performance**
  - 27CX641/642-40 $t_{AA}$ =40nS max
  - 27CX641/642-45 $t_{AA}$ =45nS max
  - 27CX641/642-55 $t_{AA}$ =55nS max
- **Low Power Consumption**
  - ICC=80mA max
- **TTL-Compatable I/O**
- **Reprogrammability**
  - Adds convenience, reduces costs
  - Windowed package for UV erasure
  - Allows 100% factory testing
- **Bipolar PROM replacement**
  - Pin-compatable with Bipolar PROMs,
  - Higher speed
  - Lower power consumption
  - 300-mil and 600-mil packages

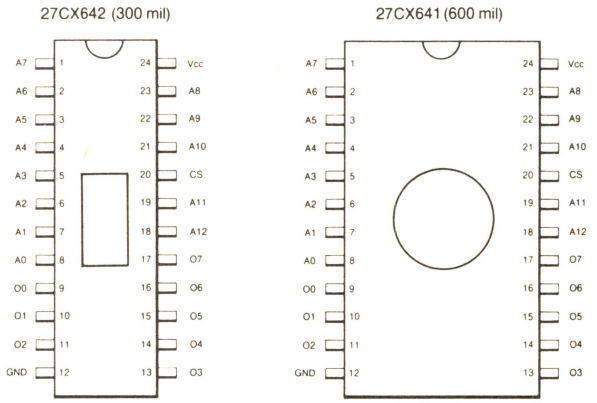
## General Description

The ICT 27CX641 and 27CX642 are 8,192 X 8 bit CMOS high-speed, UV-erasable PROMs that provide a low-power, reprogrammable alternative to bipolar fuse-link PROMs. Available in both 600mil-wide (27CX641) and 300mil-wide (27CX642) packages, these devices are pin/socket-compatable with many popular bipolar PROMs. The 27CX641/642 are designed in an advanced CMOS EPROM technology and utilize differential memory cell techniques, to provide access times comparable to high-speed bipolar PROMs (as fast as 40nS) with a significant improvement in power consumption. The reprogrammability of the 27CX641/642 not only adds convenience and reduces development and field retrofit costs, but enhances factory testability, allowing for 100% field programmability and function.

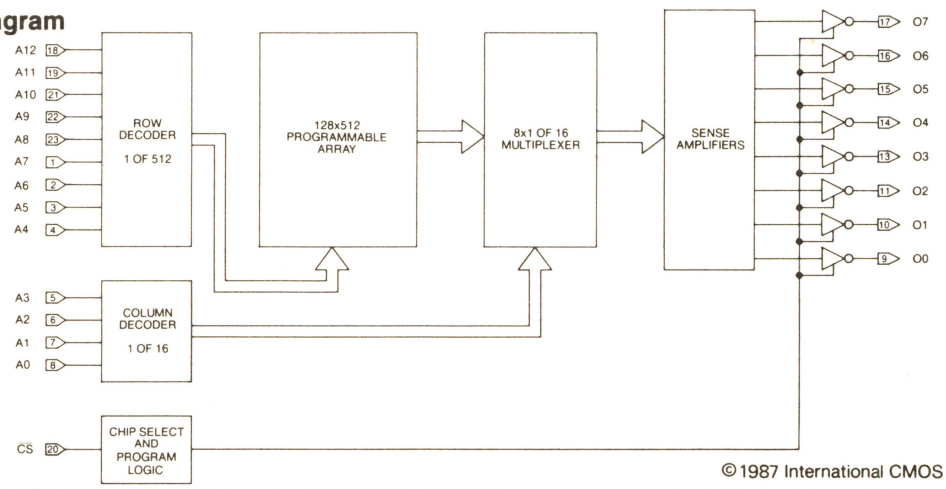
### Pin Diagrams

Pin Names

$A_0$–$A_{12}$ = Address Inputs
$O_0$–$O_7$ = Data Outputs
$\overline{CS}$ = Chip Select
GND = Ground
Vcc = Power Supply (+5V)




### Block Diagram

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INTERNATIONAL CMOS TECHNOLOGY, INC.

August 1986

# 93C46
# 1024-Bit Serial (5V only) CMOS Electrically Erasable Programmable Memory

## Features

- **ADVANCED CMOS E²PROM TECHNOLOGY**
- **READ/WRITE NON-VOLATILE MEMORY**
  - — Single 5V supply operation
  - — 1024 bits, 64 x 16 organization
  - — Easy to use yet versatile serial data interface
- **LOW POWER CONSUMPTION**
  - — 3mA Max Active
  - — 1mA Max Standby, TTL interface
  - — 100μA Max Standby, CMOS interface
- **SPECIAL FEATURES**
  - — Automatic write cycle time-out
  - — Ready/Busy status signal
  - — Software controlled write protection
- **IDEAL FOR LOW DENSITY DATA STORAGE**
  - — Low cost, space saving, 8-pin package
  - — Commercial, industrial, and military versions
  - — Interfaces with popular microcontrollers (ie., COP4XX, 8048, 8049, 8051, 8096, 6805, 6801, TMS1000, Z8) and standard microprocessors
- **APPLICATION VERSATILITY**
  - — Alarm Devices, Electronic Locks, Appliances, Terminals, Smart Cards, Satellite Receivers, Robotics, Meters, Telephones, Tuners, etc.
- **SUPER-SET COMPATIBILITY**
  - — National: NMC9306/COP494, NMC9346/COP495
  - — General Instrument: ER59256, ER5911
  - — NCR: 59306, 5930B

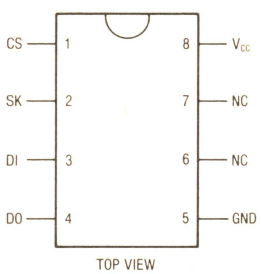
## General Description

The ICT 93C46 is a 1024-bit, 5V-only, serial, read/write, non-volatile memory device fabricated using an advanced CMOS E²PROM technology. Its 1024 bits of memory are organized into 64 registers of 16 bits each. Each register is individually addressable for serial read or write operations. A versatile serial interface, consisting of chip select, clock, data-in and data-out, can easily be controlled by popular microcontrollers (ie., COP4XX, 8048, 8049, 8051, 6805, 6801, TMS1000, Z8) or standard microprocessors.

Low power consumption, low cost, and space efficiency make the ICT 93C46 an ideal candidate for high volume, low density, data storage applications. Special features of the 93C46 include: automatic write time-out, ready/busy status signal, software controlled write protection and ultra-low standby power mode when deselected (CS low). Additionally 93C46 offers functional compatability with existing NMOS serial E²PROMs. The 93C46 is designed for applications requiring up to 10,000 erase/write cycles per register.

## Pin Diagram

**Dual-In-Line-Package**

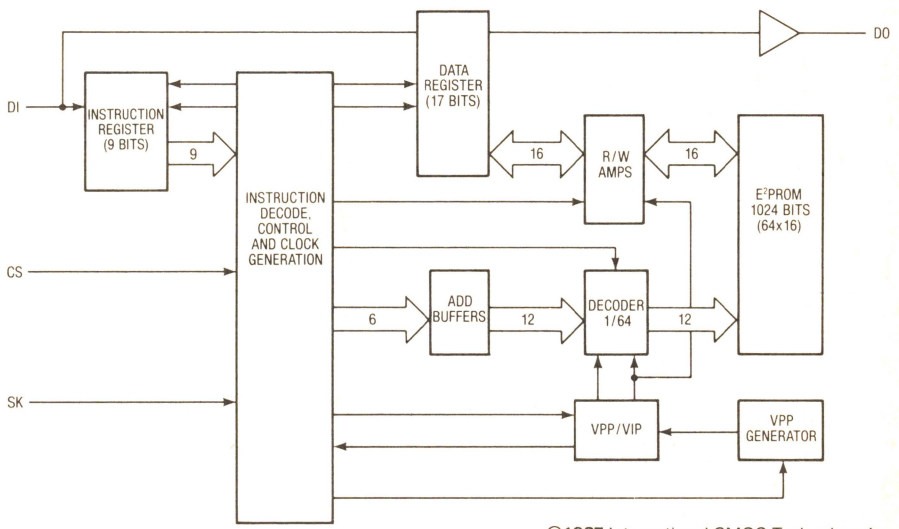



TOP VIEW

**Pin Names**

| | |
|---|---|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| $V_{CC}$ | Power Supply |
| GND | Ground |
| NC | Not Connected |

## Block Diagram

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## PROGRAMMABLE INTEGRATED CONTROLLER/SEQUENCER

**Microprocessor designed for applications requiring simple decision-making, not computation.**

LS7270: Performs logical sequencing, timing, and controlling functions. Far more easily programmed than any other μP, and program can be stored in any standard ROM, PROM, EPROM, or RAM. Low-cost, reliable replacement for hard-wired controls and relay networks. 40-pin DIP.

## DIGITAL LOCK CIRCUITS

**For automotive/marine anti-theft.**

LS7220: 5,040 4-digit combinations; out-of-sequence detection logic; 25μA standby; "Save" mode for valet parking settable in "Unlock"; built-in convenience delay hard wired programming. 14-pin DIP.

**Keyboard Programmable Keyless Locks.**

LS7222-LS7223: Stand along lock logic with 38416, 4 digit codes: 3 different user programmable codes; momentary static lock control outputs; tamper detection output; high noise immunity. 20-pin DIP.

**For area access and machine access.**

LS7225-LS7226: 5,040 4-digit combinations; toggle output (set and reset with application of code); momentary output; tamper output. 14-pin DIP.

**For serial address decoding or 2-pushbutton keyless locks.**

LS7228-LS7229: Address decoder/digital lock; code programmable through 9 parallel pins; serial decoding input can be applied through dual pulse train or two pushbuttons; pulse output; duration between entries capacitor programmable; cascadable; hard wired programming. 16-pin DIP.

## BRUSHLESS DC MOTOR SPEED CONTROLLERS

LS7261/62: 3 or 4-phase commutator chips; overcurrent sensing; brake; reverse. 20-pin DIP.

LS7263: Crystal controlled 3-phase motor speed controller; for fixed speed applications; accuracy 0.1%. 18-pin DIP.

LS7264: Crystal controlled 4-phase motor speed controller; for fixed speed applications; accuracy 0.1%. 16-pin DIP.

## PROGRAMMABLE DIGITAL DELAY TIMER

**For delaying the starting or stopping of an operation.**

LS7210: Can generate delays of ms to infinity, or add auto reset to μP system; programmed by 5 binary weighted input bits plus on chip oscillator or external clock. Operable in 4 modes; delayed operate or release, dual delay, or one-shot. All inputs CMOS, MOS, and TTL compatible. 14-pin DIP.

## TOUCH SENSITIVE LAMP DIMMER/AC MOTOR SPEED CONTROLLER

**Circuits digitally determine firing angle of a triac. Phase locked loop synchronization makes triac output "Pure AC", allowing triac to drive motor or transformer windings directly.**

LS7231-35: Momentary touch turns triac off, if on: if off, momentary touch turns triac to maximum or to firing angle stored in MEMORY (depending on circuit). Prolonged touch causes firing angle to vary. 8 pin mini-DIP.

LS7237: A touch causes firing angle to advance to next state in sequence. Three state input pin ("1", "0", or "open") selects one of 3 modes of firing angle sequence: MAX/OFF; LOW/MED/MAX/OFF; MIN/LOW/MED/MAX/OFF. Pin compatible with LS7231-LS7235. 8 pin mini-DIP.

LS7331-LS7332: Momentary touch turns triac on or off; prolonged touch causes firing angle to vary. Allows computer control of triac firing with outputs to computer when lamp is at full brightness, varying in brightness or when power loss has occurred.

## DISPLAY DRIVERS

**For liquid crystal displays requiring up to 60V.**

LS7100: BCD to 7 segment latch/decoder/driver.

LS7110: Binary addressable latched 8-channel demultiplexer/driver. Both are ion-implanted P Channel MOS circuits, compatible with CMOS and TTL systems. 16-pin DIPS.

## CMOS DIVIDERS

**For generating time bases from 50/60 Hz input.** All feature input shaping network; resettable; division select input 50/60 Hz; clock enable input; 8-pin mini-DIP.

RED 5/6: 10 pulses/sec.
RED 50/60: 1 pulse/sec.
RED 100/120: 1 pulse/2 seconds.
RED 300/360: 1 pulse/0.1 minute.
RED 500/600: 1 pulse/10 seconds.
RED 3000/3600: 1 pulse/minute.

**For generating decade-related time bases.**

RDD104: Addressable divider; divides by 10, 100, 1000, or 10,000. Input may be controlled by crystal or external frequency source. 8-pin mini-DIP.

## TONE ACTIVATED, TELEPHONE LINE ISOLATION DEVICE

LS7501-LS7510: Frequency discriminator circuits which can disconnect or switch a telephone line upon detection of a specific frequency tone. 10 standard frequency circuit versions. Telephone line checking or automatic meter reading applications.

## COUNTERS

LS7066: 24-bit multimode counter. Programmable by microprocessor, via three-state I/O bus, to operate in the following modes: binary, BCD, 24-hour clock, up, down, ÷n, quadrature, and single cycle. Modes can co-exist in different combinations. DC to 5 MHz in all modes. Includes 24-bit comparator for preset count comparison; readable status register. Input/output TTL compatible. 20-pin plastic DIP.

LS7060: DC to 10 MHz 32-bit binary up counter with 32-bit latch and multiplexer; 8-bit three-state multiplexed outputs; input/output TTL compatible; bus compatible. 18-pin DIP.

LS7062: Identical except that it is a dual 16-bit counter, with two inputs.

LS7061: DC to 10 MHz 32-bit binary up counter with 40-bit latch and multiplexer; access to 8 LSB latches allows attachment of prescalers for counting to 2.56 GHz; 8-bit three-state multiplexed outputs; input/output TTL compatible; bus compatible. 24-pin DIP.

LS7063: Identical, except that it is a dual 16-bit counter, with two inputs.

LS7030: DC to 5 MHz eight decade up counter with 8-decade latch and multiplexer, multiplexed BCD and 7 segment outputs; inputs CMOS and TTL compatible; outputs CMOS compatible; counter output latches; leading zero blanking. 40-pin DIP.

LS7031: DC to 5 MHz six decade up counter with 8-decade latch and multiplexer, access to LSD latches allows attachment of prescalers for counting to 500 MHz; multiplexed BCD outputs; leading zero blanking; inputs CMOS and TTL compatible; outputs CMOS compatible. 40-pin DIP.

LS7055: DC to 250 KHz six decade up/down counter with integral preset, presignal, and main signal store; automatic or manual preset/reset control; 3 comparators with output flags; multiplexed BCD, 7 segment outputs and blanking override; internal oscillator; high noise immunity; all inputs CMOS compatible. 40-pin DIP.

LS7056: Identical, except that it has lamp test input instead of blanking override.

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# Fixed-Point Multipliers and Multiplier-Accumulators



## Description

LSI Logic Corporation fixed-point multiplier-accumulators (MACs) offer industry standard functions and pinout options in fast, low-power 0.9-micron channel length (1.5-micron drawn gate length) HCMOS technology. The 16-bit multipliers and 16-bit MACs are available in a variety of DIP and chip carrier packages. LSI Logic multipliers and MACs are useful in Digital Signal Processing applications such as Fast Fourier Transforms, filtering, correlations and power expansions. They are also useful for general computational tasks such as graphics processing, image processing, vector processing and arithmetic acceleration operations. The products described below are available as discrete devices and as ASIC megacells or megafunctions.

The L64010, L64011 and L64012 are 16×16-bit parallel multiplier-accumulators with standard pinouts for 64-pin DIP (L64010/11) and 68-pin PLCC (L64012) packages. The L64010 features full 35-bit product register preloading. The L64011, which comes without product register preloading, contains a feed-through pin to control an optional output (pipeline) register. Pipelining greatly reduces output delay time. The L64012 offers full product register preloading and the option of converting three VDD/GND pins to signal pins. This enables the L64012 to operate in pipelined mode as the L64011 as well as to provide serial scanning of all input and output register.

The L64016 and L64017 are high-speed 16×16-bit multipliers available in 64-pin CDIP, 68-pin PLDCC, 68-pin CLCC and 68-pin CPGA packages. In a 68-pin package, both products feature on-chip serial scan testing for board and system-level testing and maintenance schemes. The L64016 has independent clocks for the X, Y, MSP (Most Significant Product) and LSP (Least Significant Product) registers. The L64017 has a single master clock and three register enables for the X, Y and full product register, allowing use in microprogrammed systems.

The L64032 is a high-speed 32×32-bit parallel multiplier-accumulator providing single precision (32×32) and multiple precision (64×64) fixed-point multiplication. In single precision (32×32) mode, the L64032 also acts as a multiplier-accumulator. The L64032's 32-bit word length yields a signal to noise ratio and dynamic range of up to 192 dB in Digital Signal Processing applications. A high-performance carry select adder, Wallace tree adders and modified Boothe encoding set the industry standard in speed. The L64032 is available in three speeds over both the military and commercial temperature range and can be packaged in a 132-pin CPGA or CLDCC package.

## Features

- 0.9-micron channel length (1.5-micron drawn gate length) HCMOS process for high speed and low power
- L64010/11/12 pin compatible with AMD 29510, TRW TDC1010, WTL2010 (L64010/12)
- L64016/17 pin compatible with AM29516/17, Cypress CY7C516 and TRW MPY106K
- 2000 V ESD and 200 mA latchup protection
- All products available in commercial and military temperature versions

## Fixed-Point MACs and Multipliers

| Device Type | Part Number | Description | Speed (ns) Commercial | Speed (ns) Military | Packages |
|---|---|---|---|---|---|
| 16-Bit MACs | L64010 | Industry Standard | 40 | 60 | 64 CDIP |
| | L64010A | | 30 | 40 | 68 CPGA |
| | L64011 | Pipelined Output | 40 | 60 | 64 CDIP |
| | L64011A | | 30 | 40 | |
| | L64012 | Pipeline and Scan Test | 40 | 60 | 68 PLDCC |
| | L64012A | | 30 | 40 | 68 CLCC |
| 16-Bit Multipliers | L64016 | 29516 Compatible | 40 | 60 | 64 CDIP |
| | L64016A | | 30 | 40 | 68 PLDCC |
| | L64017 | 29517 Compatible | 40 | 60 | 64 CDIP |
| | L64017A | | 30 | 40 | 68 CLCC |
| 32-Bit MACs | L64032 | Industry Standard | 125 | 160 | 132 CPGA |
| | L64032A | | 100 | 125 | 132 CLDCC |
| | L64032B | | 80 | 100 | |

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# L64132 Floating-Point Processor

LSI Logic Corporation
1551 McCarthy Blvd
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## Description

The L64132 is a single precision processor that combines a full floating-point multiplier and ALU on a single chip. Two 32-bit input ports and one 32-bit 3-state output port offer high performance. Implemented in 0.9-micron channel length (1.5-micron drawn gate length) fast low-power HCMOS technology, the L64132 is ideally suited for high-speed graphics and digital signal processing applications. The L64132 comes in a 144-pin grid array package and is available in three speeds (60, 80 and 125 ns) and in two single precision data formats: the ANSI/IEEE Standard P754-1985 format and the DEC F-format described in the VAX Architecture Reference Manual.

## Features

- Combines full 32-bit floating-point multiplier and floating-point ALU on a single chip
- Supports both IEEE and DEC formats
- Optimized for DSP and graphics operations
- 3-bus architecture for high throughput
- Four input registers allow full-on-chip multiplication of complex numbers
- Can independently flow through all input and output registers
- Single master clock with separate clock enables eliminates clock skew
- Conversion of floating point to and from integer format
- Supports 2-X for Newton Raphson division
- Full scan-testing of input and output registers
- 144-lead ceramic pin grid array package

## Floating-Point Processors

| Device Type | Part Number | Description | Cycle Time (ns) Commercial | Cycle Time (ns) Military | Packages |
|---|---|---|---|---|---|
| 32-Bit Floating-Point Processor | L64132 | Floating-Point Multiplier and ALU | 125 | 160 | 144 CPGA |
| | L64132A | IEEE and DEC Compatible | 80 | 100 | |
| | L64132B | | 60 | 80 | |

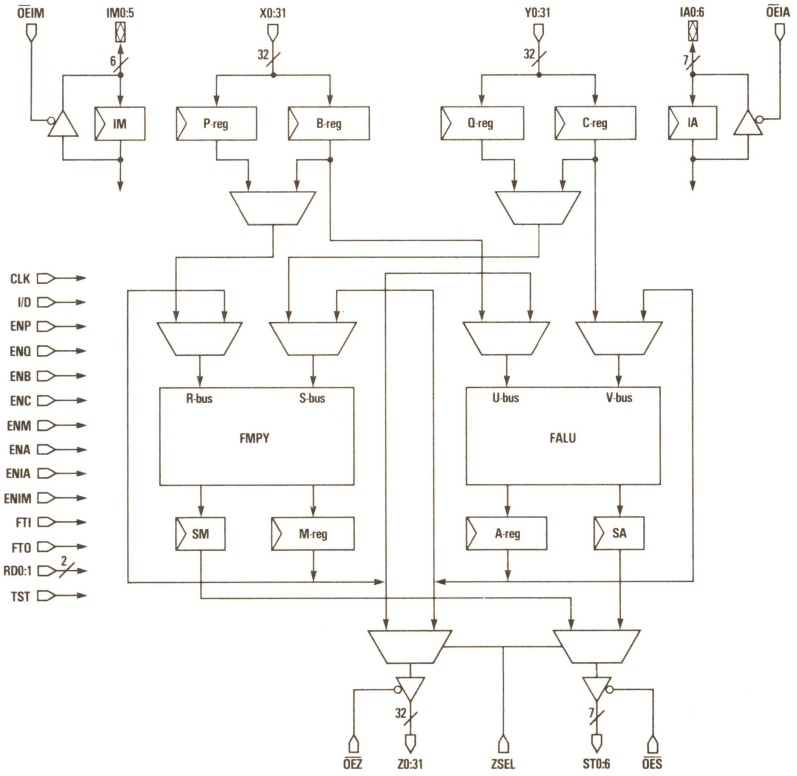


**Figure 1. Block Diagram of L64132**

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# DSP and Image Processing Devices



## Description

LSI Logic Corporation's video/radar family of high-speed DSP and image processing devices operate on linear and non-linear data and perform common DSP operations such as convolution/correlation, template matching, median filtering, binary and multi-bit FIR filtering as well as edge detection or enhancement. Designed to operate independently, as an integrated suite or with non-LSI Logic devices, the components work in stand-alone or in multi-processing configurations to enhance window size and/or precision. Component architecture includes features that maximize application flexibility, such as adjustable window size and shape and variable coefficients or mask values. The products described below are available in four speed grades (15/20 MHz Commercial, 12/16 MHz Military) with the added capabiltiy of integration as megafunctions/megacells into LSI Logic ASIC designs.

The L64210 and L64211 are high-speed Variable-Length Video Shift Registers for use separately or as video line delays for the L64200 Series filter processors. The L64210 provides four individual 8-bit shift registers, each with a length of up to 1032 words and packaged in a 68-pin PLCC or CPGA. The L64211 provides eight separate 8-bit shift registers, each with a length adjustable to 516 words and packaged in a 120-pin plastic or ceramic PGA.

The L64220 Rank-Value Filter processes sorted input values in a moving window and outputs a rank value. Rank values include maximum, minimum and median outputs, which effectively remove impulse-like ("salt and pepper") noise in non-linear signal processing applications. The Rank Value Filter is reconfigurable for operation as an 8×8, 4×16, or 2×32 filter or as a 1×64 one-dimensional filter. Since the L64220 allows users to mask values from computation, window size and shape can be adjusted to fit many applications. The L64220 is packaged in a 155-pin CPGA and allows data rates up to 20 MHz.

The L64230 is a 1024-tap high-speed Binary Filter and Template Matcher. The L64230 can be configured to filter one-dimensional (1-D) signals or two-dimensional (2-D) data for image processing applications. The processor accepts 2-D data directly from an L64210/11 Variable-Length Video Shift Register or from other video sources. Variable coefficients allow adaptive filtering and correlation operations. Maximum window size is 32×32 for a single chip. With a minimum of external logic, additional L64230 processors can expand window size and/or refine precision of a 1-D or 2-D filter. Optional video output formatting circuitry clips output to a single bit. The processor offers high performance for real-time image processing applications including video pattern matching, noise removal and morphological erosion and dilation operations. With data rates up to 20 MHz, the L64230 is also suitable for radar processing. The L64230 is packaged in a 155-lead CPGA.

The L64240 is a 64-tap Multi-Bit Filter consisting of two 32-tap sections with 8-bit coefficient and data. Each L64240 contains 64 seperate 8×8 MACs offering high-speed precision processing power. Processor reconfiguration allows filtering of one-dimensional (1-D) radar signals or two-dimensional (2-D) image data. The processor receives 2-D data directly from an L64210/11 Variable-Length Video Shift Register or from other viedo sources. Variable coeficients allow adaptive filtering and correlation operations. Maximum window size is 8×8 for a single chip. With a minimum of external logic, additional L64240 processors can expand window size and/or refine precision of a 1-D or 2-D filter. The processor is ideally suited for real-time image processing applications, including video pattern matching, noise removal, inverse filtering, edge enhancement and edge detection. Output formatting circuitry ensures total system compatibility by giving users control over gain, threshold data and data format. Worst-case commercial grade data throughput of 20MHz makes the L64240 suitable for radar processing. The L64240 is packaged in a 155-lead CPGA package.

## High-End DSP and Image Processing Devices

| Device Type | Part Number | Description | Clock Rate Commercial | Clock Rate Military | Packages |
|---|---|---|---|---|---|
| Variable-Length Video Shift Register (VSR) | L64210<br>L64210A | 1K×4×8 Line Delay | 15 MHz<br>20 MHz | 12 MHz<br>16 MHz | 68 PLDCC<br>68 CPGA |
| | L64211<br>L64211A | 512×8×8 Line Delay | 15 MHz<br>20 MHz | 12 MHZ<br>16 MHz | 120 CPGA<br>120 PPGA |
| Rank-Value Filter (RVF) | L64220<br>L64220A | 12-Bit, 64-Tap Rank-Value Filter | 15 MHz<br>20 MHZ | 12 MHz<br>16 MHZ | 155 CPGA |
| Binary Filter and Template Matcher (BFIR) | L64230<br>L64230A | 1024-Tap Binary Data FIR Filter | 15 MHz<br>20 MHz | 12 MHz<br>16 MHz | 155 CPGA |
| Multi-Bit Filter (MFIR) | L64240<br>L64240A | 64-Tap, 8-Bit Data or 32-Tap, 16-Bit Data FIR Filter | 15 MHz<br>20 MHz | 12 MHz<br>16 MHz | 155 CPGA |



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# L64500
# MIL-STD-1750A
# Microprocessor

LSI Logic Corporation
1551 McCarthy Blvd
Milpitas CA 95035

408.433.8000
Telex 172153

## Description

The LSI Logic Corporation L64500 is a monolithic 0.9-micron channel length (1.5-micron drawn gate length) HCMOS chip which implements the MIL-STD-1750A (Notice 1) Instruction Set Architecture (ISA). The L64500 is a 16-bit Central Processing Unit (CPU) used for real-time processing. The CPU uses a sophisticated ALU architecture which is expandable up to 32 bits depending on the opertion. The L64500 uses separate address and data buses to improve system performance and has advanced look-ahead capability with the optional L64550 (MBU) to minimize the probability of wait-state insertion.

The L64500 can be augmented with an L64550 (MBU) chip to implement optional enhancements of the MIL-STD-1750A. The L64550 includes the Memory Management Unit (MMU) with memory expansion capabilities up to 1M words of memory, the Block Protect Unit (BPU), Memory Fault Status Register (MFSR), the Bus Arbitration Unit (BAU) with six bus masters, Start-up ROM interface, Discrete I/O Port, Trigger-go Counter and other options.

The L64500 CPU and the L64550 MBU chips were designed as a system to optimize performance.

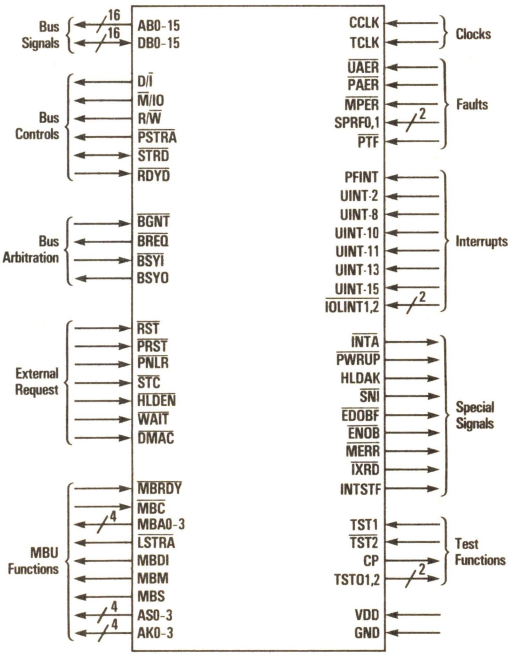
The L64500 and L64550 are included in MDE™, LSI Logic's Design System, as ASIC library elements. These elements can be used as Gigacells™ when combined with gate arrays or standard cells, or they can be used in multi-chip system simulations when adding new ASIC chips to the system.

The L64500 is available in several speed grades from 15 MHz to 25 MHz over the full military temperature range of −55°C to 125°C.

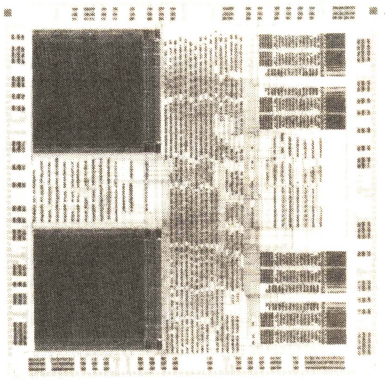
## Features

- Single-chip high performance microprocessor
- Implements MIL-STD-1750A (Notice 1) Instruction Set
- 0.9-micron channel length (1.5-micron drawn gate length) HCMOS 2-layer metal cell-based technology
- 25 MHz operation over full military range
- Power dissipation ≤ 1 W
- TTL compatible interface
- Flexible packaging capability
- Available as ASIC library element
- Performance optimized architecture
  - Split data and address bus
  - Variable width ALU: up to 32 bits
  - Instruction pre-fetch
  - Multiport register files
- Timers A and B option on-chip
- 64K word address space expandable to 3M word with optional MBU chip

## Logic Symbol and Chip Layout




**Logic Symbol**



**Chip Layout**

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# L64550
# MIL-STD-1750A
# MBU Peripheral Device

## Description

LSI Logic Corporation's L64550 is a monolithic 0.9-micron channel length (1.5-micron drawn gate length) HCMOS chip designed to support the L64500 CPU (MIL-STD-1750A ISA). The L64550 contains a number of MIL-STD-1750A support options including the Memory Management Unit (MMU) with mapping RAM, Block Protect Unit (BPU) with protection RAM, Memory Fault Status Register (MFSR), Watch-Dog timer and start-up ROM interface. In addition, the L64550 contains other options such as; a Bus Arbitrator with up to 6 bus masters, extended addressing capability to 8 M words, discrete I/O port, sophisticated CPU/MBU handshake to increase performance and bus time-out timer.

The MMU allows addressing of up to 1 M word of memory. In applications not requiring adherence to the standard, addressing can be extended to 8 M words. The MMU performs the logical-to-physical address translation and protection of logical space.

The BPU provides write protection in 1 K page granularity for up to 1 M word of physical memory for both L64500 CPU and DMA access.

If desired, the MMU and the BPU can be individually disabled.

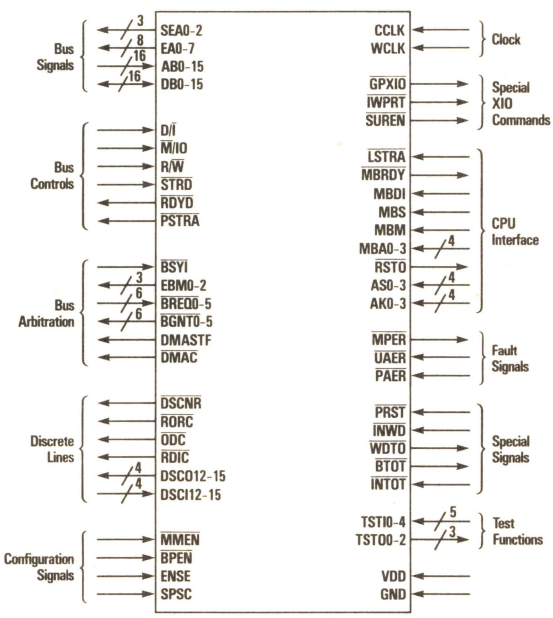
The L64550 MBU and L64500 CPU are included in MDE™, LSI Logic's Design System, as ASIC library elements. These elements can be used as Gigacells™ when combined with gate arrays or standard cells, or they can be used in multi-chip system simulations when adding new ASIC chips to the system.

The L64550 is available in several speed grades from 15 MHz to 25 MHz over the full military temperature range of −55°C to 125°C.

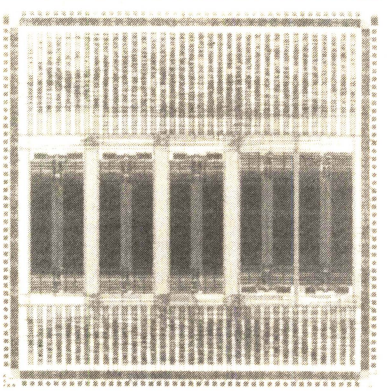
## Features

- 0.9-micron channel length (1.5-micron drawn gate length) HCMOS technology
- 25 MHz operation over full military range
- Power dissipation < 1W
- Memory Management Unit (MMU) with 512 × 16 cache RAM
- Block Protect Unit (BPU) with 128 × 16 cache RAM
- Hit/miss mechanism
- Discrete I/O ports
- Extended addressing to 8 M words
- Bus Arbitration Unit with up to 6 bus masters
- Memory Fault Status Register (MFSR)
- Start-up ROM interface
- Bus interface time-out timer
- Watch-Dog timer
- TTL compatible interface
- Flexible packaging capability
- Available as ASIC library element

## Logic Symbol and Chip Layout




Logic Symbol



Chip Layout

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# 16 × 16 Multiplier Accumulator (Signal Slice™)

# MA7010

## FEATURES

- 16 bit by 16 bit Multiplier/Accumulator with selectable accumulation and subtraction
- Pin and function compatible with IDT7210 and TDC1010 multiplier/accumulator
- 85nS multiply/accumulate time
- 55nS cycle time with optional pipeline stage
- 16 bit two's complement or unsigned magnitude inputs
- Full precision 35 bit result with optional rounding up to 19 bits
- Accumulator can be pre-loaded with a 35 bit value
- TTL compatible outputs and inputs
- Available in 64 pin DIL and 68 pin LCC and PGA
- Fully static low power CMOS/SOS

## APPLICATIONS

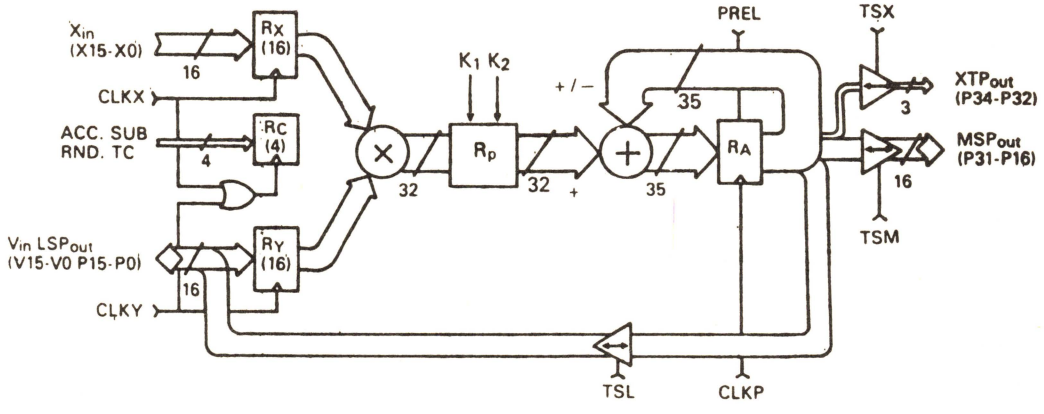
- Fast Fourier transform processing
- Array processing
- Matrix manipulations
- Radar signal processing
- General signal processing
- Minicomputer/microprocessor multiply accelerator

## DESCRIPTION

The MA7010 is a high speed 16 × 16 bit multiplier-accumulator. The input data can be specified as either two's complement or unsigned magnitude and the multiplier generates a full precision 32 bit product. Accumulation can take place to 35 bits precision.

The MA7010 is pin-for-pin compatible with the TDC1010 and IDT7210 multiplier-accumulators and is available in either 64 pin or 68 pin packages. The 68 pin version, while retaining pin-for-pin compatibility, offers the additional features controlled by the $K_1$ and $K_2$ inputs. One facility is the provision of an optional pipeline register $R_P$ which can greatly improve the multiply-accumulate rate.

Additionally, the output register $R_A$ can be set to zero. Both features are highly relevant to digital filter and matrix operations.

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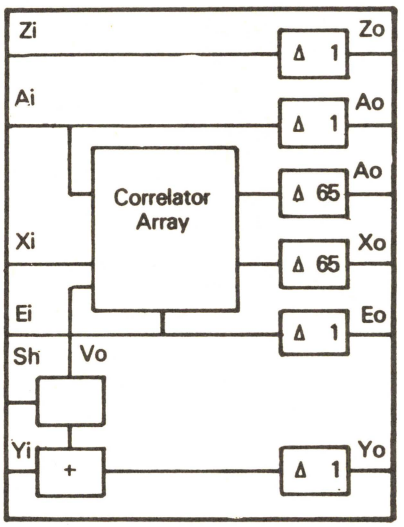
# BIT-SLICE CORRELATOR MA717O

## FEATURES

- 64 stage correlation for 1-bit reference and 4 bit data
- 10 MHz data throughput.
- 16 bit accumulate accuracy.
- Expandable correlation length, reference width and data width.
- 16 bit threshold comparator.
- CMOS/SOS technology.




The MA717O is a 64 stage bit slice all digital correlator with 4-bit data and 1-bit reference. The design allows expansion in reference length and width and data width without the need for additional logic. The MA717O computes the correlation Y(k) between 64 reference coefficients a(i) and a data sequence x(i), expressed mathematically as

$$Y(k) = \sum_{i=0}^{63} a(i) \cdot x(k+i)$$

The design, in CMOS/SOS technology, uses systolic techniques to provide a parallel correlation rate of 10 MHz. All internal operations are performed in 2's complement arithmetic but the data stream may be presented in either 2's complement or positive magnitude. The result is always in 2's complement and may be compared to a 2's complement 16 bit threshold level giving greater than and equal outputs.

Multiple chip applications are possible by utilizing the data expansion register and result shift together with the available data and reference outputs delayed by 1 or 65 clock cycles, and the result input and accumulate.

The MA717O has a single clock input which controls the correlation function.

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# 1-D/2-D Convolver (signal stream™) MA7180

## FEATURES

- (3 × 3)-stage 2-D or 9-state 1-D convolution
- 20 Msamples per second throughput
- 10-bit data, 8-bit coefficients
- Full precision 22-bit output, with optional rounding to 16 bits
- Parallel unmultiplexed data input/output
- Coefficient loading through a serial input port or using parallel data ports
- TTL compatible input/output
- 68-pin LCC or pin grid array
- Fully static CMOS/SOS

## APPLICATIONS

- High speed 1-D and 2-D FIR filtering
- Image processing for noise removal, enhancement, deblurring, industrial vision-robotics, military infra-red and medical applications
- Multibit correlation for radar and sonar
- Transversal filtering for communications (e.g., adaptive equalization)

## SUPPORT DEVICES

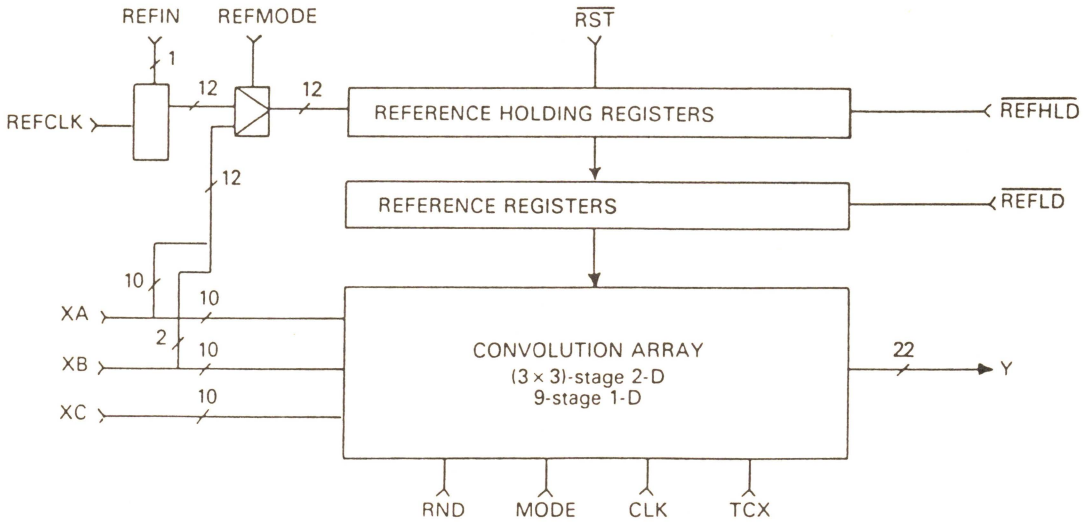
- MA7186 Video line buffer
- MA7188 Cascade-ALU

## DESCRIPTION

MA7180 is a high accuracy digital convolver which can be configured, using a mode control input, to perform (3 × 3)-stage 2-D or 9-stage 1-D convolution, with a maximum throughput of 20 Msamples per second. The device has three 10-bit data input ports and a 22-bit output port. It convolves 10 bits per pixel image or signal data with 8 bits per coefficient reference, to produce a 22-bit full precision output with optional rounding to 16 bits.

The reference coefficients can be loaded through a serial port or using the parallel data input ports. The reference is first loaded into a holding register, which, in the serial mode, allows coefficient update without interrupting the convolution. A separate clock input is provided for serial reference loading.

The MA7180 is part of a family of high performance digital signal and image processing devices being produced by MEDL. Two other devices in the family, namely MA7186 and MA7188, are particularly useful in designing systems with MA7180. The MA7188 cascade-ALU allows MA7180 devices to be easily cascaded to increase the size of the convolution reference window. The MA7186 video line buffer allows images to be entered into the convolution system in a raster scan format.




MA7180 Block Diagram

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# Video Line Buffer (Signal Stream™) MA7186

## FEATURES

- Stores 1024 words of 10 bits
- One line and two line configurations
- Programmable line lengths: 64, 128, 256, 512, 1024
- Intermediate line lengths by truncation
- Delay line and sequential access modes
- Three 10-bit parallel data ports: Input, Input/output, and Output
- Internal address generation
- 50ns cycle time
- TTL compatible inputs and outputs
- 48 pin DIL and LCC
- Fully static low power CMOS/SOS

## APPLICATIONS

- Tapped two line delay for 3× filters
- Row to column scan conversion for separated 2-D filters
- Sequential access memory
- Support chip for 1-D/2-D convolver and rank order filter

## DESCRIPTION

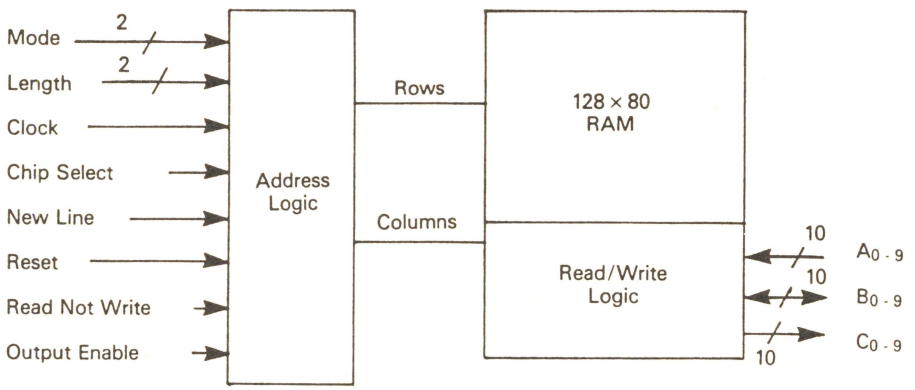
The Multi-Function Video Line Buffer can be used as a tapped line delay or as a two dimensional sequential access memory. In the delay mode, one input port and two output ports provide a total delay of up to 1024 pixels, with a tap at half the length. In the sequential access mode, one port (X) is required for the rows of the image plane and there are two Y ports for the columns. Image rows written to the X port may be read from the Y ports as columns, and columns written to the Y port may be read from the X ports as rows.

Note that X and Y refer to the directions on the image plane, the physical ports of the device (A, B and C) may be used for either the rows or columns.

In all modes, the line length may be programmed to 64, 128, 256, 512, and 1024 pixels. Intermediate line lengths may be obtained by truncation on four word boundaries. Line lengths of 512 and less provide two lines of storage.

The Mode input selects delay, X to Y or Y to X configurations and the Length input programs the natural line length. Reset initializes the pointer to the first pixel of the first line. Each pixel access is synchronous with Clock, which is enabled by Chip Select; Read Not Write determines the data direction. New Line steps the pointer to the first pixel of the next line, to facilitate truncation if required. Output Enable controls bus access from the output ports.

The two Y ports access two pixels per cycle, providing twice the peak data rate of the X port. This allows a full 20M samples/second subsystem throughput in separated 2-D rank order filter applications.

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# Cascade-ALU (Signal Stream™) MA7188

## FEATURES

- Fast ALU with a programmable delay on one input
- Three 16-bit ports: two input and one output
- ALU arithmetic functions:
  Add, subtract, min, max, absolute value
- ALU logic functions: XOR, AND
- Delay programmable from 0 to 31 cycles
- Cascadable to increase wordlength and/or delay
- 50ns clock cycle
- TTL compatible inputs and outputs
- 68 pin LCC or Pin Grid Array
- Fully static, low power, CMOS/SOS

## APPLICATIONS

- Cascading 1-D or 2-D digital convolution devices
- Combining outputs of systems with different processing latencies
- Thresholding and limiting
- Combining outputs of rank order filters and convolvers to form complex algorithms
- Removing stationary target responses in moving target indicator (MTI) radar

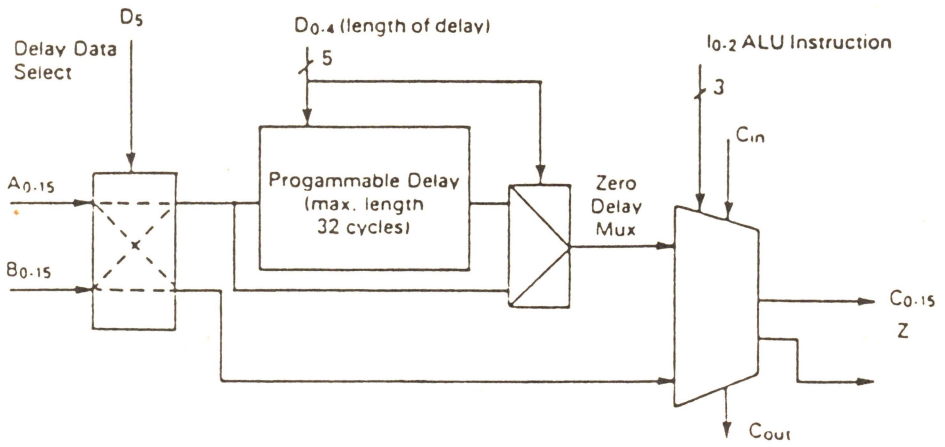
## DESCRIPTION

The MA7188 is a three port arithmetic and logic unit, ports A and B being inputs and port C the output. Provision is made for delaying either A or B before an operation is performed.

The arithmetic and logic unit supports the most common operations required when combining signal streams (add, subtract, min, max), as well as absolute value XOR and AND instructions and overflow and zero flags. Carry in and carry out signals facilitate the cascading of devices for 32-bit arithmetic and cascading in the other directions can be used to increase the programmable delay.

The device can be used to combine the outputs of two processing units having different latencies. For example, the number of stages and wordlength of convolution can be increased through use of the Cascade-ALU to connect a number of 1-D/2-D convolver devices. Another example is edge detection in images where the outputs of several convolutions or rank order filters must be combined.

The MA7188 uses the same 68-pin package as the 1-D/2-D convolver (MA7180) and the rank order filter (MA7190) in order to assist board layout.

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# Rank Order Filter (Signal Stream™)

# MA7190

## FEATURES

- One or two-dimensional separated rank order
- Programmable filter size up to (15 × 1) per device
- 10 bits unsigned magnitude data input and output
- Fully programmable rank
- Selectable filter or rank output
- 20 Msamples/sec throughput
- Parallel, TTL compatible input/output
- 68 pin LCC or Pin Grid Array
- Fully static low power CMOS-SOS

## APPLICATIONS

- High speed 1-D or 2-D nonlinear filtering
- 1-D or 2-D running order statistics
- Real-time image processing in military, industrial, medical and video communications systems
- Robotics and computer vision
- Edge and corner detectors
- Constant false alarm rate (CFAR) radar detectors
- Digital AM radio detectors

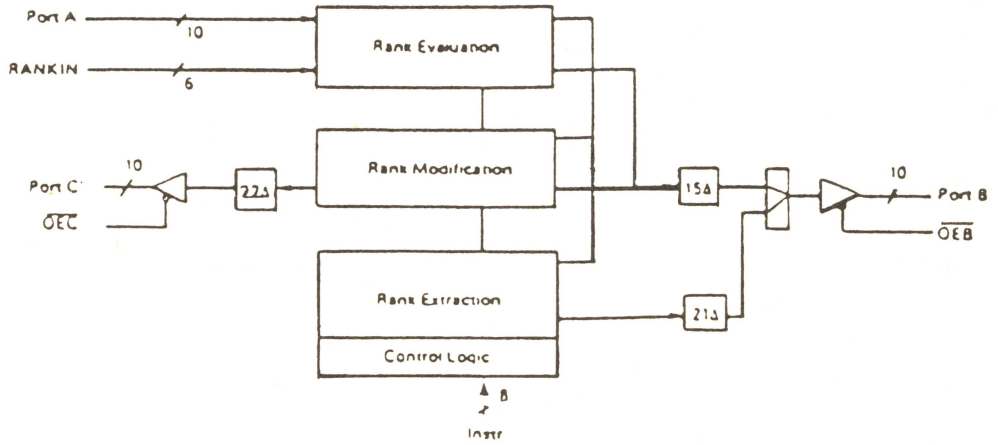
## DESCRIPTION

In many signal processing applications, such as impulse noise removal, linear filters do not provide the right sort of filter performance. Such applications frequently benefit from rank order nonlinear filters such as median, minimum and maximum filters. However rank order filters are difficult to implement on conventional hardware.

The MA7190 Rank Order Filter is a high performance nonlinear filter offering 20M samples/second performance. Its systolic array architecture permits the processing of data streams in real time for demanding applications such as image processing and radar signal processing. Although the rank order filter is inherently a 1-D filter, it can be cascaded (with suitable buffering) to perform 2-D separated filtering.

The rank order filter can be programmed to perform a number of different filter functions. The filter can be programmed to any length up to (15 × 1) although in most cases the length will be odd. The rank of the filter can also be programmed which means that min, max, median and other filters can be implemented. Two types of output can be generated by the filter; it can either output a filtered version of the input datastream or it can output the ranks of input samples.

The 10-bit wide input data stream enters the device through Port A; the rank used by the filter is supplied through the RANKIN input. The output generated by the filter may come from one or both of the output ports. In the case of the normal filtering operation, data emerges as a 10-bit value from Port B. When a rank output is requied, the two ranks emerge as 5-bit 2s complement values from Ports B and C.

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# Signal Stream™ Product Family

# MA71xx

**PRELIMINARY**

## FEATURES

- Comprehensive set of building blocks for signal stream data processing
- High level of integration to reduce part count
- High speed — family supports up to 20 M sample/sec data rates
- High computational throughput by use of pipelining and systolic array techniques
- Cascadable to extend sizes of blocks or to implement compound algorithms
- Low power CMOS-SOS technology

## APPLICATIONS

- Real time image processing
- Real time radar processing
- Digital radio
- Image/signal processing workstations
- Computer graphics
- Embedded signal processing systems

Family includes the:
MA7170 Bit-slice correlator
MA7180 1-D/2-D convolver
MA7186 Multi function video line buffer
MA7188 Cascade-ALU
MA7190 Rank order filter

## DESCRIPTION

Marconi Electronic Devices' Signal Stream family of devices provides all the major elements required in high speed digital signal processing. These products will be used where the best available computational throughput is required from available technology, and will revolutionize low level signal processing by allowing the user to build real time algorithms from Signal Stream blocks.

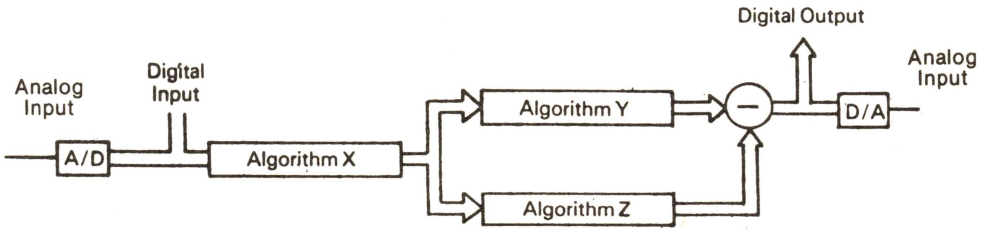
Many applications such as low level image processing, radar signal processing and computer graphics require the processing of streams of data in real time. Conventional signal processors cannot match such data rates and so novel architecture must be employed. The Signal Stream product family employs systolic array and pipelined architecture to allow very high data rates to be processed. Furthermore, the use of CMOS-SOS technology in these devices reduces the power consumption and dissipation in real time systems.

The Signal Stream concept provides a set of building blocks which are capable of performing operations on streams of data. The bit-slice correlator, 1-D/2-D convolver and rank order filter permit real time correlation, linear and non-linear filtering. Compound algorithms can be implemented by cascading several types of devices from the family including the line buffer and cascade-ALU support elements.

Signal Stream products have a high degree of integration and will considerably reduce the size of systems designed with first generation DSP circuits; for example a single 1-D/2-D convolver replaces nine multipliers and several glue logic devices. The family will allow reductions in part count board space and make system design more straightforward.

Since the product family is optimized for processing long streams of data, changes of system configuration are likely to be infrequent. In embedded applications such as front-end processors the processor instructions can be hardwired; alternatively in signal processing workstations the configuration of Signal Stream devices can be altered under microprogram control.

**Signal Stream™ Concept**

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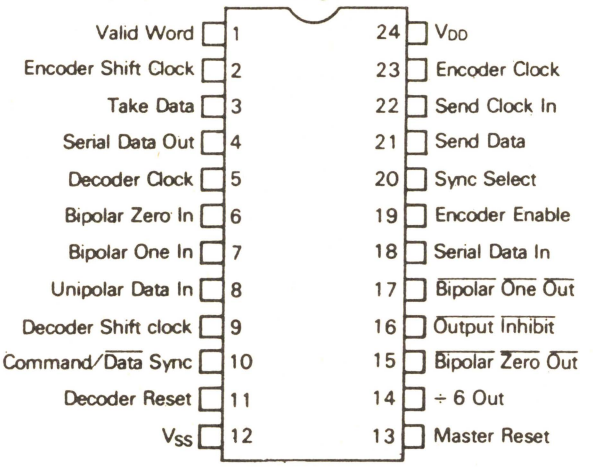
# CMOS MANCHESTER ENCODER-DECODER

**MA15530**

## FEATURES

- MIL-STD-1553 compatible.
- 1.25 megabit/sec. Maximum Data Rate.
- Sync Identification and Lock-in.
- Clock Recovery.
- Manchester II Encode/Decode.
- Separate Encoder and Decoder Sections.
- Low Operating Power.
- Military Temperature Range— 55°C.
- Direct Replacement for Harris HD15530.

*Pin Assignment*



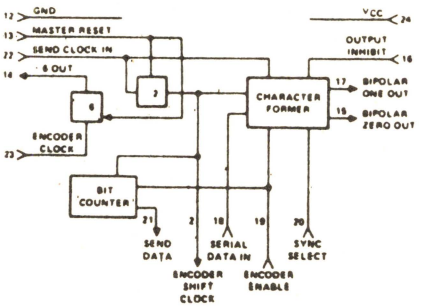

## DESCRIPTION

Marconi's MA15530 is a high performance CMOS I.C. used to implement Mil-Std-1553 and similar Manchester II encoded, time division multiplexed, serial data protocols. The device is divided into two independent sections, encoder and decoder, with a common master reset. It meets many of the requirements of Mil-Std-1553. The encoder produces the sync pulse and parity bit and encodes the data bits. The decoder recognizes the sync pulse, decodes the data bits and checks for parity.

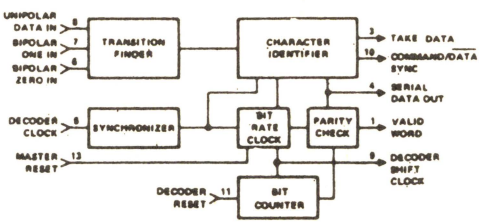
The MA15530 is fully guaranteed to support the 1 MHz data rate of Mil-Std-1553 over the full temperature and supply voltage ranges. It interfaces with CMOS, TTL or N-channel support circuitry and operates from a standard 5 volt supply. This circuit can also be used in many party line digital data communications applications.

*Block Diagrams*

ENCODER




DECODER

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# SOS 1553B BUS CONTROLLER / REMOTE TERMINAL

**MA3690**
**MA3691**

## FEATURES

- Radiation hardness
- Mil. temp. range −55 to +125°C
- Single power rail (5V)
- Dual bus capability
- Minimal subsystem interface
- Powerful bus control facility
- Complete remote terminal protocol
- Two 48 pin packages
- 16 bit highway
- Latch up immunity

## FUNCTIONS

### 1. Bus Control Mode

- Table driven or single shot mode
- Automatic retry facility
- Automatic interrupt facility
- Enhanced self monitoring with report word

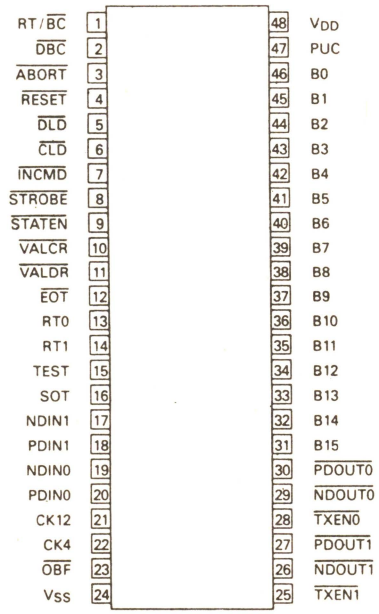
### 2. Remote Terminal Mode

- All mode commands implemented
- Selectable broadcast acceptance
- Loop test on own transmission
- Subsystem control of status bits
- Extendable 'No response' timeout
- Bit word
- Overriding commands
- RT to RT transfer
- Broadcast RT to RT transfer
- Reserved mode codes may be declared legal

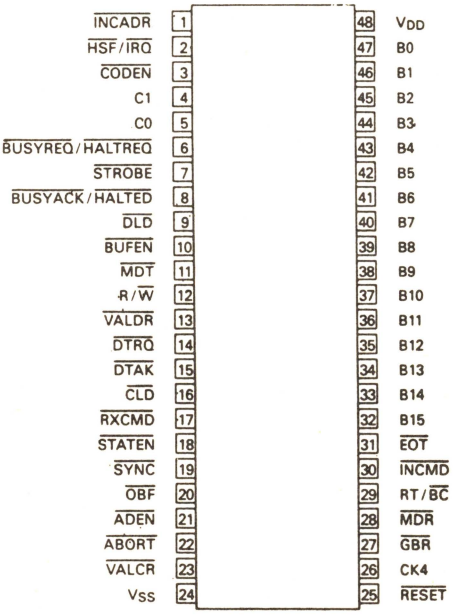
### 3. Passive Monitoring of Selected Bus

- Complete monitoring of selected bus

**TRANSCEIVER CHIP PINOUT (MA3690)**




**TERMINAL CONTROLLER CHIP PINOUT (MA3691)**

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# Radiation Hard CMOS-SOS Static RAM Family

## MASxxxx
Performance Summary

**FEATURES**
- Industry standard pin outs
- CMOS-SOS technology
- High SEU immunity
- Radiation hard
- Latch-up immune
- Fully static
- Low standby current
- Single 5V supply
- Fast access time
- Three state outputs
- Fully TTL compatible

| Device | Format | Pins | Access time (ns) |
|---|---|---|---|
| MAS5101 | 256 × 4 | 22 | 90 |
| MAS5114 | 1024 × 4 | 18 | 90 |
| MAS6116 | 2048 × 8 | 24 | 100 |
| MAS5104 | 4096 × 1 | 18 | 90 |
| MAS6167 | 16384 × 1 | 24 | 100 |
| MAS6187 | 65536 × 1 | 22 | 35* |

### SILICON ON SAPPHIRE RAM RADIATION PERFORMANCE

The MEDL Silicon on Sapphire (CMOS-SOS) process provides significant advantages over other CMOS technologies. The absence of the bulk silicon substrate reduces parasitic capacitances giving an improvement in speed. The use of a self aligning silicon gate process gives further improvements in both of the above parameters and achieves high packing densities. The sapphire substrate also removes the risk of 'latch-up' allowing greater flexibility of use in electrically severe environments and a significant improvement in radiation tolerance.

| Device | Total dose Krad (Si) | Transient gamma (soft upset) | Single event upset $\times 10^{-10}$ Errors/Bit day (Note 1) |
|---|---|---|---|
| MAS5101 | 100 | $>1.0 \times 10^{10}$ | TBD |
| MAS5114 | 100 | $>2.6 \times 10^{10}$ | 3.1 (90% worst case)<br>1.9 (solar minimum) |
| MAS6116 | 200 | $>2.6 \times 10^{10}$ | 3.1 (90% worst case)<br>1.9 (solar minimum) |
| MAS5104 | 100 | $>2.6 \times 10^{10}$ | 3.1 (90% worst case)<br>1.9 (solar minimum) |
| MAS6167 | 200 | $>2.6 \times 10^{10}$ | 3.1 (90% worst case)<br>1.9 (solar minimum) |
| MAS6187 (Note 2) | 1000 | $>5.0 \times 10^{10}$ | 3.1 (90% worst case)<br>1.9 (solar minimum) |

Note 1. — Solar minimum, geostationary orbit. Tested in cyclotron and using Californium source.
Note 2. — Target specification.

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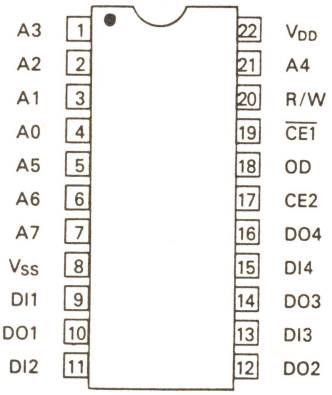
# CMOS-SOS
# 256 x 4 Bit Static RAM MAS5101
PROVISIONAL DATA

## FEATURES
- Pin compatible with 5101 series
- Latch up immune
- Directly TTL compatible, all inputs and outputs
- Three state output
- Radiation hard
- CMOS-SOS technology
- Fast access time, 100ns typical
- Low standby current, 100μA
- Fully static

## PIN ASSIGNMENT



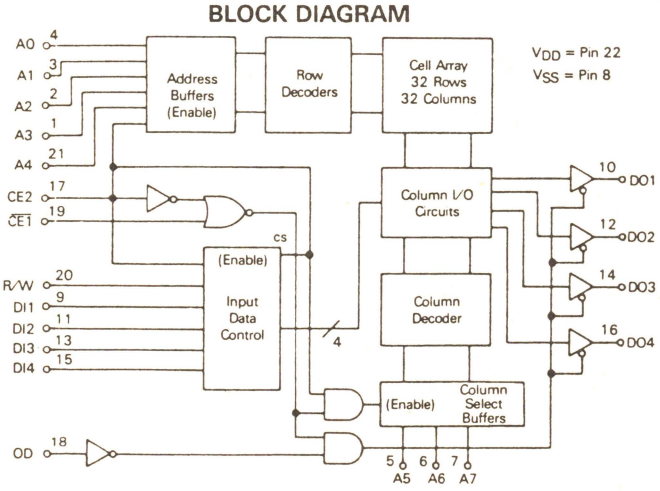

The MAS5101 1024 bit (256 x 4 bits) static RAM is fabricated using MEDL CMOS-SOS low power high performance process. The device has two chip enable inputs. Minimum standby current is drawn by this device when CE2 is at a low level.

All inputs and outputs are directly TTL compatible. The MAS5101 has separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire-OR'ed for use in common data I/O systems.

The MAS5101 has the additional feature of guaranteed data retention at a power supply voltage as low as 2 volts.

The MEDL Silicon-on-Sapphire (CMOS—SOS) provides significant advantages over other CMOS technologies. The absence of the bulk silicon substrate reduces parasitic capacitances, giving an improvement in speed. The use of a self aligning silicon gate process gives further improvements in both of the above parameters and achieves higher package densities. The sapphire substrate also removes the risk of 'latch up' allowing greater flexibility of use in electrically severe environments, and a significant improvement in radiation tolerance.

## BLOCK DIAGRAM




## TRUTH TABLE

| CE1 | CE2 | OD | R/W | Din | Output | Mode |
|---|---|---|---|---|---|---|
| H | X | X | X | X | High-Z | Not Selected |
| X | L | X | X | X | High-Z | Not Selected |
| X | X | H | H | X | High-Z | Output Disabled |
| L | H | H | L | X | High-Z | Write |
| L | H | L | L | X | Din | Write |
| L | H | L | H | X | Dout | Read |

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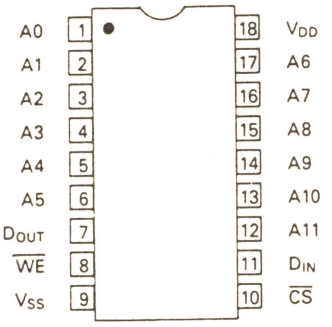
# CMOS-SOS
# 4096 x 1 Bit Static RAM
# MAS5104
PROVISIONAL DATA

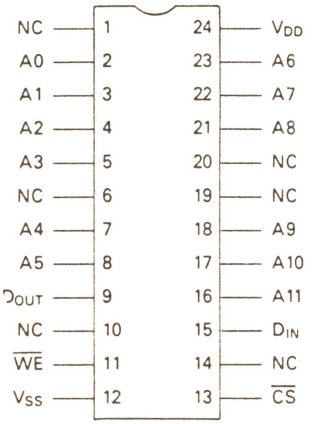
## FEATURES
- Pin compatible with 2104/5104 series
- CMOS-SOS technology
- Low standby current 25μA
- Single 5V supply
- Fast access time 90nS
- Three state outputs
- Fully TTL compatible
- Radiation hard
- Fully static
- Available in DIL or Flatpack

*Radiation Hard Features*
- Total Dose — > 100K Rad (Si)
- Transient Upset — > $10^{10}$ Rad (Si)/sec
- Latch up — Not Possible
- SEU immunity — < 2 x $10^{-10}$ errors/bit-day

## PIN ASSIGNMENT




18 LEAD CERAMIC DIL




24 LEAD CERAMIC FLATPACK

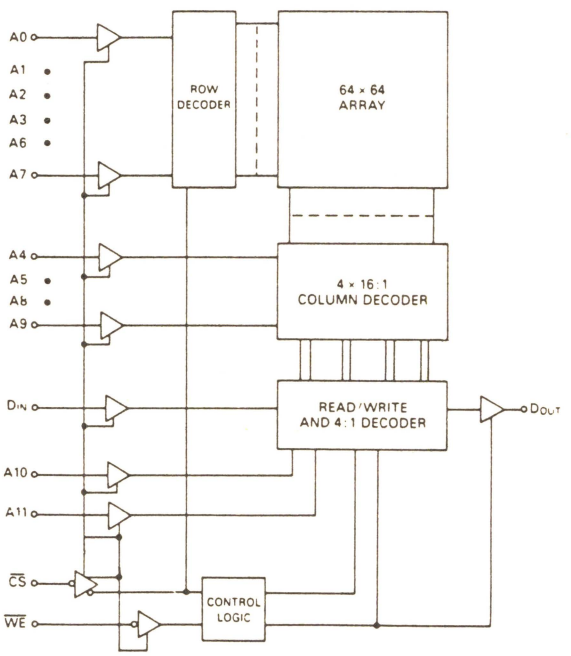
The MAS 5104 4096 Bit Static RAM is configured as 4096 by 1 bit and fabricated using MED CMOS-SOS low power, high performance process.

The MED Silicon-on-Sapphire (CMOS-SOS) process provides significant advantages over other CMOS technologies. The absence of the bulk silicon substrate reduces parasitic capacitances, giving an improvement in speed. The use of a self aligning silicon gate process gives further improvements in both of the above parameters and achieves high package densities. The sapphire substrate also removes the risk of 'latch-up' allowing greater flexibility of use in electrically severe environments, and a significant improvement in radiation tolerance.

The fully static operaion requires no clocks or refresh circuitry. The three state outputs make it possible to economically configure several MAS5104's for bus oriented systems. Address line input buffers are de-selected when CS is high.

| CS | WE | I/O Pin | Mode |
|---|---|---|---|
| H | H | High Z | Not Selected |
| H | L | High Z | Not Selected |
| L | H | Data out | Selected |
| L | L | Data in | Selected |

## BLOCK DIAGRAM

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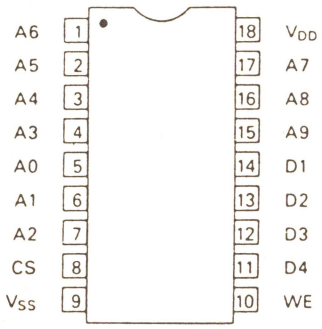
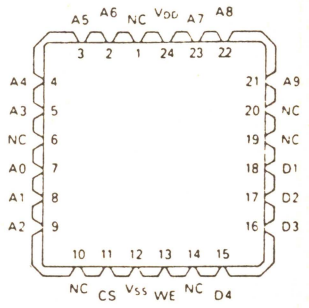
# CMOS-SOS
# 1024 × 4 Bit Static RAM MAS5114

**FEATURES**
- Pin compatible with 2114/5114 series
- CMOS-SOS technology
- Low standby current 25μA
- Single 5V supply
- Fast access time 90nS
- Three state outputs
- Fully TTL compatible
- Fully static
- Radiation hard
- Available in DIL or LCC

*Radiation Hard Features*
- Total Dose — > 100K Rad (Si)
- Transient Upset — > $10^{10}$ Rad (Si)/sec
- Latch up — Not Possible
- SEU immunity — < 2 x $10^{-10}$ errors/bit-day




18 LEAD CERAMIC DIL




24 CONTACT CERAMIC LCC

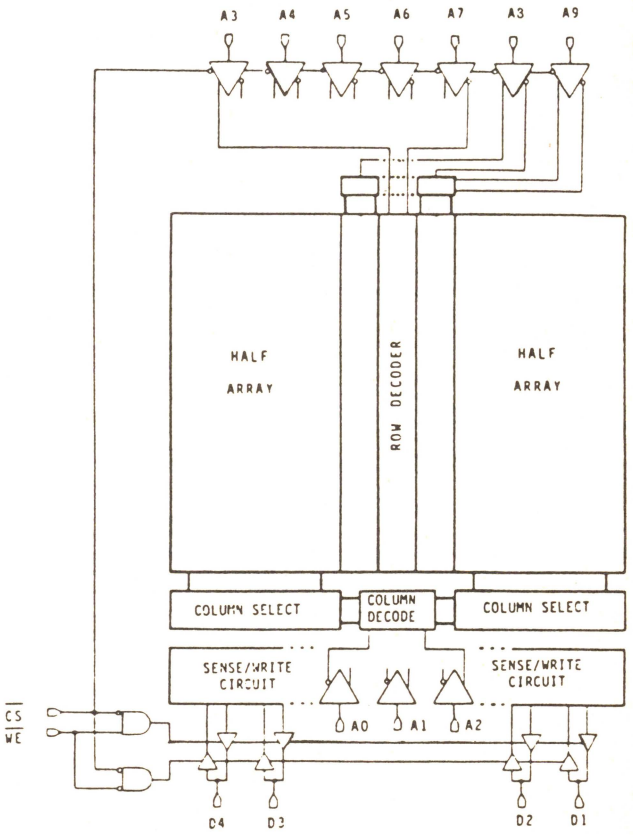
The MAS 5114 4096 Bit Static RAM is configured as 1024 by 4 bit and fabricated using MED CMOS-SOS low power, high performance process.

The MED Silicon-on-Sapphire (CMOS-SOS) process provides significant advantages over other CMOS technologies. The absence of the bulk silicon substrate reduces parasitic capacitances, giving an improvement in speed. The use of a self aligning silicon gate process gives further improvements in both of the above parameters and achieves high packing densities. The sapphire substrate also removes the risk of 'latch-up' allowing greater flexibility of use in electrically severe environments, and a significant improvement in radiation tolerance.

The fully static operation requires no clocks or refresh circuitry. The three state outputs make it possible to economically configure several MAS5114's for bus oriented systems. Address line input buffers are de-selected when CS is high.

| CS | WE | I/O Pin | Mode |
|---|---|---|---|
| H | H | High Z | Not selected |
| H | L | High Z | Not selected |
| L | H | Data out | Selected |
| L | L | Data in | Selected |

## BLOCK DIAGRAM

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# CMOS - SOS
# 2048 x 8 Bit Static RAM

# MAS6116

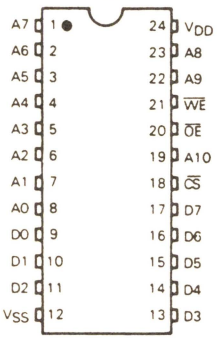
*Features*

- Pin compatible with 6116 series
- CMOS - SOS technology:
- Low standby current Typ. 100 $\mu$A
- Single 5V supply
- Fast access time
- Fully TTL compatible
- Three State Outputs
- Radiation Hard
- Fully Static
- Available in DIL or Flatpack

*Radiation Hard Features*

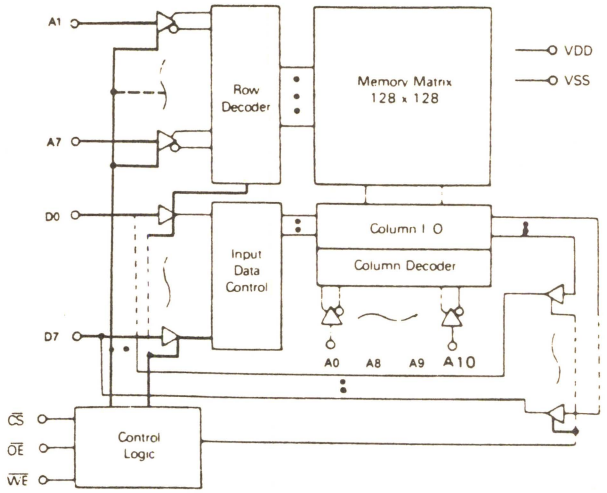
- Total Dose — > 100K Rad (Si)
- Transient Upset — > $10^{10}$ Rad (Si)/sec
- Latch up — Not Possible
- SEU immunity — < 2 x $10^{-9}$ errors/bit-day

**PIN ASSIGNMENT**




The MAS6116 16,384 bit Static RAM is configured as 2048 by 8 bits and fabricated using Marconi's CMOS - SOS low power, high performance process. Data lines are bi-directional for bus connection and are controlled by 3 inputs, Chip Select, Output Enable and Write Enable. Pin out is compatible with standard 16K EPROM/MASK ROM and all inputs and outputs are TTL compatible. It is a completely static RAM with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the high state. The Marconi Silicon-on Sapphire (CMOS-SOS) process provides significant advantages over other CMOS technologies. The absence of bulk silicon substrate reduced parastic capacitances, giving an improvement in speed. The use of a self-aligning silicon gate process gives further improvements in both of the above parameters and achieves higher package densities. The sapphire substrate also removes the risk of latch-up allowing greater flexibility of use in electrically severe environments, and a significant improvement in radiation tolerance.

**BLOCK DIAGRAM**




| CS | OE | WE | MODE | VDD CURRENT | I/O PIN |
|---|---|---|---|---|---|
| H | X | X | Not Selected | IDDL | High Z |
| L | L | H | Read | IDD | Dout |
| L | H | L | Write | IDD | Din |
| L | L | L | Write | IDD | Din |

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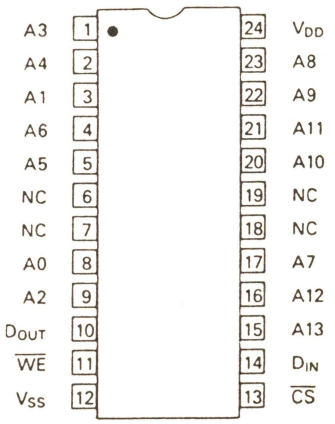
# CMOS - SOS
# 16384 x 1 Bit Static RAM

# MAS6167

*FEATURES*

- Functionally compatible with 6167 series
- CMOS - SOS technology:
- Radiation hard
- High SEU immunity
- Latch up immune
- Low standby current Typ. 100 μA
- Single 5V supply
- Fast access time 100ns
- Fully TTL compatible
- Three state outputs
- Fully Static
- Available in DIL or Flatpack

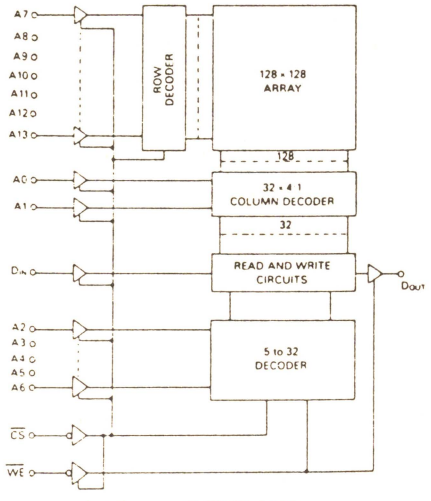
PIN ASSIGNMENT




The MAS6167 16384 bit Static RAM is configured as 16384 by 1 bits and fabricated using MEDL CMOS - SOS low power, high performance process.

The MEDL Silicon-on-Sapphire (CMOS-SOS) process provides significant advantages over other CMOS technologies. The absence of bulk silicon substrate reduces parasitic capacitances, giving an improvement in speed. The use of a self-aligning silicon gate process gives further improvements in both of the above parameters and achieves higher package densities. The sapphire substrate also removes the risk of latch-up giving greater flexibility of use in electrically severe environments, and a significant improvement in radiation tolerance.

MAS6167 has separate I/P and O/P terminals controlled by Chip Select and Write Enable. It is a completely static RAM with no clock or timing strobe required. Address input buffers are deselected when chip select is in the high state.




Block Diagram — MA6167 16K x 1 RAM

| CS | WE | Mode | $V_{DD}$ Current | I/O Pin |
|---|---|---|---|---|
| H | X | Not Selected | $I_{DDL}$ | High Z |
| L | H | Read | $I_{DD}$ | Dout |
| L | L | Write | $I_{DD}$ | Din |

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# Radiation Hard High Speed CMOS/SOS Logic

# 54 HSC & HST Series

**FEATURES**

- Plug in replacement for 54/74 LS and HCT
- Radiation Hard
- High S.E.U. immunity
- Latch up immune
- Available to Mil Std 883S & ESA 9000
- Low power CMOS-SOS Technology
- Dual in Line or Leadless Chip Carrier packages

MEDL's CMOS-SOS HSC/T octal interface gates offer the combined benefits of low power, high speed CMOS with the inherent latch up immunity, S.E.U. immunity and high level or radiation hardness of MEDL's Silicon on Sapphire technology. The family of latches offers transparent or clocked operation and has inverted or non-inverted three state output. The decoder family offers two; single 'one-of-eight' latched or unlatched or dual 'one-of-four' configurations. Bus buffering is catered for with symmetrical high current drivers with several configurations of chip select for single or bi-directional operation. The 54 HSC/T series of circuits are pin for pin compatible with the 54 LS series octal range. HSC and HST octal devices have CMO and TTL compatible inputs/outputs respectively.

**DECODERS/DEMULTIPLEXERS**

| | |
|---|---|
| **54 HSC/T137** | One of eight with latched inputs, inverted outputs |
| **54 HSC/T138** | One of eight with unlatched inputs, inverted outputs |
| **54 HSC/T237** | One of eight with latched inputs, non-inverted outputs |
| **54 HSC/T238** | One of eight with unlatched inputs, non-inverted outputs |
| **54 HSC/T139** | Dual one of four with unlatched inputs, inverted outputs |
| **54 HSC/T239** | Dual one of four with unlatched inputs, non-inverted outputs |

**BUFFERS/LINE DRIVERS**

| | |
|---|---|
| **54 HSC/T240** | Bi-directional connections inverting |
| **54 HSC/T244** | Bi-directional connections non-inverting |
| **54 HSC/T241** | Bi-directional connections, non-inverting, complementary enable |
| **54 HSC/T540** | Uni-directional connections, inverting |
| **54 HSC/T541** | Uni-directional connections, non-inverting |

**TRANSCEIVERS**

| | |
|---|---|
| **54 HSC/T245** | Non-inverting |

**TRANSPARENT LATCHES**

| | |
|---|---|
| **54 HSC/T373** | Non-inverting, 3 state outputs |
| **54 HSC/T573** | Functionally idential to 373 — different pin out |
| **54 HSC/T533** | Inverting, 3 state outputs |
| **54 HSC/T563** | Functionally identical to 533 — different pin-out |

**EDGE TRIGGERED 'D' FLIP FLOPS**

| | |
|---|---|
| **54 HSC/T374** | Non-inverting, 3 state outputs |
| **54 HSC/T574** | Functionally identical to 374 — different pin-out |
| **54 HSC/T534** | Inverting, 3 state outputs |
| **54 HSC/T564** | Functionally identical to 534 — different pin-out |

Further octal variants will be available shortly.
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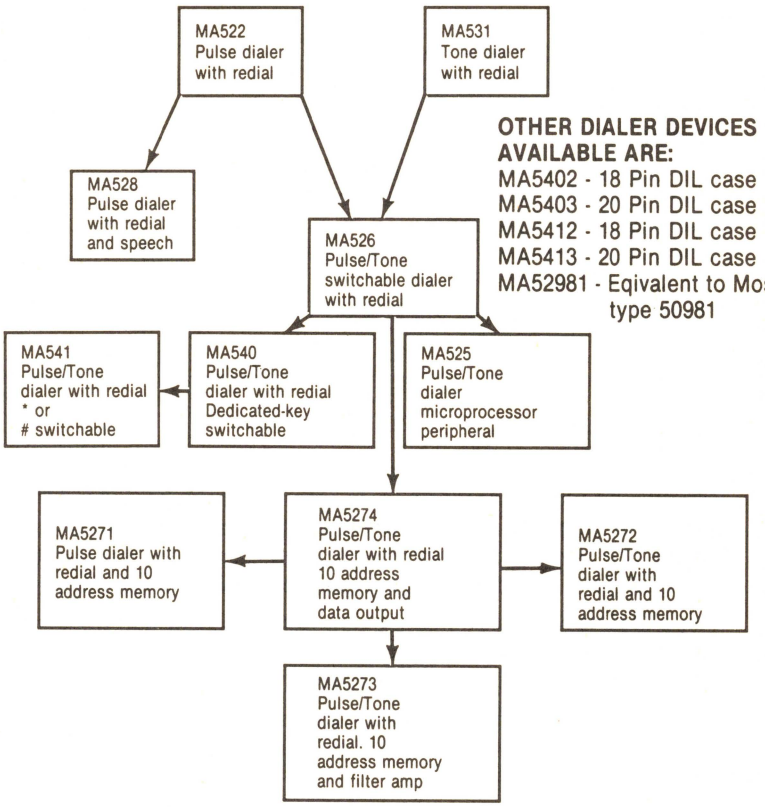
# TELEPHONE DIALER FAMILY

Marconi's unique range of LD/DTMF switchable dialer chips is unrivalled. All are designed to meet exacting PTT requirements, giving you instant compatibility with telecommunications standards and specifications, worldwide.

This comprehensive range of dialers is designed to be pin and electrically compatible. So your telephone can be reconfigured simply by exchanging one chip for another with no, or minimal, circuit modifications.

All chips are fabricated in low power CMOS. They operate from a supply voltage of 2.5 volts to 10 volts, and all chip functions are timed by the use of an accurate and inexpensive external ceramic resonator. Each chip has a last number redial capability and timed break recall. A selectable break/make ratio is also standard.




**OTHER DIALER DEVICES AVAILABLE ARE:**

MA5402 - 18 Pin DIL case
MA5403 - 20 Pin DIL case
MA5412 - 18 Pin DIL case
MA5413 - 20 Pin DIL case
MA52981 - Eqivalent to Mostek type 50981

| | Low Power CMOS Operation | Last number redial | LNR stores up to 21 digits | Selectable make/break ratio 2:1 & 3:2 | Selectable inter digit pause | Timed flash | Uses inexpensive 560 kHz resonator | Single contact keypad | Minimum supply voltage (V) | Electronic Speech circuit with gain regulation | MF tone pairs | MF tone filter amplifier | User selectable loop disconnect or DTMF dialer modes | Stores ten 18 digit numbers on chip | Scratchpad memory capability | Inter on-hook timeout | Keypad LD — MF switchover | Micro controlled applications | Works with 4 and 8 bit multiplexed bus | Single key memory access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MA 522 | * | * | * | * | * | * | * | * | 2.5 | | | | | | | * | | | | |
| MA 52981 | * | * | * | * | | | 480KHz | * | 2.5 | | | | | | | * | | | | |
| MA 528 | * | * | * | * | * | * | * | * | 2.5 | * | | | | | | * | | | | |
| MA 531 | * | * | * | | | * | * | * | 2.5 | | 16 | * | | | | * | | | | |
| MA 5262 | * | * | * | * | * | * | * | * | 2.4 | | 12 | | * | | | * | | | | |
| MA 5263 | * | * | * | * | * | * | * | * | 2.4 | | 12 | * | * | | | * | | | | |
| MA 5402 | * | save | 31 | | * | * | * | * | 2.4 | | 12 | | * | | | * | | | | |
| MA 5403 | * | save | 31 | * | | * | * | * | 2.4 | | 12 | * | * | | | * | | | | |
| MA 5412 | * | * | 31 | * | * | * | * | * | 2.4 | | 12 | | * | | | * | * | | | |
| MA 5413 | * | * | 31 | * | * | * | * | * | 2.4 | | 12 | * | * | | | * | * | | | |
| MA 5471 | * | * | * | * | * | * | * | * | 2.4 | | | | | * | * | * | | | | |
| MA 5272 | * | * | * | * | * | * | * | * | 2.4 | | 12 | | * | * | * | * | | | | |
| MA 5273 | * | * | * | * | * | * | * | * | 2.4 | | 12 | * | * | * | * | * | | | | |
| MA 5274 | * | * | * | * | * | * | * | * | 2.4 | | 12 | * | * | * | * | * | | | | |
| MA 525 | * | * | * | * | * | * | * | | 2.5 | | 16 | * | * | | | * | | * | * | |
| MA 542 | * | * | * | * | | | 480KHz | * | 2.5 | | | | | | | * | | | | |
| MA 5452 | * | * | 24 | * | * | * | * | * | 2.5 | | 12 | | * | 24 | | * | * | | | |
| MA 5453 | * | * | 24 | * | * | * | * | * | 2.5 | | 12 | * | * | 24 | | * | * | | | |
| MA 547 | * | * | 24 | * | * | * | * | * | 2.5 | | 12 | * | * | 24 | | * | * | | | * |

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# 512 x 9 FIFO (Signal Slice™)

# MA7001

## FEATURES

- First-In, First-Out dual port memory
- Memory organization of 512 x 9 bits
- Asynchronous and simultaneous read and write
- Expandable by word depth and/or bit width
- Empty and full warning flags
- Data retransmit capability
- Pin compatible with MK4501 and IDT7201
- 28 pin LCC or DIL
- Fully static low power CMOS/SOS

## APPLICATIONS

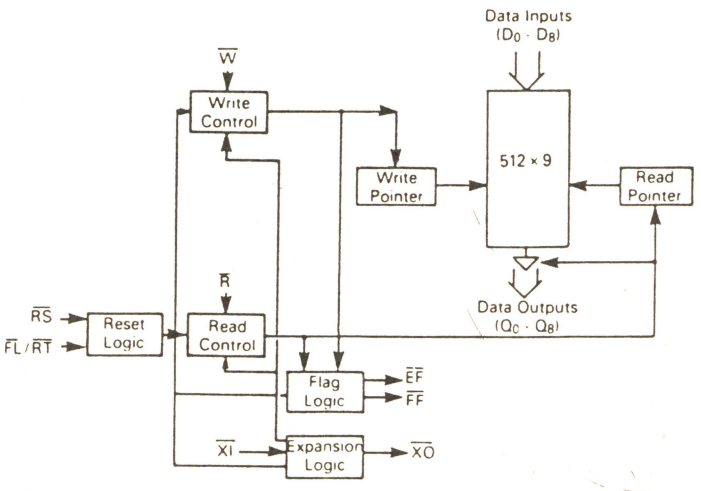
- Master/slave multiprocessing
- Rate buffer, e.g. printer, disk, video buffers
- Bidirectional buffers
- Packet switching

## DESCRIPTION

This device implements a First-In First-Out algorithm that reads and writes data on a first-in first-out basis. The dual-ort static RAM memory is organized as 512 words of 9 bits (8 bit data and 1 bit for parity or control purposes). Sequential read and write accesses are achieved using a ring pointer architecture that requires no external addressing information. Data is toggled in and out of the device by using the WRITE (W) and READ (R) pins. The device has an access time of 65nS and a read/write cycle time of 80nS (commercial).

Full and Empty status flags prevent data overflow and underflow. Expansion logic on the device allows for unlimited expansion capability in both word size and depth. A RETRANSMIT (RT) feature allows for reset of the read pointer to its initial position to allow retransmission of data.

The device is designed for applications requiring asynchronous and simultaneous read/write in multi-processing and rate buffering (sourcing and sinking data at different rates e.g. interfacing fast processors and slow peripherals).

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# SILICON-ON-SAPPHIRE RADIATION HARD STANDARD CELL ARRAYS AND GATE ARRAYS

# MACROSOS 1 DESIGN SYSTEM

## FEATURES — ALL DEVICES

- Military, Industrial and Commercial operating temperature
- Comprehensive CAD design system
- Major workstations supported (Mentor and Daisy included)
- Silicon on sapphire oxide isolated CMOS technology
- Radiation hard
- Latch-up free

## FEATURES — MACROSOS 1

* MEDL double layer metallisation, Silicon-on-Sapphire CMOS technology
* 2.5 micron gate lengths
* Typical gate delays 1.2nS — toggle rates of 70 MHz and greater achievable
* Radiation hard
* Latch-up free
* 3μW/MHz power dissipation per active gate
* Extensive CAD design and support system
* Comprehensive library of logic cells and logic function building macros
* Configurable RAM and ROM macro blocks

## FEATURES — 3μm CELLSOS

- 3 micron design rules
- Typical NAND 2-load delay: 2ns
- Typical D-Type toggle speed: 65 MHz
- 2μW/MHz/gate power dissipation
- Maximum gate count: 5000
- 3-8 v operating voltage

- Typical Radiation Hardness

| | |
|---|---|
| >100K Rads | — Total Dose |
| $>10^{10}$ Rad(Si)/sec | — Transient |
| $<10^{-9}$ error/bit/day | — SEU |
| $>10^{14}$ n/cm$^2$ | — Neutron |

## FEATURES — MA9000

- 3 micron gate length
- Typical NAND 2-load delay: 1.7ns
- Typical D-Type toggle speed: 50 MHz
- Compatible with MA2000A Library
- 3-7 v operating voltage

| ARRAY TYPE | GATES | I/O | PWR |
|---|---|---|---|
| MA9024 | 2484 | 80 | 4 |
| MA9040 | 4048 | 98 | 4 |

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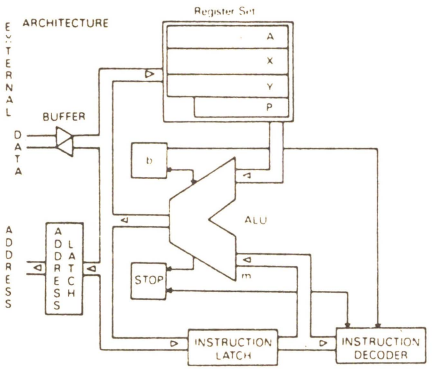
# Viper
# 32 Bit Microprocessor

Provisional Data

**FEATURES**

- Specifically designed for safety-critical applications
- 32 BIT Data
- 20 BIT Addressing
- >0.5 Million operations per second
- Halt on error
- Software support




**Introduction**

The Microprocessor is specifically designed for high integrity control systems. The hardware and software have been integrated to maintain system integrity.

The Microprocessor has applications in safety-critical systems. Safety-critical systems being those systems where loss of life, damage to the environment and loss of security are prime considerations of the total system specification. Typical applications are in the fields of aircraft and medical electronics, industrial process control, signaling, robotics and power station control. Problems can occur when using existing microprocessors due to their complex design, ambiguous documentation and implementation errors.

This microprocessor provides basic computing functions using a simple architecture. Features which unnecessarily complicate the hardware, or system testing, or add alternative programming facilities are not included. For example no provision is made for a hardware stack or interrupt requests. This microporcessor uses a simple instruction set.

The 20 BIT addressing used with the MEM I/O signal provides 1M of memory and I/O space. Data is 32 BITS to provide range and accuracy. Floating point arithmetic is excluded from the hardware, because it is inherently inexact and therefore resistant to verification.

The resulting architecture, linked with the reduced instruction set, has the following unique advantages. The Microprocessor specification and the hardware implementation has been verified by mathematical correctness techniques. The mathematics are used to describe the higher levels of design, and then prove correspondence between levels. The final product is known as VIPER® (Verifiable Integrated Processor for Enhanced Reliability).

Furthermore the hardware has built-in checks. An illegal operation, an illegal output from the ALU, or an invalid address halts the Microprocessor. The Microprocessor is also halted if the timeout on the peripherals is set. An output signal indicates the stopped state so that external remedial action can be taken.

The advantages gained from the hardware are maintained by the software. An assembler, VISTA, (VIPER Structured Assembler), has been developed for the VAX. It provides for a correspondence between the software instruction and its hardware execution. For safety-critical computing static code analysis should be applied. These special programs provide an analysis of the control flow, data use, information flow and semantics of real-time software. MALPAS is such an analyzer which can be used with VISTA programs. It exposes errors in programs, but does not by itself produce correct programs.

The VIPER design set out specifically to integrate hardware and software to enable safe and secure systems to be developed.

Systems should have N lanes ($2 < N <= 4$). End lane will use 1 VIPER. Comparisons are made between the channels, and any differences between the channels can be used to trigger special actions.

The simple architecture has the added advantage that staff can quickly learn to use VIPER/VISTA.

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# Digital Signal Processing

## The DSP56000/56001 Digital Signal Processor Sets The Pace

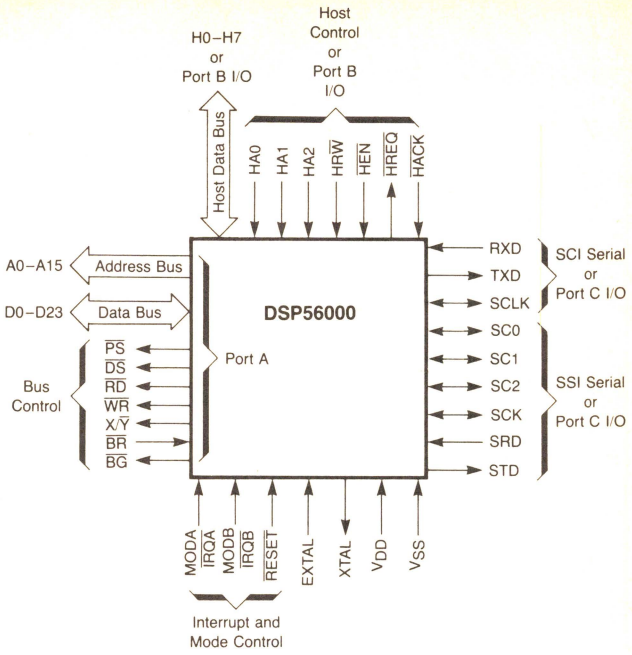
**DSP56000 BENCHMARKS**

| Benchmark | Execution Time |
|---|---|
| Finite-Impulse Response Filter with Data Shift | 0.1 $\mu$s per Tap |
| Infinite-Impulse Response Biquadratic Filter | 0.4 $\mu$s |
| 64-Point Complex Fast Fourier Transform | 0.147 ms |
| 256-Point Complex Fast Fourier Transform | 0.713 ms |
| 1024-Point Complex Fast Fourier Transform | 5 ms |

With a run rate of 10.25 million instructions per second, coupled with significant advances in chip architecture, the HCMOS DSP56000 now offers unmatched performance in digital signal processing. The new chip architecture combines 24 x 24-bit multiplication and 56-bit accumulation with two parallel data moves in a single 97.5 ns instruction cycle. Four data buses and three address buses make this throughput-enhancing parallelism possible. In fact, many of the critical DSP benchmarks (see table above) run at their theoretical maximum on the DSP56000.

The core of the DSP56000 consists of three single cycle execution units — the Data ALU, the Address Arithmetic Unit, and the Program Controller — which operate in parallel at speeds up to 10 MHz. X data, Y data and Program data memories are provided on chip and each is expandable off chip so that a total of 192K of 24-bit data can be addressed. The I/O is flexible, with two serial ports and a parallel Host port being implemented on the chip.

An MPU-like instruction set, together with a user-friendly cross assembler and simulator which run on an IBM personal computer, VAX and Sun work station, simplify algorithm development and programming. The DSP56000CLASA software package permits immediate implementation of system design, including code generation and debugging, even prior to hardware availability.




### Core Features

- 10.25 Million Instructions Per Second (MIPS)
- Single Cycle Data ALU
  - — 24 x 24 → 56-Bit Parallel Multiply/Accumulate
  - — Two 56-Bit Accumulators
  - — Ten Data Registers
  - — Two Data Bus Shifter/Limiters
- DSP Oriented Address ALU
  - — 24 Address Registers
  - — Dual Modulo Arithmetic Units
  - — Linear, Modulo, and Bit Reversed Address Generation
- Advanced Program Controller
  - — 15 Level Hardware Stack
  - — Nested Hardware DO Loops
  - — No Overhead Auto-Return Fast Interrupts
- Highly Orthogonal Instruction Set
  - — 62 MPU-Style Instruction Types
  - — Makes Pipeline Invisible
  - — Suitable for High Level Language (HLL) Compilers
- Multiple Buses
  - — Four Data Buses
  - — Three Address Buses

### On-Chip MCU-Style Peripherals

- 24 Programmable I/O Port Pins or a Combination of I/O Port Pins and
  - — 8-Bit Parallel Host MPU/DMA Interface
  - — Serial Communication Interface with Baud Rate Generator/Timer
  - — Synchronous Serial (Codec) Interface with Clock Generator

### On-Chip Memory

- Two Independent 256 x 24-Bit Data RAMs
- Two Independent 256 x 24-Bit Data ROMs
- 2K x 24-Bit Program ROM

### Off-Chip Memory Expansion

- 128K x 24-Bit Data Memory
- 64K x 24-Bit Program Memory
- Programmable Off-Chip Access Times (Wait States)

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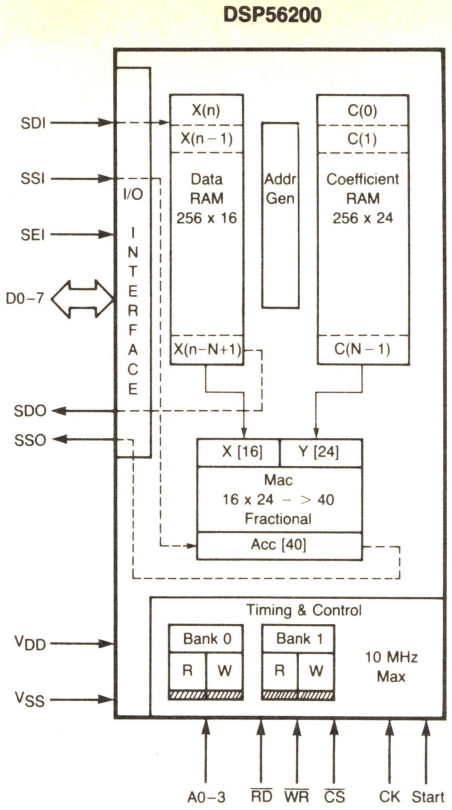
# The CAFIR Filter, DSP56200

## an Algorithm Specific DSP Peripheral

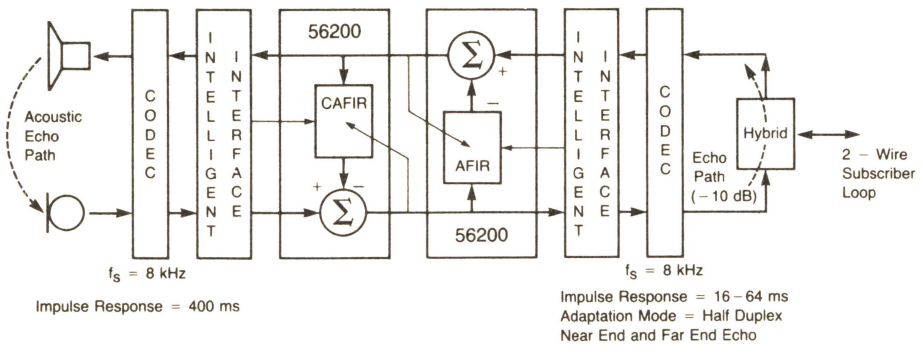
**Features**

- Low Power HCMOS
- 28 pins
- 100 ns per Tap Throughput
- 256 x 16-Bit Data RAM
- 256 x 24-Bit Coefficient RAM
- 16 x 24-Bit Multiplier, 40-Bit Accumulation
- Two FIR Modes:
  - — Single Channel
  - — Dual Channel
- Single Channel Adaptive FIR Mode
  - — Uses the Least-Mean-Squared (LMS) Coefficient Update Algorithm
- Programmable Tap Lengths Up to:
  - — 256 Taps in Single Channel Mode
  - — 128 Taps per Channel in Dual Mode
- Cascadable in Single Channel Mode
  - — Higher Sampling Frequencies
  - — Sharper Filters
  - — Longer Echoes Cancelled
- Programmable Leakage
  - — Adapting to Narrow Band Signals
- Programmable Gain
  - — Changing the Rate of Adaptation
- 8-Bit I/O Port with 7 Control Lines
- DC Tap Option
- Scratch Pad Memory
  - — Unused Data and Coefficient Memory is Available
- Power Down Mode




Accompanying the introduction of the DSP56000 will be an algorithm specific DSP peripheral chip — the DSP56200 Cascadable Adaptive Finite Impulse Response (CAFIR) Digital Filter. Capable of implementing two algorithms — the convolution sum and the least-mean-square (LMS) algorithm for updating coefficients — the CAFIR Filter is useful as a general-purpose linear phase filter and in applications requiring an adaptive filter, such as echo cancelling. An echo canceller application is illustrated below.

**Full Duplex Hands-Free Telephone**

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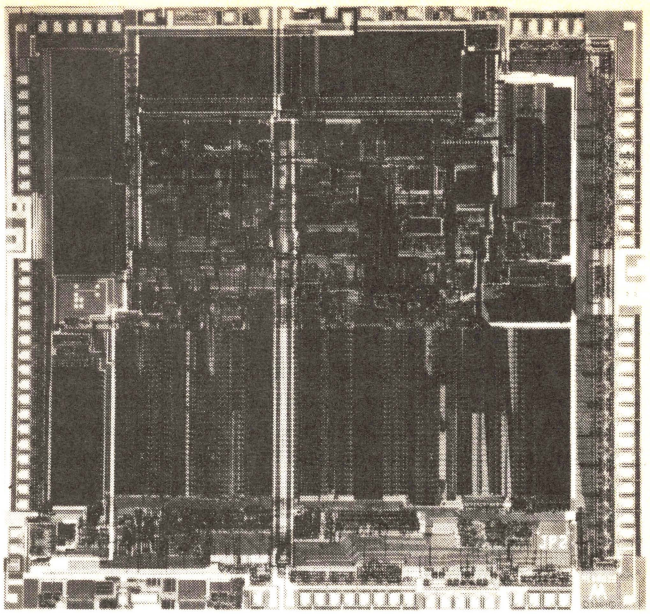
# The M68000 Family

## . . . the upward compatible 8/16/32-Bit Microprocessor Family



**MC68030 — The Second-Generation 32-Bit MPU**

## An MPU For All Functions

To designers of the most advanced microcomputer systems, the Motorola M68000 Family of microprocessors needs no introduction. Products based on its members have become the standard for systems utilizing the UNIX operating system and for CAD/CAM engineering workstations. They are invading the next generation designs of personal computers and color graphics systems, and they find widespread implementation in multi-user/multi-tasking applications and in small business systems. M68000 MPUs are found in the leading products in fault-tolerant systems requiring high performance and parallel processing, and they are the preferred components for artificial intelligence engines requiring large linear addressing capabilities. Control applications include graphics, numerical controllers, robotics, telecommunications, switching and PBX voice/data transmission.

## Upward Compatibility

The M68000 MPU Family consists of a line of processors based on a 32-bit flexible register set, a large linear address space, a simple yet powerful instruction set and flexible addressing modes. The internal architecture of the 8-, 16-, and 32-bit MPU versions, and the common instruction set, provide software compatibility and offer an easy upward migration path for products requiring increasing levels of processing power.

## A Host of Peripherals

A large selection of full-function peripheral chips complements the processor family. Compatible LSI and VLSI chips for memory management, data communications, DMA control, network control, system interfacing, general I/O and graphics, all simplify system design and reduce design and manufacturing cost while improving system performance. Then there is a comprehensive assortment of board-level products for modular integration, making Motorola the leading manufacturer of VMEmodules and VMEsystems based on the industry-standard VMEbus.

## MC68030RC
## The Second Generation 32-Bit MPU

The MC68030, oh thirty, sets the highest performance standards ever for 32-bit general-purpose microprocessors by providing up to twice the performance of the industry leading MC68020, oh twenty. The 030 takes 32-bit computing to the next logical step, while maintaining 100% upward software code compatibility with the entire M68000 product family.

The 030 started with a high performance 020 core and added many performance improvement features including increased internal parallelism, dual on-chip caches with a burst fillable mode, dual internal data and address buses, improved bus interface, and on-chip paged memory management unit.

Two independent 32-bit address buses and two 32-bit data buses allow the CPU, caches, MMU, and the bus controller to operate in parallel, so the 030 can, for example, simultaneously access an instruction from the instruction cache, data from the data cache and instruction/data from external memory. These parallel operations results in the highest performance ever.

Performance is further enhanced by on-chip instruction and data caches. Separate 256-byte data and instruction caches reduce the access time and increase CPU throughput by providing data and instructions on-chip.

Overall bus requirements are reduced and multiple processors can run more efficiently thanks to increased bandwidth of the 030 bus, achieved by the enhanced bus controller allowing high speed fills of both data and instruction caches.

The on-chip paged memory management unit translates logical addresses to the corresponding physical addresses in 1/2 the time required by the 020 and MC68851 Paged Memory Management Unit. Pipelining permits this translation to be performed in parallel with other functions so that no translation time is added to any bus cycle.

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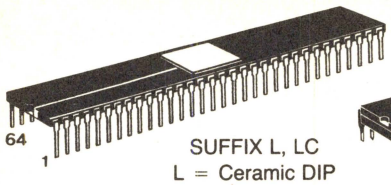
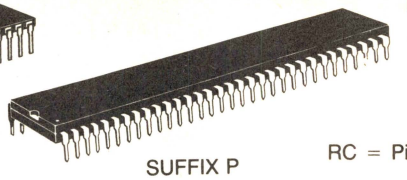
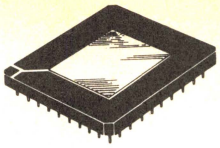
# The Compatible Processors




SUFFIX L, LC
L = Ceramic DIP
LC = Ceramic DIP, Gold Lead Finish

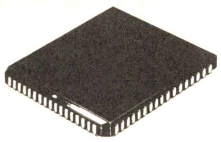


SUFFIX P
Plastic DIP



SUFFIX R, RC
R = Pin Grid Array
RC = Pin Grid Array, Gold Lead Finish

Packages shown apply to MC68000



SUFFIX FN
Plastic Leaded Chip Carrier

## MC68000L,LC,P,R,RC,FN
## The 16-Bit Foundations

As the first member of the M68000 family, the state-of-the-art technology and advance circuit design concepts of the MC68000 16-bit MPU started a new trend in microprocessor architecture. Its seventeen 32-bit data and address registers permit rapid internal execution of its powerful yet simple instruction set. It is designed for large multiprocessing systems and realtime applications with vectored interrupts, seven priority levels and a 16 megabyte linear addressing space. It offers mainframe-like performance, supporting high-level languages and sophisticated operating systems.

The MC68000 MPU has been joined by more advanced products with even greater capabilities, yet it satisfies a large segment of the existing applications. Its yield-optimized manufacturing process makes it extremely cost competitive and it remains one of the major growth products in the entire MPU line.

## MC68HC000L,LC,P,R,RC,FN
## A Micropower Alternative

HCMOS design gives the MC68HC000 all the functions and performance of its MC68000 predecessors . . . at one-tenth of the operating power requirements. With a maximum power dissipation of only 0.175 watts, the MC68HC000 is ideal for high-performance computer peripherals, industrial controllers, instrumentation and communications equipment.

## MC68010L,LC,P,R,RC,FN
## A Virtual Memory Enhancement

The internal architecture, instruction set and bus structures are identical to the MC68000, but it offers the advantage of Virtual Memory. A high-speed loop mode operation executes tight software loops faster to enhance performance. Its instruction continuation feature has made it the choice for fault-tolerant and parallel processing systems. The MC68010 can support a governing operating system which handles the supervisory chores of any number of subordinate operating systems.

## MC68008LC,P,FN
## An 8-Bit Compatible Competitor

With an 8-bit data bus and 32-bit internal architecture, the MC68008 offers performance that competes with a number of 16-bit MPUs. It has the same register set, same instructions, and the same functionality as the MC68000 with extensive exception processing. Large modular programs can be developed and executed efficiently because of the large, 1-megabit non-segmented, linear address space. It is the choice for high performance, cost effective, 8-bit designs, particularly those requiring a migration path to 16-bit or full 32-bit operation.

## MC68020RC
## The Original 32-Bit Performance Standard

The MC68020, oh twenty, is the industry's leading 32-bit microprocessor because of high performance, architecture, ease of design-in, and long-range compatible growth path.

The 020 has a full 32-bit internal and 32-bit external, regular, symmetrical architecture designed with the customer in mind. It offers all the functionality of the other M68000 Family MPUs, and maintains software user-code compatibility which controls the expense of your product migration.

Programmers appreciate the large general purpose register set, simple yet powerful instruction set and the many flexible M68000 addressing modes. The unique on-chip instruction cache helps provide burst-mode operation to 12.5 MIPS.

The 020 is the proven leader in high performance systems in office automation, engineering workstations, fault tolerant computers, parallel processors, telephone switching systems, and intelligent controllers.

## MC68881RC
## A Floating Point Coprocessor

Designed specifically for arithmetic expansion of the MC68020 MPU, this powerful coprocessor can also be used as a peripheral to all other M68000 family members, and with non-M68000 processors as well. It performs floating point math calculations in strict conformance to a full implementation of the IEEE Standard for Binary Floating Point Arithmetic (P754) and, in addition to the basic add, subtract, multiply and divide functions, it handles full selection of transcendental and non-transcendental operations. These operations include root values, trigonometric functions, exponentials, hyperbolics, and logs. All functions are calculated to 80 bits of extended precision in hardware.

## MC68882RC
## Enhanced Floating Point Coprocessor

The MC68882 is pin-to-pin hardware and software compatible with the MC68881 Floating Point Coprocessor and implements a variety of performance enhancements including dual-ported registers and an advanced pipeline. Additional circuitry allows execution of multiple instructions in parallel for more than twice the Floating Point performance of the trail-blazing MC68881. Where higher performance requirements indicate, the MC68882 is a drop-in replacement for the MC68881.

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# Memory Management & DMA Control

## MC68851RC
## Paged Memory Management Unit, PMMU

The PMMU is a 32-bit memory manager which provides full support for a demand paged virtual evnironment with the 68010 or MC68020. It supports a 4-gigabyte addressing space when used as a coprocessor with the MC68020. An on-chip address translation cache minimizes translation delays and maximizes system performance.

## MC68450L,LC,R,RC
## DMA Controller, DMAC

The DMAC maintains high-performance data movement for complex M68000 MPU-based systems. While pin compatible with the MC68440 DDMA, the DMAC offers four completely independent DMA channels. In addition to all the features of the DDMA, the DMAC also provides very sophisticated manipulation of data through sequential and linked array-chained addressing capabilities.

## MC68442R,RC,FN
## Expanded Dual DMA, EDDMA

32-bit DDMA for MC68020 based systems. The EDDMA supports up to 4 gigabytes of addressing range, and is pin compatible with the MC68440 and MC68450.

## MC68440L,LC,P,R,RC,FN
## Dual Direct Memory Access Controller, DDMA

The DDMA complements the performance capabilities of M68000 microprocessors by moving blocks of data in a quick, efficient manner with a minimum of intervention from the MPU. The DDMA performs memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers through each of two completely independent DMA channels. The DDMA also offers two interrupt vectors per channel and supports both 8-bit and 16-bit data transfers.

## MC68451L,LC,R,RC
## Memory Management Unit, MMU

The MMU is the basic element of a memory management mechanism in an M68000 based system. The MMU provides address translation and protection for the entire 16 megabyte addressing range of the M68000 microprocessor family. It provides 32 segments of variable memory size and allows for multiply MMU capabilities to expand to any number of segments. Virtual memory support is also provided for the MC68010 MPU, as is full support for the UNIX System V/68 Operating System.



# Network Devices

## MC68824RC
## Token Bus Controller, TBC

The TBC is the industry's first single-chip VLSI device to implement the IEEE 802.4 Media Access Control Sublayer of the ISO Data Link Layer, as specified by General Motors Manufacturing Automation Protocol, MAP. The TBC supports serial data rates of 1, 5, and 10 Mbps and relieves the host processor of the frame formatting and token management functions. For efficient transfer of data frames, to and from memory, the TBC features an on-chip four-channel DMA with bus master capability, a 32-bit address range, an 8- or 16-bit data bus, and a 40-byte FIFO. The MC68824 also offers support options for network bridges, real-time support and network monitoring services.

## MC68184L
## Broadband Interface Controller, BIC

The BIC, coupled with rf circuitry, makes up a broadband modem needed in each node of a MAP broadband communications network. The MC68184 implements the digital portion of IEEE802.4 broadband physical layer of the ISO/OSI (International Standards Organization/Open System Interconnect) communication model for standardized multi-vendor data communications networking. The digital portion implemented by the BIC manipulates data and provides control for the rf transmitter and receiver. The BIC supports high-speed data rates up to 10 Mbps using a duo-binary modulation technique. The IEEE802.4 recommended standard serial interface is used to connect the BIC to the Token Bus Controller (TBC), MC68824, for implementing both layers one and two of the OSI communication model.



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# Data Communications

## MC68652P
## Multi-Protocol Communication Controller, MPCC

The MPCC is a single-channel, serial data communications device that recognizes byte control and bit oriented protocols. Also included within the device is CRC (programmable error detection) circuitry. The MPCC handles data transfers of 8- or 16-bit widths at a maximum 2-Mbit/second rate.

## MC68681, MC2681L,P
## Dual Universal Asynchronous Receiver/ Transmitter, DUART

The MC68681 features two completely independent full-duplex asynchronous receiver/transmitter channels that interface directly to the MC68000 microprocessor bus. Receiver data registers are quadruple buffered and transmitter data registers are double buffered for minimum MPU intervention. Each has its own independently selectable baud rate. Multifunction 6-bit input port and 8-bit output port, a 16-bit programmable counter/timer, interrupt handling capabilities, and a maximum one-megabyte per second transfer rate make the DUART an extremely powerful device for complex data communication applications. Full device functionality with an M68000 bus interface is provided by the MC2681.

## MC68605RC
## X.25 Protocol Controller, XPC

The XPC implements the 1984 CCITT X.25 Recommendation Data Link Procedure (level 2) LAPB. In addition to handling the lower level communications functions (HDLC framing, CRC generation/checking, and zero insertion/deletion), the XPC also independently handles higher level communications functions (frame sequencing, retransmission, flow control, retries limit and timeout conditions). This allows the host to operate almost totally isolated from the task of ensuring error-free transmission and reception of data.

## MC68606RC,FN
## Multi-Link LAPD Controller CCITT Q.920/ Q.921, LAPD

The MC68606 Multi-link LAPD (MLAPD) Protocol Controller fully implements CCITT Recommendation Q.920/ Q.921 Link Layer Access Procedure (LAPD) protocol for ISDN networks. The MLAPD is designed to handle both signalling and data links in high-performance ISDN primary rate applications.

This VLSI device provides a cost-effective solution to ISDN link-level processing with simultaneous support for up to 8K logical links. The MC68606 is an intelligent communications protocol controller compatible with AT&T specifications for ISDN devices and features low power consumption and high performance, with an aggregate data rate in excess of 2.048 Mbps.

## MC68661P
## Enhanced Peripheral Communication Interface, EPCI

The EPCI is a universal synchronous/asynchronous data communications controller that interfaces to the M68000 Family and most other 8- or 16-bit microprocessors. Its receiver and transmitter are double buffered for efficient full- and half-duplex operation. An internal baud rate clock (with various baud rate sets available) eliminates the need for a system clock. The EPCI converts parallel data characters accepted from the microprocessor data bus into transmit-serial data. Simultaneously, the EPCI can convert receive-serial data to parallel data characters for input to the MPU.

# General Purpose I/O

## MC68230LC,P
## Parallel Interface/Timer, PI/T

The PI/T provides versatile double-buffered parallel interfaces and a system-oriented timer for M68000 systems. The parallel interfaces operate either in a unidirectional or bidirectional mode, either 8- or 16-bit wide. The timer is 24 bits with full programmability and a 5-bit prescaler. The PI/T has a complete M68000 bus interface and is fully compatible with the MC68450 DMAC.

## MC68901LC,P
## Multifunction Peripheral, MFP

The MFP provides basic microcomputer function requirements as a single companion chip to the M68000 Family of Microprocessors. Features provided via a direct M68000 system bus interface include a full-function, single-channel universal serial asynchronous receiver/transmitter (USART) for data communication, an 8-source interrupt controller, eight parallel I/O lines, and four 8-bit timers.

# System Interface

## MC68153L,P
## Bus Interrupt Module, BIM

The BIM interfaces an M68000 microcomputer system bus to multiple slave devices which require interrupt capabilities. It allows up to four independent sources of interrupt requests to be routed to any of the seven M68000 interrupt levels. The BIM is VMEbus and VERSAbus compatible and fully programmable.

## MC68452L,P
## Bus Arbitration Module, BAM

The BAM arbitrates the control of an M68000 system bus when multiple bus masters are involved. These bus maters can be processors, DMA controllers, and serial or parallel data communication controllers. Up to eight masters can be handled by each BAM device.

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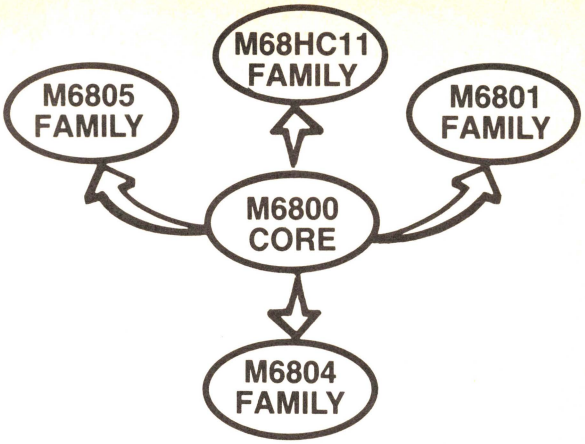
# The M6800 Families

## 8-Bit, Single-Chip Microcomputers (MCUs)




Take any basic microprocessor (MPU), add an on-chip clock, an oscillator and a timer; put in enough Read-Only Memory (ROM) to handle the program routines for dedicated applications, and enough Random Access Memory (RAM) to handle the associated data manipulations; cap it off with sufficient I/O capability to interface with a number of parallel and serial oriented peripherals . . . and you have a single-chip microcomputer (MCU).

Motorola's MCUs are grouped into four separate families, based on performance and features:

- The M68HC11 Family — the highest performance MCU family on the market, with bus speeds up to 2.1 MHz and powerful on-chip peripheral subsystems;
- The M6801 Family — with high performance and bus speeds; contains the industry-standard CPU.
- The M6805 Family — the most flexible, with more than 30 members to best serve application-specific designs;
- The M6804 Family — the most economical, designed for high-volume, low-cost applications.

**M68HC11 Family —** This high-performance HCMOS family expands the performance of the M6801 CPU by adding 91 new instructions, including 16-bit registers and mathematical operations.

Four modes of operation provide the means to test the MCU, develop code externally, and to run in single-chip mode. A new X-index register increases data handling performance in conjunction with the 2.1 MHz bus rate. High parallel I/O pin count is complemented by the inclusion of powerful on-chip peripheral subsystems. Memory features of the various family members include generous amounts of ROM, RAM and EEPROM for designs utilizing the latest in technology.

**M6801 Family —** This versatile MCU family can operate in a variety of modes, including the single-chip mode and several expanded modes. In the single-chip mode, the processors operate as monolithic microcomputers with external address or data buses. In the expanded mode the address and data bus become external signals to the appropriate bus system.

The M6801 Family, which is available in HMOS technology, includes EPROM memory versions as well as ROM-less designs.

**M6805 Family —** The flexible and rapidly expanding M6805 Family includes a number of package sizes, adapting it for various I/O functions and memory contents. EPROM, EEPROM and ROM-less versions are available among the over 30 members of this Family which are made in HMOS, CMOS and HCMOS technologies.

**M6804 Family —** The low-cost M6804 Family utilizes the proven capabilities of the M6800 instruction set, accrediting it for use in a wide variety of applications. It is processed in both HMOS and HCMOS technologies and includes EPROM versions.

### The Role of ROM-less MCUs

While MCUs are normally equipped with enough memory and the right kind of I/O to handle a designated job, it is sometimes desirable to add off-chip memory for specific applications. The ROM-less versions of the M68HC11, M6801 and M6805 Families are adaptable for these requirements.

The M6801 Family includes several bus-structure modes for off-chip expansion. These bus modes permit the number of bus pins to be optimized for the amount of address space needed off-chip. The M6805 Family offers two versions which are capable of accessing 8K bytes and 64K bytes of external address space, respectively.

### CMOS and HMOS Peripheral Support

The following tables list the current selection of individual MCUs within each product family, together with their distinctive characteristics. To support these, Motorola provides the functional and growing list of HMOS and CMOS peripheral chips.

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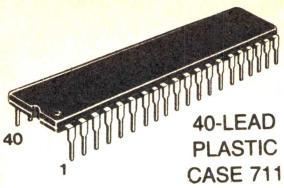
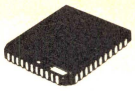


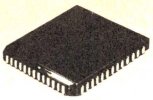

40-LEAD
PLASTIC
CASE 711

40-LEAD
CERAMIC
CASE 734



44-LEAD
PLCC
CASE 777A

48-LEAD
PLASTIC
CASE 767



52-LEAD
PLCC
CASE 778

## The M68HC11 Family

| | HCMOS | | | | | |
|---|---|---|---|---|---|---|
| | MC68HC | | | | | |
| | 11A8 | 811A2 | 811A0 | 11A1 | 811D3 | 11E9 |
| RAM (Bytes) — All saved during standby | 256 | 256 | 256 | 256 | 192 | 512 |
| ROM (Bytes) | 8192 | — | — | — | 4096 | 12288 |
| EEPROM (Bytes) | 512 | 2048 | — | 512 | — | 512 |
| Timer | 16-Bit | 16-Bit | 16-Bit | 16-Bit | 16-Bit | 16-Bit |
| Input Capture Functions | 3 | 3 | 3 | 3 | 3/3 | 4 |
| Output Compare Functions | 5 | 5 | 5 | 5 | 3/5 | 4 |
| Synchronous Serial Communications | Yes | Yes | Yes | Yes | Yes | Yes |
| Asynchronous Serial Communications | Yes | Yes | Yes | Yes | Yes | Yes |
| A/D Converter | 8-Bit | 8-Bit | 8-Bit | 8-Bit | No | 8-Bit |
| Real-Time Interrupt | Yes | Yes | Yes | Yes | Yes | Yes |
| Watchdog System | Yes | Yes | Yes | Yes | Yes | Yes |
| Parallel I/O | 38 | 38 | 38 | 38 | 30 | 38 |
| Number of Pins | 48/52* | 48/52* | 48/52* | 48/52* | 40/44* | 48/52* |

*DIP/PLCC pin count

## The M6801 Family

| | HMOS | | | |
|---|---|---|---|---|
| | MC68 | | | |
| | 01 | 03 | 01U4 | 03U4 |
| RAM (Bytes) | 128 | 128 | 192 | 192 |
| RAM (Standby) | 64 | 64 | 32 | 32 |
| ROM (Bytes) | 2048 | — | 4096 | — |
| Timer | 16-Bit | 16-Bit | 16-Bit | 16-Bit |
| Input Capture Functions | 1 | 1 | 2 | 2 |
| Output Compare Functions | 1 | 1 | 3 | 3 |
| Serial Communications | Yes | Yes | Yes | Yes |
| Real-Time Interrupt | No | No | No | No |
| Parallel I/O | 29 | 13 | 29 | 13 |
| Number of Pins | 40 | 40 | 40 | 40 |
| **EPROM Version** | **701** | — | **701U4** | — |

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## On-chip I/O

Single-chip MCUs are available in packages ranging in pin configurations from 20 pins to 52 pins. As many as 12 pins are required to serve power and control functions, leaving up to 40 pins in the largest packages to be used as I/O.

Although most digital I/O takes the form of general purpose input/output ports, several of the pins may be used in a number of designs for special serial communications interfaces.

**SCI** — The M68HC11 and M6801 Families and the HCMOS versions of the M6805 Family include a serial communications interface (SCI). The SCI is used for long-range communications, as in data transfer from an MCU to a terminal or modem. This two-line interface is also called a UART (Universal Asynchronous Receiver/Transmitter).

**SPI** — The M68HC11 Family and some members of the M6805 Family contain a serial peripheral interface (SPI). The SPI is used primarily for serial communications between chips on the same printed circuit board. A number of MCUs contain both SCI and SPI.

**Timers** — Timers are the most frequencly used on-chip functions. Timers may generate interrupts to a program at a periodic rate, measure external values, count external events and generate measured output waveforms. The M68HC11, M68HC05, and M6801 Families include a 16-bit timer that may be used to perform three of the above functions simultaneously. The M6804 and HMOS and CMOS M6805 timers consist of a programmable 8-bit counter and a selectable 7-bit prescaler.



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## MCUs (continued)

**Interrupts** — When an applications program must synchronize with two or more external events, interrupt hardware is usually necessary. Every Motorola MCU includes fully automatic interrupts (registers saved). The M68HC11, M6801 and M6805 Families contain programmable vectors for both external pins and internal timers.

**A/D Converters** — Members of the M68HC11 and M6805 Families include a multi-channel 8-bit A/D converter. The 6805R and S versions contain four analog input channels and the M68HC11 MCUs feature up to eight analog input channels.

**PLL** — On-Chip Phase Lock Loop circuitry is available on some versions of the M6805 Family.

**COP** — "Computer Operating Properly" reset timer acts as a "watchdog" to automatically reset the CPU if not reset by a program sequence in a given amount of time. All M68HC11 Family members contain this feature.

## The M6805 Family

### HMOS Versions

| | MC6805 (ROM Version) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **P2** | **P6** | **R2** | **R3** | **S2** | **S3** | **U2** | **U3** |
| RAM (Bytes) | 64 | 64 | 64 | 112 | 94 | 96 | 64 | 112 |
| User ROM (Bytes) | 1110 | 1804 | 2048 | 3776 | 1480 | 3400 | 2048 | 3776 |
| EEPROM (Bytes) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| I/O Lines Bidirectional | 20 | 20 | 24 | 24 | 21 | 14 | 24 | 24 |
| I/O Lines Unidirectional | 0 | 0 | 8 | 8 | 7 | 7 | 8 | 8 |
| SPI | | | | | X | X | | |
| A/D | | | X | X | X | X | | |
| PLL | | | | | | | | |
| COP | | | | | X | X | | |
| Number of Pins | 28 | 28 | 40 | 40 | 28 | 28 | 40 | 40 |
| **EPROM Version** | **MC68705P3*** | | **MC68705R3*** | | **MC68705S3** | | **MC68705U3*** | |

*Versions with secure EPROM are the MC68705P5, MC68705R5 and MC68705U5.

### CMOS Versions

| | HCMOS | | | | | CMOS | | | |
|---|---|---|---|---|---|---|---|---|---|
| | MC68HC05 | | | | MC68HC805 | MC146805 | | | |
| | **C4*** | **C8** | **C2** | **C3** | **C4** | **E2** | **E3** | **F2** | **G2** |
| RAM (Bytes) | 176 | 176 | 176 | 176 | 176 | 112 | 112 | 64 | 112 |
| User ROM (Bytes) | 4160 | 7744 | 2096 | 2096 | 4160** | 0 | 0 | 1089 | 2106 |
| I/O Lines Bidirectional | 24 | 24 | 24 | 24 | 24 | 16 | 16 | 16 | 32 |
| I/O Lines Unidirectional | 8 | 8 | 8 | 8 | 8 | 4 | 4 | 0 | 4 |
| Timer (Bits) | 16 | 16 | 16 | 16 | 16 | 8 | 8 | 8 | 8 |
| Special Features | SPI SCI | SPI SCI | — | SPI SCI | SPI SCI | Bus Expander to 8K | Bus Expander to 64K | | |
| Number of Pins | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 28 | 40 |
| **EPROM Version** | *** | — | — | — | — | — | — | **MC1468705F2** | **MC1468705G2** |

*Another version, the MC68HSC05C4, provides higher performance with a 4 MHz bus speed.
**EEPROM
***Use MC68HC805C4 EEPROM version

## The M6804 Family

| | HCMOS | | | HMOS | | |
|---|---|---|---|---|---|---|
| | MC68HC04 | | | MC6804 | | |
| | **J3** | **P2** | **P3** | **J1** | **J2** | **P2** |
| RAM | 30 | 32 | 124 | 32 | 32 | 32 |
| User ROM | 1672 | 1024 | 1696 | 512 | 1008 | 1024 |
| Data ROM | 72 | 72 | 72 | 72 | 72 | 72 |
| Timer | 8-Bit | 8-Bit | 8-Bit | 8-Bit | 8-Bit | 8-Bit |
| I/O Lines | 12 | 20 | 20 | 12 | 12 | 20 |
| Number of Pins | 20 | 28 | 28 | 20 | 20 | 28 |
| **EPROM Version** | — | — | — | — | — | **MC68704P2** |



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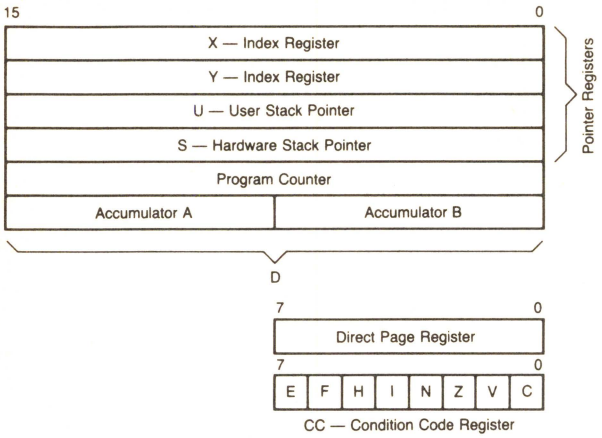
# The Viable 8-Bit MPUs




**THE M6809 FAMILY PROGRAMMING MODEL**

Large-scale integration permits combining a basic microprocessor with a variety of peripheral functions on a single chip. This has led to a series of single-chip MCUs that can represent significant cost savings in many applications. Yet, in some instances, the basic MPU has some advantages:

- Being a non-dedicated device, it can be combined with a number of peripheral chips to provide a nearly ideal circuit configuration;
- Having reached a high degree of maturity, it is cost effective and easy to implement;
- With a long history of utilization, it is supported by a wide selection of peripheral chips that maximizes system flexibility.
- Motorola provides two proven NMOS MPUs and an unexcelled list of peripherals that still bears investigation for new designs where the more elaborate MCUs don't quite fill the bill.

**The MC6809.** This MPU is the most powerful in Motorola's 8-bit line and even provides competition for some of the 16-bit machines on the market. That's because of its internal 16-bit manipulation capability which gives it 50% greater throughput than the earlier members of the M6800 Family of MPUs. It supports modern programming techniques such as position independence, reentrancy and modular programming. The **MC6809E** version has external clock inputs to allow synchronization with other MPUs and peripherals for multiprocessor operation.

**The MC6802.** This basic processor, a bit ahead of its time when first introduced, features an on-chip clock and a 128 x 8 bit RAM. Its low cost still makes it desirable for high-volume applications.

# Peripheral Support

The following list of 8-bit peripherals includes both NMOS and CMOS units that support both the MPU line and selected members of Motorola's MCU families.

## M6800-Compatible Memory

**128 x 8-Bit Static RAM** . . . . . **MCM6810**

## Memory Expansion and Control

**Dual-Port RAM Unit** — permits two MPUs to exchange data via 256 bytes of RAM. Low-power HCMOS technology. . . . . **MC68HC34**

**Direct Memory Access Controller** — bypasses MPU during data transfer between memory and peripherals. . **MC6844**

## I/O Peripherals

**Real-Time Clock Plus RAM** — CMOS for low-power battery operation; includes 50 bytes of CMOS RAM. . . **MC146818 MC146818A**

**Peripheral Interface Adapter** — two I/O ports, each controlling an independent 8-bit data bus. . . . . **MC6821**

**CMOS Parallel Interface** — 24 independently programmable I/O lines. . . . . **MC146823**

**Port Replacement Unit** — replaces ports B and C of MC68HC11 MCU when these are unavailable because of expanded or test mode operation. . . . . **MC68HC24**

**Programmable Timer** — three 16-bit binary counters. . . . . **MC6840**

**0–600 bps Digital Modem** — provides serial data communications link, over a voice grade channel at bit rates up to 600 bps. . . . . **MC6860**

**NMOS Asynchronous Communications Interface Adapter** — formats serial asynchronous data to interface with bus-organized systems. . . . . **MC6850**

**Advanced Data Link Controller** — provides serial-to-parallel and parallel-to-serial conversion of data format for data communications. . . . . **MC6854**

**Synchronous Serial Data Adapter** — interfaces between M6800 MPU system and synchronous data terminals at speeds up to 600 kbps. . . . . **MC6852**

**Hard Disk Controller** — a single-chip, VLSI device with all the resources needed to function as a hard disk controller . . . . . **MC68HC99**

**Cable Driver/Receiver** — provides single-ended, 48 mA, SCSI cable drivers and receivers in a single chip; used to interface the MC68HC99 to a small computer system interface (SCSI) bus . . . . . **MC6898**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## Graphics/Display Peripherals

**CRT Controller** — interfaces between a terminal and an M6800 MPU to simplify the development of intelligent terminals, word processing and information display devices. . . . . **MC6845**

**Video Display Generator** — interfaces the M6800 family (or similar product) to a standard color or black and white NTSC television receiver; for non-interlace systems . . . . **MC6847**

**Color TV Video Modulator** — Companion to the MC6847 provides the correct dc interconnection levels. . . . **MC1372**

## System Expansion and Enhancement

**8-Bit D-to-A Converter** — bus compatible converter capable of interfacing directly with 8-bit microprocessors. . . . . **MC6890**

**Priority Interrupt Controller** — adds prioritized responses to inputs of MPU systems. . . . . **MC6828**

**Data Security Device** — MOS circuit protects data by employment of cryptographic measures. . . . . **MC6859**

*The following devices are especially useful in SPI interface with the M68HC11 and some M6805 Family MCUs:*

### Data Converters

MC145040 — ADC; 11 inputs, SAR, external clock
MC145041 — ADC; 11 inputs, SAR, internal clock

MC144110 — DAC; six 6-bit converters
MC144111 — DAC; four 6-bit converters

MC14549B — SAR; Master Reset permits cascading
MC14559B — SAR; EOC option for $< 8$ bits

### Display Decoders/Drivers

MC14499 — 4-digit 7-segment LED driver
MC145000 — 48-segment LCD driver (master); multiplexed-by-four
MC145001 — 44-segment LCD driver (slave); multiplexed-by-four
MC145453 — LCD driver; 33 nonmultiplexed segments (for 4½-digit, 7-segment-plus-decimal display); may be paralleled for more digits.

### PLL Frequency Synthesizers

MC145155 — Single modulus; $\div$R = 14 stages, $\div$N = 14 stages
MC145156 — Dual modulus; $\div$R = 12 stages, $\div$A = 7 stages, $\div$N = 10 stages
MC145157 — Single modulus; $\div$R = 14 stages, $\div$N = 14 stages
MC145158 — Dual modulus; $\div$R = 14 stages, $\div$A = 7 stages, $\div$N = 10 stages
MC145159 — Sample and hold detector; dual modulus; $\div$R = 14 stages, $\div$A = 7 stages, $\div$N = 10 stages

### Shift Registers

MC14021B — 8-bit input port
MC74HC165 — 8-bit input port
SN74LS165 — 8-bit input port
MC74HC595 — 8-bit output port
SN74LS673 — 16-bit output port

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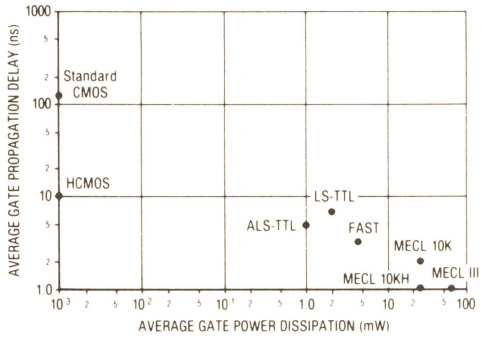
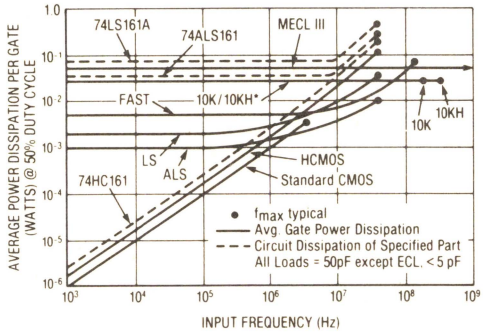
# Standard Logic Families

| | | | | | |
|---|---|---|---|---|---|
| **LSTTL:** | SN54/74LS Series | **MECL10K:** | MC10000 Series | **Standard CMOS:** | MC14000 Series |
| **FAST™:** | MC54/74F Series | **MECL10KH:** | MC10H000 Series | **High-Speed CMOS:** | MC54/74HC Series |
| | | **MECL III:** | MC1600 Series | | |




**Graph 1 — General Comparison of Speed/ Power Characteristics**




**Graph 2 — Variations in Power Dissipation as a Function of Operating Frequency**

The variety of established and newly introduced logic families challenges the system designer with choosing the best available technology for each design. Each family offers distinct advantages and limitations.

The three most often used characteristics for determining family selection are propagation delay, operating frequency, and power consumption. For Motorola logic families, these characteristics are displayed and compared in the graphs above. Graph 1 illustrates the tradeoffs between power dissipation and propagation delay at low operating frequencies. As frequency increases, the changes in power dissipation characteristics of the various families vary considerably, graph 2. These factors, plus the ever-changing impact of economics, must be considered in the selection of the most suitable logic line.

# Technical Comparisons

## Schottky TTL

Since its introduction, TTL has become the most popular form of digital logic. It has evolved from the original gold-doped saturated 7400 logic, to Schottky-Clamped logic, and finally to the modern advanced families of TTL logic. The popularity of these TTL families stems from their ease of use, low cost, medium-to-high speed operation, and good output drive capability.

Motorola offers two modern TTL logic families — LS and FAST*. They are pin and functionally compatible and can easily be combined in a system to achieve maximum performance at minimum cost.

**LS (Low Power Schottky)** is currently the more popular and commands by far the largest share of the total TTL logic market. It is low-cost and provides moderate performance at low power.

**FAST,** the state-of-the-art, high-performance TTL family, is growing rapidly and gaining a significant share of the total TTL logic market. FAST offers a 20-to-30 percent improvement in performance over the older Standard Schottky family (74S) with a 75-to-80 percent reduction in power. When compared with the Advanced Schottky family (74AS), FAST offers nearly equal performance at a 25-to-50 percent savings in power.

FAST is manufactured on Motorola's MOSAIC (oxide-isolated) process. This process provides FAST with inherent speed/power advantages over the older junction-isolated 74S and 74LS families, allowing the FAST family to be designed and specified with improved noise margins, reduced input currents, and superior line driving capabilities. Additionally, FAST designs incorporate power-down circuitry on all three-state outputs, and buffered outputs on all storage devices.

Two further advantages of FAST are the load specifications and power supply specifications. FAST ac characteristics are specified at a heavier capacitive load than the earlier families (50 pF versus 15 pF) to more accurately reflect actual in-circuit performance. And Motorola's dc and ac characteristics for FAST are specified over a full 10% supply voltage range — a significant improvement over earlier families (5% for dc, 0% for ac) and a considerable improvement over the prevalent FAST standards covering only a 5% range for both dc and ac.

* = FAST is a Fairchild Trademark

### SPEED/POWER CHARACTERISTICS FOR SCHOTTKY TTL LOGIC
**(ALL TYPICAL RATINGS)**

| Characteristic | Symbol | LS | FAST | Units |
|---|---|---|---|---|
| Quiescent Supply Current/Gate | $I_G$ | 0.4 | 1.1 | mA |
| Power/Gate (Quiescent) | $P_G$ | 2.0 | 5.5 | mW |
| Propagation Delay | $t_p$ | 9.0 | 3.7 | ns |

| Characteristic | Symbol | LS | FAST | Units |
|---|---|---|---|---|
| Speed Power Product | — | 18 | 19.2 | pJ |
| Clock Frequency (D-F/F) | $f_{max}$ | 33 | 125 | MHz |
| Clock Frequency (Counter) | $f_{max}$ | 40 | 125 | MHz |

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## MECL (ECL)

Motorola's Emitter Coupled Logic (MECL) is a nonsaturating form of digital logic which eliminates transistor storage time as a speed limiting characteristic, permitting very high speed operation.

Motorola offers three versions of MECL: MECL 10K, MECL 10KH, and MECL III.

The *MECL 10K* series has become the industry standard for high-speed applications. In order to make the circuits comparatively easy to use, edge speed was slowed to 2.0 ns while the important propagation delay was held to 2.0 ns. The slow edge speed permits use of wire-wrap and standard printed circuit lines; however, the circuits are specified to drive transmission lines for optimum performance.

The newer *MECL 10KH* family features 100% improvement in propagation delay and clock speeds while maintaining power supply current equal to MECL 10K. This new MECL family is voltage compensated which allows guaranteed dc and switching parameters over a ±5% power supply range. Noise margins of MECL 10KH are 75% better than the MECL 10K series. MECL 10KH is compatible with MECL 10K and MECL III, a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas.

*MECL III,* with its 1.0 ns gate propagation delays and greater than 1.0 GHz flip-flop toggle rates, remains the industry speed leader. The 1.0 ns rise and fall times require a transmission line environment for all but the smallest systems. For this reason, all circuit outputs are designed to drive transmission lines and all output logic levels are specified when driving 50-ohm loads. Because of MECL III's fast edge speeds, multi-layer boards are recommended above 200 MHz. MECL III's popularity is with high-speed test and communications equipment.

Speed/power comparisons for Motorola ECL families are as follows:

### SPEED/POWER CHARACTERISTICS FOR (MECL)

| (ALL TYPICAL RATINGS) | | MECL 10K | | 10KH | III | |
|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **MC101xx** | **MC102xx** | **MC10H1xx** | **MC16xx** | **Units** |
| Quiescent Supply Current/Gate | $I_G$ | 5.0 | 5.0 | 5.0 | 10 | mA |
| Power/Gate (Quiescent) | $P_G$ | 26 | 26 | 26 | 54 | mW |
| Propagation Delay | $t_p$ | 2.0 | 1.5 | 1.0 | 1.1 | ns |
| Speed Power Product | — | 52 | 39 | 26 | 59 | pJ |
| Clock Frequency (D-F/F) | $f_{max}$ | 150 | 225 | 300 | 550 | MHz |
| Clock Frequency (Counter) | $f_{max}$ | 150 | — | 300 | 1200 | MHz |

## HTL/DTL Circuits

Motorola still supplies a large selection of HTL (High-Threshold Logic) and DTL (Diode-Transistor Logic) circuits. These are recommended primarily for replacement purposes. A list of available type numbers is given below. For complete descriptions and specifications, please contact your Motorola sales office or distributor.

**MHTL Type Numbers**

MC660 MC679
MC661 MC680
MC662 MC681
MC663 MC682
MC664 MC683
MC665 MC684
MC666 MC685
MC667 MC686
MC668 MC688
MC669 MC689
MC670 MC690
MC671 MC691
MC672 MC693
MC673 MC696
MC674 MC697
MC675 MC699
MC677
MC678

**MDTL Type Numbers**

MC830 MC850 MC936 MC956
MC832 MC851 MC937 MC957
MC833 MC852 MC938 MC958
MC834 MC853 MC939 MC961
MC835 MC855 MC940 MC962
MC836 MC856 MC941 MC963
MC837 MC857 MC944
MC838 MC858 MC945
MC839 MC861 MC946
MC840 MC862 MC948
MC841 MC863 MC949
MC844 MC930 MC950
MC845 MC932 MC951
MC846 MC933 MC952
MC848 MC934 MC953
MC849 MC935 MC955





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## CMOS

Complementary MOS (CMOS) technology provides the lowest power consumption logic circuits available in the industry. The term "complementary" refers to the basic circuit building unit, where a P and an N-channel insulated gate FET are cascaded. This configuration results in extremely low quiescent current, drawing power only when being switched.

Motorola offers two versions of CMOS logic circuits: *Standard (MC14000 Series) CMOS* in metal gate technology, and *High-Speed (HC) CMOS* in silicon gate technology.

Standard CMOS logic is best suited for systems which require low power, medium speed operation. It offers a wide operating voltage range (3 to 18 V) and the highest noise immunity of any logic family. Standard CMOS circuits are classified as B or UB series devices, in accordance with JEDEC Standard 13-B. UB series gates and inverters are constructed with a single inverting stage between input and output, as opposed to multiple gain stages in the B series. The subsequent decreased gain in the UB series results in less noise immunity; however, these UB devices are useful when CMOS gates and inverters are used in a "Linear" mode to form oscillators, monostables, or amplifiers. These devices also exhibit higher speed since only a single stage is involved.

A full line of High Speed CMOS devices (54/74 HC) was developed to be both pinout and functionally equivalent to the most popular LSTTL parts. The HC family also contains devices that are pinout and functionally equivalent to some of the more popular MC14000B series CMOS parts.

The silicon-gate processing technology allows the HC family to combine the fast switching speeds of LSTTL with the low power-consumption advantages of CMOS. These devices also feature the high noise immunity that is characteristic of CMOS, and offer a wide power supply operating voltage range (2 to 6 V).

High-Speed CMOS logic circuits can directly interface with LSTTL/NMOS inputs; with pullup resistors HC devices can be driven by LSTTL/NMOS outputs. An alternative method is to use an HCT interface device which accepts LSTTL input levels without the aid of pullup resistors.

Speed/power comparisons between the two CMOS families are as follows:

### SPEED/POWER CHARACTERISTICS FOR CMOS LOGIC

**(ALL TYPICAL RATINGS)**

| Characteristic | Symbol | Standard CMOS (15 V) | Hi-Speed CMOS (6 V) | Units |
|---|---|---|---|---|
| Quiescent Supply Current/Gate | $I_G$ | .0001 | .0003 | mA |
| Power/Gate (Quiescent) | $P_G$ | .0006 | .001 | mW |
| Propagation Delay | $t_p$ | 50 | 8.0 | ns |
| Speed Power Product | — | .030 | .01 | pJ |
| Clock Frequency (D-F/F) | $f_{max}$ | 14 | 40 | MHz |
| Clock Frequency (Counter) | $f_{max}$ | 8.0 | 40 | MHz |





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# Available Functions

## Functionally Comparable Logic Integrated Circuits

The following table offers a quick guide to logic circuits in the various families available from Motorola. Devices within a single (horizontal) row perform similar functions. Pinout configuration are generally identical when the numbers in a row correspond, although there may be exceptions. Consult the appropriate data book for specific details.

The numbers in the (vertical) columns are suffixes that follow the basic line prefixes associated with each specific logic family. These prefixes are as follows:

| TTL | | CMOS | | MECL | | |
|---|---|---|---|---|---|---|
| LS | FAST | STD | HC | 10K | 10KH | III |
| PREFIXES | | | | | | |
| SN54/74LS | MC54/74F | MC14 | MC54/74HC | MC10 | MC10H | MC |

Thus, the TTL LS Quad 2-input gate (item 1 in the table) can be ordered under the part number SN54LS08 (or SN74LS08). Similarly, the MECL 10KH Quad 2-input gate can be ordered as MC10H104.

| Function | TTL | | CMOS | | | MECL | | | |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | Package* | 10K | 10KH | III | Package* |
| **AND Gates** | | | | | | | | | |
| Quad 2-Input | 08 | 08 | 081 | 08 | 632 | 104 | 104 | | 620 |
| Quad 2-Input, Open-Collector | 09 | | | | 646 | | | | 648 |
| Triple 3-Input | 11 | 11 | 073 | 11 | | | | | |
| Triple 3-Input, Open-Collector | 15 | | | | | | | | |
| Dual 4-Input | 21 | 21 | 082 | | | | | | |
| Hex | | | | | | 197 | | | |
| **NAND Gates** | | | | | | | | | |
| Quad 2-Input | 00 | 00 | 011 | 00 | 632 | | | | |
| Quad 2-Input, Open-Collector | 01 | | | | 648 | | | | |
| Quad 2-Input, Open-Collector | 03 | | | 03 | | | | | |
| Quad 2-Input, High-Voltage | 26 | | | | | | | | |
| Quad 2-Input Buffer | 37 | | | | | | | | |
| Quad 2-Input Buffer, Open-Collector | 38 | | | | | | | | |
| 13-Input | 133 | | | 133 | 620,648 | | | | |
| Triple 3-Input | 10 | 10 | 023 | 10 | 632 | | | | |
| Triple 3-Input, Open-Collector | 12 | | | | 648 | | | | |
| Dual 4-Input | 20 | 20 | 012 | 20 | | | | | |
| Dual 4-Input, Open-Collector | 22 | | | | | | | | |
| Dual 4-Input Buffer | 40 | | | | | | | | |
| 8-Input | 30 | | 068 | 30 | | | | | |
| Quad 2-Input NAND with Schmitt Trigger Inputs | 132 | | 093 | 132 | | | | | |
| **OR Gates** | | | | | | | | | |
| Quad 2-Input | 32 | 32 | 071 | 32 | 632 | 103 | 103 | 1664 | 620 |
| Dual 3-Input 3-Output | | | | | 646 | 110 | | | 648 |
| High-Speed Dual 3-Input 3-Output | | | | | | 210 | 210 | | |
| Triple 3-Input | | | 075 | 4075 | | | | | |
| Dual 4-Input | | | 072 | | | | | | |

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.





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## FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

| Function | TTL | | CMOS | | | MECL | | | |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | Package* | 10K | 10KH | III | Package* |
| **NOR Gates** | | | | | | | | | |
| Quad 2-Input | 02 | 02 | 001 | 02(36) | 632 | 102 | 102 | 1662 | 620 |
| Quad 2-Input Buffer | 28 | | | | 646 | | | | 648 |
| Quad 2-Input Buffer, Open-Collector | 33 | | | | | | | | |
| Dual 5-Input | 260 | | | | | | | | |
| Triple 3-Input | 27 | | 025 | 27 | | | | | |
| Quad 2-Input with Strobe | | | | | | 100 | 100 | | |
| Triple 4-3-3 Input | | | | | | 106 | 106 | | |
| Dual 3-Input 3-Output | | | | | | 111 | | | |
| High-Speed Dual 3-Input 3-Output | | | | | | 211 | 211 | | |
| Dual 3-Input, plus Inverter | | | 000 | | | | | | |
| Dual 4-Input | | | 002 | 4002 | | | | | |
| 8-Input | | | 078 | 4078 | | | | | |
| **Exclusive OR Gates** | | | | | | | | | |
| Quad 2-Input | 86 | 86 | 070 | 86 | 632 | 113 | 113 | | 620 |
| Quad 2-Input | 386 | | | | 646 | | | | 648 |
| Quad, Open-Collector | 136 | | | | | | | | |
| Triple 2-Input | | | | | | | | 1672 | 620 |
| **Exclusive NOR Gates** | | | | | | | | | |
| Quad, 2-Input Open Drain Output | 266 | | 077 | 266 | 632 | | | | |
| Triple 2-Input | | | | | 646 | | | 1674 | 620 |
| Quad, 2-Input | | | | 7266 | | | | | |
| **Complex Gates** | | | | | | | | | |
| Quad OR/NOR | | | | | 632 | 101 | 101 | | 620 |
| Triple 2-3-2 Input OR/NOR | | | | | 646 | 105 | 105 | 1688 | 648 |
| Triple 2-Input Exclusive OR/Exclusive NOR | | | | | | 107 | 107 | | |
| Dual 4-5 Input OR/NOR | | | | | | 109 | 109 | | |
| Dual 4-5 Input OR/NOR | | | | | | | 209 | | |
| Dual 2-Wide 2-3 Input OR-AND/OR-AND-Invert | | | | | | 117 | 117 | | |
| Dual 2-Wide 3-Input OR-AND | | | | | | 118 | 118 | | |
| 4-Wide 4-3-3-3 Input OR-AND Gate | | | | | | 119 | 119 | | |
| OR-AND/OR-AND-INVERT Gate | | | | | | 121 | 121 | | |
| High-Speed Dual 3-Input 3-Output OR/NOR | | | | | | 212 | | | |
| Dual 4-Input OR/NOR | | | | | | | | 1660 | |
| Dual AND-OR-INVERT Gate | 51 | 51 | 506 | 51 | | | | | |
| 3-2-2-3 Input AND-OR-INVERT Gate | 54 | | | | | | | | |
| 2-Wide and 4-Input AND-OR-INVERT Gate | 55 | | | | | | | | |
| 4-2-2-3 Input AND-OR-INVERT Gate | | 64 | | | | | | | |
| Triple Gate (Dual 4-Input NAND Gate and 2-Input NOR/OR Gate or 8-Input AND/NAND Gate) | | | 501 | | | | | | |
| 4-Bit AND/OR Selector (Quad 2-Channel Data Selector or Quad Exclusive NOR Gate) | | | 519 | | | | | | |
| Dual 5-Input Majority Logic Gate | | | 530 | | | | | | |
| Hex Gate (Quad Inverter plus 2-Input NOR Gate plus 2-Input NAND Gate) | | | 572 | | | | | | |
| 2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gate | | | | 58 | | | | | |

*See Surface Mount section for SO and PLCC packages.

(continued)



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| Function | TTL | | CMOS | | Package* | MECL | | | Package* |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | | 10K | 10KH | III | |
| **Inverters/Buffers (Non 3-State)** | | | | | | | | | |
| Hex Inverter | 04 | 04 | 069 | 04 | 632 | | | | 620 |
| Hex Inverter, Open-Collector | 05 | 05 | | 05 | 646 | | | | 648 |
| Dual Complementary Pair plus Inverter | | | 007 | | 620 | | | | |
| Hex Buffer | | | 050 | 4050 | 648 | | | | |
| Strobed Hex Inverter/Buffer | | | 502 | | | | | | |
| Hex Buffer with Enable | | | | | | 188 | 188 | | |
| Hex Inverter with Enable | | | | | | 189 | 189 | | |
| Hex Inverter/Buffer | | | 049 | 4049 | | 195 | | | |
| Hex Unbuffered Inverter | | | | U04 | | | | | |
| **Translators** | | | | | | | | | |
| Quad MTTL to MECL, ECL Strobe | | | | | 620 | 124 | 124 | | 620 |
| Quad TTL to MECL, TTL Strobe | | | | | 648 | | 424 | | 648 |
| Quad MECL to MTTL | | | | | | 125 | 125 | | |
| Quad MECL to TTL, Single Supply | | | | | | | 350 | | |
| Triple MECL to NMOS | | | | | | 177 | | | |
| TTL or CMOS to CMOS Hex Level Shifter | | | 504 | | | | | | |
| Quad MST-to-MECL 10,000 | | | | | | 190 | | | |
| Hex MECL 10,000 to MST | | | | | | 191 | | | |
| **Bus-Oriented 3-State Circuits** | | | | | | | | | |
| Quad Buffer, Low Enable, 3-State | 125A | | | 125 | 632 | | | | |
| Quad Buffer, High Enable, 3-State | 126A | | | 126 | 646 | | | | |
| Octal Bus/Line Driver, Inverting, 3-State | 240 | 240 | | 240 | 732 | | | | |
| Octal Bus/Line Driver, 3-State | 241 | 241 | | 241 | 738 | | | | |
| Quad Bus Transceiver, Inverting 3-State | 242 | 242 | | 242 | 632 | | | | |
| Quad Bus Transceiver, Noninverting, 3-State | 243 | 243 | | 243 | 646 | | | | |
| Octal Driver, Noninverting, 3-State | 244 | 244 | | 244 | 732 | | | | |
| Octal Bus Transceiver, Noninverting, 3-State | 245 | 245 | | 245 | 738 | | | | |
| Hex Buffer, Common Enable, 3-State | 365A | | | 365 | 620 | | | | |
| Hex Inverter, Common Enable, 3-State | 366A | | | 366 | 648 | | | | |
| Hex Buffer, 4-Bit and 2-Bit, 3-State | 367A | | 503 | 367 | | | | | |
| Hex Inverter, 4-Bit and 2-Bit, 3-State | 368A | | | 368 | | | | | |

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.





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## FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

| Function | TTL | | CMOS | | | MECL | | | |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | Package* | 10K | 10KH | III | Package* |
| **Bus-Oriented 3-State Circuits (continued)** | | | | | | | | | |
| Octal Buffer (81LS95), 3-State | 795 | | | | 732 | | | | 620 |
| Octal Buffer (81LS96), 3-State | 796 | | | | 738 | | | | |
| Octal Buffer (81LS97), 3-State | 797 | | | | | | | | |
| Octal Buffer (81LS98), 3-State | 798 | | | | | | | | |
| Octal Buffer/Line Driver, 3-State | 540 | | | 540 | | | | | |
| Octal Buffer/Line Driver, 3-State | 541 | | | 541 | | | | | |
| Octal Bus Transceiver, Inverting, 3-State | 640 | | | 640 | | | | | |
| Octal Bus Transceiver, True, Inverting, 3-State | | | | 643 | | | | | |
| Octal Bus Transceiver, Noninverting, 3-State | 645 | | | | | | | | |
| Octal Transceiver with Storage, 3-State | 623 | | | | | | | | |
| Octal Bus Transceiver, 3-State, Open-Collector | | | | | 724 | | | | |
| Octal Transceiver/Latch/Multiplexer, Noninverting, 3-State | | | | 646 | 758 | | | | |
| Octal Transceiver/Latch/Multiplexer, Inverting, 3-State | | | | 648 | | | | | |
| Dual Latching Bus Driver | | | | | | 128 | | | |
| **Bus Driver (25 ohm outputs)** | | | | | | | | | |
| Triple 4-3-3 Input | | | | | | 123 | 123 | | 620,648 |
| Quad Driver/Receiver with 2-1 Output Multiplexer | | | | | | | 330 | | 724,758 |
| Dual Driver/Receiver with 4-to-1 Output Multiplexers | | | | | | | 332 | | 732 |
| Quad Driver/Receiver with Transmit and Receiver Latches | | | | | | | 334 | | 738 |
| Triple 3-Input Driver with Enable | | | | | | | 423 | | |
| **Open-Collector Bus Transceivers** | | | | | | | | | |
| Octal Bus, Noninverting, Open-Collector | 641 | | | | 732 | | | | |
| Octal Bus, Inverting, Open-Collector | 642 | | | | 738 | | | | |
| **Schmitt Triggers** | | | | | | | | | |
| Quad 2-Input NAND | 132 | 132 | 093 | 132 | 632,646 | | | | |
| Dual | | | 583 | | 620,648 | | | | |
| Dual 4-Input | 13 | 13 | | | 632 | | | | |
| Hex | 14 | 14 | 584<br>106 | 14 | 646 | | | | |

*See Surface Mount section for SO and PLCC packages.

(continued)





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| Function | TTL | | CMOS | | | MECL | | | |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | Package* | 10K | 10KH | III | Package* |
| **Latches** | | | | | | | | | |
| 4-Bit Bi-Stable Latch with Q and Q | 75 | | 042 | 75 | 620,648 | | | | 620 |
| 4-Bit Bi-Stable Latch | 77 | | | | 632,646 | | | | 648 |
| Octal Transparent Latch, 3-State, Noninverting | 373 | 373 | | 373 | 620 | | | | |
| Quad Latch | 375 | | | | 648 | 168 | | | |
| Quad NAND R-S Latch | 279 | | 044 | | | | | | |
| 8-Bit Addressable Latch (9334) | 259 | 259 | 099 | 259 | | | | | |
| Dual 4-Bit Addressable Latch | 256 | 256 | | | | | | | |
| Octal Transparent Latch, 3-State | | | | 573 | | | | | |
| Octal Transparent Latch, 3-State, Inverting | | 533 | | 533 | | | | | |
| Dual Latch | | | | | | 130 | 130 | | 620 |
| Quad (negative transition) Latch | | | | | 620 | 133 | | | 648 |
| Quad (positive transition) Latch | | | | | 648 | 153 | | | |
| Quint Latch | | | | | | 175 | 175 | | |
| Quad NOR R-S Latch | | | 043 | | | | | | |
| Dual 4-Bit Latch | | | 508 | | 623,709 | | | | |
| 8-Bit, Bus-Compatible, 3-State Latches — Internal Counter | | | 597 | | | | | | |
| 8-Bit, Bus-Compatible, 3-State Latches — Binary Address | | | 598 | | | | | | |
| 8-Bit Addressable Latch with Bidirectional Port | | | 599 | | 707,726 | | | | |
| Octal D-Type Transparent Latch, 3-State | | | | 373 | | | | | |
| Octal D-Type Latch w/Readback, 3-State | | | | 793 | | | | | |
| **Flip-Flops/Registers** | | | | | | | | | |
| Dual JK | 73A | | 027 | 73 | 620,648 | 135 | 135 | | 620 |
| Dual D | 74A | 74 | 013 | 74 | 632,646 | 131 | 131 | | 648 |
| Dual JK | 76A | | | 76 | 620,648 | | | | |
| Dual JK with Preset | 109A | 109 | | 109 | 620,648 | | | | |
| Dual JK with Clear | 107A | | | 107 | 632,646 | | | | |
| Dual JK Edge-Triggered | 112A | | | 112 | 620,648 | | | | |
| Dual JK Edge-Triggered | 113A | | | 113 | 632,646 | | | | |

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.





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## FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

| Function | TTL | | CMOS | | Package* | MECL | | | Package* |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | | 10K | 10KH | III | |
| **Flip-Flops/Registers (continued)** | | | | | | | | | |
| Dual JK Edge-Triggered | 114A | | | | | | | | 620 |
| 4-Bit D Register, 3-State | 173 | | 076 | 173 | 620 | | | | 648 |
| Hex D with Clear | 174 | 174 | 174 | 174 | 648 | | | | |
| Hex D with Enable | 378 | 378 | | | 732,738 | | | | |
| Quad D with Clear | 175 | 175 | 175 | 175 | 620,648 | | | | |
| Octal D with Clear | 273 | | | 273 | 620 | | | | |
| Octal D, 3-State | 374 | 374 | | 374 | 648 | | | | |
| Octal D with Enable | 377 | | | | | | | | |
| 4-Bit D with Enable | 379 | 379 | | | | | | | |
| Hex D | | | | | | 176 | 176 | | |
| Hex "D" Master-Slave/with Reset | | | | | | 186 | 186 | | |
| Octal D, Inverting, 3-State | | | | 564 | 732 | | | | |
| Octal D | | | | | 738 | | | | |
| Octal D, Inverting | | | | | | | | | |
| Octal D, 3-State | | | | 574 | | | | | |
| High-Speed Dual Type D Master-Slave | | | | | | 231 | | | |
| Dual Clocked R-S | | | | | | | | 1666 | |
| Dual Clocked Latch | | | | | | | | 1668 | |
| Master-Slave Type D | | | | | | | | 1670 | |
| UHF Prescaler Type D | | | | | | | | 1690 | |
| Octal D Flip-Flop, 3-State | | 534 | | 534 | | | | | |
| **Counters** | | | | | | | | | |
| Decade | 90 | | | | 632 | | | | 620 |
| Divide-By-12 | 92 | | | | 646 | | | | 648 |
| 4-Bit Binary | 93 | | | | | 154 | | | |
| Decade, Asynchronously Presettable | 196 | | | | | | | | |
| 4-Bit Binary, Asynchronously Presettable | 197 | | | | | | | | |
| BCD Decade, Asynchronously Reset | 160A | 160A | 160 | 160 | 620 | | | | |
| 4-Bit Binary, Asynchronous Reset | 161A | 161A | 161 | 161 | 648 | 178 | 016 | 1654 | |
| BCD Decade, Synchronous Reset | 162A | 162A | 162 | 162 | | | | | |
| 4-Bit Binary, Synchronous Reset | 163A | 163A | 163 | 163 | | | | | |
| Up/Down Decade, with Clear | 192 | 192 | 510 | | | | | | |
| Up/Down Binary, with Clear | 193 | 193 | 516 | | | | | | |
| Up/Down Decade | 190 | 190 | | | | 137 | | | |
| Up/Down Binary | 191 | 191 | 029 | | | 136 | 136 | | |
| Decade (Divide By 2 and 5) | 290 | | | | 632 | 138 | | 1678 | |
| 4-Bit Binary | 293 | | | | 646 | | | | |
| Dual Decade | 390 | | 518 | 390 | 620,648 | | | | |
| Dual 4-Bit Binary | 393 | | 520 | 393 | 632,646 | | | | |
| Dual Decade | 490 | | | | 620,648 | | | | |
| Decade Up/Down, 3-State | | 568 | | | 732 | | | | |
| Binary Up/Down, 3-State | 569 | 569 | | | 738 | | | | |

*See Surface Mount section for SO and PLCC packages.

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| Function | TTL | | CMOS | | Package* | MECL | | | Package* |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | | 10K | 10KH | III | |
| **Counters (continued)** | | | | | | | | | |
| Synchronous 4-Bit Up/Down Binary | 669 | | | | 648 | | | | 693 |
| Up/Down Decade | 168 | 168 | | 168 | | | | | |
| Up/Down Binary | 169 | 169 | | 169 | | | | | |
| Programmable Decade | | | 522 | | | | | | |
| Programmable Binary | | | 526 | | | | | | |
| 4-Bit Decode, 3-State | | | | | 732 | | | | |
| 4-Bit Binary, 3-State | | | | | 738 | | | | |
| Decade Counter/Latch/Multiplexer, Asynchronous Reset, 3-State | | | | | | | | | |
| Binary Counter/Latch/Multiplexer, Asynchronous Reset, 3-State | | | | | | | | | |
| Decade Counter/Latch/Multiplexer, Synchronous Reset, 3-State | | | | | | | | | |
| Binary Counter/Latch/Multiplexer, Synchronous Reset, 3-State | | | | | | | | | |
| Decade Counter/Register/Multiplexer, 3-State | | | | | | | | | |
| Binary Counter/Register/Multiplexer, 3-State | | | | | | | | | |
| Decade Counter/Register/Multiplexer, 3-State | | | | | | | | | |
| Binary Counter/Register/Multiplexer, 3-State | | | | | | | | | |
| Seven-Stage Ripple Counter | | | 024 | 4024 | 632,646 | | | | |
| Decade Counter/Divider | | | 017 | 4017 | 620 | | | | |
| Presettable Divide-by-N | | | 018 | | 648 | | | | |
| 14-Bit Binary Counter/Divider | | | 060 | 4060 | | | | | |
| 12-Bit Binary | | | 040 | 4040 | | | | | |
| 14-Bit Binary | | | 020 | 4020 | | | | | |
| Octal Counter/Divider | | | 022 | | | | | | |
| Dual Programmable BCD/Binary | | | 569 | | | | | | |
| Three-Digit BCD | | | 553 | | | | | | |
| Real Time 5-Decade | | | 534 | | 623 | | | | |
| 1 GHz Divide-by-Four Prescaler | | | | | 709 | | | 1697 | |
| 1 GHz Divide-by-Four | | | | | | | | 1699 | 620,648 |
| **Register Files** | | | | | | | | | |
| 4 x 4 Register File, Open-Collector | 170 | | | | 620 | | | | 620 |
| 4 x 4 Register File, 3-State | 670 | | | | 648 | | | | 648 |
| 16 x 4 Bit Register File | | | | | | | 145 | | |
| **Shift Registers** | | | | | | | | | |
| 8-Bit Serial-In/Parallel-Out Shift Register | 164 | | 034 | 164 | 632,646 | | | | |
| 8-Bit Parallel-In/Serial-Out Shift Register | 165 | | 021 | 165 | 620,648 | | | | |

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.





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## FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

| Function | TTL | | CMOS | | | MECL | | | |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | Package* | 10K | 10KH | III | Package* |
| **Shift Registers (continued)** | | | | | | | | | |
| 4-Bit Shift Register | 95B | | | | 632,646 | | | | 620 |
| 8-Bit Parallel-In/Serial-Out Shift Register | 166 | | 014 | | 620,648 | | | | 648 |
| 4-Bit Shift Register | 195A | 195 | | 195 | | | | 1694 | |
| 4-Bit Universal Shift Register | 194A | 194 | 194 | 194 | | 141 | 141 | | |
| 8-Bit Shift/Storage Register, 3-State | 299 | | 094 | 299 | | | | | |
| 8-Bit Shift Register with Sign Extend, 3-State | 322A | | | | | | | | |
| 8-Bit Shift/Storage Register, 3-State | 323 | 323 | | | | | | | |
| 4-Bit Shift Register, 3-State | 395 | | | | | | | | |
| BCD Bidirectional Shift Register/Latch/Multiplexer, 3-State | | | | | | | | | |
| 16-Bit Serial-In/Serial-Out Shift Register, 3-State | 673 | | | | | | | | |
| 16-Bit Parallel-In/Serial-Out Register, 3-State | 674 | | | | | | | | |
| 18-Bit Static Shift Register | | | 006 | | 632,646 | | | | |
| 1-to-64 Bit Variable Length Shift Register | | | 557 | | 620,648 | | | | |
| Dual 64-Bit Static Shift Register | | | 517 | | 648,690 | | | | |
| 4-Bit Parallel-In/Parallel-Out Shift Register | | | 035 | | 620,648 | | | | |
| Dual 4-Bit Static Shift Register | | | 015 | | | | | | |
| 128-Bit Static Shift Register | | | 562 | | 632,646 | | | | |
| 8-Bit Parallel to Serial S.R. w/Input Latches, 3-State | | | | 589 | | | | | |
| 8-Bit Serial to Parallel S.R. 3-State | | | | 595 | | | | | |
| 8-Bit Parallel to Serial S.R. w/Input Latches | | | | 597 | | | | | |
| **Multiplexers/Data Selectors** | | | | | | | | | |
| Quad 2-Input Multiplexer, Noninverting | 157 | 157,A | 519 | 157 | 620 | 158 | 158 | | 620 |
| Quad 2-Input Multiplexer, Inverting | 158 | 158,A | | 158 | 648 | 159 | 159 | | 648 |
| Quad 2-Input Multiplexer, Noninverting, 3-State | 257A | 257,A | | 257 | | | | | |
| Quad 2-Input Multiplexer, Inverting, 3-State | 258A | 258,A | | | | | | | |
| Quad 2-Multiplexer, with Output Register | 298 | | | | | 173 | 173 | | |
| Dual 4-Input Multiplexer | 153 | 153 | 539 | 153 | | 174 | 174 | | |
| Dual 4-Input Multiplexer, 3-State | 253 | 253 | | 253 | | | | | |
| 8-Input Multiplexer | 151 | 151 | | 151 | | 164 | 164 | | |
| 8-Input Multiplexer, 3-State | 251 | 251 | 512 | 251 | | | | | |
| Dual 4-Input Multiplexer (Inverting LS153) | 352 | 352 | | | | | | | |
| Dual 4-Input Multiplexer (3-State LS352) | 353 | 353 | | | | | | | |
| QUAD 2-Input Multiplexer with Output Register | 398 | 398 | | | 732,738 | | | | |
| Quad 2-Input Multiplexer with Output Register | 399 | 399 | | | 620,648 | | | | |
| Synchronous Address Multiplexer (MC6883) | 783 | | | | 711 | | | | |
| Dual Multiplexer with Latch and Common Reset | | | | | 734 | 132 | | | |

*See Surface Mount section for SO and PLCC packages.

(continued)

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| Function | TTL | | CMOS | | Package* | MECL | | | Package* |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | | 10K | 10KH | III | |
| **Multiplexers/Data Selectors (continued)** | | | | | | | | | |
| Dual Multiplexer with Latch | | | | | 632 | 134 | | | 620 |
| Quad Analog Switch/Quad Multiplexer | | | 016 | 4016<br>4316 | 646 | | | | 648 |
| Quad Analog Switch/Quad Multiplexer | | | 066 | 4066 | | | | | |
| Triple 2-Channel Analog Multiplexer/Demultiplexer | | | 053 | 4053<br>4353 | 620 | | | | |
| Dual 4-Channel Analog Multiplexer/Demultiplexer | | | 052 | 4052<br>4352 | | | | | |
| Dual 4-Channel Analog Data Selector | | | 529 | | | | | | |
| Quad 2-Input Analog Multiplexer/Demultiplexer | | | 551 | | | | | | |
| 8-Channel Analog Multiplexer/Demultiplexer | | | 051 | 4051<br>4351 | | | | | |
| 4-to-16 Decoder | | | | 154 | 724,758 | | | | |
| 8-Input Multiplexer, 3-State | | | | 354 | 732 | | | | |
| 8-Input Multiplexer, 3-State | | | | 356 | 738 | | | | |
| **Decoders/Demultiplexers** | | | | | | | | | |
| Dual 1-of-4 Decoder/Demultiplexer | 139 | 139 | | 139 | 620 | | | | 620 |
| Dual 1-of-4 Decoder (Low) | 155 | | 556 | | 648 | 171 | 171 | | 648 |
| Dual 1-of-4 Decoder, Open-Collector | 156 | | | | | | | | |
| 1-of-10 Decoder | 42 | | | 42 | | | | | |
| 1-of-10 Decoder/Driver, Open-Collector | 145 | | | | | | | | |
| 1-of-8 Decoder/Demultiplexer (Low) | 138 | 138 | | 138 | | 161 | 161 | | |
| 3-Line to 8-Line Decoder/Demultiplexer | 137 | | | 137 | | | | | |
| 1-of-10 Decoder, 3-State | | 537 | | | | | | | |
| 1-of-8 Decoder, 3-State | | 538 | | | | | | | |
| Dual 1-of-4 Decoder, 3-State | | 539 | | | | | | | |
| Binary to 1-8 (High) | | | | | | 162 | 162 | | |
| Dual Binary 1-4 (High) | | | 555 | | | 172 | 172 | | |
| BCD-to-Decimal/Binary-to-Octal Decoder | | | 028 | | | | | | |
| 4-Bit Latch/4-to-16 Line Decoder (High) | | | 514 | 4514 | 724,758, | | | | |
| 4-Bit Latch/4-to-16 Line Decoder (Low) | | | 515 | | 709,623 | | | | |
| 1-of-8 Decoder/Demultiplexer w/Latched Inputs | | | | 237 | | | | | |
| **Display Decoder/Drivers** | | | | | | | | | |
| BCD to 7-Segment Decoder/Driver, Open-Collector | 47 | | | | 620 | | | | |
| BCD to 7-Segment Decoder/Driver with Pull-Ups | 48 | | 558 | | 648 | | | | |
| BCD to 7-Segment Decoder/Driver, Open-Collector | 247 | | | | 620 | | | | |
| BCD to 7-Segment Decoder/Driver with Pull-Ups | 248 | | | | 648 | | | | |

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.





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## FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

| Function | TTL | | CMOS | | Package* | MECL | | | Package* |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | | 10K | 10KH | III | |
| **Display Decoder/Drivers (continued)** | | | | | | | | | |
| Hex-to-Seven Segment Decoder/Driver/Latch | | | 495 | | 620 | | | | |
| BCD-to-Seven Segment Latch/Decoder/Driver | | | 511 | 4511 | 648 | | | | |
| BCD-to-Seven Segment Latch/Decoder/Driver — Ripple Blanking | | | 513 | | 707,726 | | | | |
| BCD-to-Seven Segment Latch/Decoder/Driver | | | 543 | 4543 | 620,648 | | | | |
| BCD-to-Seven Segment Latch/Decoder/Driver — Ripple Blanking | | | 544 | | 707,726 | | | | |
| BCD-to-Seven Segment Decoder/Driver — High Current | | | 547 | | 620,648 | | | | |
| 48-Segment Multiplexed LCD Driver (Master) | | | 5000 | | 623,709 | | | | |
| 48-Segment Multiplexed LCD Driver (Slave) | | | 5001 | | 707,726 | | | | |
| **Priority Encoders** | | | | | | | | | |
| 10-Line Decimal to 4-Line Priority Encoder | 147 | | | | 620 | | | | 620 |
| 8-Input to 3-Line Priority Encoder | 148 | 148 | 532 | | 648 | 165 | 165 | | 648 |
| 8-Input to 3-Line Priority Encoder | 748 | | | | | | | | |
| 8-Input to 3-Line Priority Encoder, 3-State | 348 | | | | | | | | |
| 8-Input to 3-Line Priority Encoder, 3-State | 848 | | | | | | | | |
| **Multivibrators** | | | | | | | | | |
| Retriggerable Monostable Multivibrator | 122 | | | | 632,646 | 198 | | | 620 |
| Dual Retriggerable Monostable Multivibrator | 123 | | | | 620 | | | | 648 |
| Dual One-Shot (Very Stable) | 221 | | | | 648 | | | | |
| Dual Precision Retriggerable/Resettable Monostable Multivibrator | | | 538 | | | | | | |
| **Oscillators/Timers** | | | | | | | | | |
| Voltage Controlled Oscillator | | | | | 626,693 | | | 1658 | 620 |
| 25-Stage Frequency Divider | | | 521 | | 620 | | | | 648 |
| Programmable Timer | | | 536 | | 648 | | | | 607 |
| Programmable Oscillator/Timer | | | 541 | | 632,646 | | | | 632 |
| Emitter Coupled Oscillator | | | | | | | | 1648 | 646 |
| **Receivers** | | | | | | | | | |
| Triple Line | | | | | | 114 | | | 620,648 |
| Quad Line | | | | | | 115 | 115 | 1692 | 620,650 |
| Triple Line | | | | | | 116 | 116 | | 620,648 |
| High-Speed Triple Line | | | | | | 216 | | | |
| Quad Bus | | | | | | 129 | | | |
| **Comparators** | | | | | | | | | |
| 4-Bit Magnitude Comparator | 85 | | 585 | 85 | 620,648 | | | | 620 |
| 8-Bit Magnitude Comparator | | 521 | | | 732 | | | | 648 |
| 8-Bit Magnitude Comparator, 3-State | 682 | | | | 738 | | | | |
| 8-Bit Magnitude Comparator, 3-State | 684 | | | | | | | | |
| 8-Bit Magnitude Comparator | 688 | | | 688 | | | | | |

*See Surface Mount section for SO and PLCC packages.

(continued)





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| Function | TTL | | CMOS | | Package* | MECL | | | Package* |
|---|---|---|---|---|---|---|---|---|---|
| | LS | FAST | STD | HC | | 10K | 10KH | III | |
| **Comparators (continued)** | | | | | | | | | |
| 5-Bit Magnitude Comparator | | | | | | 166 | 166 | | |
| **Arithmetic Operators** | | | | | | | | | |
| 4-Bit Full Adder | 83A | | 008 | | 620 | | | | 620 |
| 4-Bit Full Adder (Rotated LS83A) | 283 | 283 | | | 648 | | | | 648 |
| 4-Bit ALU | 181 | 181 | 581 | | 623 | 181 | 181 | | |
| 4-Bit ALU | 181 | 181<br>381<br>382 | | | 709<br>649<br>624,758 | | | | |
| 4-Bit Barrel Shifter | | 350 | | | 620,648 | | | | 620 |
| Quad 4-Bit Adder Subtractor | 385 | | | | 732,738 | | | | 648 |
| Look Ahead Carry Generator | | 182 | 582 | | 620,648 | 179 | 179 | | |
| Dual High-Speed Adder/Subtractor | | | | | | 180 | 180 | | |
| 2-Bit Logic Unit/Function Generator | | | | | | 182 | | | |
| 4 x 2 Multiplier | | | | | | 183 | | | 623 |
| 2 x 1 Array Multiplier, High-Speed | | | | | | 287 | | | 620 |
| BCD Rate Multiplier | | | 527 | | 620 | | | | 648 |
| 2 x 2 Bit Parallel Binary Multiplier | | | 554 | | 648 | | | | |
| Triple Serial Adder (Positive Logic) | | | 032 | | | | | | |
| Triple Serial Adder (Negative Logic) | | | 038 | | | | | | |
| NBCD Adder | | | 560 | | | | | | |
| 9's Complementer | | | 561 | | 632,646 | | | | |
| **Parity Generators/Checkers** | | | | | | | | | |
| 9-Bit Odd/Even Parity Generator/Checker | 280 | 280 | | 280 | 632,646 | 170 | | | 620 |
| 12-Bit Parity Generator/Checker | | | 531 | | 620,648 | 160 | 160 | | 648 |
| **Error Detection-Correction** | | | | | | | | | |
| IBM Code | | | | | | 163 | | | 620 |
| Motorola Code | | | | | | 193 | | | 648 |
| Hamming Code | | 2960 | | | 740 | | | | |

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.





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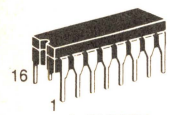
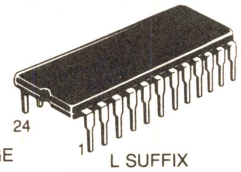
# Bipolar Memories

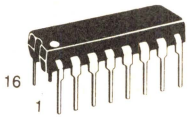
## Random Access Memories — RAMs



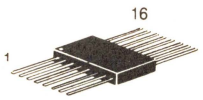

L SUFFIX
CERAMIC PACKAGE
CASE 620



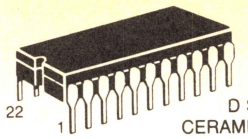

L SUFFIX
CERAMIC PACKAGE
CASE 623



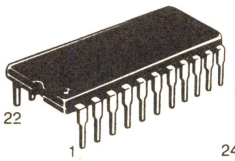

P SUFFIX
PLASTIC PACKAGE
CASE 648



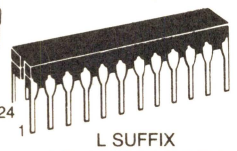

F SUFFIX
CERAMIC PACKAGE
CASE 650




D SUFFIX
CERAMIC PACKAGE
CASE 736




P SUFFIX
PLASTIC PACKAGE
CASE 708




L SUFFIX
CERAMIC PACKAGE
CASE 748

### ECL10K/10KH

Emitter-coupled logic (ECL) represents today's fastest logic form; ECL memories complement this characteristic. Motorola ECL RAMs are available to match the speed capabilities of the ECL10K and 10KH logic families, the two most pervasive ECL lines available.

| Organization | Device Type | Suffix | Access Time (ns Max.) | Power Dissipation (mW Typ) | Package | Comments |
|---|---|---|---|---|---|---|
| 8 x 2 Multiport Register File | MCM10143 | L | 15 | 610 | L-Case 623 | |
| 16 x 4 Register File | MC10H145 | P/L | 6 | 700 | L-Case 620 | |
| | MCM10145 | L | 15 | 468 | P-Case 648 | |
| 64 x 1 | MCM10148 | L | 15 | 420 | L-Case 620 | |
| 128 x 1 | MCM10147 | L | 15 | 415 | | |
| 256 x 1 | MCM10144 | L | 26 | 468 | | |
| 1K x 1 | MCM10415<br>-15<br>-20 | L | <br>15<br>20 | 520 | | |
| | MCM10146 | L | 29 | 600 | | |

# Read-Only Memories — ROMs

### ECL

High-speed PROMs fully compatible with MECL 10K and 10KH logic families.

| | | | | | | |
|---|---|---|---|---|---|---|
| 32 x 8 | MCM10139 | F/L | 20 | 520 | F-Case 650<br>L-Case 620 | |
| 256 x 4 | MCM10149 | F/L | 25 | 540 | | |
| | MCM10149-10 | | 10 | | | |

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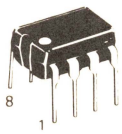
# Amplifiers and Comparators

## Operational Amplifiers

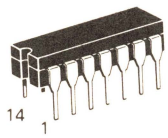
Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low-cost industry-standard types to high precision circuits, the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated "chip" form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.

CASE 601
METAL
**H, G SUFFIX**

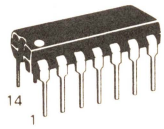
CASE 603
METAL
**G SUFFIX**



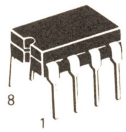
CASE 626
PLASTIC
**N, P OR P1 SUFFIX**



CASE 632
CERAMIC
**J, L SUFFIX**



CASE 646
PLASTIC
**N, N-14, P OR P2 SUFFIX**



CASE 693
CERAMIC
**J OR J-8, U, Z, JG SUFFIX**

## Single Operational Amplifiers

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V$=1) MHz Typ | SR ($A_V$=1) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Noncompensated** | | | | | | | | | | | |
| **Commercial Temperature Range (0°C to +70°C)** | | | | | | | | | | | |
| LM301A | 0.25 | 7.5 | 10 | 50 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | General Purpose | H, N/626, J/693 |
| LM308 | 7.0 | 7.5 | 15 | 1.0 | 25 | 1.0 | 0.3 | ±3.0 | ±18 | Precision | H, N/626 |
| LM308A | 7.0 | 0.5 | 5.0 | 1.0 | 80 | 1.0 | 0.3 | ±3.0 | ±18 | Precision | H, N/626 |
| MC1439 | 1.0 | 7.5 | 15 | 100 | 15 | 2.0 | 4.2 | ±6.0 | ±18 | High Slew Rate | G/601, P1 |
| MC1709C | 1.5 | 7.5 | 15 | 500 | 15 | 1.0 | 0.3 | ±3.0 | ±18 | General Purpose | G/601, P1, U |
| MC1748C | 0.5 | 6.0 | 15 | 200 | 20 | 1.0 | 0.5 | ±3.0 | ±18 | General Purpose | G/601, P1, U |
| **Industrial Temperature Range (−25°C to +85°C)** | | | | | | | | | | | |
| LM201A | 0.075 | 2.0 | 10 | 10 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | General Purpose | H, N/626, J/693 |
| LM208 | 0.002 | 2.0 | 3.0 | 0.2 | 50 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | H, N/626, J/632, J-8 |
| LM208A | 0.002 | 0.5 | 1.0 | 0.2 | 80 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | H, N/626, J/632, J-8 |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| LM101A | 0.075 | 2.0 | 10 | 10 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | General Purpose | H, J/693 |
| LM108 | 0.002 | 2.0 | 3.0 | 0.2 | 50 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | H, J, J-8/693 |
| LM108A | 0.002 | 0.5 | 1.0 | 0.2 | 80 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | H, J, J-8/693 |
| MC1539 | 0.5 | 3.0 | 15 | 60 | 50 | 2.0 | 4.2 | ±4.0 | ±18 | High Slew Rate | G/601 |
| MC1709 | 0.5 | 5.0 | 15 | 200 | 25 | 1.0 | 0.3 | ±3.0 | ±18 | General Purpose | G/601, U |
| MC1709A | 0.6 | 3.0 | 5.0 | 100 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | High Performance MC1709 | G/601 |
| MC1748 | 0.5 | 5.0 | 15 | 200 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | General Purpose | G/601, U |





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## Internally Compensated

### Commercial Temperature Range (0°C to +70°C)

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V$=1) MHz Typ | SR ($A_V$=1) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LF351 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | N/626 |
| LF355 | 200 pA | 10 | 5.0 | 50 pA | 50 | 1.0 | 5.0 | ±5.0 | ±18 | JFET Input | H/601, J/693 |
| LF355B | 100 pA | 5.0 | 5.0 | 20 pA | 50 | 2.5 | 5.0 | ±5.0 | ±22 | JFET Input | H/601, J/693 |
| LF356 | 200 pA | 10 | 5.0 | 50 pA | 50 | 2.0 | 15 | ±5.0 | ±18 | JFET Input | H/601, J/693 |
| LF356B | 100 pA | 5.0 | 5.0 | 20 pA | 50 | 5.0 | 12 | ±5.0 | ±22 | JFET Input | H/601, J/693 |
| LF357 | 200 pA | 10 | 5.0 | 50 pA | 50 | 3.0 | 75 | ±5.0 | ±18 | Wideband FET Input | H/601, J/693 |
| LF357B | 100 pA | 5.0 | 5.0 | 20 pA | 50 | 20 | 50 | ±5.0 | ±22 | JFET Input | H/601, J/693 |
| LF441C | 100 pA | 5.0 | 10 | 50 pA | 25 | 2.0 | 6.0 | ±5.0 | ±18 | Low Power JFET Input | N/626 |
| LM11C | 100 pA | 0.6 | 2.0 | 10 pA | 250 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | H, N/626, J/632, J-8/693 |
| LM11CL | 200 pA | 5.0 | 3.0 | 25 pA | 50 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | H, N/626, J/632, J-8/693 |
| LM307 | 0.25 | 7.5 | 10 | 50 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | General Purpose | N/626 |
| MC1436 | 0.04 | 10 | 12 | 10 | 70 | 1.0 | 2.0 | ±15 | ±34 | High Voltage | G/601, U |
| MC1456 | 0.03 | 10 | 12 | 10 | 70 | 1.0 | 2.5 | ±3.0 | ±18 | High Performance | G/601, P1, U |
| MC1733C | 30 | — | — | 5.0 μA | 80 | 90 | — | ±4.0 | ±8.0 | Differential Wideband Video Amp | G/601, L, P/646 |
| MC1741C | 0.5 | 6.0 | 15 | 200 | 20 | 1.0 | 0.5 | ±3.0 | ±18 | General Purpose | G/601, P1, U |
| MC1741SC | 0.5 | 6.0 | 15 | 200 | 20 | 1.0 | 10 | ±3.0 | ±18 | High Slew Rate | G/601, P1 |
| MC1776C | 0.003 | 6.0 | 15 | 3.0 | 100 | 1.0 | 0.2 | ±1.2 | ±18 | μPower, Programmable | G/601, P1, U |
| MC3476 | 0.05 | 6.0 | 15 | 25 | 50 | 1.0 | 0.2 | ±1.5 | ±18 | Low Cost μPower, Programmable | G/601, P1, U |
| MC34001 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | G/601, P/626, U |
| MC34001A | 100 pA | 2.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | G/601, P/626, U |
| MC34001B | 200 pA | 5.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | G/601, P/626, U |
| MC34071 | 0.50 | 3.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | P/626, U |
| MC34071A | 500 nA | 2.5 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | P/626, U |
| MC34080 | 200 pA | 1.0 | 10 | 100 pA | 25 | 16 | 55 | ±5.0 | ±22 | Decompensated | P/626, U |
| MC34080A | 200 pA | 0.5 | 10 | 100 pA | 50 | 16 | 55 | ±5.0 | ±22 | MC34081 for $A_V \geq 2$ | P/626, U |
| MC34081 | 200 pA | 1.0 | 10 | 100 pA | 25 | 8.0 | 30 | ±5.0 | ±22 | High Speed, JFET Input | P/626, U |
| MC34081A | 200 pA | 0.5 | 10 | 100 pA | 50 | 8.0 | 30 | ±5.0 | ±22 | High Speed, JFET Input | P/626, U |
| MC34181 | 0.1 nA | 2.0 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| OP-27E | 0.040 | 0.025 | 0.2 | 35 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | P/626 |
| OP-27F | 0.055 | 0.060 | 0.3 | 50 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | P/626 |
| OP-27G | 0.080 | 0.100 | 0.4 | 75 | 700 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | P/626 |
| TL061AC | 200 pA | 6.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| TL061BC | 200 pA | 3.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| TL061C | 200 pA | 15 | 10 | 200 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| TL071AC | 200 pA | 6.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | P/626, JG |
| TL071BC | 200 pA | 3.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | P/626, JG |
| TL071C | 200 pA | 10 | 10 | 50 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | P/626, JG |
| TL081AC | 200 pA | 6.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | P/626, JG |
| TL081BC | 200 pA | 3.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | P/626, JG |
| TL081C | 400 pA | 15 | 10 | 200 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | P/626, JG |

### Industrial Temperature Range (−25°C to +85°C)

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OP-27E | 0.040 | 0.025 | 0.2 | 35 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | Z |
| OP-27F | 0.055 | 0.060 | 0.3 | 50 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | Z |
| OP-27G | 0.080 | 0.100 | 0.4 | 75 | 700 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | Z |

### Automotive Temperature Range (−40°C to +85°C)

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MC33071 | 0.50 | 3.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | P/626, U |
| MC33071A | 500 nA | 2.5 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | P/626, U |
| MC33171 | 0.10 | 4.5 | 10 | 20 | 50 | 1.8 | 2.1 | +3.0 | +44 | Low Power, Single Supply | P/626 |
| MC33181 | 0.1 nA | 2.0 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| TL061V | 200 pA | 6.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | P/626 |



Motorola Semiconductor

## Single Operational Amplifiers (continued)

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V$=1) MHz Typ | SR ($A_V$=1) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Internally Compensated** | | | | | | | | | | | |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| LM11 | 50 pA | 0.3 | 1.0 | 10 pA | 250 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | H, J/632, J-8/693 |
| MC1536 | 0.02 | 5.0 | 10 | 3.0 | 100 | 1.0 | 2.0 | ±15 | ±40 | High Voltage | G/601, U |
| MC1556 | 0.015 | 4.0 | 10 | 2.0 | 100 | 1.0 | 2.5 | ±3.0 | ±22 | High Performance | G/601, 693, U |
| MC1733 | 0.20 | — | — | 3.0 μA | 90 | 90 | — | ±4.0 | ±8.0 | Differential Wideband Video Amp | G/603, L |
| MC1741 | 0.5 | 5.0 | 15 | 200 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | General Purpose | G/601, U |
| MC1741S | 0.5 | 5.0 | 15 | 200 | 50 | 1.0 | 10 | ±3.0 | ±22 | High Slew Rate | G/601, U |
| MC1776 | 0.0075 | 5.0 | 15 | 3.0 | 200 | 1.0 | 0.2 | ±1.2 | ±18 | μPower, Programmable | G/601, L |
| MC35001 | 100 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | G/601, U |
| MC35001A | 75 pA | 2.0 | 10 | 25 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | G/601, U |
| MC35001B | 100 pA | 5.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | G/601, U |
| MC35071 | 0.50 | 3.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | U |
| MC35071A | 500 nA | 2.5 | 10 | 50 | 50 | 4.5 | 10 | 3.0 | 44 | Single Supply | U |
| MC35080 | 200 pA | 1.0 | 10 | 100 pA | 25 | 16 | 55 | ±5.0 | ±22 | Decompensated | U |
| MC35080A | 200 pA | 0.5 | 10 | 100 pA | 50 | 16 | 55 | ±5.0 | ±22 | MC35081 for $A_V \geq 2$ | U |
| MC35081 | 200 pA | 1.0 | 10 | 100 pA | 25 | 8.0 | 30 | ±5.0 | ±22 | High Speed, JFET Input | U |
| MC35081A | 200 pA | 0.5 | 10 | 100 pA | 50 | 8.0 | 30 | ±5.0 | ±22 | High Speed, JFET Input | U |
| MC35171 | 0.10 | 4.5 | 10 | 20 | 50 | 1.8 | 2.1 | +3.0 | +44 | Low Power, Single Supply | U |
| MC35181 | 0.1 nA | 2.0 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | U |
| OP-27A | 0.040 | 0.025 | 0.2 | 35 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | Z |
| OP-27B | 0.055 | 0.060 | 0.3 | 50 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | Z |
| OP-27C | 0.080 | 0.100 | 0.4 | 75 | 700 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | Z |
| TL061M | 200 pA | 6.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | JG |
| TL071M | 200 pA | 6.0 | 10 | 50 pA | 35 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | JG |
| TL081M | 200 pA | 9.0 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | JG |

# Dual Operational Amplifiers

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V$=1) MHz Typ | SR ($A_V$=1) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Noncompensated** | | | | | | | | | | | |
| **Commercial Temperature Range (0°C to +70°C)** | | | | | | | | | | | |
| MC1437 | 1.5 | 7.5 | 10 | 500 | 15 | 1.0 | 0.25 | ±3.0 | ±18 | Dual MC1709 | L, P/646 |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| MC1537 | 0.5 | 5.0 | 10 | 200 | 25 | 1.0 | 0.25 | ±3.0 | ±18 | Dual MC1709 | L |
| **Internally Compensated** | | | | | | | | | | | |
| **Commercial Temperature Range (0°C to +70°C)** | | | | | | | | | | | |
| LF353 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | N/626 |
| LF442C | 100 pA | 5.0 | 10 | 50 pA | 25 | 2.0 | 6.0 | ±5.0 | ±18 | Low Power JFET Input | N/626 |
| LM358 | 0.25 | 6.0 | 7.0 | 50 | 25 | 1.0 | 0.6 | ±1.5 | ±18 | Single Supply | H, N/626, J/693 |
| | | | | | | | | +3.0 | +36 | (Low Power Consumption) | |
| LM833 | 1.0 | 5.0 | 2.0 | 200 | 31.6 | 15 | 7.0 | ±2.5 | ±18 | Dual, Low Noise, Audio | P/626 |
| MC1458 | 0.5 | 6.0 | 10 | 200 | 20 | 1.1 | 0.8 | ±3.0 | ±18 | Dual MC1741 | G/601, P1, U |
| MC1458C | 0.70 | 10 | 10 | 300 | 20 | 1.1 | 0.8 | ±3.0 | ±18 | Dual General Purpose | G/601, P1 |
| MC1458S | 0.5 | 6.0 | 10 | 200 | 20 | 1.0 | 10 | ±3.0 | ±18 | High Slew Rate | G/601, P1, U |
| MC1747C | 0.5 | 6.0 | 10 | 200 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | Dual MC1741 | G/603, L, P2 |
| MC3458 | 0.5 | 10 | 7.0 | 50 | 20 | 1.0 | 0.6 | ±1.5 | ±18 | Split Supplies | G/601, P1, U |
| | | | | | | | | +3.0 | +36 | Single Supply (Low Crossover Distortion) | |





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## Dual Operational Amplifiers (continued)

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V$=1) MHz Typ | SR ($A_V$=1) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Commercial Temperature Range (0°C to +70°C) (continued)** | | | | | | | | | | | |
| MC4558AC | 0.5 | 5.0 | 10 | 200 | 50 | 2.8 | 1.6 | ±3.0 | ±22 | High Frequency | P1 |
| MC4558C | 0.5 | 6.0 | 10 | 200 | 20 | 2.8 | 1.6 | ±3.0 | ±18 | High Frequency | G/601, P1, U |
| MC34002 | 100 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | G/601, P/626, U |
| MC34002A | 75 pA | 2.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | G/601, P/626, U |
| MC34002B | 100 pA | 5.0 | 10 | 70 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | G/601, P/626, U |
| MC34072 | 0.50 | 3.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | P/626, U |
| MC34072A | 500 nA | 2.5 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | P/626, U |
| MC34082 | 200 pA | 3.0 | 10 | 100 pA | 25 | 8.0 | 30 | ±5.0 | ±22 | High Speed, JFET Input | P/626, U |
| MC34082A | 200 pA | 1.0 | 10 | 100 pA | 50 | 8.0 | 30 | ±5.0 | ±22 | High Speed, JFET Input | P/626, U |
| MC34083 | 200 pA | 3.0 | 10 | 100 pA | 25 | 16 | 55 | ±5.0 | ±22 | Decompensated | P/626, U |
| MC34083A | 200 pA | 1.0 | 10 | 100 pA | 50 | 16 | 55 | ±5.0 | ±22 | MC34082 for $A_V \geq 2$ | P/626, U |
| MC34182 | 0.1 nA | 3.0 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| TL062AC | 200 pA | 6.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| TL062BC | 200 pA | 3.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| TL062C | 200 pA | 15 | 10 | 200 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| TL072AC | 200 pA | 6.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | P/626, JG/693 |
| TL072BC | 200 pA | 3.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | P/626, JG/693 |
| TL072C | 200 pA | 10 | 10 | 50 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | P/626, JG/693 |
| TL082AC | 200 pA | 6.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | P/626, JG/693 |
| TL082BC | 200 pA | 3.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | P/626, JG/693 |
| TL082C | 400 pA | 15 | 10 | 200 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | P/626, JG/693 |
| **Industrial Temperature Range (−25°C to +85°C)** | | | | | | | | | | | |
| LM258 | 0.15 | 5.0 | 10 | 30 | 50 | 1.0 | 0.6 | ±1.5<br>±3.0 | ±18<br>±36 | Split or Single Supply OP Amp | H, N/626, J/693 |
| **Automotive Temperature Range (−40°C to +85°C)** | | | | | | | | | | | |
| LM2904 | 0.25 | 7.0 | 7.0 | 50 | 100 typ | 1.0 | 0.6 | ±1.5<br>±3.0 | ±13<br>±26 | Split or Single Supply OP Amp | H, N/626, J/693 |
| MC3358 | 5.0 | 8.0 | 10 | 75 | 20 | 1.0 | 0.6 | ±1.5<br>±3.0 | ±18<br>±36 | Split Supplies<br>Single Supply | P1/626 |
| MC33072 | 0.50 | 3.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | P/626, U |
| MC33072A | 500 nA | 2.5 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | P/626, U |
| MC33077 | 1.0 | 1.0 | 2.0 | 180 | 150 | 37 | 11 | ±2.5 | ±18 | Dual, Low Noise | P/626 |
| MC33078 | 750 nA | 2.0 | 2.0 | 150 | 31.6 | 16 | 7.0 | ±5.0 | ±18 | Low Noise | N/626 |
| MC33172 | 0.10 | 4.5 | 10 | 20 | 50 | 1.8 | 2.1 | +3.0 | +44 | Low Power, Single Supply | P/626 |
| MC33182 | 0.1 nA | 3.0 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| MC33282 | 100 pA | 500μV | 5.0 | 50 pA | 50 | 30 | 12 | ±2.5 | ±18 | Low Input Offset JFET | P/646 |
| TL062V | 200 pA | 6.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | P/626 |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| LM158 | 0.15 | 5.0 | 10 | 30 | 50 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | Split Supplies<br>Single Supply (Low Power Consumption) | H, J/693 |
| MC1558 | 0.5 | 5.0 | 10 | 200 | 50 | 1.1 | 0.8 | ±3.0 | ±22 | Dual MC1741 | G/601, U |
| MC1558S | 0.5 | 5.0 | 10 | 200 | 50 | 1.0 | 10 | ±3.0 | ±22 | High Slew Rate | G/601, U |
| MC1747 | 0.5 | 5.0 | 10 | 200 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | Dual MC1741 | G/601, L |
| MC3558 | 0.5 | 5.0 | 10 | 50 | 50 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | Split Supplies<br>Single Supply | G/601, U |
| MC4558 | 0.5 | 5.0 | 10 | 200 | 50 | 2.8 | 1.6 | ±3.0 | ±22 | High Frequency | G/601, U |
| MC35002 | 100 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | G/601, U |
| MC35002A | 75 pA | 2.0 | 10 | 25 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | G/601, U |
| MC35002B | 100 pA | 5.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | G/601, U |
| MC35072 | 0.50 | 3.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | U |
| MC35072A | 500 nA | 2.5 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | U |
| MC35082 | 200 pA | 3.0 | 10 | 100 pA | 25 | 8.0 | 30 | ±5.0 | ±22 | High Speed, JFET Input | U |
| MC35082A | 200 pA | 1.0 | 10 | 100 pA | 50 | 8.0 | 30 | ±5.0 | ±22 | High Speed, JFET Input | U |





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## Dual Operational Amplifiers (continued)

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V$=1) MHz Typ | SR ($A_V$=1) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| MC35083 | 200 pA | 3.0 | 10 | 100 pA | 25 | 16 | 55 | ±5.0 | ±22 | Decompensated | U |
| MC35083A | 200 pA | 1.0 | 10 | 100 pA | 50 | 16 | 55 | ±5.0 | ±22 | MC35082 for $A_V \geq 2$ | U |
| MC35172 | 0.10 | 4.5 | 10 | 20 | 50 | 1.8 | 2.1 | +3.0 | +44 | Low Power, Single Supply | U |
| MC35182 | 0.1 nA | 3.0 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | U |
| TL062M | 200 pA | 6.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | JG |
| TL072M | 200 pA | 6.0 | 10 | 50 pA | 35 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | JG |
| TL082M | 200 pA | 6.0 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | JG |

# Quad Operational Amplifiers

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V$=1) MHz Typ | SR ($A_V$=1) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Internally Compensated** | | | | | | | | | | | |
| **Commercial Temperature Range (0°C to +70°C)** | | | | | | | | | | | |
| LF347 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | N/646 |
| LF347B | 200 pA | 5.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | N/646 |
| LF444C | 100 pA | 10 | 10 | 50 pA | 25 | 2.0 | 6.0 | ±5.0 | ±18 | Low Power JFET Input | N/646 |
| LM324 | 0.25 | 6.0 | 7.0 | 50 | 25 | 1.0 | 0.6 | ±1.5 | ±16 | Low Power | J/632, N/646 |
| | | | | | | | | +3.0 | +32 | Consumption | |
| LM348 | 0.20 | 6.0 | — | 50 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | Quad MC1741 | J/632, N/646 |
| MC3401/ LM3900 | 0.3 | — | — | — | 1.0 | 5.0 | 0.6 | ±1.5 | ±18 | Norton Input | J/632, N/646 |
| | | | | | | | | +3.0 | +36 | | |
| MC3403 | 0.5 | 10 | 7.0 | 50 | 20 | 1.0 | 0.6 | ±1.5 | ±18 | No Crossover | L, P/646 |
| | | | | | | | | +3.0 | +36 | Distortion | |
| MC4741C | 0.5 | 6.0 | 15 | 200 | 20 | 1.0 | 0.5 | ±3.0 | ±18 | Quad MC1741 | L, P/646 |
| MC34004 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | L, P/646 |
| MC34004B | 200 pA | 5.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | L, P/646 |
| MC34074 | 0.50 | 4.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | L, P/646 |
| MC34074A | 500 nA | 3.0 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | L, P/646 |
| MC34084 | 200 pA | 12 | 10 | 100 pA | 25 | 8.0 | 30 | ±5.0 | ±22 | Hi-Speed, JFET Input | P/646 |
| MC34084A | 200 pA | 6.0 | 10 | 100 pA | 50 | 8.0 | 30 | ±5.0 | ±22 | Hi-Speed, JFET Input | P/646 |
| MC34085 | 200 pA | 12 | 10 | 100 pA | 25 | 16 | 55 | ±5.0 | ±22 | Decompensated | P/646 |
| MC34085A | 200 pA | 6.0 | 10 | 100 pA | 50 | 16 | 55 | ±5.0 | ±22 | MC34084 for $A_V \geq 2$ | P/646 |
| MC34184 | 0.1 nA | 10 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | P/646 |
| TL064AC | 200 pA | 6.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | N/646 |
| TL064BC | 200 pA | 3.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | N/646 |
| TL064C | 200 pA | 15 | 10 | 200 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | N/646 |
| TL074AC | 200 pA | 6.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | J/632, N/646 |
| TL074C | 200 pA | 10 | 10 | 50 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | J/632, N/646 |
| TL084AC | 200 pA | 6.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | J/632, N/646 |
| TL084BC | 200 pA | 3.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | J/632, N/646 |
| TL084C | 400 pA | 15 | 10 | 200 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | J/632, N/646 |
| **Industrial Temperature Range (−25°C to +85°C)** | | | | | | | | | | | |
| LM224 | 0.15 | 5.0 | 7.0 | 30 | 50 | 1.0 | 0.6 | ±1.5 | ±16 | Split or Single | J/632, N/646 |
| | | | | | | | | ±3.0 | ±32 | Supply OP Amp | |
| LM248 | 0.20 | 6.0 | — | 50 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | Quad MC1741 | J/632, N/646 |
| **Automotive Temperature Range (−40°C to +85°C)** | | | | | | | | | | | |
| LM2902 | 0.5 | 10 | — | 50 | — | 1.0 | 0.6 | ±1.5 | ±13 | Differential | N/646 |
| | | | | | | | | +3.0 | +26 | Low Power | |

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## Quad Operational Amplifiers (continued)

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V$=1) MHz Typ | SR ($A_V$=1) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Automotive Temperature Range (−40°C to +85°C) (continued)** | | | | | | | | | | | |
| MC3301/ LM2900 | 0.3 | — | — | — | 1.0 | 4.0 | 0.6 | ±2.0<br>+4.0 | ±15<br>+28 | Norton Input | P/646<br>N/646 |
| MC3303 | 0.5 | 8.0 | 10 | 75 | 20 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | Differential<br>General Purpose | P/646 |
| MC33074 | 0.50 | 4.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, Single Supply | L, P/646 |
| MC33074A | 500 nA | 3.0 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Quad High Performance | L, P/646 |
| MC33079 | 750 nA | 2.5 | 2.0 | 150 | 31.6 | 16 | 7.0 | ±5.0 | ±18 | Quad Low Noise | N/646 |
| MC33174 | 0.10 | 4.5 | 10 | 20 | 50 | 1.8 | 2.1 | +3.0 | +44 | Low Power, Single Supply | P/646 |
| MC33184 | 0.1 nA | 10 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | P/646 |
| MC33284 | 100pA | 500μV | 5.0 | 50pA | 50 | 30 | 12 | ±2.5 | ±18 | Low Input Offset JFET | P/646 |
| TL064V | 200 pA | 9.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | N/646 |
| **Telecommunications Temperature Range (−40°C to +85°C)** | | | | | | | | | | | |
| MC143403 | 1.0 nA | 30 | — | 200 pA | 45 dB | 0.8 | 1.5 | 4.75 | 12.6 | CMOS, Low Power, Drives Low-Impedance Loads | L, P/646 |
| MC143404 | 1.0 nA | 30 | — | 200 pA | 60 dB | 0.8 | 1.0 | 4.75 | 12.6 | CMOS, Very Low Power | L, P/646 |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| LM124 | 0.15 | 5.0 | 7.0 | 30 | 50 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±16<br>+32 | Low Power Consumption | J/632, N/646 |
| LM148 | 0.10 | 5.0 | — | 25 | 50 | 1.0 | 0.5 | ±3.0 | ±18 | Quad MC1741 | J/632 |
| MC3503 | 0.5 | 5.0 | 7.0 | 50 | 50 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | General Purpose<br>Low Power | L, P/646 |
| MC4741 | 0.5 | 5.0 | 15 | 200 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | Quad MC1741 | L |
| MC35004 | 100 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | L |
| MC35004B | 100 pA | 5.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | L |
| MC35074 | 0.50 | 4.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, Single Supply | L |
| MC35074A | 500 nA | 3.0 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Quad High Performance | L |
| MC35084 | 200 pA | 12 | 10 | 100 pA | 25 | 8.0 | 30 | ±5.0 | ±22 | Hi-Speed, JFET Input | L |
| MC35084A | 200 pA | 6.0 | 10 | 100 pA | 50 | 8.0 | 30 | ±5.0 | ±22 | Hi-Speed, JFET Input | L |
| MC35085 | 200 pA | 12 | 10 | 100 pA | 25 | 16 | 55 | ±5.0 | ±22 | Decompensated | L |
| MC35085A | 200 pA | 6.0 | 10 | 100 pA | 50 | 16 | 55 | ±5.0 | ±22 | MC35084 for $A_V \geq 2$ | L |
| MC35174 | 0.10 | 4.5 | 10 | 20 | 50 | 1.8 | 2.1 | +3.0 | +44 | Low Power, Single Supply | L |
| MC35184 | 0.1 nA | 10 | 10 | 0.05 | 25 | 4.0 | 10 | ±2.5 | ±18 | Low Power JFET Input | L |
| TL064M | 200 pA | 9.0 | 10 | 100 pA | 4.0 | 2.0 | 6.0 | ±2.5 | ±18 | Low Power JFET Input | J/632 |
| TL074M | 200 pA | 9.0 | 10 | 50 pA | 35 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | J/632 |
| TL084M | 200 pA | 9.0 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | J/632 |





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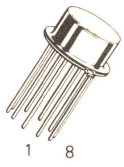
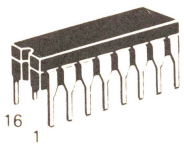
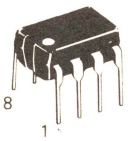
# Comparators



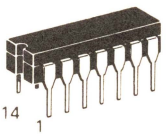

CASE 601
METAL
**H SUFFIX**



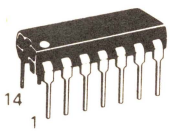

CASE 620
CERAMIC
**L SUFFIX**



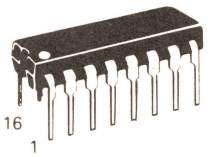

CASE 626
PLASTIC
**N SUFFIX**



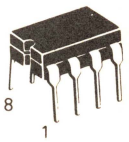

CASE 632
CERAMIC
**J SUFFIX**




CASE 646
PLASTIC
**N SUFFIX**




CASE 648
PLASTIC
**P SUFFIX**




CASE 693
CERAMIC
**J-8 SUFFIX**

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $I_{IO}$ μA Max | $A_V$ V/V Typ | $I_O$ mA Min | Response Time ns | Supply Voltage V | Description | Temperature Range (°C) | Package Suffix |
|---|---|---|---|---|---|---|---|---|---|---|
| **Single** | | | | | | | | | | |
| LM111 | 0.10 | 3.0 | 0.01 | 200K | 8.0 | 200 | +15, −15 | With strobe, will operate from | −55 to +125 | H, J-8 |
| LM211 | 0.10 | 3.0 | 0.01 | 200K | 8.0 | 200 | +15, −15 | single supply | −25 to +85 | H, J-8 |
| LM311 | 0.25 | 7.5 | 0.05 | 200K | 8.0 | 200 | +15, −15 | | 0 to +70 | H, N/626, J-8 |
| **Dual** | | | | | | | | | | |
| LM193 | 0.10 | 5.0 | 0.025 | 200K | 6.0 | 1300 | ±1.5 to | Designed for single or split | −55 to +125 | H |
| LM193A | 0.10 | 2.0 | 0.025 | 200K | 6.0 | 1300 | ±18 or | supply operation, input | −55 to +125 | H |
| LM293 | 0.25 | 5.0 | 0.050 | 200K | 6.0 | 1300 | +3.0 to +36 | common mode includes | −25 to +85 | H |
| LM293A | 0.25 | 2.0 | 0.050 | 200K | 6.0 | 1300 | | ground (negative supply) | −25 to +85 | H |
| LM393 | 0.25 | 5.0 | 0.050 | 200K | 6.0 | 1300 | | | 0 to +70 | H, N/626 |
| LM393A | 0.25 | 2.0 | 0.050 | 200K | 6.0 | 1300 | | | 0 to +70 | H, N/626 |
| LM2903 | 0.25 | 7.0 | 0.050 | 200K | 6.0 | 1500 | | | −40 to +85 | N/626 |
| MC3405 | 0.5 | 10 | 0.050 | 200K | 6.0 | 1300 | ±1.5 to | This device contains two op | 0 to +70 | L/632, P/646 |
| MC3505 | 0.5 | 5.0 | 0.050 | 200K | 6.0 | 1300 | ±7.5 or | amps and two comparators | −55 to +125 | L/632 |
| MC14575 | 0.001 | 30 | 0.0001 | 20K | 3.0 | 1000 | +3.0 to 15 | in a single package | −40 to +85 | P/648 |
| **Quad** | | | | | | | | | | |
| LM139 | 0.10 | 5.0 | 0.025 | 200K | 6.0 | 1300 | ±1.5 to | Designed for single or split | −55 to +125 | J |
| LM139A | 0.10 | 2.0 | 0.025 | 200K | 6.0 | 1300 | ±18 or | supply operation, input | −55 to +125 | J |
| LM239 | 0.25 | 5.0 | 0.050 | 200K | 6.0 | 1300 | +3.0 to +36 | common mode includes | −25 to +85 | J, N/646 |
| LM239A | 0.25 | 2.0 | 0.050 | 200K | 6.0 | 1300 | | ground (negative supply) | −25 to +85 | J, N/646 |
| LM339 | 0.25 | 5.0 | 0.050 | 200K | 6.0 | 1300 | | | 0 to +70 | J, N/646 |
| LM339A | 0.25 | 2.0 | 0.050 | 200K | 6.0 | 1300 | | | 0 to +70 | J, N/646 |
| LM2901 | 0.25 | 7.0 | 0.050 | 100K | 6.0 | 1300 | | | −40 to +85 | N/646 |
| MC3302 | 0.50 | 20 | 0.500 | 30K | 6.0 | 1300 | | | −40 to +85 | N/646 |
| MC3430 | 40 | 6.0 | 1.0 Typ | 1.2K | 16 | 33 | +5.0, −5.0 | High speed comparator/ | 0 to +70 | L, P |
| MC3431 | 40 | 10 | 1.0 Typ | 1.2K | 16 | 33 | +5.0, −5.0 | sense-amplifier | 0 to +70 | L, P |
| MC3432 | 40 | 6.0 | 1.0 Typ | 1.2K | 16 | 40 | +5.0, −5.0 | | 0 to +70 | L, P |
| MC3433 | 40 | 10 | 1.0 Typ | 1.2K | 16 | 40 | +5.0, −5.0 | | 0 to +70 | L, P |
| MC14574 | 0.001 | 30 | 0.0001 | 20K | 3.0 | 10000 | ±1.5 to ±7.5 or +3.0 to +15 | Externally programmable power dissipation with one or two resistors | −40 to +85 | L/620 |





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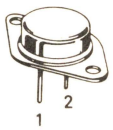
# Power Supply Circuits

## Linear Voltage Regulators

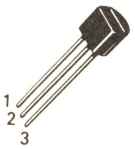
### Fixed Output

These low-cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on-card regulation employing current limiting and thermal shutdown. Low $V_{diff}$ devices are offered for battery powered systems.

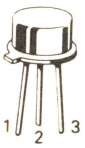
Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



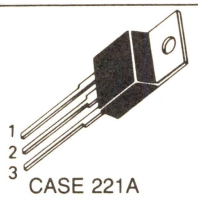

CASE 1
METAL
**K SUFFIX**



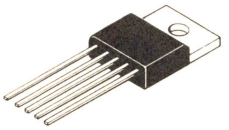

CASE 29
PLASTIC
**P, Z SUFFIX**




CASE 79
METAL
**G, H SUFFIX**




CASE 221A
PLASTIC POWER
**T, KC SUFFIX**



CASE 314D
PLASTIC
**T SUFFIX**

**Fixed-Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies**

| $V_{out}$ Volts | Tol.† Volts | $I_O$ mA Max | Device Positive Output | Device Negative Output | $V_{in}$ Min/Max | $Reg_{line}$ mV | $Reg_{load}$ mV | $\Delta V_O/\Delta T$ mV/°C Typ | Case Suffix |
|---|---|---|---|---|---|---|---|---|---|
| 5 | ±0.5 | 100 | LM2931-5.0 | — | 5.6/40 | 30 | 50 | 1.0 | Z, T |
| | ±0.25 | | MC78L05C | MC79L05C | 6.7/30 | 200 | 60 | | P, G |
| | | | LM2931A-5.0 | — | 5.6/40 | 30 | 50 | | Z, T |
| | | | MC78L05AC | MC79L05AC | 6.7/30 | 150 | 60 | | P, G |
| | | 500 | MC78M05C | MC79M05C | 7/35 | 100 | 100 | 1.0 | G, T |
| | ±0.4 | 1500 | LM109 | — | | | | 1.1 | K, H |
| | | | LM209 | — | | | | | |
| | ±0.25 | | LM309 | — | | 50 | | 1.0 | |
| | ±0.35 | | MC7805* | — | 8.0/35 | | | 0.6 | K |
| | ±0.25 | | MC7805B# | — | 8/35 | 100 | | 1.0 | T |
| | | | MC7805C | MC7905C | 7/35 | | | | K, T |
| | ±0.2 | | MC7805A* | — | 7.5/35 | 10 | 50 | 0.6 | K |
| | | | MC7805AC | MC7905AC | | | 100 | | K, T |
| | ±0.25 | | LM140-5* | — | 7.0/35 | 50 | 50 | | K |
| | ±0.2 | | LM140A-5* | — | | 10 | 25 | | |
| | ±0.25 | | LM340-5 | — | | 50 | 50 | | K, T |
| | ±0.2 | | LM340A-5 | — | | 10 | 25 | | |
| | ±0.1 | | TL780-05C | — | 7.0/35 | 5.0 | 25 | 0.06 | KC |
| | ±0.25 | 3000 | MC78T05* | — | 7.3/35 | 25 | 30 | 0.1 | K |
| | | | MC78T05C | — | | | | | K, T |
| | ±0.2 | | MC78T05A* | — | | 10 | 25 | | K |
| | | | MC78T05AC | — | | | | | K, T |

#$T_J$ = −40° to +125°C  †Output Voltage Tolerance for Worst Case  *$T_J$ = −55° to +150°C

(continued)



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## Fixed Output Voltage Regulators (continued)

| $V_{out}$ Volts | Tol.† Volts | $I_O$ mA Max | Device Positive Output | Device Negative Output | $V_{in}$ Min/Max | $Reg_{line}$ mV | $Reg_{load}$ mV | $\Delta V_O/\Delta T$ mV/°C Typ | Case Suffix |
|---|---|---|---|---|---|---|---|---|---|
| 5 | ±0.4 | 3000 | LM123* | — | 7.5/20 | 25 | 100 | 0.1 | K |
| | | | LM223 | — | | | | | |
| | ±0.25 | | LM323 | — | | | | | T |
| | ±0.2 | | LM123A | — | | | | | K |
| | | | LM223A | — | | 15 | 50 | | |
| | | | LM323A | — | | | | | T |
| 5.2 | ±0.26 | 1500 | — | MC7905.2C | 7.2/35 | 105 | 105 | 1.0 | T |
| 6 | ±0.3 | 500 | MC78M06C | — | 8/35 | 100 | 120 | 1.0 | T |
| | ±0.35 | 1500 | MC7806* | — | 9/35 | 60 | 100 | 0.7 | K |
| | ±0.3 | | MC7806B# | — | | 120 | 120 | | T |
| | | | MC7806C | MC7906C | 8/35 | | | | K, T |
| | ±0.24 | | MC7806AC | — | 8.6/35 | 11 | 100 | | T |
| | | | LM140-6* | — | 8/35 | 60 | 60 | | K |
| | ±0.3 | | LM340-6 | — | | | | | K, T |
| 8 | ±0.8 | 100 | MC78L08C | — | 9.7/30 | 200 | 80 | — | P, G |
| | | | MC78L08AC | — | | 175 | | | |
| | ±0.4 | 500 | MC78M08C | — | 10/35 | 100 | 160 | 1.0 | G, T |
| | | 1500 | MC7808* | — | 11.5/35 | 80 | 100 | | K |
| | | | MC7808B# | — | | 160 | 160 | | T |
| | | | MC7808C | MC7908C | 10.5/35 | | | | K, T |
| | ±0.3 | | MC7808AC | — | 10.6/35 | 13 | 100 | | T |
| | ±0.4 | | LM140-8* | — | 10.5/35 | 80 | 80 | | K |
| | | | LM340-8 | — | | | | | K, T |
| | | 3000 | MC78T08* | — | 10.4/35 | 35 | 30 | 0.16 | K |
| | | | MC78T08C | — | | | | | K, T |
| 12 | ±1.2 | 100 | MC78L12C | MC79L12C | 13.7/35 | 250 | 100 | — | P, G |
| | ±0.6 | | MC78L12AC | MC79L12AC | | | | | |
| | | 500 | MC78M12C | MC79M12C | 14/35 | 100 | 240 | 1.0 | G, T |
| | | 1500 | MC7812* | — | 15.5/35 | 120 | 120 | 1.5 | K |
| | | | MC7812B# | — | | 240 | 240 | | T |
| | | | MC7812C | MC7912C | 14.5/35 | | | | K, T |
| | ±0.5 | | MC7812A* | — | 14.8/35 | 18 | 50 | | K |
| | | | MC7812AC | — | | | 100 | | T |
| | ±0.6 | | LM140-12* | — | 14.5/35 | 120 | 120 | 1.5 | K |
| | ±0.5 | | LM140A-12* | — | | 18 | 32 | | |
| | ±0.6 | | LM340-12 | — | | 120 | 120 | | K, T |
| | ±0.5 | | LM340A-12 | — | | 18 | 32 | | |
| | ±0.24 | | TL780-12C | — | | 5.0 | | 0.15 | KC |
| | ±0.6 | 3000 | MC78T12* | — | 14.5/35 | 45 | 30 | 0.24 | K |
| | | | MC78T12C | — | | | | | K, T |
| | ±0.5 | | MC78T12A* | — | | 18 | 25 | | K |
| | | | MC78T12AC | — | | | | | K, T |

#$T_J$ = −40° to +125°C  †Output Voltage Tolerance for Worst Case  *$T_J$ = −55° to +150°C  (continued)

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## Fixed Output Voltage Regulators (continued)

| $V_{out}$ Volts | Tol.† Volts | $I_O$ mA Max | Device Positive Output | Device Negative Output | $V_{in}$ Min/Max | $Reg_{line}$ mV | $Reg_{load}$ mV | $\Delta V_O/\Delta T$ mV/°C Typ | Case Suffix |
|---|---|---|---|---|---|---|---|---|---|
| 15 | ±1.5 | 100 | MC78L15C | MC79L15C | 16.7/35 | 300 | 150 | — | P, G |
| | ±0.75 | | MC78L15AC | MC79L15A | | | | | |
| | | 500 | MC78M15C | MC79M15C | 17/35 | 100 | 300 | 1.0 | G, T |
| | | 1500 | MC7815* | — | 18.5/35 | 150 | 150 | 1.8 | K |
| | | | MC7815B# | — | | 300 | 300 | | T |
| | | | MC7815C | MC7915C | 17.5/35 | | | | K, T |
| | ±0.6 | | MC7815A* | — | 17.9/35 | 22 | 50 | | K |
| | | | MC7815AC | — | | | 100 | | K, T |
| | ±0.75 | | LM140-15* | — | 17.5/35 | 150 | 150 | | K |
| | ±0.6 | | LM140A-15* | — | | 22 | 35 | | |
| | ±0.75 | | LM340-15 | — | | 150 | 150 | | K, T |
| | ±0.6 | | LM340A-15 | — | | 22 | 35 | | |
| | ±0.3 | | TL780-15C | — | | 15 | 60 | 0.18 | KC |
| | ±0.75 | 3000 | MC78T15* | — | 17.5/40 | 55 | 30 | 0.3 | K |
| | | | MC78T15C | — | | | | | K, T |
| | ±0.6 | | MC78T15A* | — | | 22 | 25 | | K |
| | | | MC78T15AC | — | | | | | K, T |
| 18 | ±1.8 | 100 | MC78L18C | MC79L18C | 19.7/35 | 325 | 170 | — | P |
| | ±0.9 | | MC78L18AC | MC79L18AC | | | | | |
| | | 500 | MC78M18C | — | 20/35 | 100 | 360 | 1.0 | G, T |
| | | 1500 | MC7818* | — | 22/35 | 180 | 180 | 2.3 | K |
| | | | MC7818B# | — | | 360 | 360 | | T |
| | ±0.7 | | MC7818C | MC7918C | 21/35 | | | | K, T |
| | | | MC7818AC | — | | 31 | 100 | | T |
| | ±0.9 | | LM340-18 | — | | 180 | 180 | | T |
| 20 | ±1.0 | 500 | MC78M20C | — | 22/40 | 10 | 400 | 1.1 | G, T |
| 24 | ±2.4 | 100 | MC78L24C | MC79L24C | 25.7/40 | 350 | 200 | — | P |
| | ±1.2 | | MC78L24AC | MC79L24AC | | 300 | | | |
| | | 500 | MC78M24C | — | 26/40 | 100 | 480 | 1.2 | G, T |
| | | 1500 | MC7824* | — | 28/40 | 240 | 240 | 3.0 | K |
| | | | MC7824B# | — | | 480 | 480 | | T |
| | | | MC7824C | MC7924C | 27/40 | | | | K, T |
| | ±1.0 | | MC7824AC | — | 27.3/40 | 36 | 100 | | T |
| | ±1.2 | | LM340-24 | — | | 240 | 240 | | T |

#$T_J$ = −40° to +125°C  †Output Voltage Tolerance for Worst Case  *$T_J$ = −55° to +150°C

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# Adjustable Output Voltage Regulators

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit providing a wide range of output voltages for industrial and communications applications. The three-terminal devices require only two external resistors to set the output voltage.

## Positive Output Regulators

| $I_O$ mA Max | Device | Suffix | $V_{out}$ Volts Min | $V_{out}$ Volts Max | $V_{in}$ Volts Min | $V_{in}$ Volts Max | $V_{in} - V_{out}$ Differential Volts Min | $P_D$ Watts Max $T_A$ = 25°C | $P_D$ Watts Max $T_C$ = 25°C | Regulation % $V_{out}$ @ $T_A$ = 25°C Max Line | Regulation % $V_{out}$ @ $T_A$ = 25°C Max Load | TC $V_{out}$ Typ %/°C | $T_J$ = °C Max | Case |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 | LM317L | H,Z | 1.2 | 37 | 5.0 | 40 | 3.0 | Internally Limited | | 0.04 | 0.5 | 0.006 | 125 | 29,79 |
| | LM217L# | | | | | | | | | 0.02 | 0.3 | 0.004 | 150 | |
| | LM117L* | | | | | | | | | | | 0.003 | | |
| | LM2931C,AC | T | 3.0 | 24 | 3.16 | | 0.6 | | | 0.15 | 1.0 | — | 125 | 314D |
| 150 | MC1723 | CP | 2.0 | 37 | 9.5 | 40 | 3.0 | 1.25 | — | 0.1 | 0.3 | 0.003 | 150 | 646 |
| | | CG | | | | | | 1.0 | 2.1 | | | 0.003 | | 603C |
| | | G | | | | | | | | | | 0.002 | | |
| | | CL | | | | | | 1.5 | — | | | 0.003 | 175 | 632 |
| | | L | | | | | | | — | | | 0.002 | | |
| 500 | LM317M | T | 1.2 | 37 | 5.0 | 40 | 3.0 | Internally Limited | | 0.04 | 0.5 | 0.0056 | 125 | 221A |
| 1500 | LM317 | T | 1.2 | 37 | 5.0 | 40 | 3.0 | Internally Limited | | 0.04 | 0.5 | 0.006 | 125 | 221A |
| | LM317 | H, K | | | | | | | | | | | | 79, 1 |
| | LM217# | | | | | | | | | | | 0.004 | | |
| | LM117* | | | | | | | | | 0.02 | 0.3 | 0.003 | 150 | |
| 3000 | LM350 | T | 1.2 | 33 | 5.0 | 36 | 3.0 | Internally Limited | | 0.03 | 0.5 | 0.008 | 125 | 221A |
| | LM350 | K | | | | | | | | | | | | 1 |
| | LM250# | | | | | | | | | 0.01 | 0.3 | 0.0057 | 150 | |
| | LM150* | | | | | | | | | | | 0.0051 | | |

## Negative Output Regulators

| $I_O$ mA Max | Device | Suffix | $V_{out}$ Volts Min | $V_{out}$ Volts Max | $V_{in}$ Volts Min | $V_{in}$ Volts Max | $V_{in} - V_{out}$ Differential Volts Min | $P_D$ Watts Max $T_A$ = 25°C | $P_D$ Watts Max $T_C$ = 25°C | Regulation % $V_{out}$ @ $T_A$ = 25°C Max Line | Regulation % $V_{out}$ @ $T_A$ = 25°C Max Load | TC $V_{out}$ Typ %/°C | $T_J$ = °C Max | Case |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 500 | LM337M | T | −1.2 | −37 | 5.0 | 40 | 3.0 | Internally Limited | | 0.04 | 1.0 | 0.0048 | 125 | 221A |
| 1500 | LM337 | T | −1.2 | −37 | 5.0 | 40 | 3.0 | Internally Limited | | 0.04 | 1.0 | 0.0048 | 125 | 221A |
| | LM337 | H, K | | | | | | | | | | | | 79, 1 |
| | LM237# | | | | | | | | | 0.02 | 0.5 | 0.0034 | 150 | |
| | LM137* | | | | | | | | | | | 0.0031 | | |

#$T_J$ = −25° to +150°C *$T_J$ = −55° to +150°C





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# Switching Regulators

Used as a control circuit in PWM, push-pull, bridge and series type Switchmode supplies, the devices include a voltage reference, oscillator, pulse-width modulator, phase splitter and output drive sections. Frequency and duty cycle are independently adjustable. Most of these devices also include one or two on-chip error amplifiers for voltage or current error signal feedback.

## Single-Ended Controllers

These single-ended voltage- and current-mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 watts power output.

| $I_O$ mA Max | $V_{CC}$ Volts Min | $V_{CC}$ Volts Max | V/I Operating Mode | Ref. Volts | Max Osc. Freq. (kHz) | Device | Suffix | $T_A$ °C | Case |
|---|---|---|---|---|---|---|---|---|---|
| 250 | 7.0 | 40 | V | 5.0 ± 5.0% | 200 | MC34060 | P | 0 to +70 | 646 |
| | | | | | | | L | | 632 |
| | | | | | | MC35060 | L | −55 to +125 | |
| 500 | | | | 5.0 ± 1.5% | | MC34060A | D | 0 to +70 | 751A |
| | | | | | | | P | | 646 |
| | | | | | | MC33060A | D | −40 to +85 | 751A |
| | | | | | | | P | | 646 |
| | | | | | | MC35060A | L | −55 to +125 | 632 |
| 1000 | 4.2 | 12 | I | 1.25 ± 2.0% | 300 | MC34129 | D | 0 to +70 | 751A |
| | | | | | | | P | | 646 |
| | | | | | | MC33129 | D | −40 to +85 | 751A |
| | | | | | | | P | | 646 |
| | 11.5 | 30 | | 5.0 ± 2.0% | 500 | UC3842A | D | 0 to +70 | 751A |
| | | | | | | | N | | 626 |
| | 11 | | | 5.0 ± 1.0% | | UC2842A | D | −25 to +85 | 751A |
| | | | | | | | N | | 626 |
| | | | | | | UC1842A | J | −55 to +125 | 693 |
| | 8.2 | | | 5.0 ± 2.0% | | UC3843A | D | 0 to +70 | 751A |
| | | | | | | | N | | 626 |
| | | | | 5.0 ± 1.0% | | UC2843A | D | −25 to +85 | 751A |
| | | | | | | | N | | 626 |
| | | | | | | UC1843A | J | −55 to +125 | 693 |
| 1500 | 2.5 | 40 | V | 1.245 ± 5.2%# | 100 | μA78S40 | PC | 0 to +70 | 648 |
| | | | | | | | DC | | 620 |
| | | | | | | | PV | −40 to +85 | 648 |
| | | | | | | | DM | −55 to +125 | 620 |
| | | | | 1.25 ± 5.6%# | | MC34063 | P1 | 0 to +70 | 626 |
| | | | | | | | U | | 693 |
| | | | | | | MC33063 | P1 | −40 to +85 | 626 |
| | | | | | | | U | | 693 |
| | | | | | | MC35063 | U | −55 to +125 | |
| | | | | 1.25 ± 2.0% | | MC34063A | D | 0 to +70 | 751 |
| | | | | | | | P1 | | 626 |
| | | | | | | MC33063A | D | −40 to +85 | 751 |
| | | | | | | | P1 | | 626 |
| | | | | | | MC35063A | U | −55 to +125 | 693 |

#Tolerance applies over the specified operating temperature range.



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## Double-Ended Controllers

These double-ended voltage-mode controllers are designed for use in push-pull, half-bridge, and full-bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

| $I_O$ mA Max | $V_{CC}$ Volts Min | $V_{CC}$ Volts Max | V/I Operating Mode | Ref. Volts | Max Osc. Freq. (kHz) | Device | Suffix | $T_A$ °C | Case |
|---|---|---|---|---|---|---|---|---|---|
| 250 | 7.0 | 40 | V | 5.0 ± 5.0%# | 200 | TL494 | CN | 0 to +70 | 648 |
| | | | | | | | CJ | | 620 |
| | | | | | | | IN | −25 to +85 | 648 |
| | | | | | | | IJ | | 620 |
| | | | | | | | MJ | −55 to +125 | |
| | | | | 5.0 ± 1.5% | 300 | TL594 | CN | 0 to +70 | 648 |
| | | | | | | | IN | −25 to +85 | |
| | | | | | | | MJ | −55 to +125 | 620 |
| ±400 | 8.0 | | | 5.1 ± 2.0% | 400 | SG3525A | N | 0 to +70 | 648 |
| | | | | | | | J | | 620 |
| | | | | 5.1 ± 1.0% | | SG2525A | N | −25 to +85 | 648 |
| | | | | | | | J | | 620 |
| | | | | | | SG1525A | J | −55 to +125 | |
| | | | | 5.1 ± 2.0% | | SG3527A | N | 0 to +70 | 648 |
| | | | | | | | J | | 620 |
| | | | | 5.1 ± 1.0% | | SG2527A | N | −25 to +85 | 648 |
| | | | | | | | J | | 620 |
| | | | | | | SG1527A | J | −55 to +125 | |
| ±200 | | | | 5.0 ± 2.0% | 350 | SG3526 | N | 0 to +125* | 707 |
| | | | | | | | J | | 726 |
| | | | | 5.0 ± 1.0% | | SG2526 | N | −25 to +150* | 707 |
| | | | | | | | J | | 726 |
| | | | | | | SG1526 | J | −55 to +150* | |

*Junction Temperature Range
#Tolerance applies over the specified operating temperature range.

## Floating Voltage and Current Regulators

Designed for laboratory type power supplies. Voltage is limited only by the break down voltage of associated, external, series-pass transistors.

| $V_{out}$ Volts Min | $V_{out}$ Volts Max | $I_O$ mA Max | Device | Suffix | $V_{aux}$ Volts Min | $V_{aux}$ Volts Max | $P_D$ Watts Max | $\Delta V_{ref}/V_{ref}$ % Line | $\Delta V_{ref}/V_{ref}$ % Load | $\Delta I_L/L_L$ % Max | TC $V_{out}$ %/°C Typ | Case |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | * | * | MC1466 | L | 21 | 30 | 0.75 | 0.015 | 0.015 | 0.2 | 0.001 | 632 |
| | | | MC1566 | L | 20 | 35 | | 0.004 | 0.004 | 0.1 | 0.006 | |

*Dependent on characteristics of external series-pass elements.

## Dual ±15 V Tracking Regulators

Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

| $V_{out}$ Volts Min | $V_{out}$ Volts Max | $I_O$ mA Max | $V_{in}$ Volts Min | $V_{in}$ Volts Max | Device | Suffix | $P_D$ Watts Max | $Reg_{line}$ mV | $Reg_{load}$ mV | TC %/°C ($T_{low}$ to $T_{high}$) Typ | $T_A$ °C | Case |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14.8 | 15.2 | ±100 | 17 | 30 | MC1468 | G | 0.8 | 10 | 10 | 3.0 | 0 to +75 | 603C |
| | | | | | | L | 1.0 | | | | | 632 |
| | | | | | MC1568 | G | 0.8 | | | | −55 to +125 | 603C |
| | | | | | | L | 1.0 | | | | | 632 |



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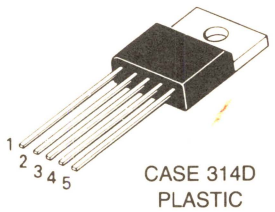
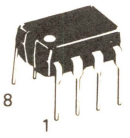
# Power/Motor Control Circuits

## Power Controllers

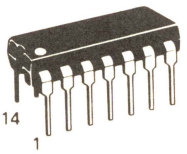
An assortment of battery and ac line-operated control ICs for specific applications are shown. They are designed to enhance system performance and reduce complexity in a wide variety of control applications.




CASE 314D
PLASTIC
**T SUFFIX**




CASE 626
PLASTIC




CASE 646
PLASTIC
**P SUFFIX**

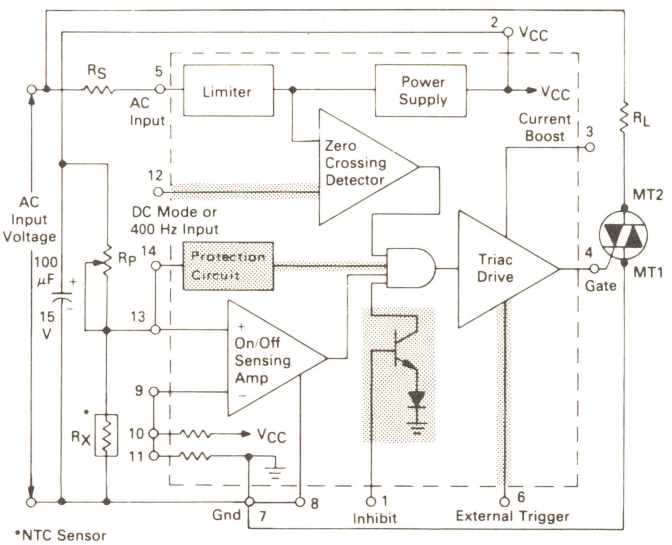
## Zero Voltage Switches

**CA3079P/CA3059P**

$T_A$ = −40° to +85°C, Case 646

. . . designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz. Features include:

- Limiter-Power Supply — Allows operation directly from an ac line.
- Differential On/Off Sensing Amplifier — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.
- Zero-Crossing Detector — Synchronizes the output pulses to the zero voltage point of the ac cycle. Eliminates RFI when used with resistive loads.
- Triac Drive — Supplies high-current pulses to the external power controlling thyristor.
- Protection Circuit (CA3059 only) — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.
- Inhibit Capability (CA3059 only) — Thyristor firing may be inhibited by the action of an internal diode gate.
- High Power DC Comparator Operation (CA3059 only) — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector).




*NTC Sensor

NOTE: Shaded Area Not Included With CA3079.

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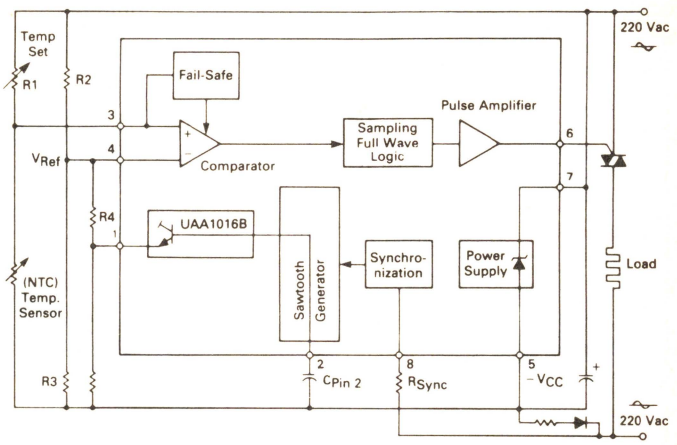
## Zero Voltage Controller

**UAA1016B** — $T_A$ = −20° to +100°C, Case 626

. . . designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. They provide the following features:

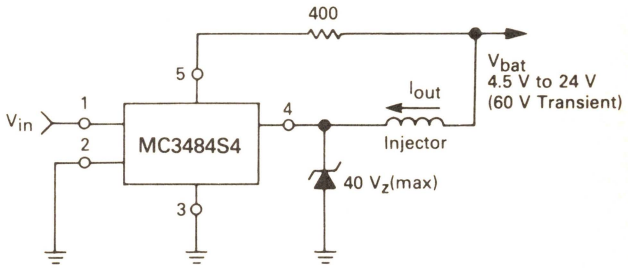
- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count




## Integrated Solenoid Driver

**MC3484S2,S4** — $T_J$ = −40° to +125°C, Case 314D

The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484S4 or 2.4 A in MC3484S2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation.

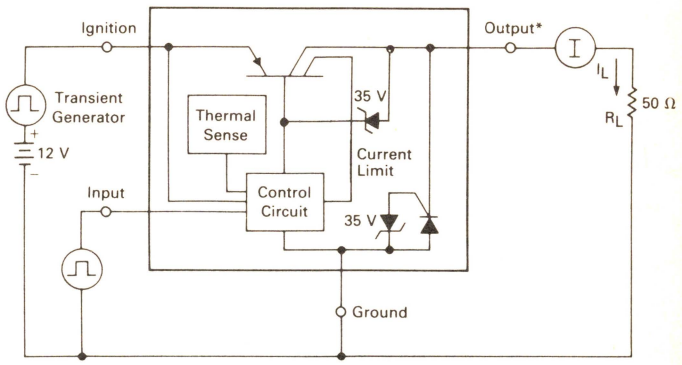



## High-Side Driver Switch

**MC3399T** — $T_J$ = −40° to +150°C, Case 314D

The MC3399T is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive- or negative-going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.




NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor ($C_O$) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.





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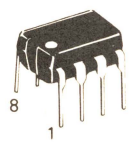
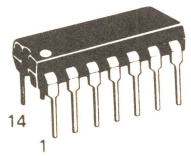
# Motor Controllers

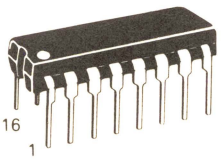
This section contains integrated circuits designed for cost effective control of specific motor-families. Included are controllers for dc servo, stepper, brushless, and universal type motors.



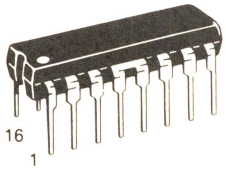

CASE 626
PLASTIC
**P SUFFIX**



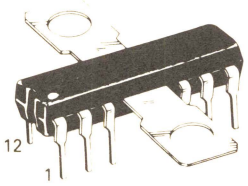

CASE 646
PLASTIC
**P SUFFIX**



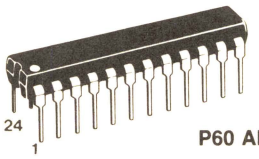

CASE 648
PLASTIC
**P SUFFIX**




CASE 648C
PLASTIC
**P SUFFIX**




CASE 721
PLASTIC

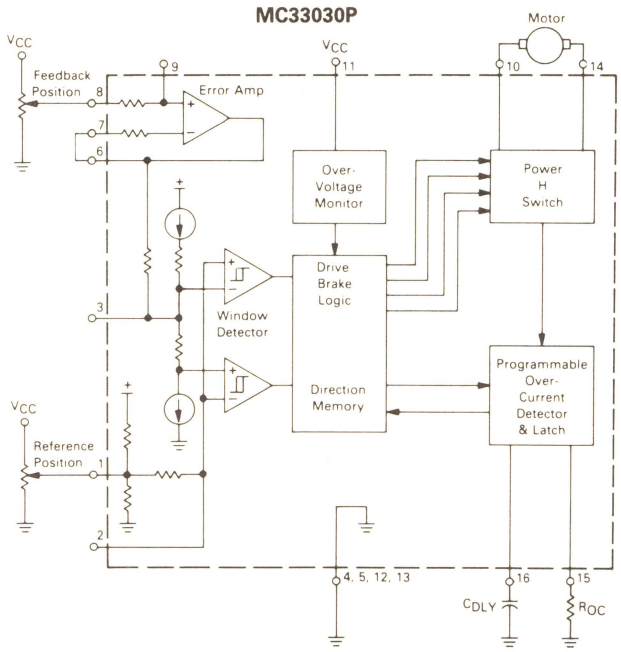



CASE 724
PLASTIC
**P60 AND P120 SUFFIX**

## DC Servo Motor Controller/Driver

**MC33030P** — $T_A$ = −40° to +85°C, Case 648C

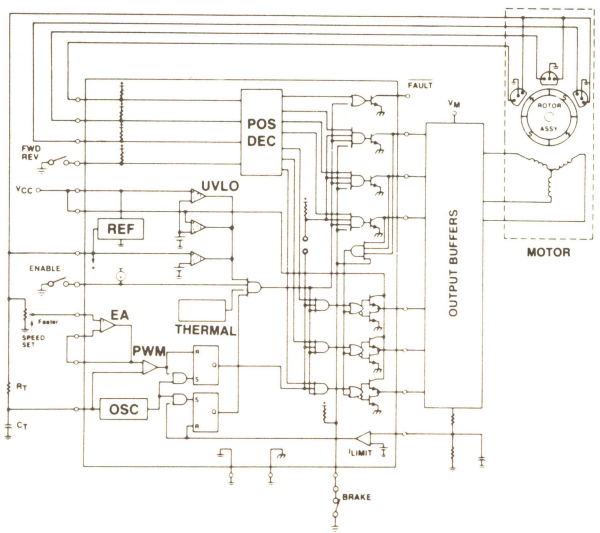
A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.




## DC Brushless Motor Controller

**MC33034P60,P120** — $T_A$ = −40° to +85°C, Case 724

The MC33034 Series is a high performance monolithic brushless motor controller containing all of the active functions required to implement a full featured open-loop three or four phase motor control system. These devices consist of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.





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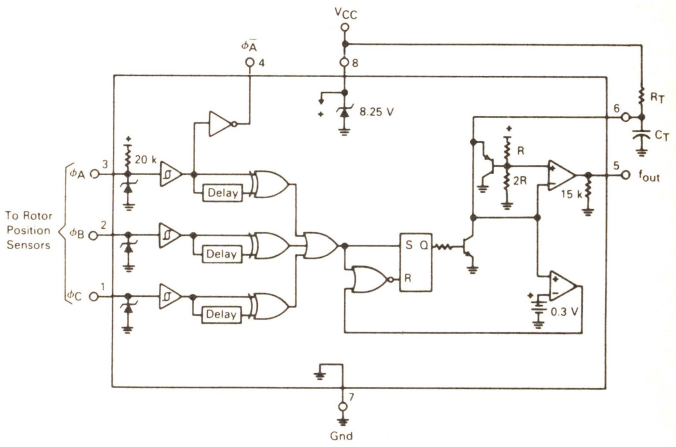
## Closed-Loop Brushless Motor Adapter

**MC33039P** — $T_A$ = −40° to +85°C, Case 626

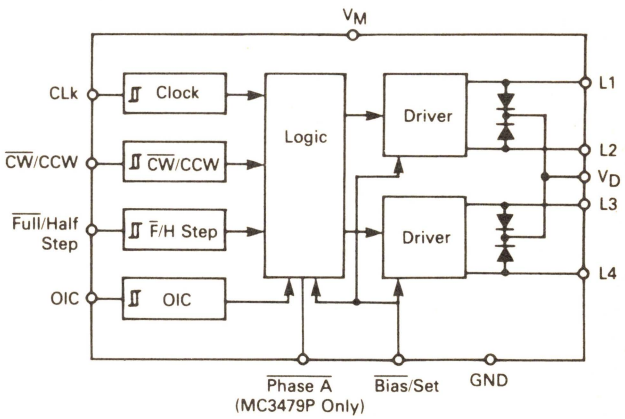
The MC33039P is a high performance closed-loop speed control adapter specifically designed for use in dc brushless motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33034 brushless motor controller, it can be used cost effectively in many other closed-loop speed control applications.




## Stepper Motor Drivers

**MC3479P** — $T_A$ = 0° to +70°C, Case 648C
**SAA1042,A** — $T_A$ = 0° to +70°C, Case 721

Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. MC3479P has added Output Impedance Control (OIC) and Phase A drive state indicator (not available on SAA1042 devices).



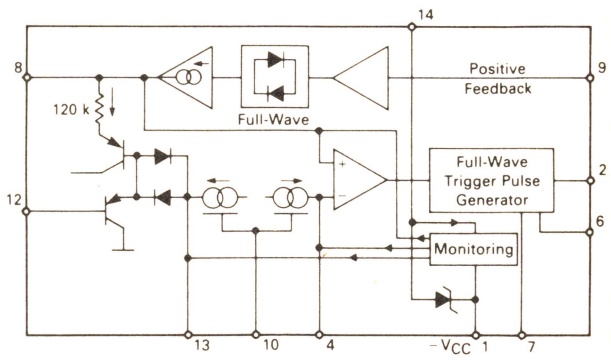

## Triac Phase Angle Controller

**TDA1185A** $T_A$ = 0° to +70°C, Case 646

. . . generates controlled triac triggering pulses and allows tacholess speed stabilization of universal motors by an integrated positive feedback function.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA

**TDA1185A**

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# Universal Motor Speed Controllers

**TDA1085A** $T_A$ = 0° to +70°C, Case 648

. . . all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Facility for defining the initial speed/time characteristic. The circuits provide a phase angle varied trigger pulse to the motor control triac

- Guaranteed Full Wave Triac Drive
- Soft Start from Power-up
- On-Chip Frequency/Voltage Converter and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line

**TDA1085C** $T_A$ = −10° to +120°C, Case 648

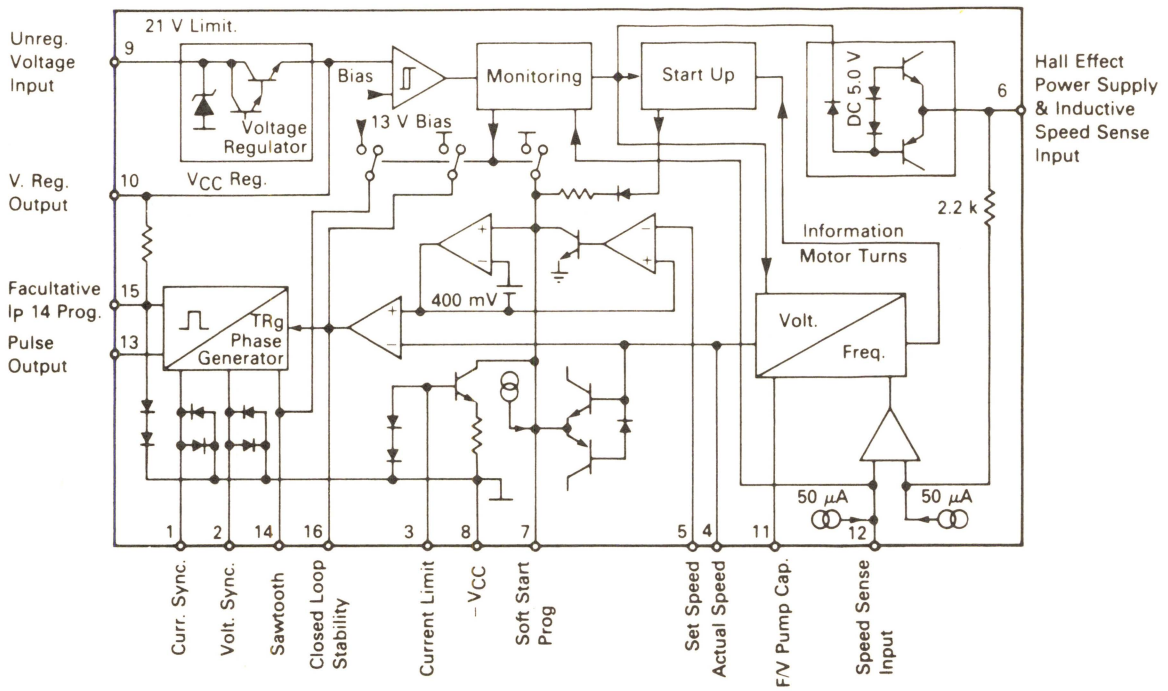
Similar to TDA1085A, but designed for commercial washing machine service.

**TDA1285A** $T_A$ = 0° to +70°C, Case 648

Similar to TDA1085A, plus:

- Repeated Trigger Pulse if Triac Fails to Latch
- Over 65 mA Output Pulse Current
- Automatic Adaptation to Inductive or Hall Effect Sensors
- Sensor Circuit Continuity Detection

**TDA1285A**

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# Data Conversion

The line of data conversion products which Motorola offers spans a wide spectrum of speed and resolution/accuracy. Features, including bus compatibility, minimize external parts count and provide easy interface to microprocessor systems. Various technologies, such as Bipolar and CMOS, are utilized to achieve functional capability, accuracy and production repeatability. Bipolar technology generally results in higher speed, while CMOS devices offer greatly reduced power consumption.

## A-D Converters

### CMOS

| Resolution (Bits) | Device | Nonlinearity (Max) | Conversion Time | Input Voltage Range | Supplies (V) | Temperature Range | Package | Comments |
|---|---|---|---|---|---|---|---|---|
| 8 | MC145040 | ±1/2 LSB | 10 μs | 0 to $V_{DD}$ | +5.0, ±10% | −55°C to +125°C<br>−40°C to +85°C | L/732<br>P/738<br>FN/775 | Requires External Clock |
| | MC145041 | | 20 μs | | | | | Includes Internal Clock |
| | MC14442 | | 32 μs | | | −40°C to +85°C | L/733<br>P/710 | μP Compatible 11-Channel MUX S.A.R. |
| | MC14549B<br>MC14559B | successive approximation registers | | | +3.0 to +18 | −55°C to +125°C<br>−40°C to +85°C | L/620<br>P/648 | Compatible with MC1408 S.A.R. 8-bit D-A Converter |
| 8–10 | MC14443/47 | ±0.5% Full Scale | 300 μs | Variable w/Supply | +5.0 to +18 | −40°C to +85°C | L/620<br>P/648 | μP Compatible, Single Slope, 6-Channel MUX |
| 3-1/2 Digit | MC14433 | ±0.05%<br>±1 Count | 40 ms | ±2.0 V<br>±200 mV | +5.0, +8.0 | | L/623<br>P/709 | Dual Slope |

### Bipolar

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 7 | MC10321 | ±1/2 LSB | 40 ns | 0 to 2.0 $V_{p-p}$ Max | +5.0 V and −3.0 V to −6.0 V | 0°C to +70°C | P/738<br>DW/751D | Video Speed, Grey Code |
| 8 | MC10319 | ±1 LSB | | | | | L/623<br>P/709<br>DW/751F<br>Die Form | Video Speed Flash Converter, Internal Grey Code |
| | MC6108 | ±1/2 LSB | 1.8 μs | ±5.0 V<br>0 to 5.0 V<br>0 to 10 V | +5.0, −5.2 | | P/710 | μP Compatible, Three-State Outputs, includes Reference |

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# D-A Converters

## CMOS

| Resolution (Bits) | Device | Suffix | Accuracy @ 25°C (Max) | Max Settling Time (±1/2 LSB) | Supplies (V) | Temperature Range | Package | Comments |
|---|---|---|---|---|---|---|---|---|
| 6 | MC144110 | P | — | — | +5.0 to +15 | 0°C to +85°C | 707 | Serial input, Hex DAC, 6 outputs |
| | MC144111 | P | | | | | 646 | Serial input, Quad DAC, 4 outputs |

## Bipolar

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 8 | DAC-08 | Q | ±1/2 LSB | 150 ns | ±4.5 to ±18 | −55°C to +125°C | 620 | High-Speed Multiplying |
| | | AQ | ±1/4 LSB | 135 ns | | | | |
| | | C | ±1 LSB | 150 ns | | 0°C to +70°C | 620 | |
| | | E | ±1/2 LSB | | | | 648 | |
| | | H | ±1/4 LSB | 135 ns | | | D/751B | |
| | MC1408 | L6/P6 | ±2 LSB | 300 ns Typ | +5.0, −5.0 to −15 | 0°C to +75°C | 620 | Multiplying |
| | | L7/P7 | ±1 LSB | | | | 648 | |
| | | L8/P8 | ±1/2 LSB | | | | | |
| | MC1508 | L8 | | | | −55°C to +125°C | 620 | |
| | MC10318 | CL6 | ±2 LSB | 10 ns Typ | −5.2 | 0°C to +70°C | 620 | ECL input Logic Levels Video Applications |
| | | CL7 | ±1 LSB | | | | | |
| | | L | ±1/2 LSB | | | | 690 | |
| | | L9 | ±1/4 LSB | | | | | |
| 4 x 3 | MC10320 | L | | 3 ns | +5.0, or ±5.0 | | 733 | 125 MHz Color Graphics Triple DAC |

# A-D/D-A Converters

## CMOS — For Telecommunications

| Resolution (Bits) | Device | Monotonicity (Bits) | Conversion Time | Input Voltage Range | Supplies (V) | Temperature Range | Package | Comments |
|---|---|---|---|---|---|---|---|---|
| 13 | MC145402 | 13 | 31.25 μs | ±3.28 V peak | ±5.0 to 6.0 | −40°C to +85°C | L/620 | Digital signal processing (e.g., echo cancelling, high-speed modems, phone systems with conferencing) |

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# Communication Circuits

## RF Communications

### Narrowband Dual Conversion Receivers — FM/FSK — VHF

| Type | $V_{CC}$ | $I_{CC}$ | Sensitivity | RF Input (Max) | IF1 (Max) | IF2 (limiter in) | Mute | RSSI | Max Data Rate | Notes | Package | Case Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MC3362 | 2–7 V | 3 mA | <1 μV | 180 MHz | 10.7 MHz | 455 kHz | — | √ | 35 kb | Includes buffered VCO output | 24 Pin DIP, SOIC | P/724 DW/751E |
| MC3363 | 2–7 V | 4 mA | <1 μV | 180 MHz | 10.7 MHz | 455 kHz | √ | √ | 35 kb | Includes RF amp transistor | 28 Pin SOIC | DW/751F |
| MC3364 | 2–7 V | 4 mA | <1 μV | 180 MHz | 10.7 MHz | 455 kHz | √ | √ | 35 kb | Includes buffered VCO output | 28 Pin SOIC | DW/751F |

### AM Receiver Medium/Short Wave

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MC13041 | 6.5–16.5 V | 25 mA | 6 μV | 10 MHz | 455 kHz | — | — | √ | — | Includes scan stop | 20 Pin DIP | P/738 DW/751D |

### Wideband Data (FM/FSK) Receivers — VHF

| Type | $V_{CC}$ | $I_{CC}$ | Sensitivity | IF1 (Max) | IF2 (limiter in) | Mute | RSSI | Max Data Rate | Notes | Package | Case Suffix |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MC3356 | 3–9 V | 25 mA | 30 μV | 200 MHz | 10.7 MHz | √ | √ | 500 kb | Includes front end mixer/L.O. | 20 Pin DIP/PLCC | P/738 FN/775 |

### Narrowband IF's — FM/FSK

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MC3357 | 4–8 V | 5 mA | 5 μV | 45 MHz | 455 kHz | √ | — | — | | 16 Pin DIP/SOIC | P/648 D/751B |
| MC3359 | 4–9 V | 7 mA | 2 μV | 45 MHz | 455 kHz | √ | — | — | | 18 Pin DIP/SOIC | P/707 DW/751C |
| MC3361 | 2–8 V | 6 mA | 2 μV | 60 MHz | 455 kHz | √ | — | — | | 16 Pin DIP/SOIC | P/648 D/751B |
| MC3367 | 1–5 V | 1 mA | <1 μV | 75 MHz | 455 kHz | √ | — | 35 kb | 1 Cell Operation | 28 Pin SOIC | DW/751F |
| MC3371 | 2–8 V | 6 mA | 2 μV | 60 MHz | 455 kHz | √ | √ | — | (1Q88 Intro) | 16 Pin DIP/SOIC | P/648 D/751B |
| MC13055 | 3–12 V | 25 mA | 20 μV | — | 40 MHz | √ | √ | 2 Mb | | 16 Pin DIP/SOIC | P/648 D/751B |

### Transmitters — FM/FSK

| Type | $V_{CC}$ | $I_{CC}$ | $P_{out}$ | Max RF Freq. Out | Battery Check | Tone OSC | Max Med. Freq. | Notes | Package | Case Suffix |
|---|---|---|---|---|---|---|---|---|---|---|
| MC2831A | 3–8 Vdc | 5 mA | −30 dBm | 50 MHz | √ | √ | 50 kHz | | 16 Pin DIP/SOIC | P/648 D/751B |
| MC2833 | 3–8 Vdc | 3 mA | −30 dBm | 150 MHz | — | — | 50 kHz | Includes two frequency multiplier transistors — (4Q87) | 16 Pin DIP/SOIC | P/648 D/751B |

### Balanced Modulator/Demodulator

| Type | $V_{CC}$ | $I_{CC}$ | Function | Package | Case Suffix |
|---|---|---|---|---|---|
| MC1596 | 5–30 V | 10 mA | Carrier Balance >50 dB General purpose balanced modulator/ demodulator for AM, SSB, FM Detection | 10 Pin Metal | G/603 |
| MC1496 | 5–30 V | 10 mA | | 14 Pin Ceramic DIL, DIP, SOIC | L/632 P/646 D/751A |

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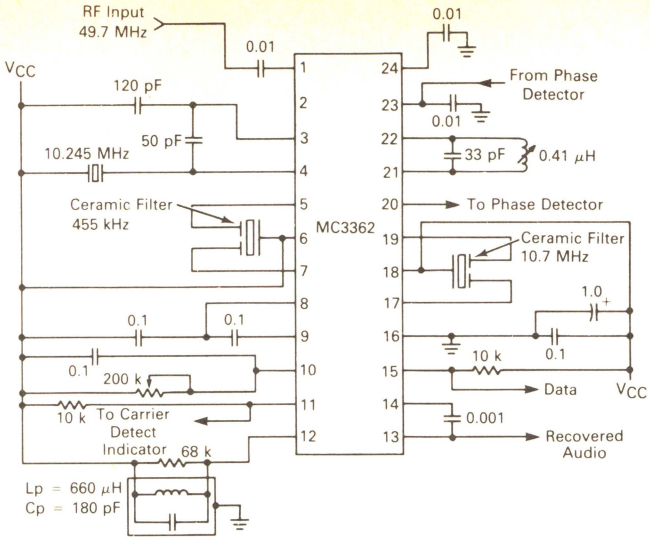
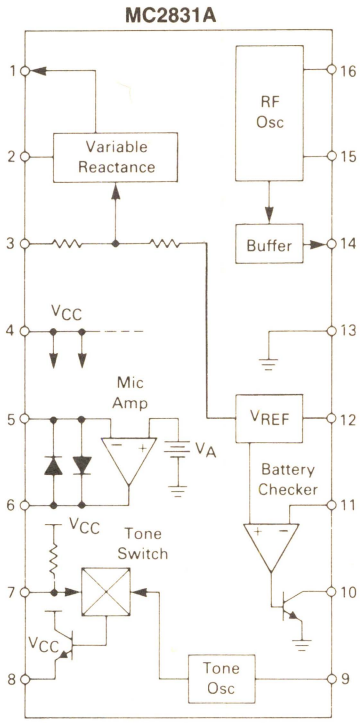
# MOSAIC® 1.5 VHF Narrowband Dual-Conversion Receivers

**MC3362/MC3363** — $T_A$ = −40°C to +85°C, Case 724, 751A

- Operation to 180 MHz
- 2–8 V dc Supply
- >1 μV for 20 dB Quieting Sensitivity
- Analog and Data Modulation Recovery
- >60 dB Dynamic Range RSSI
- Crystal or VCO First L.O. Operation
- On-Chip RF Amp/MC3363




# Low Power FM Transmitter System

**MC2831A** — $T_A$ = −30° to +75°C, Case 648, 751B

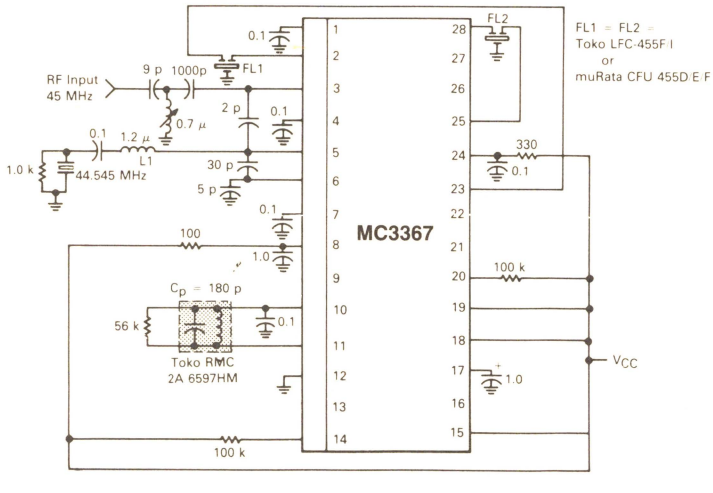
- Complete VHF FM Transmitter/Exciter
- Mike Preamp with Limiting
- Tone Generator for CTSS or AFSK
- Crystal or L-C VCO Operation
- Buffer/Multiplier Output Stage
- Low Voltage (internal reference) Warning Circuit
- Easily Partitioned for Semicustom Applications

# Low Voltage FM Narrowband Receiver

**MC3367** — $T_A$ = 0°C to +70°C, Case 751F

- Single Cell Operation to 0.9 $V_{CC}$
- Single Conversion Operation to 75 MHz
- Current Drain of 1 mA
- Split I.F. Amplifier for Single or Dual Filters
- Analog and Data Outputs
- Sensitivity of 0.7 μV Typ for 20 dB Quieting
- Low Battery Voltage Indicator

(All capacitors in μF unless otherwise stated. Resistors in ohms. Inductors in Henries.)

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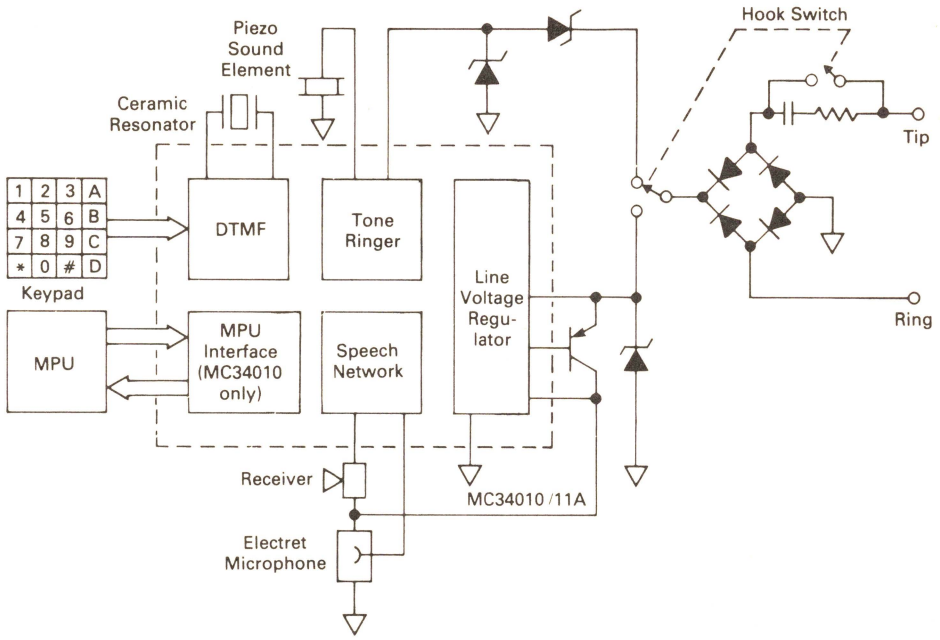
# Electronic Telephone

## The Complete Electronic Telephone Circuit

**MC34010/11A** — $T_A$ = −20° to +60°C, Case 711, 777




The conventional transformer-driven telephone handset is undergoing major innovations. The bulky transformer is disappearing. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2-to-4 wire conversion, DTMF dialing, tone ringing, and a variety of related activities.

The culmination of these capabilities is the Electronic Telephone Circuit, the MC34010/11A. These IC's place all of the above mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar linear ($I^2L$) technology and provide all the necessary elements of a modern tone-dialing telephone. The MC34010 even incorporates an MPU interface circuit for the inclusion of automatic dialing in the final system.

### Features

- Provides All Basic Telephone Functions, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA-470 Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- $I^2L$ Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- MC34010P Provides Microprocessor Interface Port for Automatic Dialing Features





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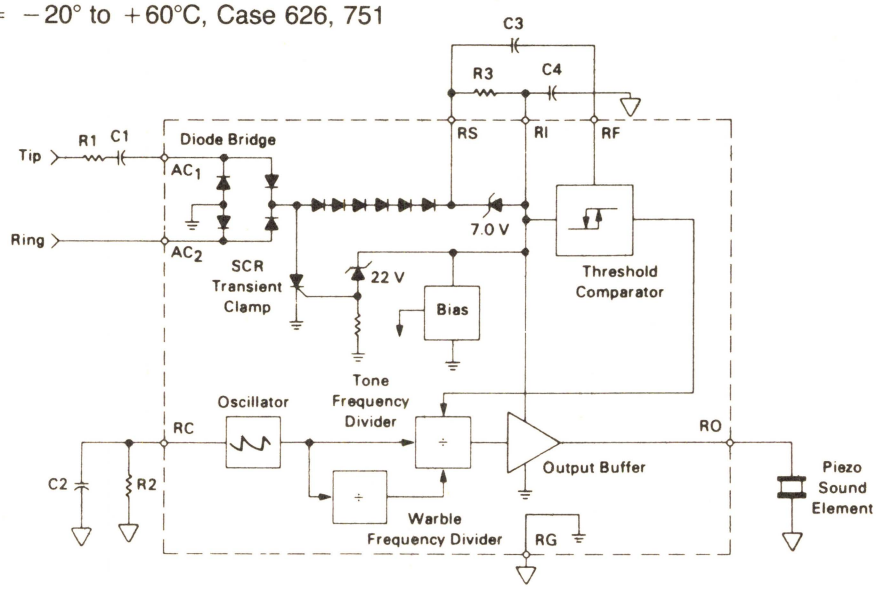
# Tone Ringers

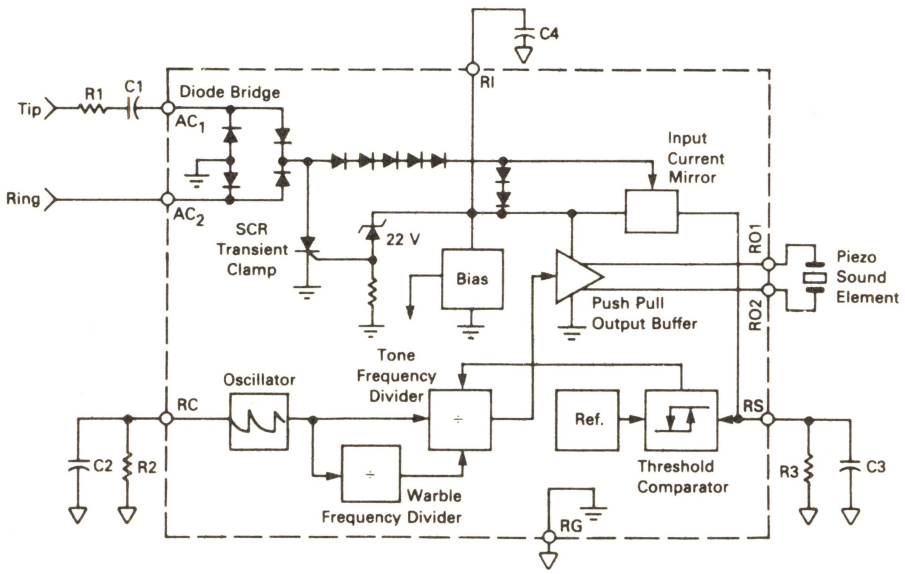
The MC34012 and MC34017 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are on the line. The MC34012 series and the MC34017 series were designed to meet those requirements.

**MC34012** — $T_A$ = −20° to +60°C, Case 626, 751




- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options — MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Push Pull Output Stage for Greater Output Power Capability (MC34017)
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

**MC34017** — $T_A$ = −20° to +60°C, Case 626, 751

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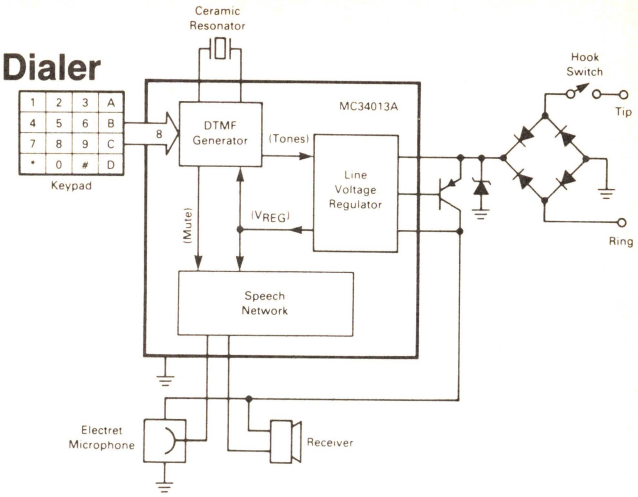
## Telephone Speech Network and Tone Dialer

**MC34013A** — $T_A$ = −20° to +60°C, Case 710,776

- Linear/$I^2L$ Technology Provides Low 1.4 Volt Operation in Both Speech and Dialing Modes
- Speech Network Provides 2–4 Wire Conversion with Adjustable Sidetone Utilizing an Electret Microphone
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- Dialer Mutes Speech Network with Internal Delay for Click Suppression on DTMF Key Release

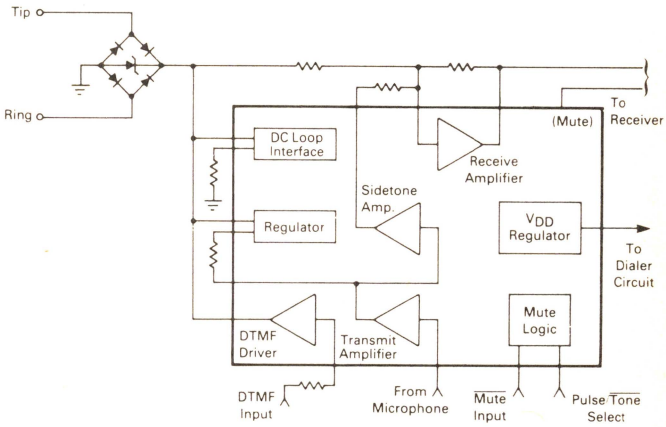



## Speech Network with Dialer Interface

**MC34014** — $T_A$ = −20° to +60°C, Case 707, 775

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, line interface circuit, dialer interface, and a regulated output voltage for a dialer circuit. It includes an equalization circuit to compensate for various line lengths and the conversion from 2-to-4 wire is accomplished with supply voltages as low as 1.5 volts.

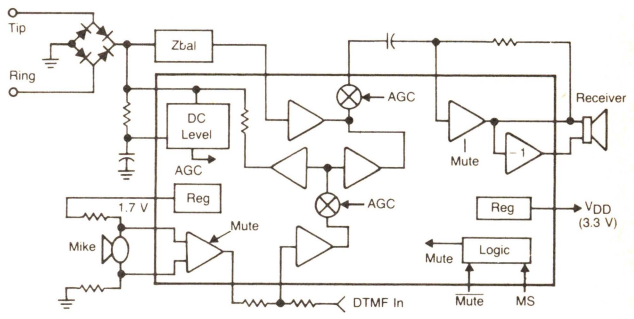
- Transmit, Receive, and Sidetone Gains Set By External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 Volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher




## Telephone Speech Network with Dialer Interface

**MC34114** — $T_A$ = −20° to +70°C, Case 707, 751D

- Operation Down to 1.2 Volts
- Externally Adjustable Transmit, Receive, and Sidetone Gains
- Differential Microphone Amplifier Input Minimizes RFI
- Transmit, Receive, and Sidetone Equalization on both Voice and DTMF Signals
- Regulated 1.7 Volts Output for Biasing Microphone
- Regulated 3.3 Volts Output for Powering External Dialer
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 150 Ω and Higher
- MC34114 Complies with Bell Telephone and BT Standards





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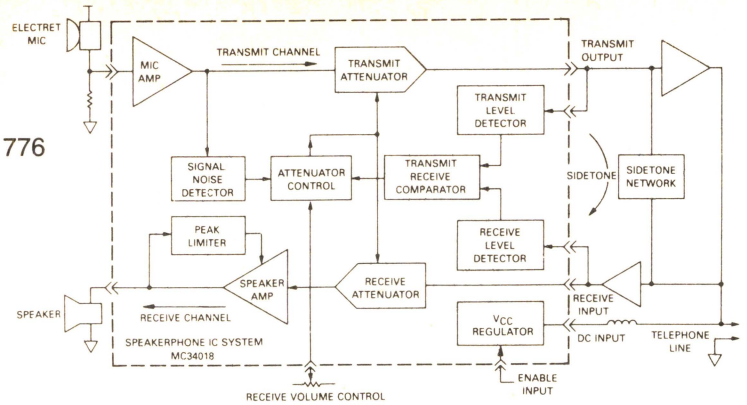
## Voice Switched Speakerphone Circuit

**MC34018** — $T_A$ = −20° to +60°C, Case 710, 776

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.




- All Necessary Level Detection and Attenuation Controls for a Hands-Free Telephone in a Single Integrated Circuit
- Background Noise Level Monitoring with Long Time Constant
- Wide Operating Dynamic Range Through Signal Compression
- On-chip Supply and Reference Voltage Regulation
- Typical 100 mW Output Power (into 25 Ω) with Peak Limiting to Minimize Distortion
- Chip Select Pin for Active/Standby Operation
- Linear Volume Control Function

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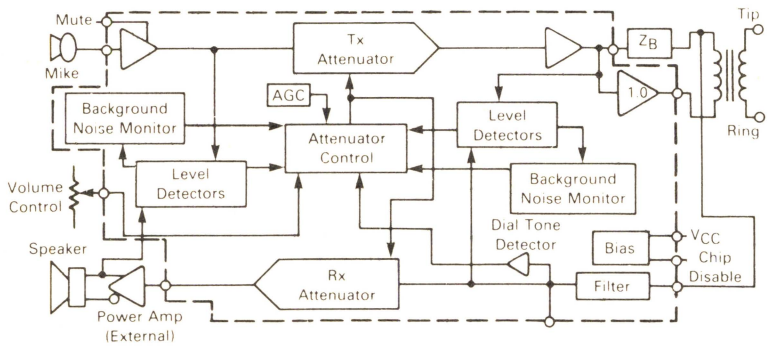
## Voice Switched Speakerphone Circuit

**MC34118** — $T_A$ = −20° to +60°C, Case 710, 751F

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.




- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0–6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Compatible with MC34119 Speaker Amplifier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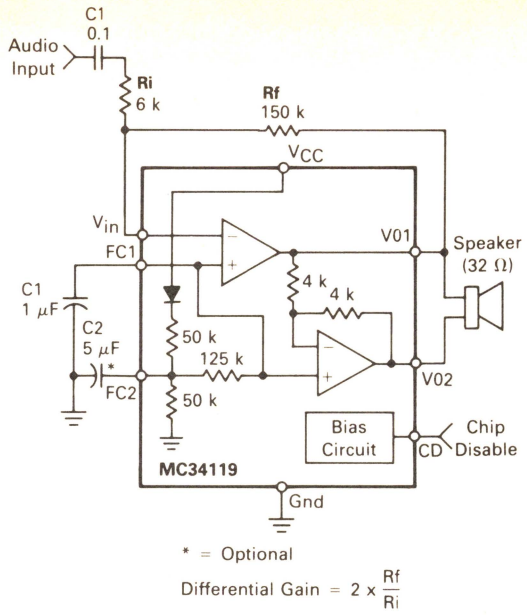
## Audio Amplifier

**MC34119** — $T_A$ = 0° to +70°C, Case 626, 751

A low power audio amplifier circuit intended (primarily) for telephone applications, such as speakerphones. Provides differential speaker outputs to maximize output swing at low supply voltages (2 volt min.). Coupling capacitors to the speaker, and snubbers, are not required. Overall gain is externally adjustable from 0 to 46 dB. A Chip Disable pin permits powering-down to mute the audio signal and reduce power consumption.

- Drives a Wide Range of Speaker Loads (16–100 Ω)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Distortion (THD = 0.4% Typical)
- Wide Operating Supply Voltage (2–16 Volts) — Allows Telephone Line Powered Applications.
- Low Quiescent Supply Current (2.5 mA Typical)
- Low Power-Down Quiescent Current (60 μA Typical)




## Current Mode Switching Regulator

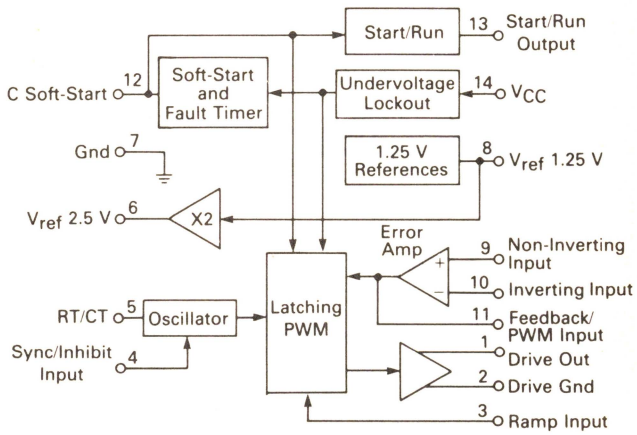
**MC34129** — $T_A$ = 0° to +70°C, Case 646, 751A

High performance current mode switching regulator for low-power digital telephones. Unique internal fault timer provides automatic restart for overload recovery. A start/run comparator is included to implement bootstrapped operation of $V_{CC}$.

Although primarily intended for digital telephone systems, these devices can be used cost effectively in many other applications.

On-chip functions and features include:

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Latched-Off or Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- Input Undervoltage Lockout

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# Consumer Electronic Circuits

## Entertainment Radio Receiver Circuits

### C-QUAM® AM Stereo Decoders

| Function | Features | Suffix/Case | Device |
|---|---|---|---|
| Basic AM Stereo Decoder | Monaural/Stereo AM Detector, Indicator, 6–10 V Operation | P/738 | MC13020 |
| Advanced AM Stereo Decoder | Medium Voltage 2–8 V, Decoder and IF Amp | DW/751F | MC13022 |
| AM Stereo Personal Radio | Complete Low Voltage AM Stereo Receiver | P/724 | MC13024 |
| Tuning Stabilizer | Companion for MC13020 for Manual Tuned Receivers | P/648 | MC13021 |
| AM Broadcast Receiver | AM Receiver Subsystem — Ideal Companion for MC13020 | P/738 | MC13041 |

### FM Stereo Decoder

| Function | Channel Separation dB Typ | THD % Typ | Stereo/Indicator Lamp Driver mA Max | Features | Suffix/Case | Device |
|---|---|---|---|---|---|---|
| FM Multiplex Stereo Decoder | 62 | 0.1 | 100 | Low Signal Blend for Noise Reduction | —/648 | TCA4500A |

### Audio Amplifiers

| Function | $P_O$ Watts | $V_{CC}$ Vdc Max | $V_{in}$ @ rated $P_O$ mV Typ | $I_D$ mA Typ | $R_L$ Ohms | Suffix/Case | Type |
|---|---|---|---|---|---|---|---|
| Mini Watt SOIC Audio Amp | 1.0 W | 35 | 80 | 11 | 16 | D/751 | MC13060 |
| Low Power Audio Amp | 400 mW | 16 | — | 2.5 mA | 8–100 | D/751<br>P/626 | MC34119 |

### Audio Attenuators/Controls

| Function | $V_{CC}$ Range Vdc | THD % | Tone Control Range dB Typ | Attenuation Range dB Typ | Suffix/Case | Device |
|---|---|---|---|---|---|---|
| Electronic Attenuator | 9.0–18 | 0.6 Typ | — | 90 | P/626 | MC3340P |
| Stereo, Volume, Bass, Treble, Balance | 8.5–18 | 0.1 Typ | ±14 | 80 | P/707 | TCA5550 |
| Stereo, Volume, Bass, Treble, Balance | 3–18 | 0.5 Max | ±15 | 80 | P/707 | TDA1524 |





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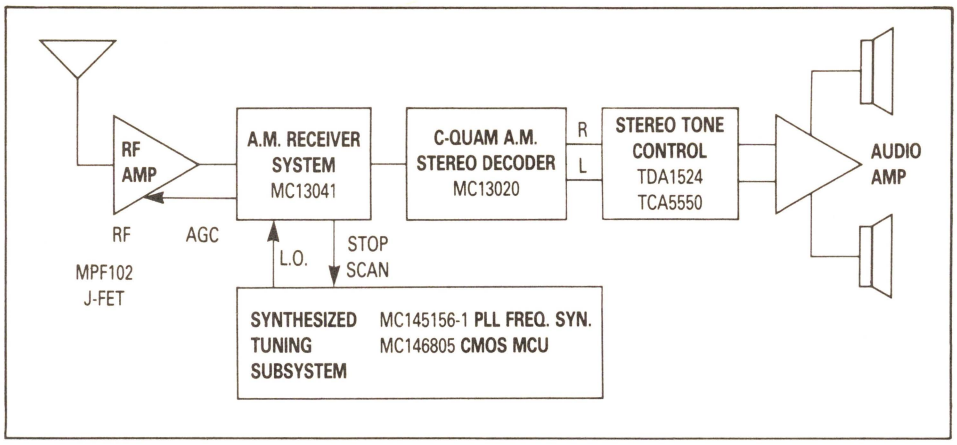


When AM stereo broadcasting was sanctioned by the F.C.C. in 1982, there were five different systems vying for user approval. Since then C-QUAM® has become the defacto standard in the U.S.A., as the market and broadcasters recognize its performance advantages. It is the legal standard in Canada, Australia and Brazil where A.M. is the dominant radio medium. C-QUAM is available from nearly 50 automobile radio makers and a dozen home receiver builders (for as little as $60 in a basic tuner).

Based on the field-proven C-Quam performance, Motorola has developed a low-cost, high performance C-Quam AM Stereo Decoder chip, with fully compatible, no-compromise mono performance, as the basis for both broadcast and receiving equipment. Additional IC components from Motorola's inventory offer a single supply source for state-of-the-art radio receiver designs. New products cover virtually every type of receiver — home, auto, and personal portable.

# Radio Circuits (See Communications Section)

# Video Circuits

## Modulators

| Function | Features | Suffix/Case | Device |
|---|---|---|---|
| Color TV Video Modulator | Chroma Oscillator and Clock Driver, Lead and Lag Network, Chroma Modulator, RF Oscillator, and Modulator | P/646 | MC1372 |
| | RF Oscillator and Modulator | P/626 | MC1373 |
| TV Modulator (Hi Quality) | RF Oscillator/Modulator, and FM Sound Oscillator/Modulator | P/646 | MC1374 |
| Video RGB to PAL/NTSC Encoder | RGB and Sync Inputs, Composite Video Out — PAL/NTSC Switch Selectable | P/738 | MC1377 |
| Video Synchronizer | Complete Color TV Video Overlay Synchronizer | P/711 | MC1378 |

## Demodulators

| | | | |
|---|---|---|---|
| Color Processor | PAL/NTSC Input, RGB Output, also RGB Inputs, Plus Fast Blanking Input. Ideal for Text, Graphics, Overlays | P/711 | TDA3301 TDA3303 |
| Color Processor | PAL/NTSC Input, RGB Outputs, On-Chip Hue Control | P/724 | TDA3330 |
| Color Processor | PAL/NTSC Input, Color Difference Outputs On-Chip Hue Control | P/707 | TDA3333 |
| Video Line Driver — RGB | 3 Line Video Amp — RGB — Sync on Green | P/648C | MC1379 |

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## Tuning System

| Function | Features | Suffix/Case | Device |
|---|---|---|---|
| Remote Control Amplifier | Infrared Diode Signal Amplifier Shaper | P/626 | MC3373 |
| PLL-Tuning Circuit | TV Tuning System — Prescaler — M-Bus Control | DW/751C | μAA4802 |

## Deflection

| | | | |
|---|---|---|---|
| Horizontal Processor | Linear Balanced Phase Detector, Oscillator and Predriver, Adjustable dc Loop Gain, Adjustable Duty Cycle | P/626 | MC1391 |

## Sound

| | | | |
|---|---|---|---|
| Sound IF Detector, dc Volume Control, Preamplifier | 30 μV, 3.0 dB Limiting, Excellent AMR | —/646 | TBA120C |
| Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier | Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; $V_{CC}$ = 24 V; $R_L$ = 16 Ω | P/648C | TDA3190 |
| | 750 mW Output | P/648C | TDA1190 |
| Stereo Sound Control System | Stereo Balance, Volume, Bass, Treble Control | P/707 | TCA5550 |

## Transistor Arrays

| Function | $I_{C(max)}$ mA | $V_{CEO}$ Volts Max | $V_{CBO}$ Volts Max | $V_{EBO}$ Volts Max | Suffix/Case | Device |
|---|---|---|---|---|---|---|
| One Differentially Connected Pair and Three Isolated Transistors | 50 | 15 | 20 | 5.0 | P/646 D/751A | MC3346 |
| Dual Independent Differential Amplifiers with Associated Constant Current Transistors | 50 | 15 | 20 | 5.0 | P/646 | CA3054 |

## Television Subsystems

| Function | Features | Suffix/Case | Device |
|---|---|---|---|
| MONOMAX — 1-Chip Black and White TV Subsystem | Video IF, Detector, AGC, Video Amplifier, Horizontal Processor, Vertical Processor, and Sync For 525 Line Systems | P/710 | MC13001X |
| | Same as Above Except For 625 Line Systems | P/710 | MC13002X |
| Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier, Power Amplifier | Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; $V_{CC}$ = 24 V; $R_L$ = 16 Ω | P/648C | TDA3190 |
| | Same as TDA1190Z Except for 750 mW Output | P/648C | TDA1190 |
| MONOMAX Audio/Vertical Output | High Level 750 mW Audio Output — Vertical Yoke Driver | P/648C | MC13014 |

## Video IF Amplifiers

| Function | Features | Suffix/Case | Device |
|---|---|---|---|
| 1st and 2nd Video IF Amplifier | IF Gain @ 45 MHz = 60 dB typ, AGC Range = 70 dB Min | P/626 | MC1349 |
| | IF Gain @ 45 MHz = 50 dB typ, AGC Range = 60 dB min | P/626 | MC1350 |
| 1st and 2nd Video IF, AGC Keyer and Amplifier | IF Gain @ 45 MHz = 53 dB typ, AGC Range = 75 dB min, "Forward AGC" Provided for Tuner | P/646 | MC1352 |
| 3rd IF, Video Detector, Video Buffer, and AFC Buffer | Low-Level Detection, Low Harmonic Generation, Zero Signal dc Output Voltage of 7.0 to 8.2 V | P/626 | MC1330A1P |
| | Same as MC1330A1 Except Zero Signal dc Output Voltage of 7.8 to 9.0 V | P/626 | MC1330A2P |
| SAW Preamp, IF Amplifier, Detector, AGC, AFC | Complete Video IF or Parallel Sound IF System Complete AFT System with Simple Quadrature Detector | P/707 | MC13010P |
| Advanced Video IF | Complete Video/Audio IF System for High Performance Analog TV Receivers | DW/751F | MC13011 |





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# Interface Circuits

## Memory Interface and Control

Motorola's line of circuits in this category have well established industry standards for reading and writing in a floppy disk system. The write circuits are designed for both straddle erase and tunnel erase heads, and provide both the writing and erasing functions. The read circuits include all the circuitry for peak detection, filtering, wave shaping, and guaranteed peak shift specifications.

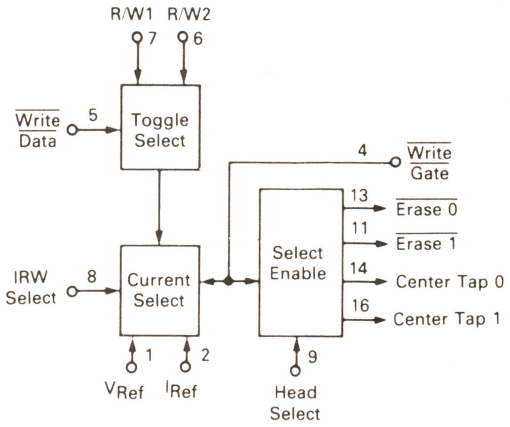
### Floppy Disk Write Controllers

#### Straddle Erase Controller

**MC3469P** — $T_A$ = 0° to +70°C, Case 648

Designed to provide the entire interface between floppy disk heads and the head control and write data signals for straddle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

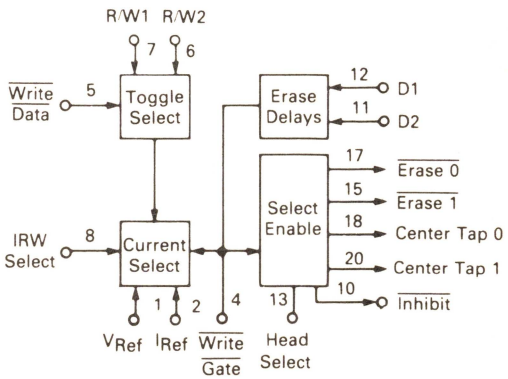



#### Tunnel/Straddle Erase Controller

**MC3471P** — $T_A$ = 0° to +70°C, Case 738

Provides the entire interface between the write data and head control signals and the heads (write and erase) for either tunnel or straddle-erase floppy disk systems.

Has provisions for external adjustment of degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.

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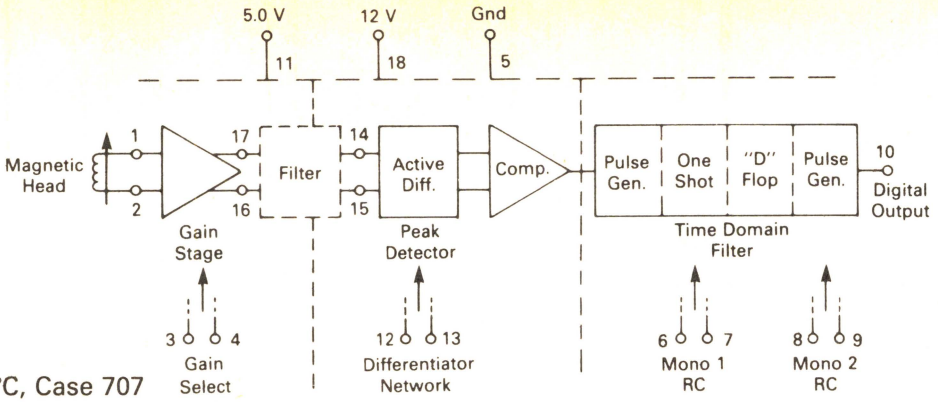
# Floppy Disk Read Amplifier System




**MC3470,A** — $T_A$ = 0° to +70°C, Case 707

Designed as monolithic Read Amplifier System for obtaining digital information from floppy disk storage. These devices accept differential ac signals produced by the magnetic head and provides a digital output pulse that corresponds to each peak of the input signal. A gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output. These devices provide all the active circuitry to perform the floppy disk Read amplifier function, and guarantee to have a maxximum peak shift of 5.0%, adjustable to zero, for the MC3470P and 2.0%, adjustable to zero, for the MC3470AP.

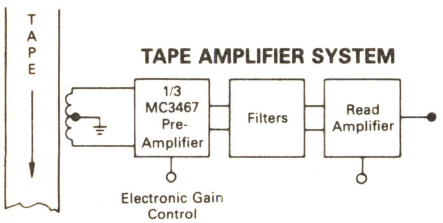
| Device Number | Peak Shift (f = 250 kHz, $V_{ID}$ = 1.0 Vpp) | Differential Input Voltage Gain (f = 200 kHz, $V_{ID}$ = 5.0 mV [RMS]) | | Input Common Mode Range (5% Max THD) | |
|---|---|---|---|---|---|
| | | V/V | | V | |
| | % Max | Min | Max | Min | Max |
| MC3470 | 5.0 | 80 | 130 | −0.1 | 1.5 |
| MC3470A | 2.0 | 100 | 130 | | |

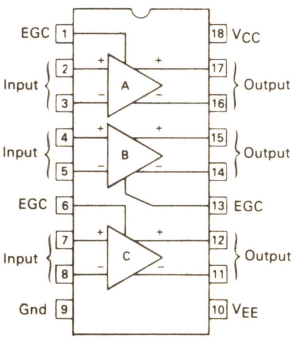
# Magnetic Tape Sense Amplifier

**MC3467L,P** — $T_A$ = 0° to +70°C, Case 726, 707

The MC3467 provides three independent preamplifiers with individual electronic gain control, optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V. Minimum small-signal bandwidth is 10 MHz, and Common-Mode Input Voltage range is 1.5 V min.



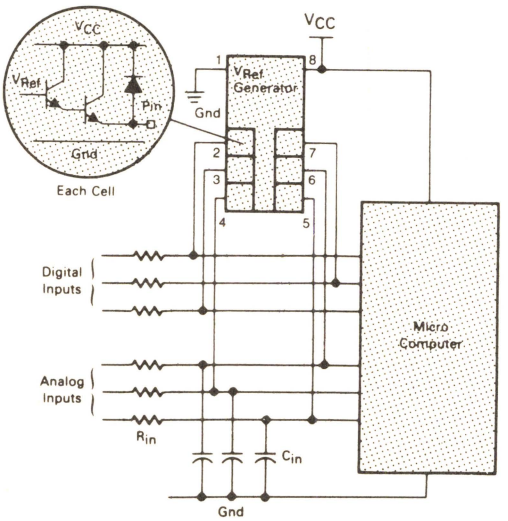




# Peripheral Clamping Array

**TCF6000P1,D** — $T_A$ = −40° to +85°C, Case 626, 751

. . . designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods

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# Microprocessor Bus Interface

Motorola offers a spectrum of line drivers and receivers which provide interfaces to many industry standard specifications. Many of the devices add key operational features, such as hysteresis, short circuit protection, clamp diode protection, or special control functions.

## Address and Control Bus Extenders

These devices are designed to extend the drive capabilities of today's standard microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

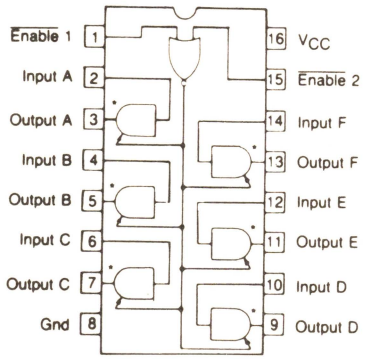
| $V_{OL(max)}$ @ 48 mA | $V_{OH(min)}$ @ −5.2 mA | Propagation Delay Max (ns) | Buffers Per Package | Device | Package | Comments |
|---|---|---|---|---|---|---|
| 0.5 | 2.4 | 13 | 6 | MC8T95/ MC6885 | L/620 P/648 | Non-Inverting |
| 0.5 | 2.4 | 11 | 6 | MC8T96/ MC6886 | L/620 P/648 | Inverting |
| 0.5 | 2.4 | 13 | 6 | MC8T97/ MC6887 | L/620 P/648 | Non-Inverting |
| 0.5 | 2.4 | 11 | 6 | MC8T98/ MC6888 | L/620 P/648 | Inverting |

### Hex 3-State Buffers/Inverters — $T_A$ = 0° to +75°C

These devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

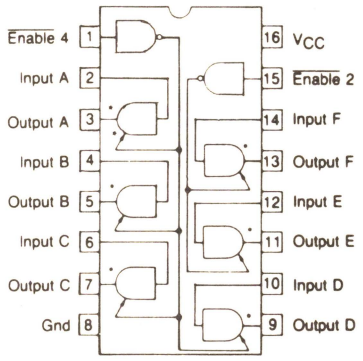
#These devices may be ordered by either of the paired numbers.

**MC8T95/MC6885#** — Noninverting
**MC8T96/MC6886#** — Inverting
Two-input Enable controls all six buffers




*Add inverter for MC6886/MC8T96.

**MC8T97/MC6887#** — Noninverting
**MC8T98/MC6888#** — Inverting
Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.




*Add inverter for MC6888/MC8T98.

## Microprocessor Data Bus Extenders

| Driver Characteristics | | Receiver Characteristics | | | | |
|---|---|---|---|---|---|---|
| Output Current (mA) | Propagation Delay Max (ns) | Propagation Delay Max (ns) | Transceivers Per Package | Device | Package/ Suffix | Comments |
| 48 | 14 | 14 | 4 | MC8T26A (MC6880A) | P/648 L/620 | Inverting Logic |
| 48 | 17 | 17 | 4 | MC8T28 (MC6889) | P/648 L/620 | Non-Inverting Logic |





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# Single-Ended Bus Transceivers

## For Instrumentation Bus, Meets GPIB/IEEE Standard 488

| Driver Characteristics | | Receiver Characteristics | | | | |
|---|---|---|---|---|---|---|
| Output Current (mA) | Propagation Delay Max (ns) | Propagation Delay Max (ns) | Transceivers Per Package | Device | Package/ Suffix | Comments |
| 48 | 50 | 50 | 4 | MC3446A | P/648 | MOS Compatible, Input Hysteresis |
| 48 | 30 | 50 | 8 | MC3447 | P3/724<br>L/623 | Input Hysteresis, Open Collector, 3-State Outputs with Terminations |
| 48 | 17 | 25 | 4 | MC3448A | P/648<br>L/620 | Input Hysteresis, Open Collector 3-State Outputs with Terminations |
| 100 | 30 | 30 | 4 | MC3440A | P/648 | Input Hysteresis, Enable for 3 Drivers |
| | | | | MC3441A | | Common Enable, Input Hysteresis |

## For High-Current Party-Line Bus for Industrial and Data Communications

| | | | | | | |
|---|---|---|---|---|---|---|
| 100 | 15 | 15 | 4 | MC26S10 | P/648<br>L/620 | Open Collector, Outputs, Common Enable |

# Line Receivers

## General-Purpose

| S = Single Ended<br>D = Differential | Type* Of Output | $t_{prop}$ Delay Time Max (ns) | Party-Line Operation | Strobe Or Enable | Power Supplies (V) | Device | Package/ Suffix | Receivers Per Package | Companion Drivers | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| D<br>D | TP<br>OC | 25<br>25 | Yes<br>Yes | Yes<br>Yes | ±5<br>±5 | MC3450<br>MC3452 | P/648<br>L/620 | 4<br>4 | MC3453 | Quad version of MC75107/8 |
| D<br>D | TP<br>OC | 25<br>25 | Yes<br>Yes | Yes<br>Yes | ±5<br>±5 | MC75107<br>MC75108 | P/646<br>L/632 | 2<br>2 | MC75S110 | Dual version of MC3450/2 |
| S | TP | 30 | Yes | Yes | +5 | MC3437 | P/648<br>L/620 | 6 | | Input Hysteresis |

## 360/370 I/O Interface

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S | TP | 30 | Yes | No | +5 | MC75125<br>MC75127 | P/648<br>L/620 | 7 | MC3481<br>MC3485 | Schottky Circuitry |
| S | TP | 30 | Yes | Yes | +5 | MC75128<br>MC75129 | P/738<br>L/732 | 8 | MC3481<br>MC3485 | Active high strobe<br>Active low strobe |

*OC = Open Collector, TP = Totem-pole output

## EIA Standard

| S = Single Ended<br>D = Differential | Type* Of Output | $t_{prop}$ Delay Time Max (ns) | Party-Line Operation | Strobe Or Enable | Power Supplies (V) | Device | Package/ Suffix | Receivers Per Package | Companion Drivers | EIA Standard |
|---|---|---|---|---|---|---|---|---|---|---|
| S | R | 85 | No | No | +5 | MC1489<br>MC1489A | P/646<br>L/632 | 4 | MC1488 | (RS-232)<br>EIA-232-D |
| S, D<br>S, D | TP<br>TP | 30<br>30 | Yes<br>Yes | Yes<br>Yes | +5<br>+5 | AM26LS32<br>MC3486 | P/648<br>L/620 | 4<br>4 | AM26LS31<br>MC3487 | (RS-422/423)<br>EIA-422/423 |
| S, D<br>S, D | TP<br>TP | 35<br>35 | Yes<br>Yes | Yes<br>Yes | +5<br>+5 | SN75173<br>SN75175 | N/648<br>J/620 | 4<br>4 | SN75172<br>SN75174 | (RS-422/423/485)<br>EIA-422/423/485 |

*R = Resistor Pull-up, TP = Totem-pole output



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# Line Drivers

## General Purpose

| Output Current Capability (mA) | $t_{prop}$ Delay Time Max (ns) | S = Single Ended D = Differential | Party-Line Operation | Strobe Or Enable | Power Supplies (V) | Device | Package/ Suffix | Drivers Per package | Companion Receivers | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 15 | D | Yes | Yes | ±5 | MC3453 | P/648<br>L/620 | 4 | MC3450<br>MC3452 | Quad version of MC75S110 |
| 15 | 15 | D | Yes | Yes | ±5 | MC75S110 | P/646<br>L/632 | 2 | MC75107<br>MC75108 | Dual version of MC3453 |

## 360/370 I/O Interface

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 60 | 45 | S | Yes | Yes | +5 | MC3481 | P/648<br>L/620 | 4 | MC75125<br>MC75127 | Short Circuit Fault Flag |
| 60 | 45 | S | Yes | Yes | +5 | MC3485 | P/648<br>L/620 | 4 | MC75128<br>MC75129 | Short Circuit Fault Flag |

## EIA Standard

| Output Current Capability (mA) | $t_{prop}$ Delay Time Max (ns) | S = Single Ended D = Differential | Party-Line Operation | Strobe Or Enable | Power Supplies (V) | Device | Package/ Suffix | Drivers Per Package | Companion Receivers | EIA Standard |
|---|---|---|---|---|---|---|---|---|---|---|
| 85<br>85 | 35<br>35 | D<br>D | Yes<br>Yes | Yes<br>Yes | +5<br>+5 | SN75172<br>SN75174 | N/648<br>J/620 | 4<br>4 | SN75173<br>SN75175 | (RS-485)<br>EIA-485 |
| 48 | 20 | D | Yes | Yes | +5 | MC3487 | P/648<br>L/620 | 4 | MC3486 | (RS-422) EIA-422 with 3-State Outputs |
| 48 | 20 | D | Yes | Yes | +5 | AM26LS31 | P/648<br>D/620 | 4 | AM26LS32 | |
| 20 | — | S | No | No | ±12 | MC3488A<br>(μA9636A) | P1/626<br>U/693 | 2 | MC3486<br>AM26L532 | (RS-423/232)<br>EIA-423/232-D |
| 10 | 350 | S | No | Yes | ±9 to<br>±12 | MC1488 | P/646<br>L/632 | 4 | MC1489<br>MC1489A | (RS-232)<br>EIA-232-D |

# Line Transceivers

| Driver Prop Delay (Max ns) | Receiver Prop Delay (Max ns) | CE = Common Enable<br>DE = Driver Enable<br>RE = Receiver Enable | Party Line Operation | Power Supply (V) | Device | Package/ Suffix | Drivers Per Package | Receivers Per Package | EIA Standard |
|---|---|---|---|---|---|---|---|---|---|
| 20 | 30 | DE, RE | Yes | +5 | MC34050 | L/620<br>P/648 | 2 | 2 | (RS-422)<br>EIA-422 |
| 20 | 30 | DE | Yes | +5 | MC34051 | L/620<br>P/648 | 2 | 2 | (RS-422)<br>EIA-422 |
| 22 | 35 | DE, RE | Yes | +5 | SN75176 | 626 | 1 | 1 | EIA-422/485 |
| 22 | 40 | CE | Yes | +5 | SN75177 | 626 | 1 | 1 | EIA-422/485 |
| 22 | 40 | CE | Yes | +5 | SN75178 | 626 | 1 | 1 | EIA-422/485 |





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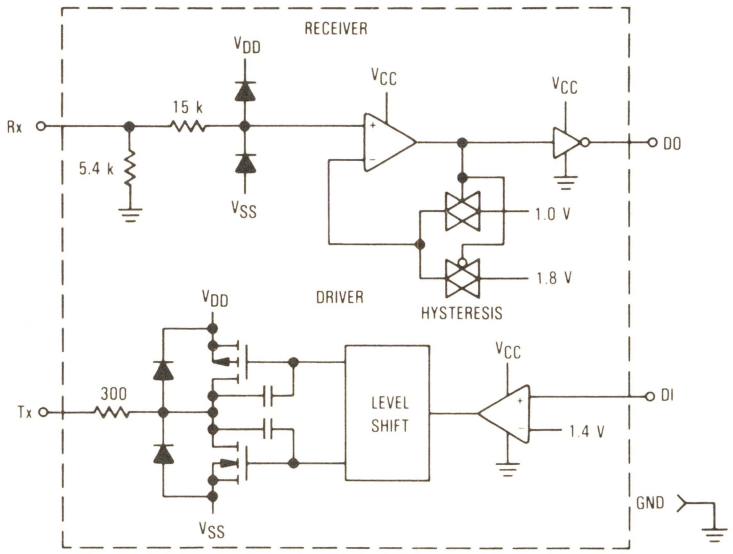
# EIA-232-D/V.28 Driver/Receiver

**MC145406L,P** — $T_A$ = −40° to +85°C, Case 620, 648

The MC145406 is a silicon-gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of EIA-232-D and CCITT V.28. Using ±12 volt supplies and a +5.0 volt supply, this 16-pin device consumes a maximum of 15 mW.




# Peripheral Drivers

| Output Current Capability (mA) | Input Capability | Propagation Delay Time Max (μs) | Output Clamp Diode | Off State Voltage Max (V) | Device | Drivers Per Package | Package/ Suffix | Logic Function |
|---|---|---|---|---|---|---|---|---|
| 300 | TTL, DTL | 1.0 | Yes | 70 | MC1472 | 2 | P1/626 U/693 | NAND |
| 500 | TTL, CMOS, PMOS | 1.0 | Yes | 50 | ULN2801 | 8 | A/707 | Invert |
| 500 | 14 V to 25 V PMOS | 1.0 | Yes | 50 | ULN2802 | 8 | A/707 | Invert |
| 500 | TTL, CMOS | 1.0 | Yes | 50 | ULN2803 | 8 | A/707 | Invert |
| 500 | 6.0 V to 15 V MOS | 1.0 | Yes | 50 | ULN2804 | 8 | A/707 | Invert |
| 500 | TTL, CMOS PMOS | 1.0 | Yes | 50 | MC1411 (ULN2001A) | 7 | P/648 | Invert |
| 500 | 14 V to 25 V PMOS | 1.0 | Yes | 50 | MC1412 (ULN2002A) | 7 | P/648 | Invert |
| 500 | TTL, 5.0 V CMOS | 1.0 | Yes | 50 | MC1413 (ULN2003A) | 7 | P/648 | Invert |
| 500 | 8.0 V to 18 V MOS | 1.0 | Yes | 50 | MC1416 (ULN2004A) | 7 | P/648 | Invert |
| 1500 | TTL, 5.0 V CMOS | 1.0 | Yes | 50 | ULN2068B | 4 | B/648 | Invert |
| 1500 | TTL, 5.0 V CMOS | 1.0 | No | 50 | ULN2074 | 4 | B/648 | Collector, Emitter available at Pins |





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# STANDARD MILITARY PRODUCT MARKING

**MINIMUM MARKING REQUIREMENT:** All Motorola standard military product receives the following marking:

1. Motorola Symbol (logo): Example — Ⓜ
2. Seal Date Code (per MIL-M-38510): Example — 8511
3. ESD Identifier, Equilateral Triangle: Example — Δ
4. Device Part Number: Example — as shown in Table II
5. Index Point (defines starting point for numbering leads and/or mechanical orientation and shall consist of either a pin 1 dot, package notch or a dog-leg or pin 1 terminal).
6. Motorola's manufacturer's designating symbol CGG per NAV-SHIPS 0967-190-4010. *
7. If package material contains beryllium oxide, the part is marked with the designator "BeO".

*CGG not marked on can packages

**ADDITIONAL MARKING:**

883 product also receives the following marking:

a. Multiple part numbers (when applicable) is defined below:
   — MOTOROLA 883 part number
   — SMD/DESC DRAWING part number (if applicable).

b. Country of Origin (marked on backside of CERDIP, CERFLAT, and LCCC package types and on the side or bottom of "Metal Can" packages).

   NOTE: A unique perfix code may be added to the Inspection Lot Identification Code (seal date) which identifies the country of origin for both assembly and test. See table below.

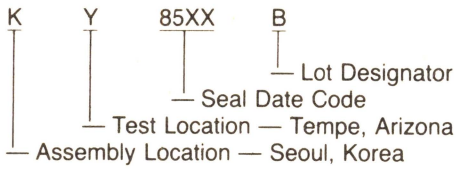
c. "883" MIL-STD-883 General Provisions paragraph 1.2.1 compliance marking.

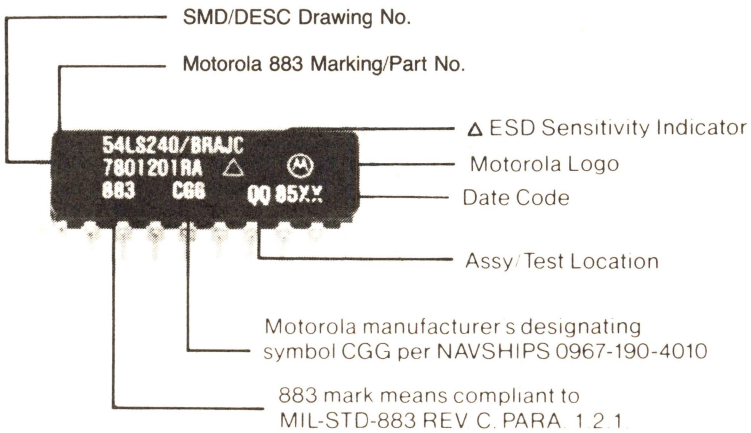
## LOCATOR CODES FOR ASSEMBLY OR TEST

| | | | | | |
|---|---|---|---|---|---|
| D | — | Austin, TX | Q | — | Kuala Lumpur, Malaysia (KLM) |
| E | — | Oakhill, TX | R | — | Seremban, Malaysia |
| I | — | Ariam, Korea (Contractor) | T | — | France |
| K | — | Seoul, Korea (MKL) | W | — | Guadalajara, Mexico |
| L | — | Hong Kong | Y | — | Tempe, AZ |
| M | — | Mesa, AZ | Z | — | Scotland |

The prefix letter closest to the date code is the Test Location Code. The letter to the left of the Test Location Code is the Assembly Location Code.

Example:



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# Military IC Numbering System

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Standard Military Drawing (SMD/DESC)** | **5962** FEDERAL STOCK CODE | – | **86710** DETAIL SPECIFICATION | **01 (54F381)** DETAIL DEVICE | | **R** CASE (SEE TABLE) | | **A** LEAD FINISH (SEE TABLE) |
| **MIL-M-38510 (JAN)** | **J** INDICATES A QUALIFIED DEVICE | | **M38510** MILITARY DESIGNATOR | **/300** DETAIL SPECIFICATION | **01** DETAIL DEVICE | **B** CLASS B | **C** CASE (SEE TABLE) | **A** LEAD FINISH (SEE TABLE) |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **MIL-STD-883 (883C)** | 1) | **DIP** | **54LS00** | | **/B** | **C** | **A** | **JC** |
| | 2) | **LCC** | **54LS00** DEVICE | **M** MOTOROLA CASE OUTLINE TABLE | **/B** CLASS B | **2** CASE (SEE TABLE) | **A** LEAD FINISH (SEE TABLE) | **JC** INDICATES MARKING PER JEDEC PUBL. #101 |

## MIL-M-38510 CASE OUTLINE TABLE

| LETTER | APPENDIX C DESIGNATION | DESCRIPTION | LETTER | APPENDIX C DESIGNATION | DESCRIPTION |
|---|---|---|---|---|---|
| A | F-1 | 14-lead FP (1/4″ x 1/4″) | L | D-9 | 24-lead DIP (1/4″ x 1-1/4″) |
| B | F-3 | 14-lead FP (3/16″ x 1/4″) | M | A-3 | 12-lead can |
| C | D-1 | 14-lead DIP (1/4″ x 3/4″) | P | D-4 | 8-lead DIP (1/4″ x 3/8″) |
| D | F-2 | 14-lead FP (1/4″ x 3/8″) | Q | D-5 | 40-lead DIP (9/16″ x 2-1/16″) |
| E | D-2 | 16-lead DIP (1/4″ x 7/8″) | R | D-8 | 20-lead DIP (1/4″ x 1-1/16″) |
| F | F-5 | 16-lead FP (1/4″ x 3/8″) | S | F-9 | 20-lead FP (1/4″ x 1/2″) |
| G | A-1 | 8-lead can | V | D-6 | 18-lead DIP (1/4″ x 15/16″) |
| H | F-4 | 10-lead FP (1/4″ x 1/4″) | W | D-7 | 22-lead DIP (3/8″ x 1-1/8″) |
| I | A-2 | 10-lead can | 2 | C-2 | 20-Terminal SQ. CCP (.350″ x .350″) |
| J | D-3 | 24-lead DIP (1/2″ x 1-1/4″) | 3 | C-4 | 28-Terminal SQ. CCP (.450″ x .450″) |
| K | F-6 | 24-lead FP (3/8″ x 5/8″) | | | |

## JEDEC CASE OUTLINE TABLE

The undesignated package letters are as follows:

U = Leadless chip carrier
X = DIP
Y = Flat Pack
Z = All other configurations

## MOTOROLA CASE OUTLINE TABLE

M = Motorola designator for the 75 Mil Multi-Layer Leadless Chip Carrier

| Dimension | Inches |
|---|---|
| Maximum Height | 0.075 |

## LEAD FINISH TABLE MIL-M-38510

A — Kovar or Alloy 42, with hot solder dip
B — Kovar or Alloy 42, with fused matte tin plate
C — Kovar, Alloy 42, or Co-Fired, with gold plate

X — Any of above, for ordering purposes only.


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MPO **Military Products Operations**

# STANDARD MILITARY PRODUCT FLOWS

TABLE I details the screening and quality conformance inspection procedures for Motorola's standard military flows. Motorola has established two distinct product flows which are designed to meet the following applications:

1. **MOTOROLA SMD/883 CLASS B FLOW:** Motorola SMD/883 Class B products are offered for use in airborne or ground system applications. SMD/883 product is screened and tested per the applicable requirements of MIL-M-38510, MIL-STD-883 including general provision paragraph 1.2 (and subordinate paragraphs), and applicable SMD/DESC drawing. Marking shall be in accordance with JEDEC Publication No. 101. Fabrication, screening and testing are not restricted to U.S.A. facilities.
2. **MIL-M-38510 JAN CLASS B FLOW:** JAN Class B products are offered for use in airborne or ground system applications. Fabrication, screening and testing are restricted to DESC certified lines.

**CLASS B FLOW(S):** The Class B flow has become the "Industry standard flow." This product receives all the 100% screening tests specified by Method 5004, MIL-STD-883. These tests include *visual inspection* to the requirements of Condition B of Method 2010 (and Method 5004 paragraph 3.3), *burn-in,* Condition A, B, C, D or E per Method 1015, for 160 hours at +125° (or equivalent per Table I or Method 1015), and *static electrical testing at high and low rated temperatures.*

## TABLE I

| | MIL-STD-883 and SMD | | MIL-M-38510 JAN | |
|---|---|---|---|---|
| **SCREEN** | **METHOD** | **REQM'T.** | **METHOD** | **REQM'T.** |
| Internal Visual (Precap) | 2010 Condition B and 38510 1/ | 100% | 2010 Cond. B and 38510 1/ | 100% |
| Stabilization Bake | 1008 24 hours min. Condition C or equivalent. | 100% | 1008 24 hours min. Condition C or equivalent. | 100% |
| Temperature Cycling | 1010 Condition C | 100% | 1010 Condition C | 100% |
| Constant Acceleration | 2001 Condition E (min.) in $Y_1$ Plane 2/ | 100% | 2001 Conditon E (min.) in $Y_1$ Plane 2/ | 100% |
| Seal Fine & Gross | 1014, Conditions B & C | 100% | 1014, Conditions B & C | 100% |
| Interim Electrical | Per applicable device specification 3/ | Optional | JAN slash sheet electrical specification | Optional |
| Burn-In Test | 1015 160 hours @ 125°C or equivalent 4/ | 100% | 1015 160 hours @ 125°C or equivalent 4/ | 100% |
| Final Electrical Tests<br>(A) Static Tests<br>(1) 25°C (Subgroup 1, Table 1, 5005) 11/<br>(2) Max & min rated op temperature (Subgroups 2 & 3, Table 1, 5005)<br>(B) Dynamic Test or Switching Tests 25°C (Subgroup 4 or 9, Table 1, 5005)<br>(C) Functional Test 25°C (Subgroup 7, Table 1, 5005) | Per applicable device specification 3/ | 100%<br>100%<br>100%<br>100% | JAN slash sheet electrical specifications | 100%<br>100%<br>100%<br>100% |
| Quality Conformance Inspection: Group A<br>(A) Static<br>(1) 25°C (Subgroup 1)<br>(2) Temp. (Subgroup 2 & 3)<br>(B) Dynamic & Switching Tests<br>(1) 25°C (Subgroup 4 or 9)<br>(2) Temp. (Subgroup 5 & 6 or 10 & 11 10/<br>(C) Functional<br>(1) 25°C (Subgroup 7) | 5005 Class B | 5/ | 5005 Class B | 5/ |
| Group B | 5005 Class B | 6/ | 5005 Class B | 6/ |
| Group C | 5005 Class B | 7/ 9/ | 5005 Class B | 26 wks. prod. |
| Group D | 5005 Class B | 8/ 9/ | 5005 Class B | 36 wks. pkg. prod. |
| External Visual | 2009 | 100% | 2009 | 100% |

1/Alternate screens per Paragraph 3.3 of Method 5004, MIL-STD-883 will be used on bipolar digital logic and memory product.
2/For packages with cavity perimeter of >2 inches or a package mass >5 grams, lesser stress levels will be used.
3/See "Test Program" column in the Cross Reference Charts of Sections 3, 4, 5, 6 and Note 2 page 12 of IC Military Handbook (BR149), free upon request from Motorola Literature Center, P.O. Box 20912, Phoenix, AZ 85036.
4/Burn-in time/temperature per Table I of Method 1015, MIL-STD-883. PDA per method 5004, MIL-STD-883.
5/Sample size selection per 12MRM 03627A (sample sizes and acceptance levels are tighter than the requirements of Table I of Method 5005, MIL-STD-883).
6/Each package and lead finish for each week of seal for each assembly location.
7/JAN generic data may be used. If JAN generic data is not available, Group C inspection shall be periodically performed per general provision paragraph 1.2.1 of MIL-STD-883.
8/Group D inspection shall be periodically performed per general provision paragraph 1.2.1 of MIL-STD-883.
9/Endpoint electrical endpoints for Group(s) C and D inspection shall be subgroups 1, 2, & 3 of the applicable device specification.
10/When limits are available per applicable device specification. For SSI Class B devices, tests are performed as a part of Group C. For MSI and greater complexity Class B devices, tests are performed as a part of Group A.
11/Lead Finish "A" applied after completion of subgroup $A_1$, electrical tests.



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# Surface Mount Technology

## Linear and Interface

All the major bipolar analog families are now represented in surface mount packaging. Standard SOIC and PLCC packages are augmented by SOP-8 and DPAK for Linear regulators. In addition, tape and reel shipping to the updated EIA-481A is now on line for the industry's largest array of op-amps, regulators, interface, data conversion, consumer, telecom and automotive Linear ICs.

| Device | Function | Package |
|---|---|---|
| DAC-08CD,ED | High-Speed 8-Bit Multiplying D-to-A Converter | SO-16 |
| LF347D | Quad BIFET Operational Amplifiers | SO-14 |
| LF351D | Single BIFET Operational Amplifier | SO-8 |
| LF353D | Dual BIFET Operational Amplifiers | SO-8 |
| LF412CD | Dual BIFET High Power Operational Amplifiers | SO-8 |
| LF441CD | Single BIFET Low Power Operational Amplifier | SO-8 |
| LF442CD | Dual BIFET Low Power Operational Amplifiers | SO-8 |
| LF444CD | Quad BIFET Low Power Operational Amplifiers | SO-14 |
| LM201AD | General Purpose Adjustable Operational Amplifier | SO-8 |
| LM208D,AD | Precision Operational Amplifier | SO-8 |
| LM211D | High Performance Voltage Comparator | SO-8 |
| LM224D | Quad Low Power Operational Amplifiers | SO-14 |
| LM239D,AD | Quad Single Supply Comparators | SO-14 |
| LM258D | Dual Low Power Operational Amplifiers | SO-8 |
| LM293D | Dual Comparators | SO-8 |
| LM301AD | General Purpose Adjustable Operational Amplifier | SO-8 |
| LM308D,AD | Precision Operational Amplifier | SO-8 |
| LM311D | High Performance Voltage Comparator | SO-8 |
| LM317LD | Positive Adjustable 100 mA Voltage Regulator | SOP-8 |
| LM324D,AD | Quad Low Power Operational Amplifiers | SO-14 |
| LM339D,AD | Quad Single Supply Comparators | SO-14 |
| LM348D | Quad MC1741 Operational Amplifiers | SO-14 |
| LM358D | Dual Low Power Operational Amplifiers | SO-8 |
| LM385D-1.2 | Micropower Voltage Reference Diodes | SO-8 |
| LM385D-2.5 | Micropower Voltage Reference Diodes | SO-8 |
| LM393D | Dual Comparators | SO-8 |
| LM833D | Dual Audio Amplifiers | SO-8 |
| LM2931AD-5.0,D-5.0 | Low Dropout Voltage Regulator | SOP-8 |
| LM2931ACD*,CD* | Adjustable Low Dropout Voltage Regulator | SOP-8 |
| LM2901D | Quad Single Supply Comparators | SO-14 |
| LM2902D | Quad Low Power Operational Amplifiers | SO-14 |
| LM2903D | Dual Comparators | SO-8 |
| LM2904D | Dual Low Power Operational Amplifiers | SO-8 |
| LM3900D | Quad Single Supply Operational Amplifiers | SO-14 |
| MC1377DW* | Color Television RGB to PAL/NTSC Encoder | SO-20 |
| MC1378FN | Video Overlay Synchronizer | PLCC-44 |
| MC1403D | Precision Low Voltage Reference | SO-8 |
| MC1413D | Peripheral Driver Array | SO-16 |
| MC1436D,CD | High Voltage Operational Amplifier | SO-8 |
| MC1455D | Timing Circuit | SO-8 |
| MC1458D,CD | Dual Operational Amplifiers | SO-8 |
| MC1458SD | High Slew Rate Dual Operational Amplifiers | SO-8 |
| MC1488D | Quad EIA-232C Drivers | SO-14 |
| MC1489D | Quad EIA-232C Receivers | SO-14 |
| MC1496D | Balanced Modulator-Demodulator | SO-14 |
| MC1723CD | Adjustable Positive Or Negative Voltage Regulator | SO-14 |
| MC1741CD | General Purpose Operational Amplifier | SO-8 |
| MC1741SCD | High Slew Rate Operational Amplifier | SO-8 |
| MC1747CD | Dual MC1741 Operational Amplifiers | SO-14 |
| MC1776CD | Programmable Operational Amplifier | SO-8 |

*To Be Introduced.



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## LINEAR AND INTERFACE (continued)

| Device | Function | Package |
|---|---|---|
| MC26LS31D | Quad EIA-422/3 Receivers | SO-16 |
| MC26LS32D | Quad EIA-422 Drivers | SO-16 |
| MC2831AD | FM Transmitter | SO-16 |
| MC3346D | General Purpose Transistor Array | SO-14 |
| MC3356FN | FSK Receiver | PLCC-20 |
| MC3357D | Low Power FM IF Amplifier | SO-16 |
| MC3359DW | Low Power Narrowband FM IF Amplifier | SO-20 |
| MC3361D | Low Voltage Narrowband FM IF Amplifier | SO-16 |
| MC3362DW | Dual Conversion Receivers | SO-28 |
| MC3363DW* | Dual Conversion Receivers | SO-28 |
| MC3364DW* | Narrowband Dual Conversion Receiver | SO-28 |
| MC3367DW | Low Voltage VHF Receiver | SO-28 |
| MC3371D* | Low Voltage FM Receiver with RSSI | SO-16 |
| MC3401D | Quad Operational Amplifiers | SO-14 |
| MC3403D | Quad Differential-Input Operational Amplifiers | SO-14 |
| MC3423D | Overvoltage Sensing Circuit | SO-8 |
| MC3448AD | Quad GPIB Transceivers | SO-16 |
| MC3450D | Quad Line Receivers | SO-16 |
| MC3452D | Quad Line Receivers | SO-16 |
| MC3458D | Dual Low Power Operational Amplifiers | SO-8 |
| MC3486D | Quad EIA-422/3 Receivers | SO-16 |
| MC3487D | Quad EIA-422 Drivers | SO-16 |
| MC4558CD | Dual High Frequency Operational Amplifiers | SO-8 |
| MC4741CD | Quad MC1741 Operational Amplifiers | SO-14 |
| MC78L05ACD | Positive Voltage Regulator, 5 V, 100 mA | SOP-8 |
| MC78L08ACD | Positive Voltage Regulator, 8 V, 100 mA | SOP-8 |
| MC78L12ACD | Positive Voltage Regulator, 12 V, 100 mA | SOP-8 |
| MC78L15ACD | Positive Voltage Regulator, 15 V, 100 mA | SOP-8 |
| MC78M05CDT* | Positive Voltage Regulator, 5 V, 500 mA | DPAK |
| MC78M12CDT* | Positive Voltage Regulator, 12 V, 500 mA | DPAK |
| MC78M15CDT* | Positive Voltage Regulator, 15 V, 500 mA | DPAK |
| MC79L05ACD | 3-Terminal Negative Fixed Voltage Regulator, −5 V, 100 mA | SOP-8 |
| MC79L12ACD | 3-Terminal Negative Fixed Voltage Regulator, −12 V, 100 mA | SOP-8 |
| MC79L15ACD | 3-Terminal Negative Fixed Voltage Regulator, −15 V, 100 mA | SOP-8 |
| MC79M05CDT* | 3-Terminal Negative Fixed Voltage Regulator, −5 V, 500 mA | DPAK |
| MC79M12CDT* | 3-Terminal Negative Fixed Voltage Regulator, −12 V, 500 mA | DPAK |
| MC79M15CDT* | 3-Terminal Negative Fixed Voltage Regulator, −15 V, 500 mA | DPAK |
| MC13011DW* | High Performance Video IF | SO-28 |
| MC13022DW* | Medium Voltage AM Stereo C-QUAM Decoder | SO-28 |
| MC13024DW* | Low Voltage C-QUAM Receiver | SO-24 |
| MC13041DW* | AM Receiver Subsystem | SO-20 |
| MC13055D | VHF LAN Receiver — FSK | SO-16 |
| MC13060D | 1 Watt Audio Amp | SOP-8 |
| MC33077D | Dual, Low Noise High Frequency Operational Amplifiers | SO-8 |
| MC33078D | Dual Audio, Low Noise Operational Amplifiers | SO-8 |
| MC33079D | Low Power, Single Supply Operational Amplifier | SO-14 |
| MC33171D | Single, Low Power, Single Supply Operational Amplifier | SO-8 |
| MC33172D* | Dual, Low Power, Single Supply Operational Amplifiers | SO-8 |
| MC33174D* | Quad, Low Power, Single Supply Operational Amplifiers | SO-14 |
| MC33282D* | Dual Precision Low Input JFET Operational Amplifiers | SO-14 |
| MC33284D* | Quad Precision JFET Operational Amplifiers (Trim-in-the-Package) | SO-14 |
| MC34001D,AD,BD | Single JFET Input Operational Amplifier | SO-8 |
| MC34002D,AD,BD | Dual JFET Input Operational Amplifiers | SO-8 |
| MC34004D,BD | Quad JFET Input Operational Amplifiers | SO-14 |
| MC34011AFN | Electronic Telephone Circuit | PLCC-44 |
| MC34012-1D | Telephone Tone Ringer | SO-8 |
| MC34012-2D | Telephone Tone Ringer | SO-8 |
| MC34012-3D | Telephone Tone Ringer | SO-8 |
| MC34013AFN | Speech Network and Tone Dialer | PLCC-28 |
| MC34014FN | Telephone Speech Network with Dialer Interface | PLCC-20 |
| MC34017-1D | Telephone Tone Dialer | SO-8 |
| MC34017-2D | Telephone Tone Dialer | SO-8 |
| MC34017-3D | Telephone Tone Dialer | SO-8 |
| MC34018DW | Voice Switched Speakerphone Circuit | SO-28 |

*To Be Introduced.





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| Device | Function | Package |
|---|---|---|
| MC34018FN | Voice Switched Speakerphone Circuit | PLCC-28 |
| MC34060AD* | Switchmode Pulse Width Modulation Control Circuit | SO-14 |
| MC34063AD | Precision DC-to-DC Converter Control Circuit | SO-8 |
| MC34071D | Single, High Speed, Single Supply Operational Amplifier | SO-8 |
| MC34072D* | Dual, High Speed, Single Supply Operational Amplifiers | SO-8 |
| MC34074D* | Quad, High Performance, Single Supply Operational Amplifiers | SO-14 |
| MC34080D | High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | SO-8 |
| MC34081D | High Speed JFET Input Operational Amplifier | SO-8 |
| MC34114DW | Speech Network II | SO-18 |
| MC34118DW | Speakerphone II | SO-28 |
| MC34119D | Telephone Speaker Amplifier | SO-8 |
| MC34129D | Power Supply Controller | SO-14 |
| MC34181D | Single, Low Power, High Speed JFET Operational Amplifier | SO-8 |
| MC34182D | Dual, Low Power, High Speed JFET Operational Amplifiers | SO-8 |
| MC34184D | Quad, Low Power, High Speed JFET Operational Amplifiers | SO-14 |
| NE592D | Video Amplifier | SO-14 |
| TL061CD | Single BIFET Low Power Operational Amplifier | SO-8 |
| TL062CD | Dual BIFET Low Power Operational Amplifiers | SO-8 |
| TL064CD | Quad BIFET Low Power Operational Amplifiers | SO-14 |
| TL071CD,ACD,BCD | Single, Low Noise JFET Input Operational Amplifier | SO-8 |
| TL072CD,ACD,BCD | Dual, Low Noise JFET Input Operational Amplifiers | SO-8 |
| TL074CD,ACD,BCD | Quad, Low Noise JFET Input Operational Amplifiers | SO-14 |
| TL081CD,ACD,BCD | Single, JFET Input Operational Amplifier | SO-8 |
| TL082CD,ACD,BCD | Dual, JFET Input Operational Amplifiers | SO-8 |
| TL084CD,ACD,BCD* | Quad, JFET Input Operational Amplifiers | SO-14 |
| TL431CD | Programmable Precision Reference | SOP-8 |
| TYA1350D | IF Amplifier (M1350D) | SO-8 |
| UAA1041D | Automotive Direction Indicator | SO-8 |
| UC3842AD | Off-Line Current Mode PWM Controller | SO-14 |
| UC3843AD | Current Mode PWM Controller | SO-14 |

# Surface Mount Technology Package Overview

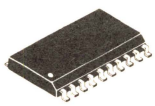
CASE 369A
PLASTIC
DPAK
**DT SUFFIX**

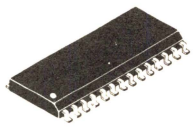
CASE 751
PLASTIC
SO-8, SOP-8
**D SUFFIX**

CASE 751A
PLASTIC
SO-14
**D SUFFIX**

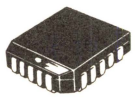
CASE 751B
PLASTIC
SO-16
**D SUFFIX**

CASE 751D
PLASTIC
SO-20
**DW SUFFIX**

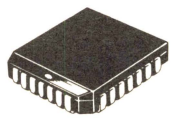




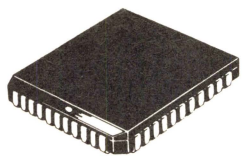
CASE 751F
PLASTIC
SO-28
**DW SUFFIX**



CASE 775
PLASTIC
PLCC-20
**FN SUFFIX**



CASE 776
PLASTIC
PLCC-28
**FN SUFFIX**



CASE 777
PLASTIC
PLCC 44
**FN SUFFIX**

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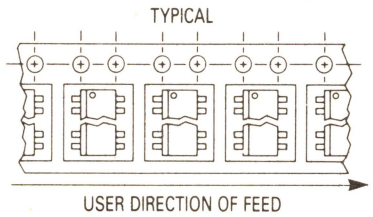
# Tape and Reel

## Standard Bipolar Logic, Bipolar Analog and MOS Integrated Circuits

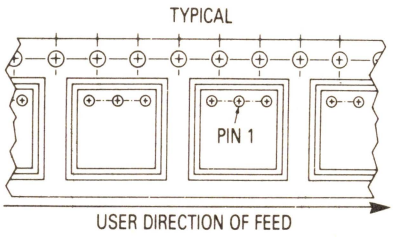
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. Two reel sizes are available, for all but the largest types, to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The anti-static embossed tape provides a secure cavity, sealed with a peel-back cover tape.

### Mechanical Polarization

**SOIC DEVICES**




**PLCC DEVICES**




| Package | Tape Width (mm) | Device per Reel | Reel Size* (inch) | Tape & Reel Lot Size(1) (Min) | Device Suffix |
|---|---|---|---|---|---|
| SO-8, SOP-8 | 12<br>12 | 750<br>2,500 | 7<br>13 | 5,000<br>5,000 | R1<br>R2 |
| SO-14 | 16<br>16 | 750<br>2,500 | 7<br>13 | 5,000<br>5,000 | R1<br>R2 |
| SO-16 | 16<br>16 | 750<br>2,500 | 7<br>13 | 5,000<br>5,000 | R1<br>R2 |
| SO-16 WIDE | 16<br>16 | 250<br>1,000 | 7<br>13 | 5,000<br>5,000 | R1<br>R2 |
| SO-20 WIDE | 24<br>24 | 250<br>1,000 | 7<br>13 | 5,000<br>5,000 | R1<br>R2 |
| SO-24 WIDE | 24<br>24 | 250<br>1,000 | 7<br>13 | 5,000<br>5,000 | R1<br>R2 |
| SO-28 WIDE | 24<br>24 | 200<br>1,000 | 7<br>13 | 3,000<br>3,000 | R1<br>R2 |
| PLCC-20 | 16<br>16 | 200<br>1,000 | 7<br>13 | 3,000<br>3,000 | R1<br>R2 |
| PLCC-28 | 24<br>24 | 200<br>500 | 7<br>13 | 2,400<br>2,500 | R1<br>R2 |
| PLCC-44 | 32<br>32 | 200<br>500 | 7<br>13 | 2,000<br>2,000 | R1<br>R2 |
| PLCC-52<br>PLCC-68<br>PLCC-84 | 32<br>44<br>44 | 500<br>250<br>250 | 13<br>13<br>13 | 2,000<br>2,000<br>2,000 | R2<br>R2<br>R2 |
| TO-92(2) | 18 | 1800 | 13 | 10,000 | RA, RB or RP only |

Notes: 1. Minimum lot size information applies to OEM customers. Distributors may break lots or reels at their option, however broken reels may not be returned.
2. Integrated Circuits in TO-92 packages are available in Styles A and B only, with optional "Ammo Pack" (Suffix RP).

For ordering information please contact your local Motorola Semiconductor Sales Office.
Distribution minimum order quantity is 1 reel.
*Reel Size: 7"/178 mm, 13"/330 mm.

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# PERFORMANCE ELECTRONIC PACKAGING SERVICES, INC.

6354-B CORTE DEL ABETO □ CARLSBAD, CALIFORNIA 92009 □ 619•931•7824


## DRAM MEMORY MODULES

| PART NUMBER | ORGANISATION | DIMENSIONS | PKG. |
|---|---|---|---|
| **64 K DRAM BASED MODULES SPEEDS**—120, 150, 200 nS. | | | |
| PEP4064EC4 | 64K × 4 | 2.2 × 0.42 × 0.180 | 22 PIN SIP |
| PEP4064EC5 | 64K × 5 | 2.9 × 0.42 × 0.180 | 24 PIN SIP |
| PEP4064EL8* | 64K × 8 | 3.0 × 0.60 × 0.180 | 30 PIN SIP |
| PEP4064EL9* | 64K × 9 | 3.0 × 0.60 × 0.180 | 30 PIN SIP |
| **256 K DRAM BASED MODULES**—60, 70, 80, 100, 120, 150 nS. | | | |
| PEP4256EC4 | 256K × 4 | 2.2 × 0.42 × 0.180 | 22 PIN SIP |
| PEP4256EC5 | 256K × 5 | 2.9 × 0.42 × 0.180 | 24 PIN SIP |
| PEP4256EL8* | 256K × 8 | 3.0 × 0.60 × 0.180 | 30 PIN SIP |
| PEP4256EL9* | 256K × 9 | 3.0 × 0.60 × 0.180 | 30 PIN SIP |
| PEP4256EL8-LP | 256K × 8 | 3.0 × 0.45 × 0.320 | 30 PIN SIP |
| PEP4256EL9-LP | 256K × 9 | 3.0 × 0.45 × 0.320 | 30 PIN SIP |
| **1M BIT DRAM BASED MODULES**—80, 100, 120 nS. | | | |
| PEP1MX4 | 1M × 4 | 2.8 × 0.42 × 0.180 | 24 PIN SIP |
| PEP1MX5 | 1M × 5 | 3.5 × 0.42 × 0.180 | 26 PIN SIP |
| PEP4MX1 | 4M × 1 | 2.8 × 0.42 × 0.180 | 26 PIN SIP |
| PEP1MX4Z | 1M × 4 | 1.5 × 0.350 × 0.440 | 26 PIN SIP |
| PEP4MX1Z | 4M × 1 | 1.5 × 0.35 × 0.44 | 23 PIN SIP |
| PEP1MX8* | 1M × 8 | 3.2 × 0.775 × 0.190 | 30 PIN SIP |
| PEP1MX9* | 1M × 9 | 3.2 × 0.775 × 0.190 | 30 PIN SIP |
| PEP1MX8-LP | 1M × 8 | 3.5 × 0.435 × 0.320 | 30 PIN SIP |
| PEP1MX9-LP | 1M × 9 | 3.5 × 0.435 × 0.320 | 30 PIN SIP |
| PEP1MX16 | 1M × 16 | 3.3 × 1.50 × 0.320 | 64 PIN SIP |
| PEP2MX8 | 2M × 8 | 3.3 × 1.50 × 0.320 | 64 PIN SIP |

PLEASE CALL US FOR OUR STATIC RAM AND CUSTOM MODULE PRODUCTS.

### NOTES

1. *ALSO AVAILABLE IN SIMM PACKAGE
2. LP- STANDS FOR LOW PROFILE MODULES WITH DRAMS MOUNTED ON BOTH SIDES AND AN OPTIONAL PARITY CHECKER (74F280) ON THE MODULE.
3. 256K AND I MBIT DRAM BASED MODULES ARE AVAILABLE WITH PAGE, NIBBLE AND STATIC COLUMN DEVICES.





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# ADC-908

## CMOS MICROPROCESSOR-COMPATIBLE FAST 8-BIT A/D CONVERTER

Precision Monolithics Inc.

### FEATURES

- **8-Bit Resolution and Accuracy**
- **No Missing Codes Over Full Temperature Range**
- **6μs Conversion Time**
- **Flexible μP Interface**
- **2.5mA Maximum Standby Current**
- **Replaces AD7574 With Improved Speed**

### ORDERING INFORMATION†

| | | PACKAGE: 18-PIN DIP AND SO | | |
|---|---|---|---|---|
| | | MILITARY* TEMPERATURE | INDUSTRIAL TEMPERATURE | COMMERCIAL TEMPERATURE |
| INL (LSB) | DNL (LSB) | −55°C TO +125°C | −40°C TO +85°C | 0°C TO 70°C |
| ±1/2 | ±3/4 | ADC908AX | ADC908EX | ADC908GP |
| ±3/4 | ±7/8 | ADC908BX | ADC908FX | ADC908HP |
| ±1/2 | ±3/4 | — | — | ADC908GS†† |

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

††For availability and burn-in information on SO and PLCC packages, contact your local sales office.

### GENERAL DESCRIPTION

The ADC-908 is a monolithic CMOS successive-approximation analog-to-digital converter. When used with a 1.35MHz clock, a conversion time of 6μs is achieved, with full accuracy over the operating temperature range.

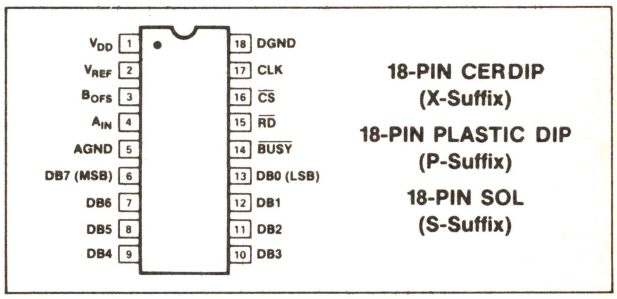
The ADC-908 outputs use 3-state logic, allowing direct connection to the data bus or system input port. Active-LOW chip select ($\overline{CS}$) and read/write ($\overline{RD}$) inputs are used to control all operations. This input structure permits the ADC-908 to be used as a memory-mapped input device. Depending on the control timing waveforms, the ADC-908 is interfaced like static RAM, ROM, or slow memory.

The low power consumption of the ADC-908 is derived from a single +5V supply. A negative reference voltage must also be supplied. Optimum accuracy is achieved when the reference is at −10.00V with a low output resistance. For a low-cost precision −10V/−10.24V reference, ask your PMI sales representative about the REF-08.

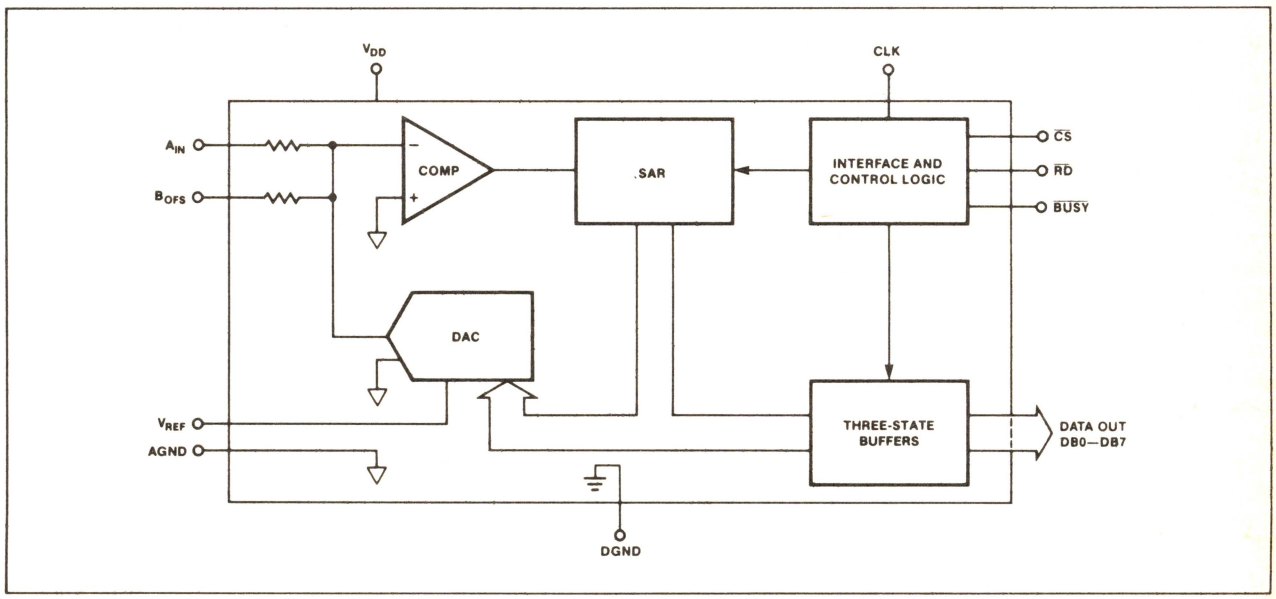
With its on-board comparator, interface logic, optional internal clock, and +5V operation, the ADC-908 is the ideal low-cost solution for microprocessor-based 8-bit A/D systems.

PMI's ADC-908 is pin-and-function compatible with the PM-7574, but offers faster conversion time and faster microprocessor bus interface timing. Conversion time has been reduced by 60% and most key timing specifications, including data access time, START command propagation delay ($t_{WBPD}$), and reset time, have been improved.

### PIN CONNECTIONS




### FUNCTIONAL DIAGRAM




10/87, Rev. A

Precision Monolithics Inc.

# DAC-8212

## DUAL 12-BIT BUFFERED MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

### FEATURES

- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- On-Chip Latches for Both DACs
- 12-Bit Endpoint Linearity (±1/2 LSB)
- +5V to +15V Single Supply Operation
- DACs Matched to 1%
- Four-Quadrant Multiplication
- Low Power Consumption

### APPLICATIONS

- Automatic Test Equipment
- Robotics
- Programmable Instrumentation Equipment
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

### ORDERING INFORMATION†

| RELATIVE ACCURACY | GAIN ERROR | PACKAGE: MILITARY* TEMPERATURE −55°C to +125°C | PACKAGE: INDUSTRIAL TEMPERATURE −25°C to +85°C | PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C |
|---|---|---|---|---|
| ±1/2 LSB | ±2 LSB | DAC8212AV | DAC8212EV | DAC8212GP |
| ±1 LSB | ±4 LSB | DAC8212BV | DAC8212FV | DAC8212HP |
| ±1 LSB | ±4 LSB | — | — | DAC8212HPC†† |

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

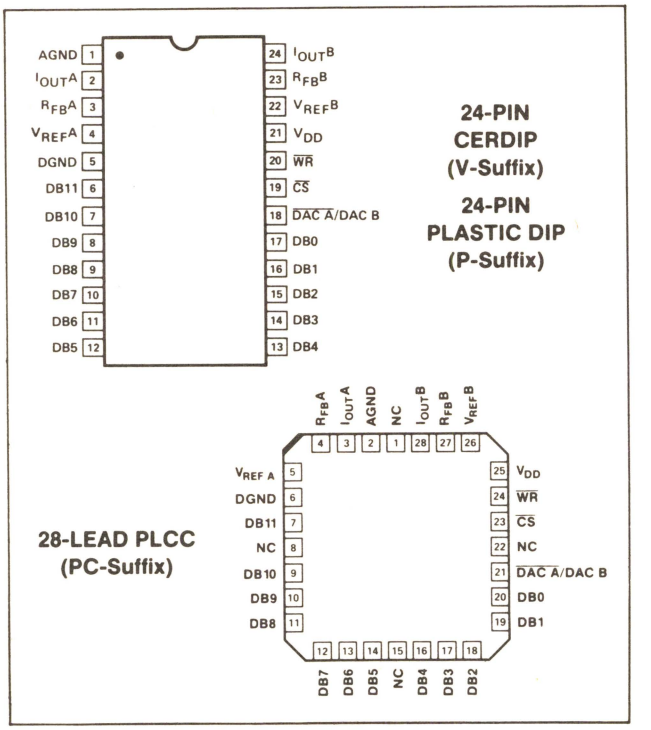
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

### GENERAL DESCRIPTION

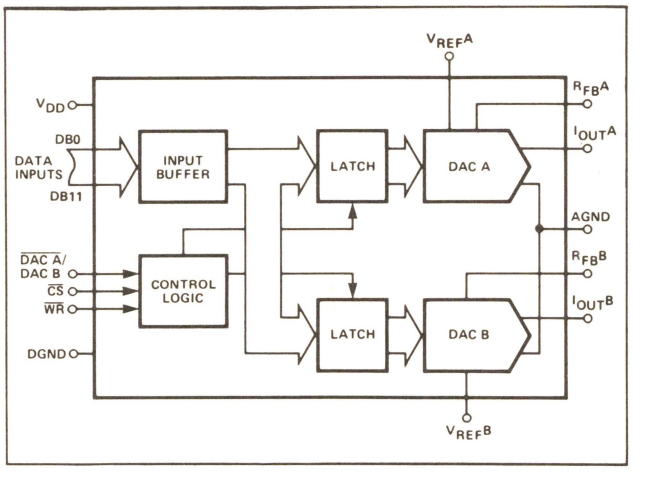
The DAC-8212 combines two identical 12-bit, multiplying, digital-to-analog converters into a single CMOS chip. Monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC-8212 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. The DAC-8212 can operate on a single supply from +5V to +15V. Maximum power dissipation with CMOS logic levels and a +5V supply is less than 0.5mW. The DAC-8212 is manufactured using PMI's highly-stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

A common 12-bit (TTL/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. With $\overline{WR}$ and $\overline{CS}$ lines at logic low, the input data latches are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by $\overline{DAC\ A}$/DAC B control input.

### PIN CONNECTIONS




### FUNCTIONAL DIAGRAM




9/87, Rev. A3

Precision Monolithics Inc.



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# OP-42

## HIGH-SPEED, FAST-SETTLING PRECISION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

### FEATURES

**Fast**

- **Slew Rate** ..... **50V/μs Min**
- **Settling-Time (0.01%)** ..... **1μs Max**
- **Gain-Bandwidth Product** ..... **10MHz Typ**

**Precise**

- **Common-Mode Rejection** ..... **88dB Min**
- **Open-Loop Gain** ..... **500V/mV Min**
- **Offset Voltage** ..... **750μV Max**
- **Bias Current** ..... **200pA Max**

**Excellent Radiation Hardness**

### ORDERING INFORMATION†

| $T_A$ = 25°C $V_{OS}$ MAX (mV) | PACKAGE TO-99 8-PIN | PACKAGE HERMETIC DIP 8-PIN | PACKAGE HERMETIC LCC 20-PIN | OPERATING TEMPERATURE RANGE |
|---|---|---|---|---|
| 1.0 | OP42AJ* | OP42AZ* | OP42ARC/883 | MIL |
| 0.75 | OP42EJ | OP42EZ | — | IND |
| 1.5 | OP42FJ | OP42FZ | — | IND |

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

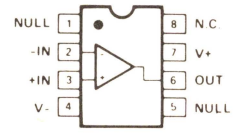
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

### GENERAL DESCRIPTION

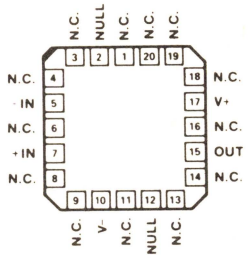
The OP-42 is a fast precision JFET-input operational amplifier. Similar in speed to PMI's OP-17, the OP-42 offers a symmetric 58V/μs slew rate and is internally compensated for unity-gain operation. OP-42 speed is achieved with a supply current of less than 6mA. Unity-gain stability, a wide full-power bandwidth of 900kHz, and a fast settling-time of 800ns to 0.01% make the OP-42 an ideal output amplifier for fast digital-to-analog converters.

Equal attention was given to both speed and precision in the OP-42 design. Its tight 750μV maximum input offset voltage combined with well-controlled drift of less than 10μV/°C eliminates the need for external nulling in many circuits. The OP-42's common-mode rejection of 88dB minimum over a ±11V input voltage range is exceptional for a high-speed amplifier. High CMR combined with a minimum 500V/mV

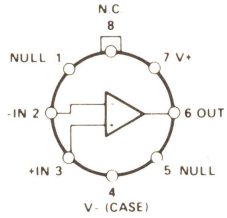
### PIN CONNECTIONS




**8-PIN HERMETIC DIP**
**(Z-Suffix)**

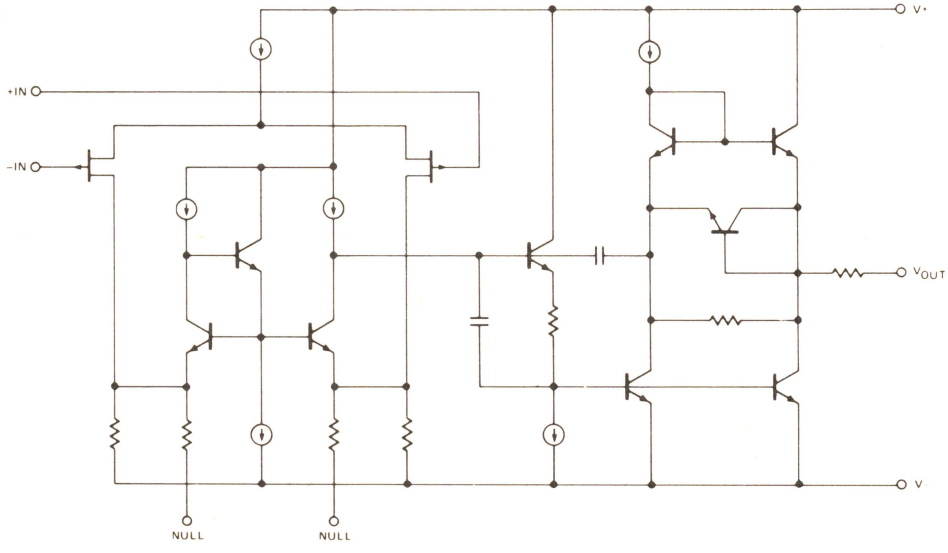



**20-LEAD HERMETIC LCC**
**(RC-Suffix)**




**TO-99**
**(J-Suffix)**

### SIMPLIFIED SCHEMATIC




**9/87, Rev. B1**

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Precision Monolithics Inc.

# OP-44

## HIGH-SPEED, PRECISION OPERATIONAL AMPLIFIER ($A_{VCL} \geq 3$)

Precision Monolithics Inc.

### FEATURES

- **Slew Rate** ..... **100V/μs Min**
- **Gain-Bandwidth Product** ..... **15MHz Min**
- **Common-Mode Rejection** ..... **86dB Min**
- **Open-Loop Gain** ..... **500V/mV Min**
- **Offset Voltage** ..... **750μV Max**
- **Bias Current** ..... **200pA Max**
- **Excellent AC CMR and PSR**
- **Radiation Hard**

### ORDERING INFORMATION†

| $T_A = 25°C$ $V_{OS}$ MAX (mV) | PACKAGE TO-99 | HERMETIC DIP | LCC | OPERATING TEMPERATURE RANGE |
|---|---|---|---|---|
| 1.00 | OP44AJ* | OP44AZ* | OP44ARC/883* | MIL |
| 0.75 | OP44EJ | OP44EZ | — | IND |
| 1.50 | OP44FJ | OP44FZ | — | IND |

Plastic Mini-Dip and SOIC to be announced.

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

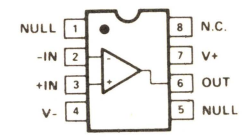
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

### GENERAL DESCRIPTION

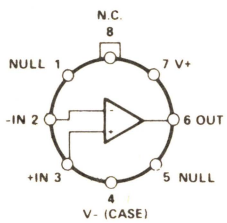
The OP-44 is a fast precision JFET-input operational amplifier delivering a 120V/μs typical slew rate in closed-loop gains of three or more. Full-power bandwidth is 2MHz for a $20V_{p-p}$ sine-wave, and 4MHz for a $10V_{p-p}$ signal. Gain-bandwidth product is typically 23MHz. Settling time to 0.1% is 200ns, and to 12 bits (0.01%) is 800ns, typical. Wideband noise is minimized by only $12nV/\sqrt{Hz}$ flatband noise.

Excellent DC precision makes the OP-44 unique among high-speed amplifiers. Offset voltage below 750μV and 10μV/°C maximum drift eliminates the need for external nulling potentiometers in most applications. Common-mode rejection of 86dB minimum and an open-loop gain of 500V/mV ensures high linearity. Errors due to bias current are virtually eliminated with the OP-44's 200pA maximum input current.

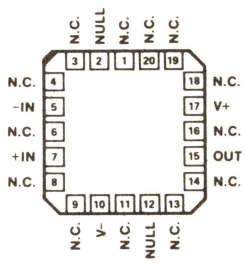
### PIN CONNECTIONS




**8-PIN HERMETIC DIP (Z-Suffix)**

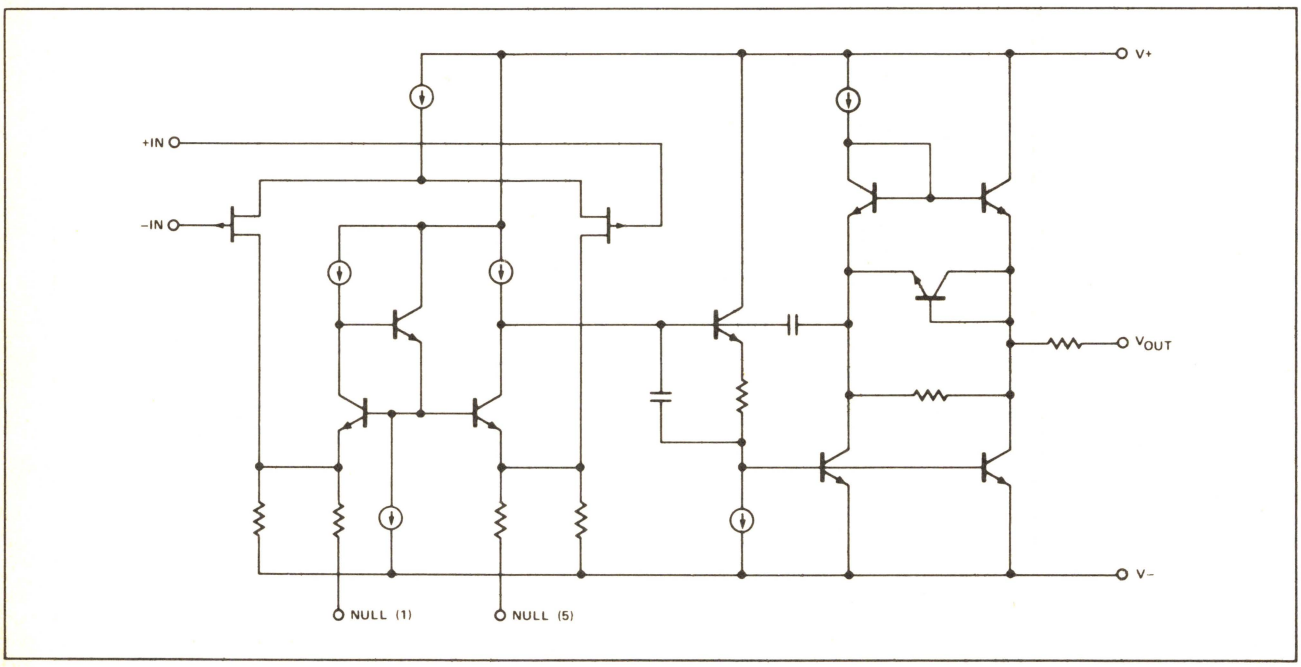



**TO-99 (J-Suffix)**




**20-CONTACT HERMETIC LCC (RC-Suffix)**

### SIMPLIFIED SCHEMATIC




**8/87, Rev. B**

Precision Monolithics Inc.



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PMI®

# OP-80

ULTRA-LOW BIAS CURRENT
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

**PRELIMINARY**

## FEATURES

- **Ultra-Low Bias Current (25°C) ..... 60fA Max**
- **High-Temp Bias Current (125°C) ..... 20pA Max**
- **Low Supply Current ..... 300μA Max**
- **True Single-Supply Operation**
  - **— Common-Mode Range Includes Ground**
  - **— Output Swings to Within 400μV of Ground**
- **Extended Industrial Temp Range ..... −40°C to +85°C**

## ORDERING INFORMATION†

| $I_B$ (pA) | PACKAGE | | OPERATING TEMPERATURE RANGE |
|---|---|---|---|
| | TO-99 | PLASTIC | |
| 0.150 | OP80AJ* | — | MIL |
| 0.060 | OP80EJ | — | XIND |
| 0.300 | OP80FJ | — | XIND |
| 2.5 | OP80GJ | OP80GP | XIND |
| 2.5 | — | OP80GS†† | XIND |

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information see 1988 Data Book, Section 2.

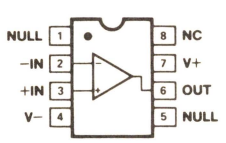
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

## GENERAL DESCRIPTION

The OP-80 CMOS operational amplifier offers exceptionally low bias currents over its entire operating temperature range. At 125°C, the OP-80 typically has a bias current of only 10pA. During room-temperature operation, the OP-80's bias current is equivalent to a mere 125 electrons per millisecond, only 20fA typical. The OP-80 is capable of operation with either single or dual supplies. Its low cost makes it attractive as a general-purpose amplifier for low-voltage systems, as well as systems demanding the highest level of precision in current-to-voltage conversion.

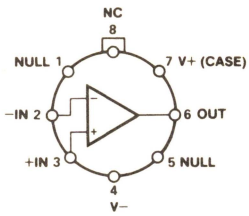
The low supply current minimizes thermal power dissipation, virtually eliminating the effects of chip self-heating. System power-supply demand is reduced as well, resulting in lower overall costs. The OP-80's CMOS design gives a good speed/power ratio, permitting a 0.2V/μs minimum slew rate and a 300kHz gain-bandwidth product with unity-gain stability.

## PIN CONNECTIONS



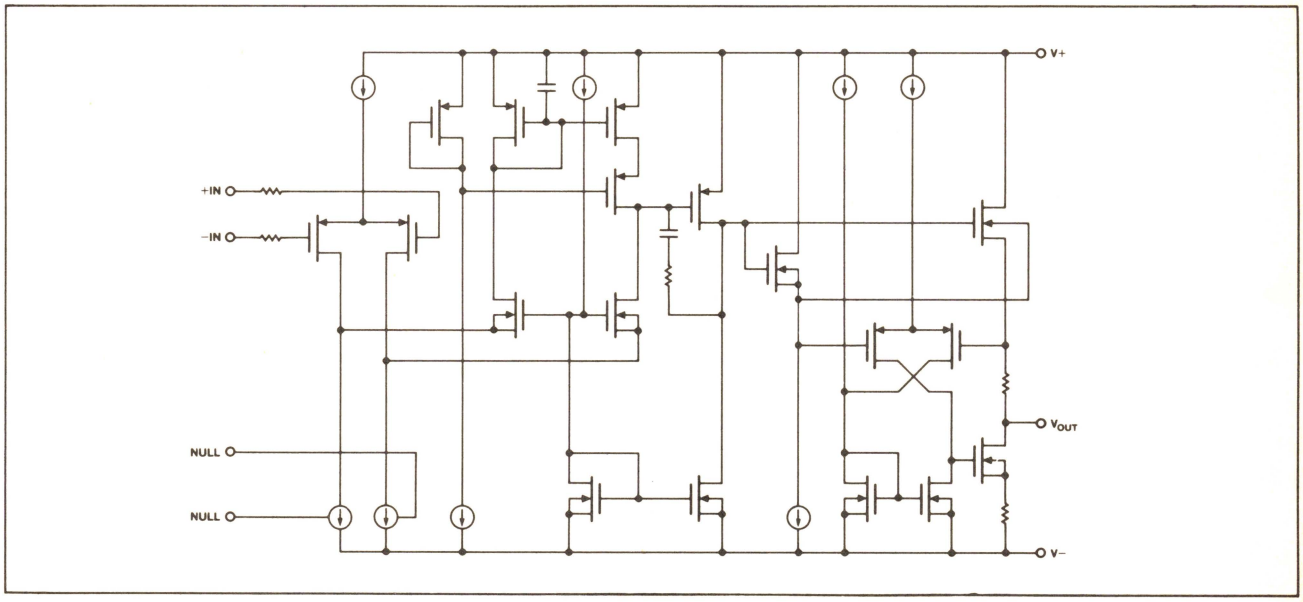

**8-PIN PLASTIC DIP**
**(P-Suffix)**

**8-PIN SO**
**(S-Suffix)**




**TO-99**
**(J-Suffix)**

## SIMPLIFIED SCHEMATIC




Manufactured under U.S. Patent Number: 4,675,561.

**This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.**

**9/87, Rev. A2**

Precision Monolithics Inc.

PMI

# OP-97

## LOW-POWER, HIGH-PRECISION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

### FEATURES

- **Low Supply Current** ..... **600μA Max**
- **OP-07 Type Performance**
  - **Offset Voltage** ..... **25μV Max**
  - **Offset Voltage Drift** ..... **0.6μV/°C Max**
- **Very Low Bias Current**
  - **25°C** ..... **100pA Max**
  - **−55°C to +125°C** ..... **250pA Max**
- **High Common-Mode Rejection** ..... **114dB Min**
- **Extended Industrial Temp. Range** ..... **−40°C to +85°C**

### ORDERING INFORMATION†

| PACKAGE | | | OPERATING TEMPERATURE RANGE |
|---|---|---|---|
| TO-99 | CERDIP | PLASTIC | |
| OP97AJ* | OP97AZ* | — | MIL |
| OP97EJ | OP97EZ | OP97EP | XIND |
| OP97FJ | OP97FZ | OP97FP | XIND |
| — | — | OP97FS†† | XIND |

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

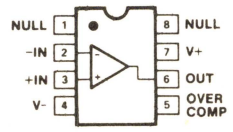
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

### GENERAL DESCRIPTION

The OP-97 is a low-power alternative to the industry-standard OP-07 precision amplifier. The OP-97 maintains the standards of performance set by the OP-07 while utilizing only 600μA supply current, less than 1/6 that of an OP-07. Offset voltage is an ultra-low 25μV, and drift over temperature is below 0.6μV/°C. External offset trimming is not required in the majority of circuits.

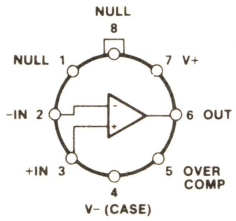
### PIN CONNECTIONS




**EPOXY MINI-DIP**
**(P-Suffix)**

**8-PIN CERDIP††**
**(Z-Suffix)**

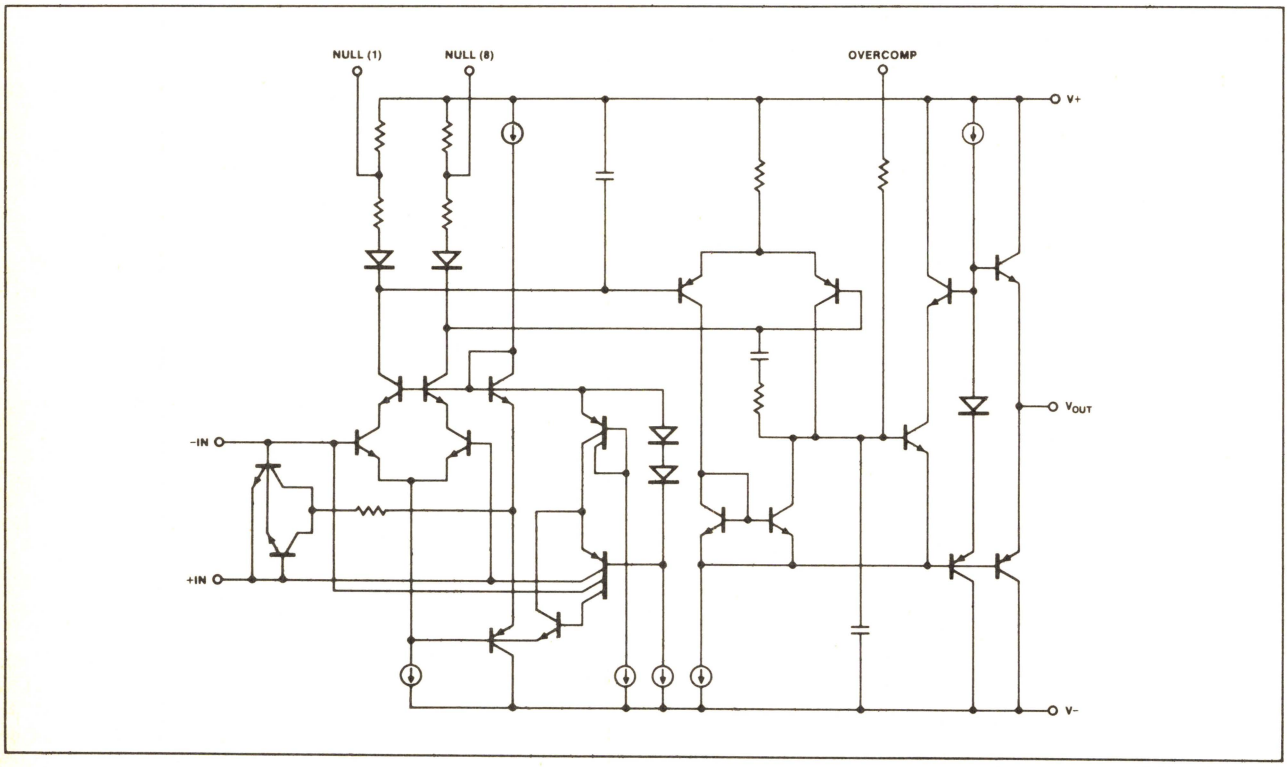
**EPOXY SO††**
**(S-Suffix)**




**TO-99**
**(J-Suffix)**

**††To be announced**

### SIMPLIFIED SCHEMATIC




**10/87, Rev. B**

Precision Monolithics Inc.



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# REF-43

## +2.5V LOW-POWER PRECISION VOLTAGE REFERENCE

**Precision Monolithics Inc.**

**PRELIMINARY**

### FEATURES

- **+2.5 Volt Output** ..... **±0.05% Max**
- **Low Temperature Coefficient** ..... **10ppm/°C Max**
- **Excellent Regulation**
  - **Load Regulation** ..... **20ppm/mA Max**
  - **Line Regulation** ..... **2ppm/V Max**
- **Supply Current** ..... **350μA Max**
- **Operating Voltage Range** ..... **+4.5V to +40V**
- **Extended Industrial Temp Range** ..... **−40°C to +85°C**

### ORDERING INFORMATION†

| | PACKAGE | | | OPERATING TEMPERATURE RANGE |
|---|---|---|---|---|
| $TCV_O$ | TO-99 | CERDIP | PLASTIC | |
| 10 | REF43BJ* | REF43BZ* | — | MIL |
| 10 | REF43FJ | REF43FZ | — | XIND |
| 20 | REF43GJ | REF43GZ | REF43GP | XIND |

REF43ARC/833 will be available in hermetic LCC package.

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

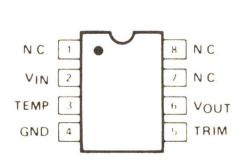
†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information see 1988 Data Book, Section 2.

### GENERAL DESCRIPTION

The REF-43 is a low-power precision reference providing a stable +2.5V output independent of variations in supply voltage, load conditions or ambient temperature. It is suitable as a reference level for 8, 10 and 12-bit data acquisition systems, or wherever a stable, known voltage is required.

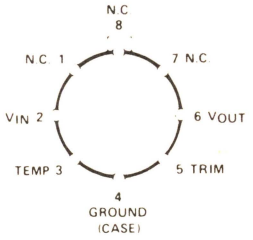
Tight output tolerances and low thermal drift are assured by zener-zap trimming of both output voltage and its temperature coefficient. A unique curvature correction circuit reduces the thermal curvature characteristic of many previous bandgap references.

### PIN CONNECTIONS



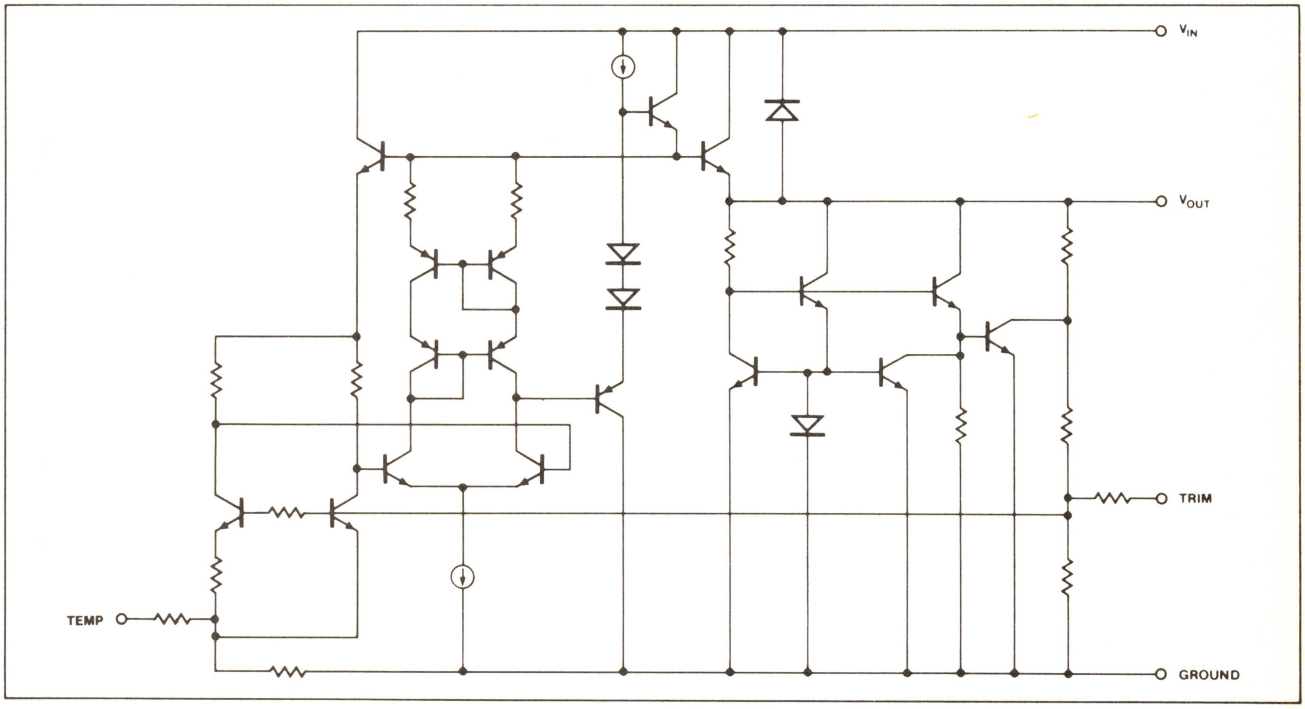

**8-PIN CERDIP**
**(Z-Suffix)**

**8-PIN PLASTIC DIP**
**(P-Suffix)**




**TO-99**
**(J-Suffix)**

### SIMPLIFIED SCHEMATIC




**This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.**

**9/87, Rev. B1**

Precision Monolithics Inc.

# PMI Product Selection Guides
# Operational Amplifiers and Conversion Products

## Low Offset Voltage Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP07 | 25 | 2 | 2 | 110 | 10 | 300 | 0.1 | 0.6 | 4 | 10.3 | 9.6 | 10.5 | 1 | 1 |
| OP27 | 25 | 40 | 35 | 114 | 10 | 1000 | 1.7 | 8 | 4.7 | 3.5 | 3 | 16.7 | 1 | 1 |
| OP37 | 25 | 40 | 35 | 114 | 10 | 1000 | 11 | 63 | 4.7 | 3.5 | 3 | 16.7 | 1 | 1.4 |
| OP50 | 25 | 5 | 1 | 126 | 0.5 | 10000 | 2.5 | 15 | 3.3 | 5.5 | 4.5 | 60 | 1 | 2.4.6 |
| OP77 | 25 | 2 | 1.5 | 120 | 3 | 5000 | 0.1 | 0.6 | 2 | 10.3 | 9.6 | 12 | 1 | 1 |
| OP97 | 25 | 0.1 | 0.1 | 114 | 2 | 300 | 0.1 | 0.6 | 0.6 | 17 | 14 | 5 | 1 | 1.9 |
| PM1012 | 35 | 0.1 | 0.1 | 114 | 2 | 300 | 0.1 | 0.6 | 0.6 | 17 | 14 | 5 | 1 | 1 |
| OP270 | 50 | 10 | 10 | 110 | 1.8 | 1000 | 1.4 | 6 | 2.5 | 2.6 | 2.0 | 6 | 2 | 1.9 |
| OP200 | 75 | 2 | 1 | 120 | 1.8 | 5000 | 0.1 | 0.5 | 0.725 | 22 | 11 | 5.5 | 2 | 1 |
| OP227 | 80 | 40 | 35 | 114 | 10 | 1000 | 1.7 | 8 | 4.7 | 3.5 | 3 | 16.7 | 2 | 2 |
| OP207 | 100 | 3 | 2.8 | 106 | 20 | 200 | — | 0.6 | 4 | 10.3 | 9.6 | 10 | 2 | 2 |
| OP21 | 100 | 100 | 4 | 100 | 6 | 1000 | — | 0.6 | 0.23 | — | — | 1.4 | 1 | 1 |
| PM1008 | 120 | 0.1 | 0.1 | 114 | 2 | 200 | 0.1 | 0.9 | 0.6 | 17 | 14 | 5 | 1 | 1.6 |
| OP05 | 150 | 2 | 2 | 114 | 10 | 300 | 0.1 | 0.6 | 4 | 10.3 | 9.6 | 10.5 | 1 | 1 |
| OP08 | 150 | 2 | 0.2 | 104 | 7 | 80 | — | — | 0.6 | 22 | 20 | 5 | 1 | 1.6 |
| OP12 | 150 | 2 | 0.2 | 104 | 7 | 80 | — | 0.8 | 0.6 | 22 | 20 | 5 | 1 | 1 |
| OP220 | 150 | 20 | 1.5 | 95 | 10 | 1000 | — | 0.2 | 0.09 | — | — | 0.56 | 2 | 1.7 |
| OP221 | 150 | 80 | 3 | 95 | 10 | 1500 | 0.2 | 0.6 | 0.4 | — | — | 1.4 | 2 | 1 |
| OP290 | 150 | 15 | 3 | 100 | 5.6 | 700 | 0.005 | 0.02 | 0.02 | 60 | 60 | 5.5 | 2 | 2.7.9 |
| OP400 | 150 | 3 | 1 | 120 | 1.8 | 5000 | 0.1 | 0.5 | 0.725 | 22 | 11 | 5.5 | 4 | 2 |
| OP90 | 150 | 15 | 3 | 100 | 5.6 | 700 | 0.005 | 0.02 | 0.02 | 60 | 60 | 5.5 | 1 | 1.7 |
| OP06 | 200 | 70 | 2 | 114 | 2 | 1000 | — | — | 4 | 9 | 7 | 11 | 1 | 1.6 |
| OP20 | 250 | 25 | 1.5 | 100 | 6 | 1000 | — | 0.1 | 0.055 | — | — | 0.56 | 1 | 1.7 |
| OP41 | 250 | 0.005 | 0.001 | 100 | 25 | 1000 | 1 | 0.5 | 1 | — | 32 | 12 | 1 | 1 |
| OP43 | 250 | 0.005 | 0.001 | 100 | 25 | 1000 | 5 | 2.5 | 1 | — | 32 | 12 | 1 | 1 |

## Low Power Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP22 | 300 | — | — | 100 | 6 | 1000 | — | — | — | — | — | — | 1 | 1.8 |
| OP32 | 300 | — | — | 100 | 6 | 1000 | — | — | — | — | — | — | 1 | 1.5.8 |
| OP290 | 150 | 15 | 3 | 100 | 5.6 | 700 | 0.005 | 0.02 | 0.02 | 60 | 60 | 5.5 | 2 | 1.7.9 |
| OP490 | 500 | 15 | 3 | 100 | 5.6 | 700 | 0.005 | 0.02 | 0.02 | 60 | 60 | 5 | 4 | 2.7 |
| OP90 | 150 | 15 | 3 | 100 | 5.6 | 700 | 0.005 | 0.02 | 0.02 | 60 | 60 | 5.5 | 1 | 1.7 |
| OP20 | 250 | 25 | 1.5 | 100 | 6 | 1000 | — | 0.1 | 0.055 | — | — | 0.56 | 1 | 1.7 |
| OP220 | 150 | 20 | 1.5 | 95 | 10 | 1000 | — | 0.2 | 0.09 | — | — | 0.56 | 2 | 1.7 |
| OP420 | 2500 | 20 | 1.5 | 83 | 30 | 600 | — | 0.15 | 0.09 | — | — | 0.56 | 4 | 2.7 |
| OP80 | 1000 | 0.00006 | — | 72 | 700 | 100 | 0.2 | 0.3 | 0.2 | — | 70 | 10 | 1 | 1.7.9 |
| OP21 | 100 | 100 | 4 | 100 | 6 | 1000 | — | 0.6 | 0.23 | — | — | 1.4 | 1 | 1 |
| OP221 | 150 | 80 | 3 | 95 | 10 | 1500 | 0.2 | 0.6 | 0.4 | — | — | 1.4 | 2 | 1 |
| OP421 | 2500 | 50 | 5 | 83 | 30 | 200 | 0.25 | 1.9 | 0.45 | 20 | 15 | 1.4 | 4 | 2 |
| OP08 | 150 | 2 | 0.2 | 104 | 7 | 80 | — | — | 0.6 | 22 | 20 | 5 | 1 | 1.6 |
| OP12 | 150 | 2 | 0.2 | 104 | 7 | 80 | — | 0.8 | 0.6 | 22 | 20 | 5 | 1 | 1 |
| OP97 | 25 | 0.1 | 0.1 | 114 | 2 | 300 | 0.1 | 0.6 | 0.6 | 17 | 14 | 5 | 1 | 1.9 |
| PM1008 | 120 | 0.1 | 0.1 | 114 | 2 | 200 | 0.1 | 0.6 | 0.6 | 17 | 14 | 5 | 1 | 1.6 |
| PM1012 | 35 | 0.1 | 0.1 | 114 | 2 | 300 | 0.1 | 0.6 | 0.6 | 17 | 14 | 5 | 1 | 1 |
| PM108 | 500 | 2 | 0.2 | 96 | 15 | 80 | — | — | 0.6 | — | — | 1.3 | 1 | 1.6 |
| PM2108 | 500 | 2 | 0.2 | 96 | 15 | 80 | — | — | 0.6 | — | — | 1.3 | 2 | 3.6 |
| OP200 | 75 | 2 | 1 | 120 | 1.8 | 5000 | 0.1 | 0.5 | 0.725 | 22 | 11 | 5.5 | 2 | 1 |
| OP400 | 150 | 3 | 1 | 120 | 1.8 | 5000 | 0.1 | 0.5 | 0.725 | 22 | 11 | 5.5 | 4 | 2 |
| OP41 | 250 | 0.005 | 0.001 | 100 | 25 | 1000 | 1 | 0.5 | 1 | — | 32 | 12 | 1 | 1 |
| OP43 | 250 | 0.005 | 0.001 | 100 | 25 | 1000 | 5 | 2.5 | 1 | — | 32 | 12 | 1 | 1 |

## DEFINITIONS

$V_{OS}$ = Maximum Offset Voltage
$I_B$ = Maximum Bias Current
$I_{OS}$ = Maximum Offset Current
CMR = Minimum Common-Mode Rejection
PSRR = Maximum Power-Supply Rejection Ratio
$A_{VO}$ = Minimum Large-Signal Voltage Gain
SR = Minimum Slew Rate
GBW = Typical Gain-Bandwidth Product
$I_{SY}$ = Maximum Supply Current (per amplifier)
$e_n$ @ 10Hz = Typical 10Hz Voltage Noise Density
$e_n$ @ 1kHz = Typical 1kHz Voltage Noise Density
$I_{OUT}$ = Minimum Output Current Drive
# of Ampls = Number of Amplifiers in Package

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## Low Bias Current Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP80 | 1000 | 0.00006 | — | 72 | 700 | 100 | 0.2 | 0.3 | 0.2 | — | 70 | 10 | 1 | 1,9 |
| OP41 | 500 | 0.005 | 0.001 | 100 | 25 | 1000 | 1 | 0.5 | 1 | — | 32 | 12 | 1 | 1 |
| OP43 | 250 | 0.005 | 0.001 | 100 | 25 | 1000 | 5 | 2.5 | 1 | — | 32 | 12 | 1 | 1,4 |
| OP15 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 10 | 6 | 4 | — | 15 | 5.5 | 1 | 1 |
| OP16 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 18 | 8 | 7 | — | 15 | 5.5 | 1 | 1 |
| OP17 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 45 | 30 | 7 | — | 15 | 5.5 | 1 | 1,4 |
| PM155A | 2000 | 0.05 | 0.01 | 85 | 57 | 50 | 3 | 2.5 | 4 | — | 20 | 5 | 1 | 1 |
| PM156A | 2000 | 0.05 | 0.01 | 85 | 57 | 50 | 10 | 4.5 | 7 | — | 12 | 5 | 1 | 1 |
| PM157A | 2000 | 0.05 | 0.01 | 85 | 57 | 50 | 40 | 20 | 7 | — | 12 | 5 | 1 | 1,4 |
| OP215 | 1000 | 0.1 | 0.05 | 86 | 51 | 150 | 10 | 5.7 | 4.25 | — | 15 | 5.5 | 2 | 1,2 |
| OP97 | 25 | 0.1 | 0.1 | 114 | 2 | 300 | 0.1 | 0.6 | 0.6 | 17 | 14 | 5 | 1 | 1,9 |
| PM1008 | 120 | 0.1 | 0.1 | 114 | 2 | 200 | 0.1 | 0.9 | 0.6 | 17 | 14 | 5 | 1 | 1,6 |
| PM1012 | 35 | 0.1 | 0.1 | 114 | 2 | 300 | 0.1 | 0.6 | 0.6 | 17 | 14 | 5 | 1 | 1 |
| OP42 | 750 | 0.2 | 0.04 | 88 | 40 | 500 | 50 | 10 | 6 | 38 | 13 | 20 | 1 | 1 |
| OP44 | 750 | 0.2 | 0.04 | 86 | 40 | 500 | 100 | 23 | 7 | 38 | 13 | 20 | 1 | 1,10 |

## Low-Noise Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP270 | 50 | 10 | 10 | 110 | 1.8 | 1000 | 1.4 | 6 | 2.5 | 2.6 | 2.0 | 6 | 2 | 1,9 |
| OP27 | 25 | 40 | 35 | 114 | 10 | 1000 | 1.7 | 8 | 4.7 | 3.5 | 3 | 16.7 | 1 | 1 |
| OP227 | 80 | 40 | 35 | 114 | 10 | 1000 | 1.7 | 8 | 4.7 | 3.5 | 3 | 16.7 | 2 | 2 |
| OP37 | 25 | 40 | 35 | 114 | 10 | 1000 | 11 | 63 | 4.7 | 3.5 | 3 | 16.7 | 1 | 1,4 |
| OP470 | 400 | 25 | 10 | 110 | 1.8 | 1000 | 1.4 | 6 | 2.75 | 3.8 | 3.2 | 6 | 4 | 2 |
| OP50 | 25 | 5 | 1 | 126 | 0.5 | 10000 | 2.5 | 15 | 3.3 | 5.5 | 4.5 | 60 | 1 | 2,4,6 |
| OP271 | 300 | 10 | 10 | 110 | 5.6 | 1000 | 6.5 | 6.5 | 2.5 | 9 | 6.5 | 6 | 2 | 1,9 |
| OP471 | 800 | 25 | 10 | 105 | 5.6 | 500 | 6.5 | 6.5 | 2.75 | 9 | 6.5 | 6 | 4 | 2 |

## High Slew-Rate Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP44 | 750 | 0.2 | 0.04 | 86 | 40 | 500 | 100 | 23 | 7 | 38 | 13 | 20 | 1 | 1,10 |
| OP06 | 200 | 70 | 2 | 114 | 2 | 1000 | — | — | 4 | 9 | 7 | 11 | 1 | 1,6 |
| OP42 | 750 | 0.2 | 0.04 | 88 | 40 | 500 | 50 | 10 | 6 | 38 | 13 | 20 | 1 | 1 |
| OP17 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 45 | 30 | 7 | — | 15 | 5.5 | 1 | 1,4 |
| PM157A | 2000 | 0.05 | 0.01 | 85 | 57 | 50 | 40 | 20 | 7 | — | 12 | 5 | 1 | 1,4 |
| OP16 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 18 | 8 | 7 | — | 15 | 5.5 | 1 | 1 |
| OP01 | 700 | 30 | 2 | 85 | 60 | 50 | 12 | 2.5 | 3 | — | — | 6 | 1 | 1 |
| OP37 | 25 | 40 | 35 | 114 | 10 | 1000 | 11 | 63 | 4.7 | 3.5 | 3 | 16.7 | 1 | 1,4 |
| OP15 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 10 | 6 | 4 | — | 15 | 5.5 | 1 | 1 |
| OP215 | 1000 | 0.1 | 0.05 | 86 | 51 | 150 | 10 | 5.7 | 4.25 | — | 15 | 5.5 | 2 | 1,2 |
| PM156A | 2000 | 0.05 | 0.01 | 85 | 57 | 50 | 10 | 4.5 | 7 | — | 12 | 5 | 1 | 1 |
| OP271 | 300 | 10 | 10 | 110 | 5.6 | 1000 | 6.5 | 6.5 | 2.5 | 9 | 6.5 | 6 | 2 | 1,9 |
| OP471 | 800 | 25 | 10 | 105 | 5.6 | 500 | 6.5 | 6.5 | 2.75 | 9 | 6.5 | 6 | 4 | 2 |
| OP43 | 250 | 0.005 | 0.001 | 100 | 25 | 1000 | 5 | 2.5 | 1 | — | 32 | 12 | 1 | 1,4 |

## Wideband Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP06 | 200 | 70 | 2 | 114 | 2 | 1000 | — | — | 4 | 9 | 7 | 11 | 1 | 1,6 |
| OP37 | 25 | 40 | 35 | 114 | 10 | 1000 | 11 | 63 | 4.7 | 3.5 | 3 | 16.7 | 1 | 1,4 |
| OP17 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 45 | 30 | 7 | — | 15 | 5.5 | 1 | 1,4 |
| OP44 | 750 | 0.2 | 0.04 | 86 | 40 | 500 | 100 | 23 | 7 | 38 | 13 | 20 | 1 | 1,10 |
| PM157A | 2000 | 0.05 | 0.01 | 85 | 57 | 50 | 40 | 20 | 7 | — | 12 | 5 | 1 | 1,4 |
| OP50 | 25 | 5 | 1 | 126 | 0.5 | 10000 | 2.5 | 15 | 3.3 | 5.5 | 4.5 | 60 | 1 | 2,4,6 |
| OP42 | 750 | 0.2 | 0.04 | 88 | 40 | 500 | 50 | 10 | 6 | 38 | 13 | 20 | 1 | 1 |
| OP32 | 300 | — | — | 100 | 6 | 1000 | — | — | — | — | — | — | 1 | 1,5,8 |
| OP16 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 18 | 8 | 7 | — | 15 | 5.5 | 1 | 1 |
| OP227 | 80 | 40 | 35 | 114 | 10 | 1000 | 1.7 | 8 | 4.7 | 3.5 | 3 | 16.7 | 2 | 2 |
| OP27 | 25 | 40 | 35 | 114 | 10 | 1000 | 1.7 | 8 | 4.7 | 3.5 | 3 | 16.7 | 1 | 1 |
| OP271 | 300 | 10 | 10 | 110 | 5.6 | 1000 | 6.5 | 6.5 | 2.5 | 9 | 6.5 | 6 | 2 | 1,9 |
| OP471 | 800 | 25 | 10 | 105 | 5.6 | 500 | 6.5 | 6.5 | 2.75 | 9 | 6.5 | 6 | 4 | 2 |
| OP15 | 500 | 0.05 | 0.01 | 86 | 51 | 100 | 10 | 6 | 4 | — | 15 | 5.5 | 1 | 1 |
| OP270 | 50 | 10 | 10 | 110 | 1.8 | 1000 | 1.4 | 6 | 2.5 | 2.6 | 2.0 | 6 | 2 | 1,9 |
| OP470 | 400 | 25 | 10 | 110 | 1.8 | 1000 | 1.4 | 6 | 2.75 | 3.8 | 3.2 | 6 | 4 | 2 |

## 8-Pin Dual Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP270 | 50 | 10 | 10 | 110 | 1.8 | 1000 | 1.4 | 6 | 2.5 | 2.6 | 2.0 | 6 | 2 | 1,9 |
| OP200 | 75 | 2 | 1 | 120 | 1.8 | 5000 | 0.1 | 0.5 | 0.725 | 22 | 11 | 5.5 | 2 | 1 |
| OP220 | 150 | 20 | 1.5 | 95 | 10 | 1000 | — | 0.2 | 0.09 | — | — | 0.56 | 2 | 1,7 |
| OP221 | 150 | 80 | 3 | 95 | 10 | 1500 | 0.2 | 0.6 | 0.4 | — | — | 1.4 | 2 | 1 |
| OP290 | 150 | 15 | 3 | 100 | 5.6 | 700 | 0.005 | 0.02 | 0.02 | 60 | 60 | 5.5 | 2 | 1,7,9 |
| OP271 | 300 | 10 | 10 | 110 | 5.6 | 1000 | 6.5 | 6.5 | 2.5 | 9 | 6.5 | 6 | 2 | 1,9 |
| OP14 | 750 | 50 | 5 | 85 | 60 | 100 | 0.25 | 1.3 | 3 | 25 | 21 | 6 | 2 | 1 |
| OP215 | 1000 | 0.1 | 0.05 | 86 | 51 | 150 | 10 | 5.7 | 4.25 | — | 15 | 5.5 | 2 | 1,2 |

## 14-Pin Quad Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP400 | 150 | 3 | 1 | 120 | 1.8 | 5000 | 0.1 | 0.5 | 0.725 | 22 | 11 | 5.5 | 4 | 2 |
| OP470 | 400 | 25 | 10 | 110 | 1.8 | 1000 | 1.4 | 6 | 2.75 | 3.8 | 3.2 | 6 | 4 | 2 |
| OP09 | 500 | 300 | 20 | 100 | 32 | 100 | 0.7 | 3 | 1.5 | 18 | 12 | 5.5 | 4 | 2 |
| OP11 | 500 | 300 | 20 | 100 | 32 | 100 | 0.7 | 3 | 1.5 | 18 | 12 | 5.5 | 4 | 2 |
| OP490 | 500 | 15 | 3 | 100 | 5.6 | 700 | 0.005 | 0.02 | 0.02 | 60 | 60 | 5 | 4 | 2,7 |
| OP471 | 800 | 25 | 10 | 105 | 5.6 | 500 | 6.5 | 6.5 | 2.75 | 9 | 6.5 | 6 | 4 | 2 |
| OP420 | 2500 | 20 | 1.5 | 83 | 30 | 600 | — | 0.15 | 0.09 | — | — | 0.56 | 4 | 2,7 |
| OP421 | 2500 | 50 | 5 | 83 | 30 | 200 | 0.25 | 1.9 | 0.45 | 20 | 15 | 1.4 | 4 | 2 |

## 14 & 16 Pin Dual Operational Amplifiers

| Product | $V_{OS}$ μV | $I_b$ nA | $I_{OS}$ nA | CMR dB | PSRR μV/V | $A_{VO}$ V/mV | SR V/μs | GBW MHz | $I_{SY}$ mA | $e_n$@10Hz nV/√Hz | $e_n$@1kHz nV/√Hz | $I_{OUT}$ mA | # of Ampls | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OP227 | 80 | 40 | 35 | 114 | 10 | 1000 | 1.7 | 8 | 4.7 | 3.5 | 3 | 16.7 | 2 | 2 |
| OP207 | 100 | 3 | 2.8 | 106 | 20 | 200 | — | 0.6 | 4 | 10.3 | 9.6 | 10 | 2 | 2 |
| OP10 | 500 | 3 | 2.8 | 110 | 10 | 200 | — | 0.6 | 4 | 10.3 | 9.6 | 10.5 | 2 | 2 |
| PM2108 | 500 | 2 | 0.2 | 96 | 15 | 80 | — | — | 0.6 | — | — | 1.3 | 2 | 6,8 |
| OP04 | 750 | 50 | 5 | 85 | 60 | 100 | 0.25 | 1.3 | 3 | 25 | 21 | 6 | 2 | 2 |
| OP215 | 1000 | 0.1 | 0.05 | 86 | 51 | 150 | 10 | 5.7 | 4.25 | — | 15 | 5.5 | 2 | 1,2 |
| PM747 | 5000 | 500 | 200 | 70 | 150 | 50 | — | — | 2.8 | — | — | 5 | 2 | 2 |

**NOTES**

1. 8 pin package
2. 14 pin package
3. 16 pin package
4. $A_{VCL} \geq 5$
5. $A_{VCL} \geq 10$
6. Externally compensated
7. Single-supply capable
8. Programmable supply current
9. Preliminary specifications
10. $A_{VCL} \geq 3$





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## 8-Bit Resolution Analog-to-Digital Converters

| Product | Type | Conversion Time (μs) | Linearity Error | Supply Voltage | Reference Voltage | Input Voltage Range | Digital Output Coding |
|---|---|---|---|---|---|---|---|
| PM0820 | CMOS Half-Flash | 1.5 | ±1/2LSB | +5 | +5 | +5 | Binary |
| ADC908 | CMOS SAR | 6 | ±1/2LSB | +5 | −10 | +10<br>±10 | Binary<br>Offset Binary |
| PM7574 | CMOS SAR | 15 | ±1/2LSB | +5 | −10 | +10<br>±10 | Binary<br>Offset Binary |

## 10-Bit Resolution Analog-to-Digital Converter

| Product | Type | Conversion Time (μs) | Linearity Error | Supply Voltage | Reference Voltage | Input Voltage Range | Digital Output Coding |
|---|---|---|---|---|---|---|---|
| ADC910 | Bipolar SAR | 6 | ±1/2LSB | ±5 | 2.5<br>Int | +5, +10<br>±5, ±10 | Binary<br>Offset Binary |

## 12-Bit Resolution Analog-to-Digital Converter

| Product | Type | Conversion Time (μs) | Linearity Error | Supply Voltage | Reference Voltage | Input Voltage Range | Digital Output Coding |
|---|---|---|---|---|---|---|---|
| ADC9012 | CMOS SAR | 12 | ±1/2LSB | +5, −12 | −5 | +10 | Binary |

## 8-Bit Resolution Single Digital-to-Analog Converters

| Product | Type | Settling Time to 1/2LSB (μs) | Linearity INL | Linearity DNL | Gain Error | Output Range | Ref. Input | Power Dissipation (mW) | Digital Input Coding | Digital Interface Architecture |
|---|---|---|---|---|---|---|---|---|---|---|
| DAC08 | Bipolar | 0.135 | 0.1%FS | ±1LSB | 2.5%FS | 2mA | 2mA | 136 | Binary | Parallel |
| DAC20 | Bipolar | 0.150 | ±1/2LSB | ±1LSB | 2.5%FS | 2mA | 2mA | 194 | 2 Digit BCD | Parallel |
| PM7524 | CMOS | 0.300 | ±1/8LSB | ±1/4LSB | 1LSB | 1mA | 10V | 5 | Binary | Latch |
| DAC888 | Bipolar | 0.400 | 0.1%FS | ±1LSB | 2.5%FS | 2mA | 2mA | 190 | Binary | Latch |
| DAC208 | Bipolar | 0.750† | 0.1%FS | ±1/2LSB | 15%FS | +5 or ±10V | Int Ref | 315 | Sign-Magnitude | Parallel |
| PM7224 | CMOS | 5.0 | ±1/2LSB | ±1/2LSB | ±1/2LSB | 10V | 10V | 60 | Binary | Double-Latch |

## 8-Bit Resolution, Dual Digital-to-Analog Converters

| Product | Type | Settling Time to 1/2LSB (μs) | Linearity INL | Linearity DNL | Gain Error | Output Range | Ref. Input | Power Dissipation (mW) | Digital Input Coding | Digital Interface Architecture |
|---|---|---|---|---|---|---|---|---|---|---|
| PM7528 | CMOS | 0.350 | ±1/2LSB | ±1LSB | ±1LSB | 1mA | 10V | 5 | Binary | Latch |

## 8-Bit Resolution, Quad Digital-to-Analog Converters

| Product | Type | Settling Time to 1/2LSB (μs) | Linearity INL | Linearity DNL | Gain Error | Output Range | Ref. Input | Power Dissipation (mW) | Digital Input Coding | Digital Interface Architecture |
|---|---|---|---|---|---|---|---|---|---|---|
| DAC8408 | CMOS | 0.250 | ±1/4LSB | ±1/2LSB | ±1LSB | 1mA | 10V | 5 | Binary | Readback-Latch |
| PM7226 | CMOS | 5.0 | ±1/2LSB | ±1/2LSB | ±1/2LSB | 10V | 10V | 250 | Binary | Latch |

† Typical Value

## 8-Bit Resolution, Companding Digital-to-Analog Converters

| Product | Type | Settling Time to 1/2LSB (μs) | Linearity INL | Linearity DNL | Gain Error | Output Range | Ref. Input | Power Dissipation (mW) | Digital Input Coding | Digital Interface Architecture |
|---|---|---|---|---|---|---|---|---|---|---|
| DAC88 | Bipolar, μ-law | 0.5† | ±1/2STEP | | ±1/2STEP | 2mA | 0.5mA | 263 | Sign-Chord Step | Parallel |
| DAC89 | Bipolar, A-law | 0.5† | ±1/2STEP | | ±1/2STEP | 2mA | 0.5mA | 263 | Sign-Chord Step | Parallel |

## 10-Bit Resolution Single Digital-to-Analog Converters

| Product | Type | Settling Time to 1/2LSB (μs) | Linearity INL | Linearity DNL | Gain Error | Output Range | Ref. Input | Power Dissipation (mW) | Digital Input Coding | Digital Interface Architecture |
|---|---|---|---|---|---|---|---|---|---|---|
| DAC10 | Bipolar | 0.150 | ±1/2LSB | ±1LSB | 0.09%FS | 4mA | 2mA | 285 | Binary | Parallel |
| DAC100 | Bipolar | 0.300 | 0.05%FS | ±1LSB | 11%FS | 2mA | Int Ref | 250 | Complementary | Parallel |
| PM7533 | CMOS | 0.600† | 0.05%FS | ±1LSB | 1.4%FS | 1mA | 10V | 30 | Binary | Parallel |
| DAC06 | Bipolar | 1.5 | 0.1%FS | ±1LSB | 15%FS | ±5V | Int Ref | 300 | 1's Complement | Parallel |
| DAC210 | Bipolar | 1.5 | 0.05%FS | ±1LSB | 15%FS | ±10V | Int Ref | 315 | Sign-Magnitude | Parallel |
| DAC03 | Bipolar | 2.0 | 0.1%FS | ±1LSB | 15%FS | +5 or +10V | Int Ref | 350 | Sign-Magnitude | Parallel |

## 12-Bit, Resolution, Single Digital-to-Analog Converters

| Product | Type | Settling Time to 1/2LSB (μs) | Linearity INL | Linearity DNL | Gain Error | Output Range | Ref. Input | Power Dissipation (mW) | Digital Input Coding | Digital Interface Architecture |
|---|---|---|---|---|---|---|---|---|---|---|
| DAC312 | Bipolar | 0.5 | 0.05%FS | ±1/2LSB | 1.6%FS | 4mA | 1mA | 305 | Binary | Parallel |
| DAC8012 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±1LSB | 1mA | 10V | 10 | Binary | Readback-Latch |
| DAC8043 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±1LSB | 1mA | 10V | 10 | Binary | Serial |
| PM7541 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±12.5LSB | 1mA | 10V | 10 | Binary | Parallel |
| PM7541A | CMOS | 1.0 | ±1/2LSB | ±1/2LSB | ±1LSB | 1mA | 10V | 10 | Binary | Parallel |
| PM7542 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±1LSB | 1mA | 10V | 10 | Binary | Nibble |
| PM7543 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±1LSB | 1mA | 10V | 10 | Binary | Serial |
| PM7545 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±1LSB | 1mA | 10V | 10 | Binary | Latch |
| PM7548 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±1LSB | 1mA | 10V | 10 | Binary | Byte-Latch |
| PM7645 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±1LSB | 1mA | 10V | 10 | Binary | Latch |
| PM562 | Bipolar | 1.5† | ±1/4LSB | ±1/2LSB | 0.2%FS† | 2mA | 10V | 465 | Binary | Parallel |

## 12-Bit Resolution, Dual Digital-to-Analog Converters

| Product | Type | Settling Time to 1/2LSB (μs) | Linearity INL | Linearity DNL | Gain Error | Output Range | Ref. Input | Power Dissipation (mW) | Digital Input Coding | Digital Interface Architecture |
|---|---|---|---|---|---|---|---|---|---|---|
| DAC8212 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±2LSB | 1mA | 10V | 10 | Binary | Latch |
| DAC8221 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±2LSB | 1mA | 10V | 10 | Binary | Latch |
| DAC8222 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±2LSB | 1mA | 10V | 10 | Binary | Double-Latch |
| DAC8248 | CMOS | 1.0 | ±1/2LSB | ±1LSB | ±2LSB | 1mA | 10V | 10 | Binary | Byte-Latch |

† Typical Value




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PMI also makes:

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  - AMP-01 Low-Noise Precision Instrumentation Amplifier
  - AMP-05 Fast-Settling JFET Instrumentation Amplifier
- High-Speed Buffer
  - BUF-03 High-Speed Voltage Follower/Buffer
- Voltage Comparators
  - CMP-01 Fast Precision Comparator
  - CMP-02 Low-Input-Current Precision Comparator
  - CMP-04 Quad Low-Power Precision Comparator
  - CMP-05 High-Speed Precision Comparator
  - CMP-08 High-Speed Comparator with ECL Outputs
  - CMP-404 Quad Low-Power Precision Comparator
  - PM-111/211 Precision Voltage Comparators
  - PM-119/219 Dual Comparators
  - PM-139/139A Quad Low-Power Voltage Comparators
- Precision Matched Transistors
  - MAT-01 Matched Monolithic Dual NPN Transistor
  - MAT-02 Low-Noise, Matched Dual Monolithic NPN Transistor
  - MAT-03 Low-Noise, Matched Dual PNP Transistor
  - MAT-04 Matched Monolithic Quad NPN Transistor
- Precision Voltage References
  - REF-01 +10V Precision Voltage Reference
  - REF-02 +5V Precision Voltage Reference/Temperature Transducer
  - REF-03 +2.5V Low-Cost Precision Voltage Reference
  - REF-05 +5V Precision Voltage Reference
  - REF-08 −10V/−10.24V Voltage Reference
  - REF-10 +10V Precision Voltage Reference
  - REF-43 +2.5V Low-Power Precision Voltage Reference
- Analog Switches and Multiplexers
  - SW01/02 Quad SPST JFET Analog Switches
  - SW-06 Quad SPST JFET Analog Switch
  - SW-201/202 Quad SPST JFET Analog Switches
  - SW-7510/7511 Quad SPST JFET Analog Switches
  - MUX-08/24 8-Channel/Dual 4-Channel JFET Analog Multiplexers
  - MUX-16/28 16-Channel/Dual 8-Channel JFET Analog Multiplexers
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  - SMP-10/11 Low-Droop-Rate/Accurate Sample-and-Hold Amplifiers
  - SMP-81 Telecommunications Sample-and-Hold Amplifier
- Special Analog Functions
  - PKD-01 Monolithic Peak Detector
- Communications Products
  - RPT-82/83 PCM Repeaters
  - RPT-86/87 Low Power PCM Repeaters
  - LIU-01 Serial Data Receiver

| ANALOG DEVICES | PRECISION MONOLITHICS | PMI PRICE ($)* | |
|---|---|---|---|
| AD7224 | PM7224HP | 3.96 | (Available 3rd Qtr. 1987) |
| AD7225 | DAC8408HP | 8.03 | (Functional replacement with data readback) |
| AD7226BCHIPS | PM7226GBC | 19.24 | (DICE) |
| AD7226BQ | PM7226FR | 19.96 | |
| AD7226KN | PM7226HP | 14.80 | |
| AD7226KP | PM7226HPC | 16.80 | (PLCC Package available 3rd Qtr. 1987) |
| AD7226TQ | PM7226BR | 51.80 | |
| AD7226TQ/883 | PM7226BR/883 | 65.40 | |
| AD7226TE/883 | PM7226BRC/883 | — | (LCC Package available 3rd Qtr. 1987) |
| AD7520JD, KD | PM7533FQ | 4.98 | (Improved exact replacements) |
| AD7520JN, KN | PM7533HP | 3.55 | |
| AD7520LD | PM7533EQ | 5.69 | |
| AD7520LN | PM7533GP | 4.26 | |
| AD7520SD, TD | PM7533BQ | 13.41 | |
| AD7520SD/, TD/883 | PM7533BQ/883 | 14.90 | |
| AD7520UD | PM7533AQ | 15.33 | |
| AD7520UD/883 | PM7533AQ/883 | 17.53 | |
| AD7521JD, KD, LD | PM7541FX | 7.07 | (Improved exact replacements) |
| AD7521JN, KN, LN | PM7541HP | 6.37 | |
| AD7521SD, TD, UD | PM7541BX | 20.66 | |
| AD7521SD/, TD/, UD/883 | PM7541BX/883 | 24.22 | |
| AD7523JN, KN | PM7524HP | 3.15 | (Exact replacement when N/C pins 12 & 13 tied to GND) |
| AD7523LN | PM7524GP | 5.25 | |
| AD7524ACHIPS | PM7524GBC | 4.67 | (DICE) |
| AD7524AD, AQ, BD, BQ | PM7524FQ | 6.80 | |
| AD7524CD, CQ | PM7524EQ | 9.18 | |
| AD7524JN, KN | PM7524HP | 3.15 | |
| AD7524LN | PM7524GP | 5.25 | |
| AD7524JP, KP | PM7524HPC | — | (PLCC package available 3rd Qtr. 1987) |
| AD7524SD, TD, TQ | PM7524BQ | 15.81 | |
| AD7524UD, UQ | PM7524AQ | 21.79 | |
| AD7524SD/, TD/883 | PM7524BQ/883 | 23.97 | |
| AD7524SQ/, TQ/883 | PM7524BQ/883 | 23.97 | |
| AD7524UD/883 | PM7524AQ/883 | 30.86 | |
| AD7524UQ/883 | PM7524AQ/883 | 30.86 | |
| AD7528ACHIPS | PM7528GBC | 4.89 | (DICE) |
| AD7528AQ, BQ | PM7528FR | 7.95 | |
| AD7528CQ | PM7528ER | 11.20 | |
| AD7528JN, KN | PM7528HP | 4.75 | |
| AD7528JP, KP | PM7528HPC | — | (PLCC package available 3rd Qtr. 1987) |
| AD7528LN | PM7528GP | 7.95 | |
| AD7528SE/, TE/883 | PM7528BRC/883 | — | (LCC package available 3rd Qtr. 1987) |
| AD7528SQ, TQ | PM7528BR | 17.42 | |
| AD7528UQ | PM7528AR | 20.35 | |
| AD7528SQ/, TQ/883 | PM7528BR/883 | 21.18 | |
| AD7528UQ/883 | PM7528AR/883 | 24.42 | |
| AD7530JD, KD | PM7533FQ | 4.98 | (Improved exact replacements) |
| AD7530JN, KN | PM7533HP | 3.55 | |
| AD7530LD | PM7533EQ | 5.69 | |
| AD7530LN | PM7533GP | 4.26 | |
| AD7531JD, KD | PM7541FX | 7.07 | (Improved exact replacements) |
| AD7531LD | PM7541EX | 7.78 | |
| AD7531JN, KN | PM7541HP | 6.37 | |
| AD7531LN | PM7541GP | 7.07 | |
| AD7533AQ, BQ | PM7533FQ | 4.98 | |
| AD7533CQ | PM7533EQ | 5.69 | |
| AD7533JN, KN | PM7533HP | 3.55 | |
| AD7533LN | PM7533GP | 4.26 | |
| AD7533SQ, TQ | PM7533BQ | 13.41 | |
| AD7533SQ/, TQ/883 | PM7533BQ/883 | 14.90 | |
| AD7533UQ | PM7533AQ | 15.33 | |
| AD7533UQ/883 | PM7533AQ/883 | 17.53 | |

| ANALOG DEVICES | PRECISION MONOLITHICS | PMI PRICE ($)* | |
|---|---|---|---|
| AD7537 | DAC8248 | — | (Improved functional replacement. Available 4th Qtr. 1987) |
| AD7541AACHIPS | PM7541AGBC | 9.31 | (DICE) |
| AD7541AAQ | PM7541AFX | 7.97 | |
| AD7541ABQ | PM7541AEX | 8.77 | |
| AD7541AJN | PM7541AHP | 7.17 | |
| AD7541AKN | PM7541AGP | 7.97 | |
| AD7541ASD | PM7541ABX | 23.25 | |
| AD7541ASD/883 | PM7541ABX/883 | 36.59 | |
| AD7541ATD | PM7541AAX | 27.12 | |
| AD7541ATD/883 | PM7541AAX/883 | 41.61 | |
| AD7541AD | PM7541FX | 7.07 | |
| AD7541BD | PM7541EX | 7.78 | |
| AD7541JN | PM7541HP | 6.37 | |
| AD7541KN | PM7541GP | 7.07 | |
| AD7541SD | PM7541BX | 20.66 | |
| AD7541SD/883 | PM7541BX/883 | 24.22 | |
| AD7541TD | PM7541AX | 24.10 | |
| AD7541TD/883 | PM7541AX/883 | 27.66 | |
| AD7542 | PM7542 | — | (Available 4th Qtr. 1987) |
| AD7543 | PM7543 | — | (Available 4th Qtr. 1987) |
| AD7545ACHIPS | PM7545GBC | 8.32 | (DICE) |
| AD7545AQ, BQ, CQ | PM7545FR | 7.60 | |
| AD7545GCQ | PM7545ER | 15.36 | |
| AD7545GLN | PM7545GP | 13.39 | |
| AD7545GUD, GUQ | PM7545AR | 46.08 | |
| AD7545GUD/, GUQ/883 | PM7545AR/883 | 54.49 | |
| AD7545JN, KN, LN | PM7545HP | 6.40 | |
| AD7545JP, KP, LP | PM7545HPC | — | (PLCC package available 3rd Qtr. 1987) |
| AD7545SD, SQ | PM7545BR | 21.60 | |
| AD7545SD/, SQ/883 | PM7545BR/883 | 27.23 | |
| AD7545TD, TQ | PM7545BR | 21.60 | |
| AD7545TD/, TQ/883 | PM7545BR/883 | 27.23 | |
| AD7545UD, UQ | PM7545BR | 21.60 | |
| AD7545UD/, UQ/883 | PM7545BR/883 | 27.23 | |
| AD7545SE/, TE/, UE/883 | PM7545BRC/883 | — | (LCC package available 3rd Qtr. 1987) |
| AD7547 | DAC8212HP | 13.05 | (Improved functional replacement) |
| AD7548AQ | PM7548FR | 9.04 | |
| AD7548BQ | PM7548ER | 10.56 | |
| AD7548JN | PM7548HP | 7.58 | |
| AD7548KN | PM7548GP | 9.20 | |
| AD7548SD | PM7548BR | 27.20 | |
| AD7548SD/883 | PM7548BR/883 | 37.08 | |
| AD7548TD | PM7548AR | 30.92 | |
| AD7548TD/883 | PM7548AR/883 | 41.36 | |

| MICROPOWER SYSTEMS | PRECISION MONOLITHICS | PMI PRICE ($)* |
|---|---|---|
| MP7623AD | PM7541AFX | 7.97 |
| MP7623BD | PM7541AEX | 8.77 |
| MP7623JN | PM7541AHP | 7.17 |
| MP7623KN | PM7541AGP | 7.97 |
| MP7623SD | PM7541ABX | 23.25 |
| MP7623TD | PM7541AAX | 27.12 |
| MP7628AD | DAC8408FT | 13.50 |
| MP7628BD | DAC8408ET | 18.90 |
| MP7628JN | DAC8408HP | 8.03 |
| MP7628KN | DAC8408GP | 13.50 |
| MP7628SD | DAC8408BT | 30.56 |
| MP7628TD | DAC8408AT | 35.82 |
| MP7645AD | PM7645FR | 7.60 |
| MP7645BD, CD | PM7645ER | 15.36 |
| MP7645JN | PM7645HP | 6.40 |
| MP7645KN, LN | PM7645GP | 13.39 |
| MP7645SD | PM7645BR | 21.60 |
| MP7645TD, UD | PM7645AR | 46.08 |

*100 piece US OEM price

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## Ordering Information

PM-7541 | BI | E | X | /883

**Device Type/Model Number**

**Burn-In Option**

PMI offers all 0°/70°C and −25°/+85°C devices with burn-in pin method 1015.5 of MIL-STD-883, 160 hours at +125°C or 80 hours at +150°C at PMI's option. Insert "BI" if burn-in is required. (For example, to order PM-7541EX with burn-in, the part number is PM-7541BIEX.)

**Electrical Grade**

Select electrical grade from data sheet.

**MIL-M-38510**

PMI's factory is certified to produce JAN parts per MIL-M-38510. Consult factory for availability of specific slash sheet part numbers.

**MIL-STD-883, Class B, Revision C Option**

**Package Type Suffix**

*Ceramic Dip:*

**Z** = 8 lead device package
**Y** = 14 lead device package
**Q** = 16 lead device package
**X** = 18 lead device package
**R** = 20 lead device package
**V** = 24 lead device package
**T** = 28 lead device package

**W** = *Ceramic "Skinny" DIP*

**P** = *Epoxy DIP*

*Leadless Chip Carrier (LCC):*

**RC** = 20 position device
**TC** = 28 position device

**PC** = *Plastic Leaded Chip Carrier (PLCC)*

**S** = *Small Outline Package (SOIC)*

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FAX 215-675-7463




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# High Performance Operational Amplifiers

| Device | Description | Maximum Input Specifications | | | Typical Input Noise Specifications | | | | Typ. Slew Rate (V/μS) | Typ. Unity Gain BW (MHz) | Max. Sply Volt. (±V) | Pins | Temp. Range |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Offset Volt. (mV) | Offset Cur. (nA) | Bias Cur. (nA) | 1kHz Volt. Density $\frac{nV}{\sqrt{Hz}}$ | Low Freq. Corner $e_N$ (Hz) | 1kHz Cur. Density $\frac{pA}{\sqrt{Hz}}$ | Low Freq. Corner $i_N$ (Hz) | | | | | |
| OP-05 | Single Inst. Op Amp | 0.50 | 2.8 | ±3 | 10 | 10 | 0.14 | 50 | 0.17 | 0.6 | 22 | 8 | M |
| OP-05A | Single Inst. Op Amp | 0.15 | 2.0 | ±2 | 10 | 10 | 0.14 | 50 | 0.17 | 0.6 | 22 | 8 | M |
| OP-05C | Single Inst. Op Amp | 1.3 | 6.0 | ±7 | 10 | 10 | 0.14 | 50 | 0.17 | 0.6 | 22 | 8 | C |
| OP-05E | Single Inst. Op Amp | 0.50 | 3.8 | ±4 | 10 | 10 | 0.14 | 50 | 0.15 | 0.6 | 22 | 8 | C |
| OP-07 | Single Ultra Low Offset Voltage | 0.075 | 2.8 | ±3 | 10 | 10 | 0.14 | 50 | 0.17 | 0.6 | 22 | 8 | M |
| OP-07A | Single Ultra Low Offset Voltage | 0.025 | 2.0 | ±2 | 10 | 10 | 0.14 | 50 | 0.17 | 0.6 | 22 | 8 | M |
| OP-07C | Single Ultra Low Offset Voltage | 0.150 | 6.0 | ±7 | 10.5 | 10 | 0.15 | 50 | 0.17 | 0.6 | 22 | 8 | C |
| OP-07D | Single Ultra Low Offset Voltage | 0.150 | 6.0 | ±12 | 10.5 | 10 | 0.15 | 50 | 0.17 | 0.6 | 22 | 8 | C |
| OP-07E | Single Ultra Low Offset Voltage | 0.075 | 3.8 | ±4 | 10.3 | 10 | 0.14 | 50 | 0.17 | 0.6 | 22 | 8 | C |
| OP-27A | Single Ultra Low Noise | 0.025 | 35 | ±40 | 3.0 | 2.7 | 0.4 | 140 | 2.8 | 8.0 | 22 | 8 | M, C |
| OP-27B | Single Ultra Low Noise | 0.060 | 50 | ±55 | 3.0 | 2.7 | 0.4 | 140 | 2.8 | 8.0 | 22 | 8 | M, C |
| OP-27C | Single Ultra Low Noise | 0.100 | 75 | ±80 | 3.2 | 2.7 | 0.4 | 140 | 2.8 | 8.0 | 22 | 8 | M, C |
| OP-27E | Single Ultra Low Noise | 0.025 | 35 | ±40 | 3.0 | 2.7 | 0.4 | 140 | 2.8 | 8.0 | 22 | 8 | M, C |
| OP-27F | Single Ultra Low Noise | 0.060 | 50 | ±55 | 3.0 | 2.7 | 0.4 | 140 | 2.8 | 8.0 | 22 | 8 | M, C |
| OP-27G | Single Ultra Low Noise | 0.100 | 75 | ±80 | 3.2 | 2.7 | 0.4 | 140 | 2.8 | 8.0 | 22 | 8 | M, C |
| OP-37A | Single High Slew Rate Low Noise | 0.025 | 35 | ±40 | 3.0 | 2.7 | 0.4 | 140 | 17 | 63 | 22 | 8 | M, C |
| OP-37B | Single High Slew Rate Low Noise | 0.060 | 50 | ±55 | 3.0 | 2.7 | 0.4 | 140 | 17 | 63 | 22 | 8 | M, C |
| OP-37C | Single High Slew Rate Low Noise | 0.100 | 75 | ±80 | 3.2 | 2.7 | 0.4 | 140 | 17 | 63 | 22 | 8 | M, C |
| OP-37E | Single High Slew Rate Low Noise | 0.025 | 35 | ±40 | 3.0 | 2.7 | 0.4 | 140 | 17 | 63 | 22 | 8 | M, C |
| OP-37F | Single High Slew Rate Low Noise | 0.060 | 50 | ±55 | 3.0 | 2.7 | 0.4 | 140 | 17 | 63 | 22 | 8 | M, C |
| OP-37G | Single High Slew Rate Low Noise | 0.100 | 75 | ±80 | 3.2 | 2.7 | 0.4 | 140 | 17 | 63 | 22 | 8 | M, C |
| OP-47B* | Low Noise, High Slew Op Amp | 0.06 | 50 | ±55 | 3.0 | 2.7 | 0.4 | 140 | 50 | 70 | 22 | 8 | M |
| OP-47F* | Low Noise, High Slew Op Amp | 0.06 | 50 | ±55 | 3.0 | 2.7 | 0.4 | 140 | 50 | 70 | 22 | 8 | C |
| OP-47G* | Low Noise, High Slew Op Amp | 0.10 | 75 | ±80 | 3.2 | 2.7 | 0.4 | 140 | 50 | 70 | 22 | 8 | C |
| RC714 | Single Precision | 0.075 | 2.8 | ±3 | 9.6 | 10 | 0.12 | 140 | 0.17 | 0.5 | 22 | 8 | C |
| RC714C | Single Precision | 0.150 | 6.0 | ±7 | 9.8 | 10 | 0.13 | 140 | 0.17 | 0.5 | 22 | 8 | C |
| RC714E | Single Precision | 0.075 | 3.8 | ±4 | 9.6 | 10 | 0.12 | 140 | 0.17 | 0.5 | 22 | 8 | C |
| RC714L | Single Precision | 0.250 | 20 | ±30 | 9.8 | 10 | 0.13 | 140 | 0.17 | 0.5 | 22 | 8 | C |
| RC3078 | Single Micropower | 4.5 | 32 | 170 | 19 | 100 | 1.0 | 200 | 0.04 | 0.1 | 7 | 8 | M, C |
| RC3078A | Single Micropower | 3.5 | 2.5 | 12 | 36 | 100 | 0.4 | 200 | 0.04 | 0.1 | 18 | 8 | M, C |
| RM5534 | Single High Perform. Low Noise | 2.0 | 200 | 800 | 4.0 | 100 | 0.6 | 200 | 13 | 10 | 22 | 8 | M, C |
| RM5534A | Single High Perform. Low Noise | 2.0 | 200 | 800 | 3.5 | 100 | 0.4 | 200 | 13 | 10 | 22 | 8 | M, C |

Notes: ( ) Denotes guaranteed specifications
M = Military/883B -55°C to 125°C
C = Commercial 0°C to 70°C
* = Preliminary specifications

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# RC/RM4207 Precision Monolithic Dual Operational Amplifier

## Features

- Low noise 0.1Hz to 10Hz — 0.35$\mu V_{p-p}$
- Ultra-low $V_{OS}$ — 30$\mu$V
- Ultra-low $V_{OS}$ drift — 0.2$\mu$V/°C
- Long term stability — 0.2$\mu$V/Mo
- Dual precision in 8-pin format
- Fits 4558, 1558 sockets
- Industry standard pinout
- Low input and offset current — ±3nA typical
- High gain — 1.0 × $10^6$V/V

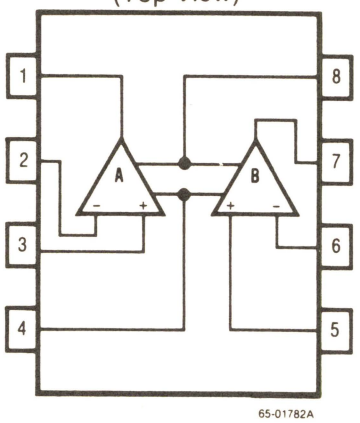
## Description

Designed for low level signal conditioning and instrumentation applications, the 4207 is a precision dual amplifier combining excellent dc input specifications with low input noise characteristics. Ultra low offset voltage, low drift, high CMRR, and low input bias currents serve to reduce input related errors to less than 0.01% in a typical high gain instrumentation amplifier system (Av = 1000). The 4207 contains two separate amplifiers with a high degree of isolation between them; each is complete, requiring no external compensation capacitors or offset nulling potentiometers. The inherent $V_{OS}$ is typically less than 150$\mu$V, resulting in superior temperature drift, and this low initial offset is further reduced by "Zener-zap" nulling when the wafers are tested.

Advanced thin film and nitride dielectric processing allows the 4207 to achieve its high performance and small size (the 4207 is offered in 8-lead DIPs). The 4207 fits the industry standard 8-lead op amp pin-out.

## Connection Information

**8-Lead**
**Dual In-Line Package**
(Top View)




| Pin | Function |
|---|---|
| 1 | Output A |
| 2 | Input A Inverting |
| 3 | Input A Non-Inverting |
| 4 | $-V_S$ |
| 5 | Input B Non-Inverting |
| 6 | Input B Inverting |
| 7 | Output B |
| 8 | $+V_S$ |

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# RC/RM4227 Precision Monolithic Dual Operational Amplifier

## Features

- Very low noise
  Spectral noise density — 3.0nV/$\sqrt{Hz}$
  1/f noise corner frequency — 2.7Hz
- Very low $V_{OS}$ drift
  0.2$\mu$V/Mo
  0.2$\mu$V/°C
- High gain — 1.8 × $10^6$V/V
- High output drive capability — ±10V into 1K load
- High slew rate — 2.7V/$\mu$S
- Wide gain bandwidth product — 8MHz
- Good common mode rejection ratio — 126dB
- Low input offset voltage — 20$\mu$V typ
- Low frequency noise — 0.08$\mu V_{p-p}$ 0.1Hz to 10Hz
- Low input offset current — 9nA typ
- Standard dual 8-lead pinout

## Description

The 4227 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70°) in a unity gain configuration. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 75$\mu$V max. Input bias current cancellation techniques are used to obtain ±55nA max. input bias currents.

The 4227 is especially useful for instrumentation and professional quality audio systems. The 4227 has an undistorted output up to its power bandwidth frequency of 34kHz, and an undistorted output of 8.0$V_{p-p}$ at 100kHz. This device provides performance adequate for the most demanding high fidelity applications.

In addition to providing superior performance for the professional audio market the 4227 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 120dB. A phase margin of 70° at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000pF[1]. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The performance of the 4227 is achieved through the usage of precision amplifier design techniques coupled with a process that combines nitride transistors and capacitors with precision thin-film resistors. The die size savings of nitride capacitors and thin film resistors allow for the 4227 to be offered in an 8-pin minidip package and fit the industry standard dual op amp pinout.

[1]By decoupling the load capacitance with a series resistor of 50 or more, load capacitances larger than 2000pF can be accommodated.

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# RC/RM4292 Negative Switch Mode Power Supply Controller

## Features

- Converts a negative voltage into positive and/or negative voltages
- Wide application voltage range: -20V minimum, -120V maximum
- High efficiency: 70% typical
- Adjustable output voltage
- Accurate oscillator frequency: ±10%
- Wide frequency range: 20 kHz to 100 kHz
- Bandgap voltage reference: 50 ppm/°C
- Good line regulation: 0.1%/V
- PWM feedback circuitry
- Short circuit protection
- Soft start
- 8-lead mini DIP
- Load power up to 10W
- Undervoltage lockout

## Applications

- Small power supplies
- Local on-card regulators
- Telephone peripheral equipment
- Converts -48V off-hook voltage
- Battery operated equipment

## Description

The RC4292 is a monolithic IC containing all the high level functional blocks required to build small power supplies. Although designed specifically for converting -48V off-hook telephone power at PBX and branch office exchanges, this IC is versatile and can be used for a variety of DC-to-DC converter applications, such as on-card regulators and battery operated equipment. The RC4292 controller IC interfaces with a transistor which serves as the power switch. A 350 mA output current drives this power switch transistor, which in turn controls the current in primary of a transformer. Passive components are used to steer and filter the transformer current, set the output voltage, set the level of current limiting, and determine the free-running oscillator frequency.

Contained internally are seven major circuit functions: temperature stabilized voltage reference, error amplifier, temperature stabilized oscillator, current comparator, PWM control flip-flop and logic, shunt regulator, and an output driver to interface with the external transistor. The combination of these elements with a simple application circuit yields a compact and efficient power supply. The high efficiency, low quiescent current, small size, and wide input voltage range of the 4292 make it ideal for telephone peripherals and also many other negative input switch mode regulator applications.

## Ordering Information

| Part Number | Package | Operating Temperature Range |
|---|---|---|
| RC4292DE | Ceramic | 0°C to +70°C |
| RC4292NB | Plastic | 0°C to +70°C |
| RM4292DE | Ceramic | -55°C to +125°C |

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# RC/RM4190 Micropower Switching Regulators

## Features

- High efficiency — 85% typical
- Low quiescent current — 215 $\mu$A
- Adjustable output — 1.3V to 30V
- High switch current — 150 mA
- Bandgap reference — 1.31V
- Accurate oscillator frequency — ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8-lead packages including small outline (S.O.)

## Description

The RC4190 monolithic IC is a low power switch mode regulator intended for miniature power supply applications. This DC-to-DC converter IC provides all of the active functions needed to create supplies for micropower circuits (load power up to 400 mW, or up to 10W with an external power transistor). Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

Application areas include on-card circuits where a non-standard voltage supply is needed, or in battery operated instruments where a 4190 can be used to extend battery lifetime.

These regulators can achieve up to 80% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 $\mu$A.

The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the 4190 adaptable to a wide range of miniature power supply applications.

The 4190 is most suited for single ended step-up circuits because the internal switch transistor is referenced to ground. It is complemented by another Raytheon micropower switching regulator, the 4391, which is dedicated to step-down and negative output (inverting) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the 4391 data sheet for step-down and inverting applications.

With some optional external components the application circuit can be designed to signal a display when the battery has decayed below a predetermined level, or designed to signal a display at one level and then shut itself off after the battery decays to a second level. See the applications section for these and other unique circuits.

The 4190 micropower switching regulator consists of two devices, each with slightly different specifications. The RM4190 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The RC4190 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical. Each type is available in plastic and ceramic DIPs, or S.O. packages..

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# RLA Linear Macrocell Array

## Device Features

### General

- Dual-layer metal for ease of interconnect routing and maximum array utilization
- Binarily weighted thin-film resistors having superior performance and ease of use
- Bipolar transistors arranged as:
  - User-configurable gain cells of 10 transistors each
  - Small NPN transistors
  - Small PNP transistors
  - 200mA NPN transistors
- Wide supply voltage range — 2V to 32V (±1V to ±16V)
- Available in LCC, PLCC and other packages
- Die size —
  - 135 mils × 95 mils (RLA80)
  - 148 mils × 119 mils (RLA120)
  - 189 mils × 123 mils (RLA160)

### Component

- Resistors:
  - ±10% absolute resistor tolerance (max)
  - ±1% resistor matching (identical values)
  - ±100 ppm per °C absolute resistor tempco
  - ±5 ppm per °C resistor tempco tracking
- With macro gain cell in op amp configuration:
  - Slew rates to 5 V/μS (2 V/μS in unity gain)
  - Unity gain bandwidth to 20 MHz
  - 1 mV input offset voltage (5 mV max)
  - 30 nA input bias current
  - 1 nA input offset current
  - 80 dB dc voltage gain into 10 kΩ load
- With macro gain cell in comparator configuration:
  - Propagation delay to 300 nS
  - 1 mV input offset voltage (5 mV max)
  - 1 mA output sink current (min)
- Transistors:
  - Breakdown voltage: 32V
  - 500 MHz NPN $F_T$
  - 4 MHz PNP $F_T$
  - NPN $H_{FE}$ = 100 (min)
  - PNP $H_{FE}$ = 30 (min)

## Device Description

RLA ICs are primarily made up of op amp/comparator cells and thin-film resistors. Other components are included to help support these cells and resistors in creating a wide variety of application circuits. The user integrates op amps, comparators, precision resistors, and NPN/PNP transistors into a specific design. The final result is a monolithic IC containing feedback amplifiers, filters, one shots, and other circuits, combined together to attain high-level functions.

### IC Processing

Wafers are manufactured using Raytheon's standard bipolar planar process at Raytheon's own Mountain View, California site. This process, which has been well characterized, is used to make many military and commercial IC products. The use of this process has two advantages: it allows building military grade parts and it allows any semicustom design to be easily converted to a full custom design. This provides a trouble-free transition from low volume to high volume production, with semicustom devices turned around quickly and low-cost, full custom devices arriving later.

The process uses bipolar transistors to form op amps capable of withstanding ±16V supply voltages.

**RLA Series Comparison Chart**

| | RLA80 | RLA120 | RLA160 |
|---|---|---|---|
| Gain Cells | 8 | 12 | 15 |
| Large NPN | 3 | 4 | 4 |
| Small NPN | 46 | 39 | 43 |
| Small PNP | 19 | 16 | 10 |
| Resistors | 95 | 196 | 240 |
| Bonding Pads | 24 | 24 | 44 |
| Voltage Reference | No* | No* | Yes |

*May easily be configured.


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# 29000 Series Field Programmable Read-Only Memories

## Features

- Low power Schottky technology
- Highly reliable nichrome fuses
- Three-state outputs
- PROM and SPROM versions of all configurations
- Typical SPROM "OFF" power is 25% of standard power
- SPROMs feature guaranteed access times and full $V_{CC}$ tolerance under power-switched conditions
- All devices use same programming techniques (generic)
- All devices available in both commercial (0° C to +75° C) and military (-55° C to +125° C) versions
- All devices are industry standard pin-out
- All devices available in flat packages
- 16K and 32K devices available in 0.3" wide 24-pin dual in-line packages
- 8K and 32K devices available in leadless chip carriers

## Applications

- Prototyping/volume production
- Non-volatile fixed instructions
- Microprogram control storage
- Complex LSI logic simulation
- Custom look-up tables
- Security encoding/decoding
- Error correction
- Code conversion
- Character generation

## Description

Raytheon's 29000 Series of Bipolar Field Programmable Read-Only Memories includes most of the popular PROM configurations in both standard and power-switched versions. The power-switched devices (SPROMs) were originated by Raytheon to reduce overall power dissipation in large PROM arrays. This technique takes advantage of the non-volatile nature of PROMs by removing power when a particular device is not being used in the system. Unlike previous power-switching schemes, which employed external transistors and resistors, the SPROM includes all power-switching circuitry on the same chip as the memory. Moreover, the power switch is activated by the same Chip Select (CS) input that is used to address a standard PROM; thus, in most cases, SPROMs can be directly substituted for standard devices without system redesign.

All Raytheon 29000 Series PROMs and SPROMs are manufactured with nichrome fuses and low power Schottky technology. The devices are shipped with all bits in the HIGH (logical ONE) state. To achieve a LOW state in a given bit position, the nichrome link is fused open by passing a short, high-current pulse through the link. All 29000 Series devices are programmed using the same programming technique.

Raytheon

**Raytheon Company**
**Semiconductor Division**
350 Ellis Street
Mountain View, CA 94039-7016
(415) 968-9211
TWX: 910-379-6484

65-1057I 10/85

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## Absolute Maximum Ratings (Above which the useful life may be impaired).

Junction Temperature ..... -65°C to +175°C
Storage Temperature ..... -65°C to +150°C
Temperature
Under Bias ..... -55°C to +125°C
Supply Voltage to Ground
Potential (Continuous) .... -0.5V to +7.0V
DC Voltage Applied to
Outputs (Except During
Programming) ..... -0.5V to +$V_{CC}$ Max

DC Input Voltage
(Address Inputs) ..... -0.5V to +5.5V
DC Voltage Applied to Outputs
During Programming ..... 26V
Output Current into Outputs
During Programming ..... 250mA
DC Input Voltage
(Chip Select Input-Pin) ..... -0.5V to +33V
DC Input Current ..... -30mA to +5.0mA

## Operating Range

| | | | |
|---|---|---|---|
| 29000XC | $T_A$ = 0°C to +75°C | $V_{CC}$ = 5.0V ±5% | Commercial |
| 29000XM | $T_C$ = -55°C to +125°C | $V_{CC}$ = 5.0V ±10% | Military |

X denotes package type. Refer to the ordering information for complete details.

## Common Electrical Characteristics Over Operating Range (unless otherwise noted)

| Parameter | Description | Test Conditions | | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{CC}$ = Min, $I_{OH}$ = -2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | 3.6 | | V |
| $V_{OL}$[3] | Output Low Voltage | $V_{CC}$ = Min | $I_{OL}$ = 8.0mA | | 0.30 | 0.4 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA | | 0.35 | 0.5 | |
| $V_{IH}$ | Input High Level | Guaranteed Input Logical High Voltage for All Inputs | | 2.0 | | 5.5 | V |
| $V_{IL}$ | Input Low Level | Guaranteed Input Logical Low Voltage for All Inputs | | 0.0 | | 0.8 | V |
| $I_{IL}$ | Input Low Current | $V_{CC}$ = Max, $V_{IN}$ = 0.4V | | | -10 | -250 | μA |
| $I_{IH}$ | Input High Current | $V_{CC}$ = Max, $V_{IN}$ = 2.7V | | | | 10 | μA |
| | | $V_{CC}$ = Max, $V_{IN}$ = 5.5V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = Max, $V_{OUT}$ = 0.2V (Note 2) | | -12 | -35 | -85 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_{IN}$ = -18mA | | | | -1.5 | V |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = Max | $V_O$ = 4.5V | | | +100 | μA |
| | | Chip Disabled | $V_O$ = 0.45V | | | -100 | |

Notes: 1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = +25°C
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. This characteristic cannot be tested prior to programming; it is guaranteed by factory testing.

Raytheon


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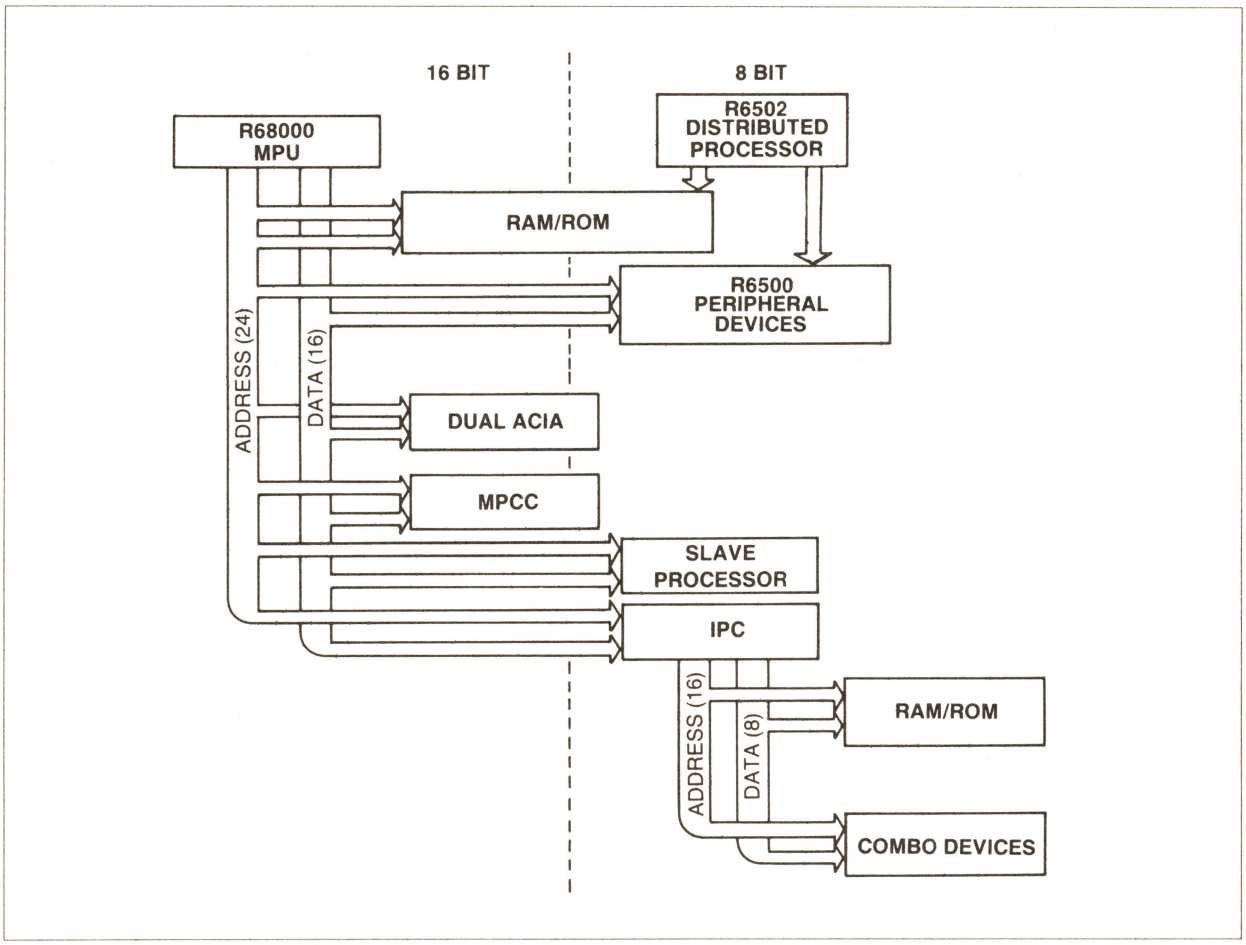
# ROCKWELL INTERNATIONAL
# SEMICONDUCTOR PRODUCTS DIVISION
## Providing Solutions for Your System Requirements

Rockwell International designs and manufactures a family of VLSI products to serve your system requirements. As shown in the diagram below, compatible controller products are available for a wide range of 16-bit and 8-bit applications. Peripheral devices operate on either the 68000 or the 6500 microprocessor bus structure. Many of the peripheral devices are now being used on additional bus structures such as 8085, 80286 and Z80, just to name a few.

These products are produced in high volume at a modern state-of-the-art facility located in Newport Beach, California, and are packaged in a newly constructed, fully automated manufacturing facility in Mexicali, Mexico. The class 10,000 clean room environment produces devices to the most stringent industry standards. Rockwell has the organization, systems and support to manufacture products to existing and future quality levels.

Rockwell is the first and only semiconductor company to offer a 5 year warranty. You can rely on customer satisfaction and service when choosing a Rockwell semiconductor product.

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Rockwell International

# CMOS and NMOS 8-Bit Microcomputers
# Highest Industry Performers

The R6500 single-chip CMOS and NMOS microcomputers provide high-speed and low-power CMOS while being completely software compatible with the 8-bit multi-chip family. They let you move easily from a multi-chip to a single-chip solution when the application warrants. They also function as intelligent peripheral controllers. The R65C10, a CMOS version of the R6500/1, combines the low power of CMOS with advanced pipelining architecture to provide an efficient high-speed single-chip system solution.

We also offer a set of extremely versatile FORTH language devices. The R65F11 and R65F12 contain both the high level language and operating system that can put your product on the market in the shortest possible time.

| FEATURE/MODELS | R6500/1 | R6500/11 | R6500/12 | R6500/13 | R6500/15 | R65C10 |
|---|---|---|---|---|---|---|
| • INSTRUCTION SPEED | 1000ns | 1000ns | 1000ns | 1000ns | 1000ns | 500ns |
| • ROM (x8) | 2K | 3K | 3K | 256 | 4K | 2K |
| • RAM (x8) | 64 | 192 | 192 | 192 | 192 | 64 |
| • I/O LINES | 32 | 32 | 56 | 32 | 32 | 32 |
| • SERIAL COMM. | — | USART | USART | USART | USART | — |
| • 16-BIT COUNTERS | ONE | TWO | TWO | TWO | TWO | ONE |
| • EXPANSION BUS | — | 16K | 16K | 65K | 16K | — |
| • INTERRUPTS | | | | | | |
| — EXTERNAL | 5 | 6 | 6 | 6 | 6 | 5 |
| — INTERNAL | 1 | 4 | 4 | 4 | 4 | 1 |
| • OPERATING POWER (mW) | 750 | 800 | 800 | 800 | 800 | 40 |
| • STANDBY (mW) | 35* | 12* | 12* | 12* | 12* | 12 |
| • PACKAGE | 40 DIP<br>44 PLCC | 40 DIP<br>44 PLCC | 64 QUIP<br>68 PLCC | 64 QUIP<br>68 PLCC | 40 DIP<br>44 PLCC | 40 DIP<br>44 PLCC |

* STANDBY RAM

**Rockwell Microcomputers**

| FEATURE/MODELS | R6501Q | R6511Q | R6518 |
|---|---|---|---|
| • INSTRUCTION SPEED | 1000ns | 1000ns | 1000ns |
| • RAM (x8) | 192 | 192 | 192 |
| • I/O LINES | 32 | 32 | 16 |
| • SERIAL COMM. | USART | USART | USART |
| • 16-BIT COUNTERS | TWO | TWO | TWO |
| • EXTERNAL MEMORY | 64K | 64K | 16K |
| • INTERRUPTS | | | |
| — EXTERNAL | 6 | 6 | 6 |
| — INTERNAL | 4 | 4 | 4 |
| • OPERATING POWER (mW) | 800 | 800 | 800 |
| • STANDBY RAM (mW) | 12 | 12 | 12 |
| • PACKAGE | 64 QUIP<br>68 PLCC | 64 QUIP<br>68 PLCC | 64 QUIP<br>44 PLCC |

**Rom-Less Microcomputers**

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Semiconductor Products Division

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Rockwell International

# 16-Bit Microprocessor and Peripherals Meeting System Communications Needs

Rockwell peripherals give a designer the communication control elements for the 68000 processor. They allow you to design functional systems utilizing all the speed and data handling potential of the 16-bit 68000 family.

The R68561 Multi-Protocol Communications Controller (MPCC) is one of the highest throughput communications devices ever commercially made. It operates up to 4 Mbits/sec and supports all major communication protocols. It is available to work with either a 16-bit or 8-bit bus and can be adapted to function with essentially any of today's more common busses.

The R68C552 Dual Asynchronous Interface Adapter (DACIA) provides an easily implemented, programmed controlled interface between 16-bit microprocessor-based systems and serial communication data sets and modems. This device is the first CMOS ACIA in the industry.

**16-Bit Processor**

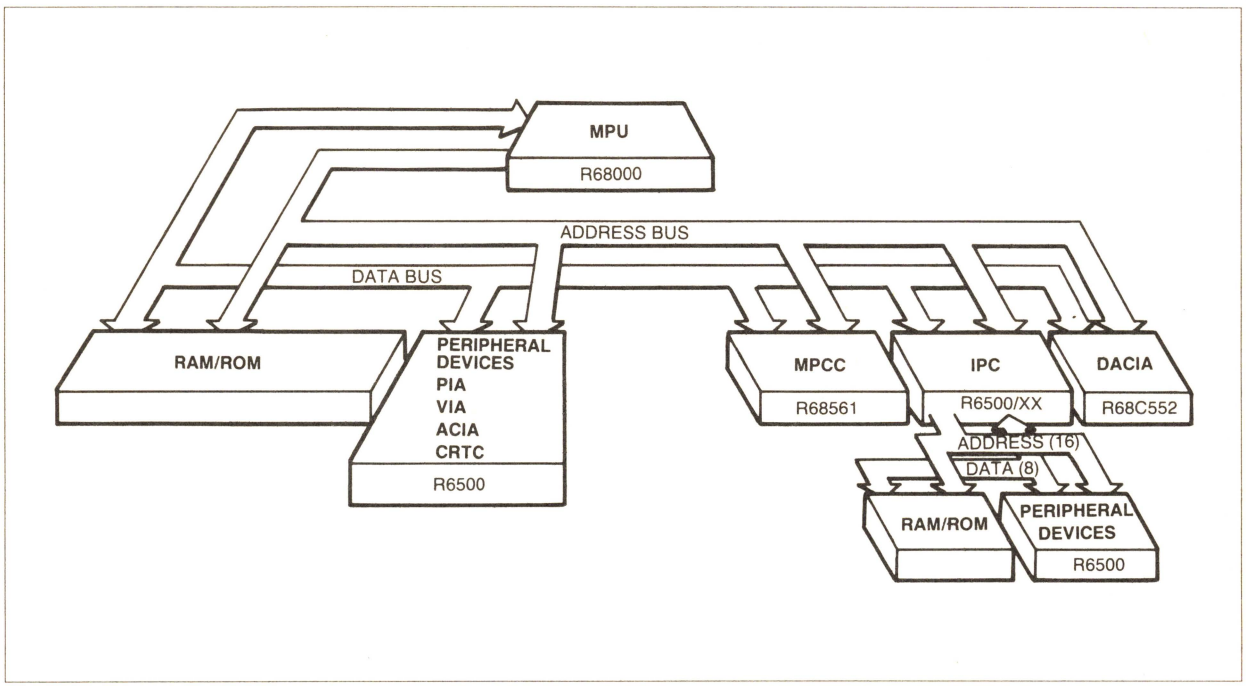
**R68000:** 16-bit Microprocessor Unit (MPU) performs high speed computations using powerful and flexible 8-, 16-, and 32-bit instructions, and can directly address up to 16 Mbyte of memory.

**16-Bit Peripherals** — Compatible with 68000 bus

**R68561:** Multi-Protocol Communications Controller (MPCC) interfaces to a single high speed channel (up to 4 Mbps.) supports popular synchronous or asynchronous formats, and performs protocol handling and checking.

**R68802:** Local Area Network Controller (LNET) implements the IEEE 802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CS) method to connect to a local network at rates up to 10 Mbps.

**R68C552:** Dual Synchronous Communications Adapater (DACIA) with on-board baud generator interfaces two independent asynchronous channels with 5-8 data bits. 1 or 2 stop bits, and odd, even or no parity; at 1 of 15 selectable rates (to 38,000 baud) or 1/16 external clock rate.




**R68000/R6500 Peripheral Migration**

Rockwell International
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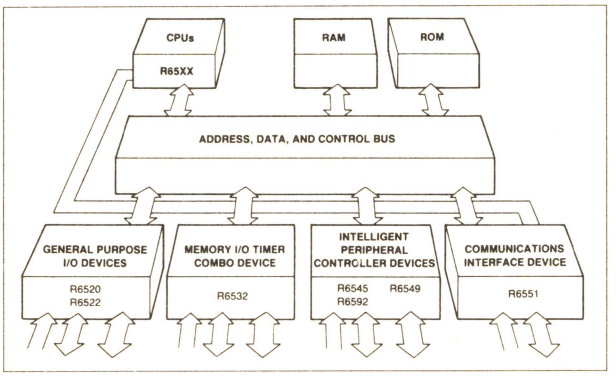
Rockwell International

# NMOS 8-bit Microprocessors and Peripherals Largest Selling 8-Bit Family

The NMOS R6500 microprocessor family has a wide range of CPUs and peripheral controllers plus versatile memory-I/O timer combinations. It is software compatible with the CMOS microprocessor and peripheral family, as well as, with the family of single-chip microcomputers. Fast instruction execution (1 $\mu$s and 2 $\mu$s) is available in 2 and 2 MHz versions, respectively.

The entire 8-bit R6500 family is upward compatible with the 16-bit 68000 bus, software compatible with the Rockwell 8-bit microcomputers, and are the building blocks for a wide range of system applications.




**NMOS R65XX Microprocessor Family**

**NMOS**

**8-Bit Processor**

**R6502:** 8-Bit Microprocessor Unit (MPU) provides high performance (down to 1 $\mu$s instruction time) using memory efficient byte-level instructions.

**8-Bit Peripherals** — 6500/6800 bus compatible

**R6520:** Peripheral Interface Adapter (PIA) interfaces two 8-bit bidirectional parallel data ports with four control lines and an interrupt request ouput on each port.

**R6522:** Versatile Interface Adapter (VIA) interfaces two 8-bit bidirectional parallel data ports, two 16-bit times, and an 8-bit serial port.

**R6530:** ROM-RAM-I/O Timer (RRIOT) combines 1K bytes read-only memory, 64 bytes random access memory, two 8-bit bidirectional ports, and an 8-bit interval timer.

**R6531:** ROM-RAM-I/O Counter (RRIOC) combines 2K bytes read-only memory, 128 bytes random access memory, a 16-bit counter/latch, and an 8-bit serial channel.

**R6545:** CRT Controller (CRTC) controls a a CRT raster scan video display at a character clock frequency of 2.5 MHz or 3.7 MHz using 19 registers to program display parameters such as number of rows, number of lines, sync positions and widths, row/column or straight binary addressing selection, and interlace/non-interlaced scan selection.

**R6551:** Asynchronous Communications Adapter (ACIA) with on-board baud generator interfaces an asynchronous channel with 5–8 data bits; 1 or 2 stop bits; and odd, even or no parity; at 1 of 15 selectable rates (to 38,000 baud), or 1/16 external clock rate.

**R6765:** Double-Density Floppy Disk Controller (DDFDC) controls up to four floppy disk drives, requires minimal external components, supports single-density (FM) and double-density (MDM) formats, and interfaces to an 8080 bus.

**Single Chip Controller**

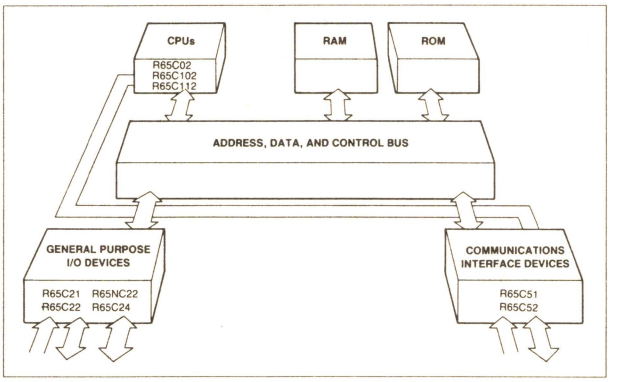
**R6592:** Printer Controller controls a wide range of Epson dot-matrix printers, generates 96 standard ASCII characters and 6 special characters, and requires a minimum of support circuitry.

# CMOS 8-bit Microprocessors & Peripherals Fastest Executing — Low Power

There is no CMOS microprocessor family easier to implement than the R65CXX. It is the fastest instruction executing 8-bit family available. It's software compatible with a family of single-chip microcomputers and has three powerful CPUs and peripherals for parallel and serial I/O.

In the 8-bit range, nothing gives faster instruction execution (500 $\mu$s) with most parts available in 1, 2, 3 and 4 MHz versions.

Because of its inherent characteristics, advanced Rockwell CMOS provides low power consumption, high noise immunity and high speed operation. Its 2 MHz CPU dissipates only 40 mW (compared to 800 mW in NMOS) and requires only 10 mA standby current. Instruction memory requirements are 20% less due to added bit manipulation features.




**CMOS R65CSS Microprocessor Family**

**8-Bit Processor and Peripherals**

**CMOS**

8-Bit Processors — 6500/6800 bus compatible

**R65C02/R65C102/R65112:** 8-Bit Microprocessor Units (MPUs) provides a high performance (down to 55 ns instruction time) using memory efficient bit and byte-level instructions.

**8-Bit Peripherals** — 6500/6800 bus compatible

**R65C21:** Peripheral Interface Adapter (PIA) interfaces two 8-bit bidirectional parallel data ports with four control lines and an interrupt request output on each port.

**R65C22:** Versatile Interface Adapted (VIA) interfaces two 8-bit bidirectional parallel data ports plus two 16-bit timers and an 8-bit serial port.

**R65C24:** Peripheral Interface Adapter/Timer (PIAT) interfaces two 8-bit bidirectional parallel data ports and a 16-bit Counter/Timer.

**R65C51:** Asynchronous Communications Adapter (ACIA) with on-board baud generators interfaces an asynchronous channel with 5–8 data bits; 1 or 2 stop bits; and odd, even or no parity; at 1 of 15 selectable rates (to 38,000 baud) or 1/16 external clock rate.

**R65C52:** Dual Asynchronous Communications Adapter (DACIA) with on-board baud generator interfaces two independent asynchronous channels with 5–8 data bits, and odd, even or no parity at 1 of 15 selectable rates (to 38,000 baud) or 1/16 external clock rate.

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Rockwell International

## HIGH DENSITY 5 VOLT EEPROMS

| Part no. | Speed | Icc (max/min) | Write Cycle | Endurance | Comments |
|---|---|---|---|---|---|
| 2804A | 250 ns | 80/25 ma | 10 ms | 10,000 cy | 512 byte EEPROM |
| 2816A | 200 ns | 100/25 ma | 10 ms | 10,000 cy | 2K byte EEPROM [3] |
| 2816AH | 200 ns | 100/25 ma | 2 ms | 10,000 cy | High speed byte write [3] |
| 5516A | 200 ns | 100/25 ma | 10 ms | 1,000,000 cy | High endurance/reliability [3] |
| 2817A | 200 ns | 100/25 ma | 10 ms | 10,000 cy | 2K bytes with ready-busy [2,3] |
| 2817AH | 200 ns | 100/25 ma | 2 ms | 10,000 cy | Fast byte write [2,3] |
| 5517A | 200 ns | 100/25 ma | 10 ms | 1,000,000 cy | High endurance/reliability [2,3] |
| 52B13 | 200 ns | 80/30 ma | 9 ms | 10,000 cy | 2K byte low cost [3] |
| 52B13H | 200 ns | 80/30 ma | 1 ms | 10,000 cy | High speed byte write [3] |
| 52B33 | 200 ns | 110/40 ma | 9 ms | 10,000 cy | 8K byte low cost [2,3] |
| 52B33H | 200 ns | 110/40 ma | 1 ms | 10,000 cy | High speed byte write [2,3] |
| 2864 | 200 ns | 100/35 ma | 10 ms | 10,000 cy | 8K bytes with ready-busy [2,3] |
| 2864H | 200 ns | 100/35 ma | 2 ms | 10,000 cy | Fast byte write [2,3] |
| 28C64 | 200 ns | 60 ma/150 μa | 10 ms | 10,000 cy | CMOS 64K with page mode [2,3] |
| 28C256 | 250 ns | 60 ma/150 μa | 10 ms | 10,000 cy | CMOS 256K with page mode [2,3] |
| 36C16 | 35 ns | 100 ma | 5 ms | 100 cy | 2K byte bipolar PROM pinout [1,3] |
| 38C16 | 35 ns | 100/50 ma | 5 ms | 10,000 cy | 2K byte JEDEC bytewide pinout [3] |
| 36C32 | 35 ns | 100 ma | 5 ms | 100 cy | 4K byte bipolar PROM pinout [1,3] |
| 38C32 | 35 ns | 100/50 ma | 5 ms | 10,000 cy | 4K byte JEDEC bytewide pinout [3] |

## FLASH EEPROM

| | | | | | |
|---|---|---|---|---|---|
| 48128 | 170 ns | 100/30 ma | 2 ms | 100 cy | 16K x 8 low cost; 20 second bulk chip erase [2] |
| 48C512 | 200 ns | 60 ma/100 μa | 600 μs | 1000 cy | 64K x 8 CMOS [2,3] |
| 48C1024 | 200 ns | 60 ma/100 μa | 600 μs | 1000 cy | 128K x 8 CMOS [2,3] |

## INDUSTRY STANDARD EPROMS

| | | | | | |
|---|---|---|---|---|---|
| 2764 | 160 ns | 100/30 ma | 5 ms | n/a | 21 volt $V_{pp}$ [3] |
| 27128 | 200 ns | 100/30 ma | 5 ms | n/a | 21 volt $V_{pp}$ [3] |
| 27C256 | 200 ns | 40 ma/150 μa | 4 ms | n/a | 12.5 volt $V_{pp}$ [2,3] |

## SINGLE-CHIP MICROCOMPUTER WITH EEPROM

| | | | | | |
|---|---|---|---|---|---|
| 72720 | 16 MHz | 150 ma | 8 ms | 10,000 cy | 2K bytes EEPROM/ 256 bytes of RAM |

## LOCAL AREA NETWORK PRODUCTS

| | | | | | |
|---|---|---|---|---|---|
| 8001 | 10 MHz | 200 ma | n/a | n/a | IEEE 802.3/Ethernet controller |
| 8003 | 10 MHz | 200 ma | n/a | n/a | IEEE 802.3/Ethernet controller |
| 8023A | 10 MHz | 100 ma | n/a | n/a | IEEE 802.3 Manchester codec [2] |
| 8005 | 10 MHz | 300 ma | n/a | n/a | IEEE 802.3/Ethernet controller with local buffer interface |
| 8020 | 10 MHz | 100 ma | n/a | n/a | IEEE 802.3 Manchester codec [2] |

## CMOS $E^2$PALS

| | | | | | |
|---|---|---|---|---|---|
| 20RA10Z | 35 ns | 100 μa | n/a | 100 cy | High speed, low power $E^2$PAL. Replaces bipolar PAL pin-for-pin [1,2,3] |

[1] Available in 300 mil wide D.I.P.
[2] Also available in surface mount package.
[3] Available with Mil-Std 883C class B screening.

1849 Fortune Drive, San Jose, California 95131 (408) 432-7400

883 C Class B

# NEW PRODUCTS FOR 1988

## 8005

The 8005 is a second-generation Ethernet/IEEE 802.3 controller designed for low chip-count high performance network interfaces. It features a multi-port 64K byte local buffer interface that buffers the host bus from high rate data traffic by using just two 64K x 4 dynamic RAMS. Both 8 and 16 bit buses are supported for either Intel or Motorola compatible bus signals. The 8005 can filter 6 specific station addresses and provides chip enable decode and address input to an attached PROM for configuration data, powerful features which are unavailable in other controllers. The 8005 is packaged in a 68 pin PLCC and connects directly to the 8020 Manchester Code Converter, which is also available in a PLCC.

## 20RA10Z

The 20RA10Z is the first in a family of CMOS Electrically Erasable PLD's (programmable logic devices) and a result of a joint process/device development agreement between Seeq and Monolithic Memories. This device is pin and function compatible with its bipolar PAL20RA10 counterpart. It is a registered asynchronous PAL®* and features 20 input terms, 10 output terms and individually programmable register outputs which can be bypassed by using the available direct set and reset terms. Because the programmable elements in the 20RA10Z are electrically erasable, it can be reprogrammed and has guaranteed 100% programming yield. Active power consumption is one third that of a bipolar device and special internal circuitry reduces the supply current to 100 $\mu$a when the inputs are D.C. The 20RA10Z is available in a 24 pin 0.3" wide DIP with commercial and military screening.

## 48C512/48C1024

These two devices are CMOS Flash™ EEPROMS organized as 64K x 8 and 128K x 8 respectively. They feature on-chip latches and a timer for easy in-circuit reprogrammability, low power consumption and endurance of 100 cycles. Optional 1000 cycle screening is also available. The 48C512 and 48C1024 are available in DIP and surface-mount packages at commercial, industrial and military temperature ranges.

*PAL is a registered trademark of Monolithic Memories.

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Seeq Technology

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SHARP

Sharp Electronics Corporation
Sharp Plaza
Mahwah, New Jersey 07430
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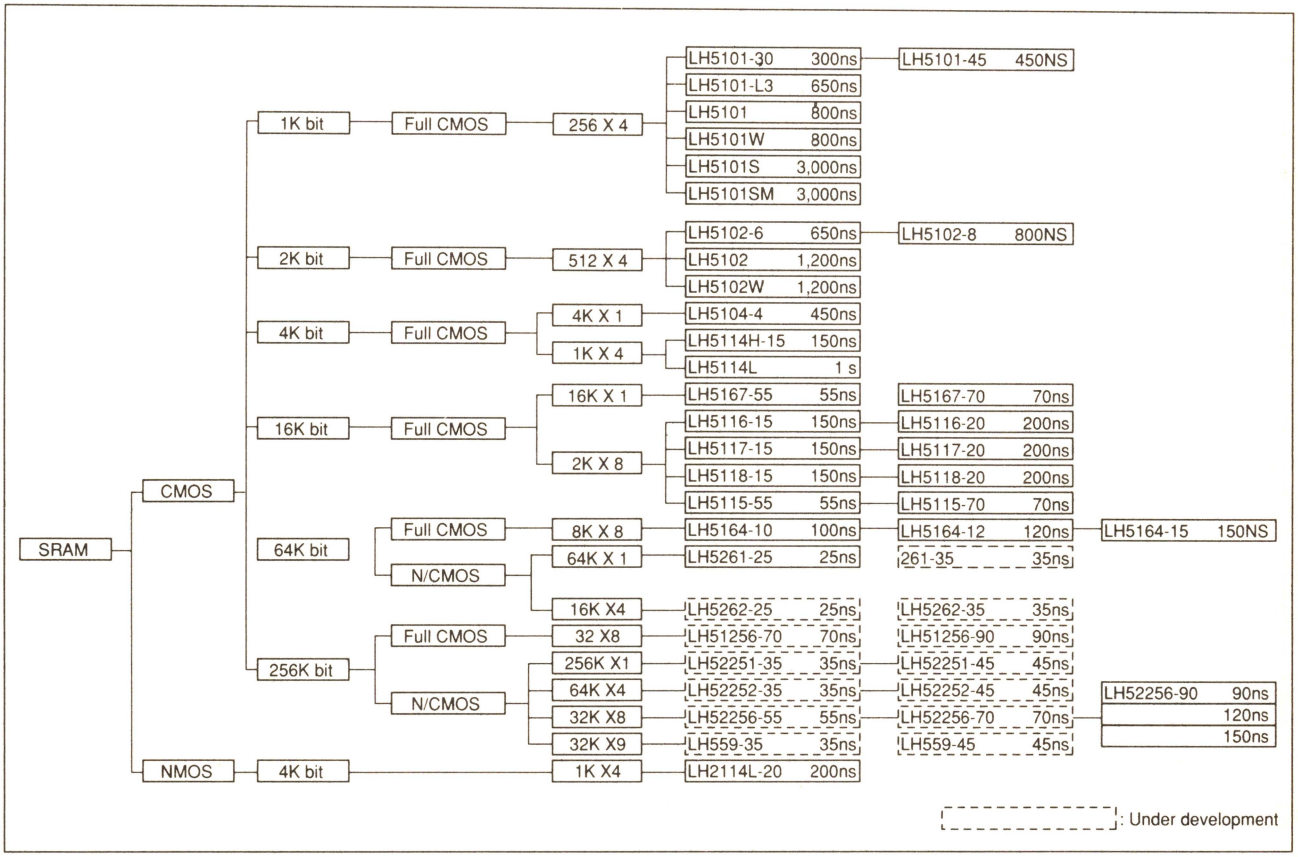
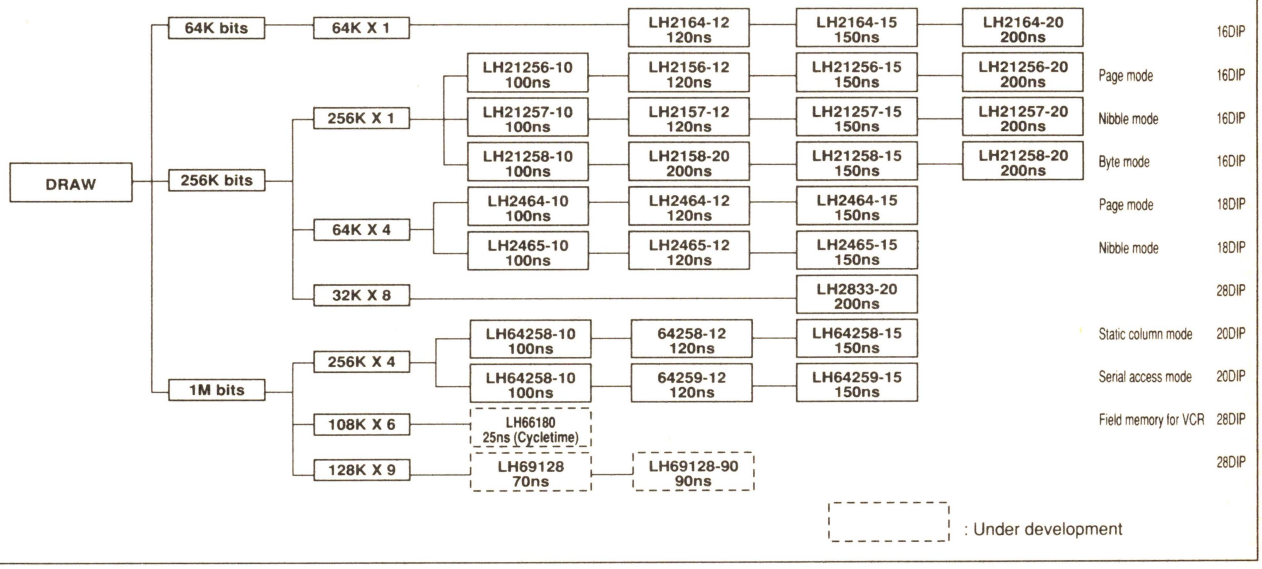
# Static RAMs/Dynamic RAMs

## Static RAMs




## Dynamic RAMs




Sharp Electronics

SHARP®

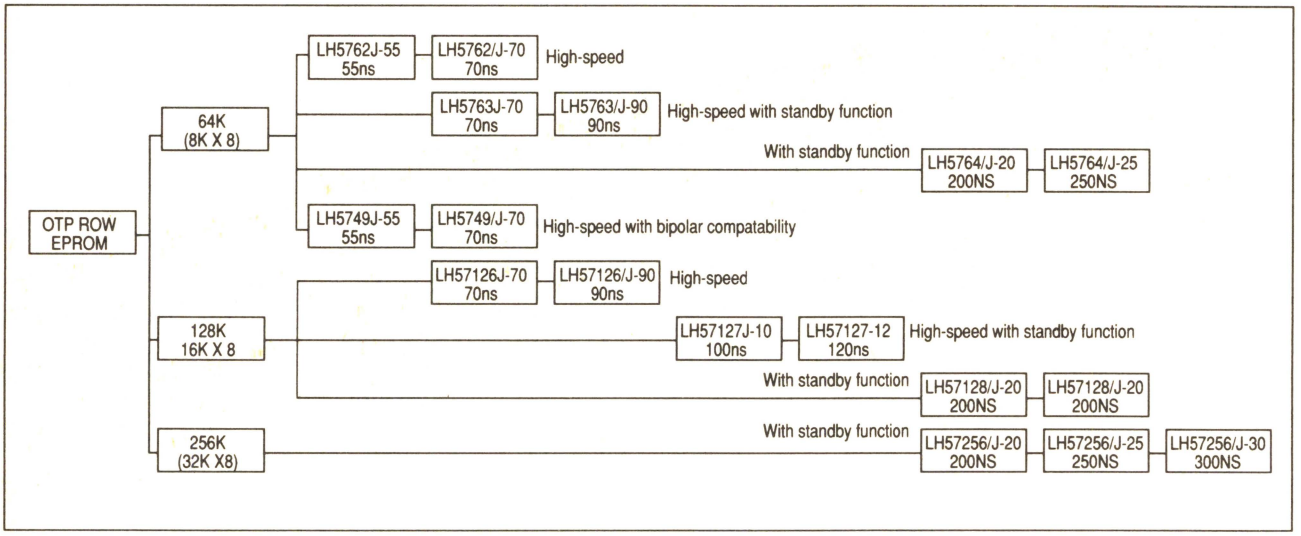
Sharp Electronics Corporation
Sharp Plaza
Mahwah, New Jersey 07430
(201) 529-8757

## Mask ROMs

| Model No. | Process | Capacity (bit) | Access time (ns) MAX. | Cycle time (ns) MIN. | Spply Voltage (V) | Power consumption MAX. (mm) | Package |
|---|---|---|---|---|---|---|---|
| LH5332 | CMOS | 32K | 450 | 550 | 5±10% | 85 | 24DIP |
| LH5367 | | 64K | 450 | 750* | 4~5 | 60 | 44QFP |
| LH53257** | | 256K | 250 | 250 | 5±10% | 165 | 28DIP |
| LH53513** | | 512K | 250 | 250 | 5±10% | 140 | |
| LH531000 | | 1M | 250 | 250 | 5±10% | 140 | 28DIP/44QFP |
| LH531100 | | 1M | 270 | 270 | 5±10% | 165 | 28DIP |
| LH532000** | | 2M | 200 | 200 | 5±10% | 195 | 40DIP |
| | | | 250 | 250 | 5±10% | 195 | |
| LH532100**** | | | 150 | 150 | 5±10% | 220 | 32DIP |
| | | | 250 | 250 | 5±10% | 220 | |
| LH534000**** | | 4M | 200 | 200 | 5±10% | 275 | 40DIP |
| | | | 250 | 250 | 5±10% | 275 | |
| LH2331A | NMOS | 32K | 350 | 350 | 5±10% | 605 | 24DIP |
| LH2332A | | | 350 | 350 | 5±5% | 605 | 24DIP |
| LH2362B | | 64K | 250 | 250 | 5±5% | 880 | 24DIP |
| LH2369** | | | 250 | 250 | 5±10% | 330 | 28DIP |
| LH23126** | | 128K | 250 | 250 | 5±10% | 440 | 28DIP |
| LH23257** | | 256K | 250 | 250 | 5±10% | 440 | 28DIP |
| LH231000** | | 1M | 250 | 250 | 5±10% | 550 | 28DIP |

* Under Development
** Short turnaround type

## EPROMs/OTPROMs




Models with no affix "J" represent OTPROMs. (Ex.) LH5762J: EPROM, LH5762: OTPROM





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Sharp Plaza
Mahwah, New Jersey 07430
(201) 529-8757

# LH52256-55/-70/-90/-12/-15

## CMOS 262144-Bit Static Random Access Memory

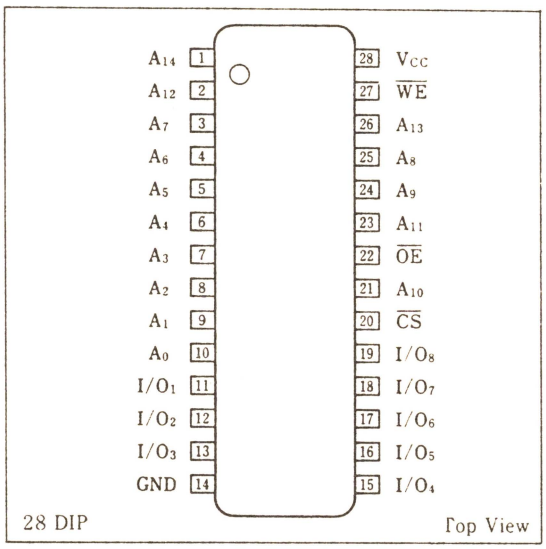
### ■ Description

The LH52256/LH52256L are fully statics RAMs organized as 32,768×8-bit by using silicon-gate CMOS process technology.

### ■ Features

1. Access time (MAX.)
   - LH52256-55····· 55ns
   - LH52256-70····· 70ns
   - LH52256-90····· 90ns
   - LH52256-12·····120ns
   - LH52256-15·····150ns
2. Low power consumption (MAX.)
   - Operating mode:
     - LH52256-55/-70·····80mA
     - LH52256-90/-12/-15·····70mA
   - Standby mode: LH52256 ·····2mA
   - Low power type
   - Standby mode: LH52256L·····0.1mA
3. Single +5V power supply
4. Fully static operation
5. All inputs and outputs TTL compatible
6. Three-state output
7. 28-pin dual-in-line package

### ■ Pin Connections




### ■ Pin Description

| Signal | Pin name |
|---|---|
| $A_0 \sim A_{14}$ | Address inputs |
| $\overline{CS}$ | Chip select |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $I/O_1 \sim I/O_8$ | Data inputs and outputs |
| $V_{CC}$ | Power supply |
| GND | Ground |

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Mode | $I/O_1 \sim I/O_8$ |
|---|---|---|---|---|
| H | X | X | Deselect | High Z |
| L | H | L | Read | $D_{OUT}$ |
| L | H | H | Read | High Z |
| L | L | L | Write | $D_{IN}$ |



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# LH64258-10/-12/-15

## CMOS 1048576-Bit Dynamic Random Access Memory

### ■ Description

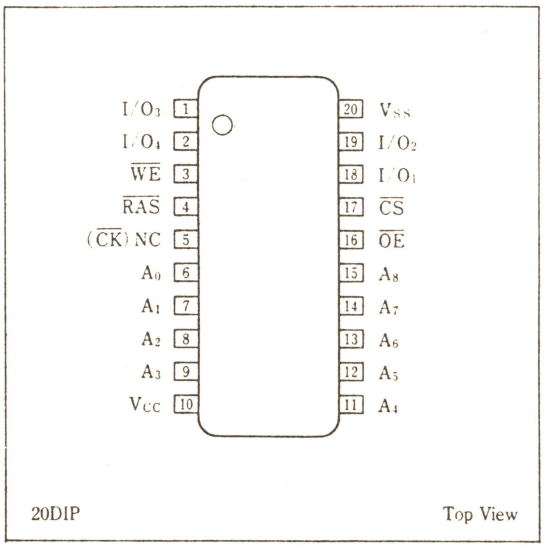
The LH64258 is 262,144 words × 4 bits Dynamic Random Access Memories fabricated on SHARP's advanced CMOS double-level polysilicon gate technology. With its address inputs multiplexed and packaged in the standard 300 mil wide 20pin DIP, it is easy to realize memory systems with high speed, low power dissipation and large memory capacity The LH64258 operates on single + 5V power supply and the built-in biasing voltage generator circuit.

The LH64258 allows static column mode operation.

### ■ Features

1. 262,144 word × 4 bits
2. Standard 20 pin DIP
3. Access time (MAX.)
   100ns (LH64258-10)
   120ns (LH64258-12)
   150ns (LH64258-15)
4. Cycle time (MIN.)
   160ns (LH64258-10)
   190ns (LH64258-12)
   240ns (LH64258-15)
5. Static column mode operation
6. Power supply +5V±10%
7. Power consumption (MAX.)
   330mW (LH64258-10 operating $t_{RC}$= 190ns)
   275mW (LH64258-12 operating $t_{RC}$= 220ns)
   220mW (LH64258-15 operating $t_{RC}$= 260ns)
   11mW (stand-by)
8. All inputs and outputs are TTL compatible
9. $\overline{OE}$=Don't care in early write operation
10. Effective $\overline{RAS}$ time-out function (it is easy to set up the rising time of $\overline{RAS}$ at minimum cycle using $\overline{RAS}$ time-out function)
11. $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CS}$ before $\overline{RAS}$ refresh capability
12. On-chip refresh counter
13. 512 refresh cycle (refresh period (MAX.)= 8ns)

### ■ Pin Connections




20DIP Top View

### ■ Pin Description

| Signal | Pin name |
|---|---|
| $A_0$~$A_8$ | Address input |
| $\overline{RAS}$ | Row address strobe |
| $\overline{CS}$ | Chip select enable |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $I/O_1$~$I/O_4$ | Data input/output |
| $V_{CC}$ | Power supply (+5V) |
| $V_{SS}$ | Power supply (0V) |

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# SELECTION GUIDE

## A/D CONVERTERS

| PART NO. | RESOLUTION (BITS) | SAMPLE RATE (MSPS) | CONVERSION TIME (μs) | LOGIC FAMILY | LINEARITY INT | LINEARITY DIF | FEATURES |
|---|---|---|---|---|---|---|---|
| HADC 77200A | 8 | 150 | | ECL | ½ | ½ | DATA READY AND OVERRANGE OUTPUTS, QUARTER POINT LADDER TAPS, IMPROVED ANALOG PERFORMANCE |
| HDAC 77200B | 8 | 150 | | ECL | ¾ | ¾ | |
| HADC 77100A | 8 | 150 | | ECL | ½ | ½ | PRE AMPLIFIER DESIGN |
| HDAC 77100B | 8 | 150 | | ECL | ¾ | ¾ | |
| HADC 77600 | 10 | 50 (75 TYP) | | ECL | 1 | ½ | ON BOARD BUFFER, METASTABLE STATE ERROR REDUCTION |
| HADC 674A | 12 | | 15 | TTL | ½ | ½ | S/H FUNCTION, LOW POWER, NO NEGATIVE SUPPLY REQUIRED, NO TRANSIENTS AT INPUT, FULL BIPOLAR INPUT, ALTERNATES FOR HI574, HI674 AND AD574 |
| HADC 674B | 12 | | 15 | TTL | ½ | ½ | |
| HADC 674C | 12 | | 15 | TTL | 1 | 1 | |
| HADC 574A | 12 | | 25 | TTL | ½ | ½ | |
| HADC 574B | 12 | | 25 | TTL | ½ | ½ | |
| HADC 574C | 12 | | 25 | TTL | 1 | 1 | |

## D/A CONVERTERS

| PART NO. | RESOLUTION (BITS) | UPDATE RATE (MSPS) | SETTLING TIME (ns) | LOGIC FAMILY | LINEARITY INT | LINEARITY DIF | FEATURES |
|---|---|---|---|---|---|---|---|
| HDAC 34020 | 4 | 100 | 4 | TTL | ½ | ½ | TRIPLE 4-BIT, REF, VIDEO CONTROL |
| HDAC 34010 | 4 | 200 | 4 | ECL | ½ | ½ | TRIPLE 4-BIT, REF, VIDEO CONTROL |
| HDAM 51100 | 8 | 125 | 3 | ECL | ½ | ½ | 512 X 8 PALETTE, REF, VIDEO CONTROL |
| HDAC 51600 | 8 | 165 (250 TYP) | 3 | TTL | ½ | ½ | 5:1, 4:1, MUX, REF, VIDEO CONTROL |
| HDAC 10180B | 8 | 180 | 3 | ECL | ½ | ½ | VIDEO CONTROL, ALTERNATE FOR TDC 1018 |
| HDAC 10181B | 8 | 180 | 3 | ECL | ½ | ½ | REF, VIDEO CONTROL |
| HDAM 51200 | 8 | 200 | 3 | ECL | ½ | ½ | 512 X 8 PALETTE, REF, VIDEO CONTROL |
| HDAC 97000 | 8 | 200 | 10 | ECL | ½ | ½ | REF, ALTERNATE FOR AD9700 |
| HDAC 10180A | 8 | 275 | 3 | ECL | ½ | ½ | VIDEO CONTROL, ALTERNATE FOR TDC 1018 |
| HDAC 10181A | 8 | 275 | 3 | ECL | ½ | ½ | REF, VIDEO CONTROL |
| HDAC 51400 | 8 | 385 | 3 | ECL | ½ | ½ | REF, VIDEO CONTROL |
| HDAC 7541Z | 12 | | 500 | TTL | ½ | ½ | ALTERNATE FOR AD7541A |
| HDAC 7542A | 12 | | 500 | TTL | ½ | ½ | ALTERNATE FOR AD7542 |
| HDAC 7543A | 12 | | 500 | TTL | ½ | ½ | ALTERNATE FOR AD7543 |
| HDAC 7545A | 12 | | 500 | TTL | ½ | ½ | ALTERNATE FOR AD7545 |
| HDAC 50500 | 12 | | 500 | TTL | ½ | ½ | MICROPROCESSOR INTERFACE |
| HDAC 50600 | 14 | | 500 | TTL | ½ | ½ | PARALLEL INPUT |
| HDAC 50800 | 14 | | 500 | TTL | ½ | ½ | 2 BYTE INPUT |
| HDAC 52160 | 16 | | 150 | TTL | ½ | ½ | PARALLEL INPUT |

## COMPARATORS

| PART NO. | tr/tf (ns) | PROP DELAY (ns) | $V_{CM}$ (V) | $V_{OS}$ (mV) | $R_{IN}$ (kΩ) | AV (V/V) | FEATURES |
|---|---|---|---|---|---|---|---|
| HCMP 96850 | 1.76/1.72 | 3.0 | ±2.5V | ±3.0 | 60 | 4K | SYMETRICAL $t_r/t_f$, ALTERNATE FOR SP9685, AM6685 |
| HCMP 96870A | 1.2/1.2 | 2.3 | ±2.5 | ±3.0 | 60 | 4k | HIGH PERFORMANCE ALTERNATE FOR SP9687, AM6687 |
| HCMP 96900 | 1.6/1.6 | 4.2 | +10 −3 | ±0.5 | 10,000 | 1k | HIGH Vcm RANGE, SYMETRICAL $t_r/t_f$ AND PROP DELAY INDEPENDENT OF OVERDRIVE AND Vcm |

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## INSTRUMENTATION AMPLIFIERS

| PART NO. | NON-LINEARITY | Vos (μV) | GAIN BANDWIDTH (MHz) | SUPPLY VOLTAGE (V) | FEATURES |
|---|---|---|---|---|---|
| HINA 522 | .001% MAX AV = 1 | 25 | | ± 15 | ALTERNATE SOURCES FOR ANALOG DEVICES MONOLITHIC CONSTRUCTION |
| HINA 524 | .003% MAX AV = 1 | 25 | 25 AV = 1000 | ± 15 | |
| HINA 624 | .001% MAX AV = 1 | 25 | 25 AV = 1000 | ± 15 | |

## FILTER

| PART NO. | DYNAMIC RANGE (dB) | MAX BANDEDGE (kHz) | BANDEDGE TOLERANCE (%) | SUPPLY VOLTAGE (V) | FEATURES |
|---|---|---|---|---|---|
| HSCF 24040 | 85 | 20 | ± 0.5 | ± 5 | 7TH ORDER LOW PASS, > 76dB STOPBAND ATTENUATION, ON CHIP ANTIALIAS FILTER, DIGITALLY PROGRAMMABLE BANDEDGE AND DC GAIN |

| EVALUATION BOARDS | FEATURED PRODUCT | FEATURES |
|---|---|---|
| EB 100 | HADC77100 | 150MSPS A/D, D/A |
| EB 101 | HADC77200 | 150MSPS A/D, D/A |
| EB 102 | N/A | 100MHz BUFFER AMP, 8-BITS |
| EB 103 | HADC77200 | 300MSPS A/D, D/A PING-PONG |
| EB 104 | HADC574/674 | A/D, D/A, OPTIONAL S/H |
| EB 105 | HSCF24040 | ON BOARD OR EXTERNAL PROGRAMMING |

## FEATURES & FUNCTIONS A/D CONVERTERS

### S/H FUNCTION
(Transparent if not required)

HADC574
HADC674

### TTL LOGIC

HADC574
HADC674

### ECL LOGIC

HADC77100
HADC77200
HADC77600

### ON BOARD BUFFER

HADC77600

### 8-BIT RESOLUTION

HADC77100
HADC77200

### 10-BIT RESOLUTION

HADC77600

### 12-BIT RESOLUTION

HADC574
HADC674

### LOW POWER

HDAC574
HDAC674

### ON BOARD REFERENCE

HADC574
HADC674

## FEATURES & FUNCTIONS D/A CONVERTERS

### HIGH SPEED/VIDEO

HDAC34010
HDAC34020
HDAC97000
HDAC10180
HDAC10181
HDAM51100
HDAM51200
HDAC51400
HDAC51600

### MULTIPLEXED

HDAC51600

### MEMORY

HDAM51100
HDAM51200

### TRIPLE DAC

HDAC34010
HDAC34020

### MICROPROCESSOR INTERFACE

HDAC50500
HDAC7542A
HDAC7543A
HDAC7545A

### HIGH PRECISION

HDAC7541Z
HDAC7542A
HDAC7543A
HDAC7545A
HDAC50500
HDAC50600
HDAC50610
HDAC50800
HDAC50810
HDAC52160

### ON-CHIP REFERENCE

HDAC34010
HDAC34020
HDAC97000
HDAC10181
HDAC51400
HDAM51100
HDAM51200
HDAC51600

### ECL LOGIC

HDAC34010
HDAC97000
HDAC10180
HDAC10181
HDAC51400
HDAC51100
HDAC51200

### TTL LOGIC

HDAC34020
HDAC51600
HDAC7541Z
HDAC7542A
HDAC7543A
HDAC7545A
HDAC50500
HDAC52120
HDAC50600
HDAC50610
HDAC50800
HDAC50810
HDAC52160

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# PRODUCT CROSS REFERENCE GUIDE

| INDUSTRY PART NO. | SPT EQUIVALENT |
|---|---|
| AD522AD | HINA522BIJ |
| AD522BD | HINA522AIJ |
| AD522SD | HINA522BMJ |
| AD524AD | HINA524CIJ |
| AD524BD | HINA524BIJ |
| AD524CD | HINA524AIJ |
| AD524SD | HINA524CMJ |
| AD574AJD | HADC574ZCCJ |
| AD574AJN | HADC574ZCCN |
| AD574AKD | HADC574ZBCJ |
| AD574AKN | HADC574ZBCN |
| AD574ALD | HADC574ZACJ |
| AD574ALN | HADC574ZACN |
| AD624AD | HINA624CIJ |
| AD624BD | HINA624BIJ |
| AD624CD | HINA624AIJ |
| AD624SD | HINA624CMJ |
| AD7541AAQ | HDAC7541ZBID |
| AD7541ABQ | HDAC7541ZAID |
| AD7541ACHIPS | HDAC7541ZBCU |
| AD7541AJN | HDAC7541ZBCN |
| AD7541AKN | HDAC7541ZACN |
| AD7541ASD | HDAC7541ZBMD |
| AD7541ATD | HDAC7541ZAMD |
| AD7542AD | HDAC7542ABID |
| AD7542BD | HDAC7542AAID |
| AD7542CHIPS | HDAC7542ABCU |
| AD7542GBD | HDAC7542AAID/G |
| AD7542GKN | HDAC7542AACN/G |
| AD7542GTD | HDAC7542AAMD/G |
| AD7542JN | HDAC7542ABCN |
| AD7542KN | HDAC7542AACN |
| AD7542SD | HDAC7542ABMD |
| AD7542TD | HDAC7542AAMD |
| AD7543AD | HDAC7543ABID |
| AD7543BD | HDAC7543AAID |
| AD7543CHIPS | HDAC7543ABCU |
| AD7543GBD | HDAC7543AAID/G |
| AD7543GKN | HDAC7543AACN/G |
| AD7543GTD | HDAC7543AAMD/G |
| AD7543JN | HDAC7543ABCN |
| AD7543KN | HDAC7543AACN |
| AD7543SD | HDAC7543ABMD |
| AD7543TD | HDAC7543AAMD |

| INDUSTRY PART NO. | SPT EQUIVALENT |
|---|---|
| AD7545AQ | HDAC7545ABID |
| AD7545BQ | HDAC7545ABID |
| AD7545CHIPS | HDAC7545ABCU |
| AD7545CQ | HDAC7545AAID |
| AD7545GCQ | HDAC7545AAID/G |
| AD7545GLN | HDAC7545AACN/G |
| AD7545GUD | HDAC7545AAMD/G |
| AD7545JN | HDAC7545ABCN |
| AD7545KN | HDAC7545ABCN |
| AD7545LN | HDAC7545AACN |
| AD7545SD | HDAC7545ABMD |
| AD7545TD | HDAC7545ABMD |
| AD7545UD | HDAC7545AAMD |
| AD9700D22A | HDAC97000SJM |
| AM6685DL | HCMP96850SID |
| AM6687DL | HCMP96870SID |
| AM6687LL | HCMP96870SIC |
| CX20116 | HADC77100AIJ |
| HI1-574AJD-5 | HADC574ZCCJ |
| HI1-574AKD-5 | HADC574ZBCJ |
| HI1-574ALD-5 | HADC574ZACJ |
| HI1-674AJD-5 | HADC674ZCCJ |
| HI1-674AKD-5 | HADC674ZBCJ |
| HI1-674ALD-5 | HADC674ZACJ |
| MP7542 | HDAC7542ABCU |
| MP7542AD | HDAC7542ABID |
| MP7542BD | HDAC7542AAID |
| MP7542JN | HDAC7542ABCN |
| MP7542KN | HDAC7542AACN |
| MP7542SD | HDAC7542ABMD |
| MP7542TD | HDAC7542AAMD |
| MP7543 | HDAC7543ABCU |
| MP7543AD | HDAC7543ABID |
| MP7543BD | HDAC7543AAID |
| MP7543JN | HDAC7543ABCN |
| MP7543KN | HDAC7543AACN |
| MP7543SD | HDAC7543ABMD |
| MP7543TD | HDAC7543AAMD |
| MP7545 | HDAC7545ABCU |
| MP7545AD | HDAC7545ABID |
| MP7545BD | HDAC7545ABID |
| MP7545CD | HDAC7545AAID |
| MP7545JN | HDAC7545ABCN |
| MP7545KN | HDAC7545ABCN |

| INDUSTRY PART NO. | SPT EQUIVALENT |
|---|---|
| MP7545LN | HDAC7545AACN |
| MP7545SD | HDAC7545ABMD |
| MP7545TD | HDAC7545ABMD |
| MP7545UD | HDAC7545AAMD |
| MP7623 | HDAC7541ZCCU |
| MP7623AD | HDAC7541ZBID |
| MP7623BD | HDAC7541ZAID |
| MP7623JN | HDAC7541ZBCN |
| MP7623KN | HDAC7541ZACN |
| MP7623SD | HDAC7541ZBMD |
| MP7623TD | HDAC7541ZAMD |
| PM7542AQ | HDAC7542AAMD/G |
| PM7542BQ | HDAC7542AAMD |
| PM7542BQ | HDAC7542ABMD |
| PM7542EQ | HDAC7542AAID/G |
| PM7542FQ | HDAC7542AAID |
| PM7542FQ | HDAC7542ABID |
| PM7542G | HDAC7542ABCU |
| PM7542GP | HDAC7542AACN/G |
| PM7542HP | HDAC7542AACN |
| PM7542HP | HDAC7542ABCN |
| PM7543AQ | HDAC7543AAMD/G |
| PM7543BQ | HDAC7543AAMD |
| PM7543BQ | HDAC7543ABMD |
| PM7543EQ | HDAC7543AAID/G |
| PM7543FQ | HDAC7543AAID |
| PM7543FQ | HDAC7543ABID |
| PM7543G | HDAC7543ABCU |
| PM7543GP | HDAC7543AACN/G |
| PM7543HP | HDAC7543AACN |
| PM7543HP | HDAC7543ABCN |
| PM7545AR | HDAC7545AAMD/G |
| PM7545BR | HDAC7545AAMD |
| PM7545BR | HDAC7545ABMD |
| PM7545ER | HDAC7545AAID/G |
| PM7545FR | HDAC7545AAID |
| PM7545FR | HDAC7545ABID |
| PM7545G | HDAC7545ABCU |
| PM7545GP | HDAC7545AACN/G |
| PM7545HP | HDAC7545AACN |
| PM7545HP | HDAC7545ABCN |
| SP9685DG16 | HCMP96850SID |
| SP9687DG16 | HCMP96870AID |
| TDC1018J7C | HDAC10180AMJ |



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Telex: 290651

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## ASIC CAPABILITIES

The standard products listed in this brochure indicate the level of performance that is achievable using Honeywell SPT's design and processing capabilities. The chart below lists some key features of our current state-of-the-art processing technologies. SPT's expertise can be used to create ultra high performance ICs taylored to your specific needs. Please contact us for further information.

| TECHNOLOGIES | ADB-III | BEMOS-II | CMOS-III |
|---|---|---|---|
| • **LITHOGRAPHY** | | | |
| — DIMENSION | 1.2μ | 3μ | 1.2μ |
| — METHOD | 5:1 Stepper | OPTICAL | 10:1/5:1 Stepper |
| • **INTERCONNECT** | | | |
| — METAL PITCH | 3μ | 9μ | 3μ(1st)/5μ(2nd) |
| — NO. LEVELS | 3 Metal | 2 Poly/1 Metal | 1 Poly/2 Metal |
| • **PERFORMANCE** | | | |
| — GATE SPEED | 0.3ns | 3ns-5ns | 1ns |
| — GATE POWER | 0.5mw | 20μw/MHz | 4μw/MHz |
| — DIGITAL | 300 MHz | 15 MHz | 100 MHz |
| — ANALOG | 250 MHz | 10 MHz | 50 MHz |
| • **CHIP DENSITY** | 15K-30K Gates | 10K Gates | 25K-50K Gates |
| • **ANALOG FEATURES** | | NPN, Thin Film Poly-Poly Cap | |
| • **I/O** | 10V | 10V | 5V |
| • **CKT APPLICATIONS** | High speed data acquisition, control and signal proc. | DAC, ADC, Filters analog signal proc. | Digital signal processing, FFT, Digital ASIC |

## APPLICATION NOTES AND BRIEFS

- **AN100** EB100 Evaluation Board (HADC77100)
- **AN101** Introduction to Flash Converters
- **AN102** EB101 Evaluation Board (HADC77200)
- **AN103** EB103 Evaluation Board (Ping-Pong Mode Flash Converters)
- **AN104** Video Dacs and Raster Graphics
- **AN106** EB104 Evaluation Board (HADC574/674)
- **AN108** Thermal Considerations for High Performance Devices
- **AN109** EB105 Evaluation Board (HSCF24040 Programmable 7th Order Low Pass Active Filter)
- **AB100** Using ECL DACS With TTL Logic
- **AB101** External SYNC Circuit for Video DACS
- **AB102** Charge Scaling Data Converters
- **AB103** HADC574/674 Analog Input Structure
- **AB104** Using the LTS2020 to Test the HADC574/674

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# EVALUATION BOARDS

## EB100 EVALUATION BOARD, 8-BIT, 150 MSPS FLASH A/D CONVERTER AND 8-BIT, 165 TO 400 MWPS RASTER D/A CONVERTER WITH REFERENCE.

### FEATURES

- **150 MSPS MINIMUM CONVERSION RATE**
- 70 MHz Full Scale input Bandwidth
- ½ LSB Integral Linearity (Adjustable)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- Clock produced from any signal generator
- Improved Output Drive (Doubly-Terminated 50Ω)
- Optional clock divider board provided

### GENERAL DESCRIPTION

The EB100 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77100A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board.

## EB101 EVALUATION BOARD, 8-BIT, 150 MSPS FLASH CONVERTER AND 8-BIT, 165 TO 400 MWPS RASTER D/A CONVERTER WITH REFERENCE.

### FEATURES

- **150 MSPS MINIMUM COVERSION RATE**
- 70 MHz Full Scale input Bandwidth
- ½ LSB Integral Linearity (Adjustable with three reference ladder taps)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- ECL clock produced from any signal generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

### GENERAL DESCRIPTION

The EB101 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77200A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board.

## EB102 EVALUATION BOARD, HIGH SPEED BUFFER AMPLIFIER

### FEATURES

- **USE WITH EB100/101 EVALUATION BOARDS**
- 70 MHz Full Scale input Bandwidth driving the converters
- Up to ± 100mA Drive current
- Low Distortion
- 15ns Settling Time

### GENERAL DESCRIPTION

The EB102 is intended to demonstrate the high performance achievable with the HADC77100/200 flash A/D converters. The EB102 is a very low distortion, 70MHz buffer amplifier board. It provides for higher frequency operation than the buffer on the EB100 or EB101 evaluation boards. Included on the unit is either the Comlinear CLC221 Operational Amplifier or CLC231 Buffer-Amplifier.



SIGNAL PROCESSING TECHNOLOGIES 1150 E. Cheyenne Mountain Blvd., Colorado Springs, CO 80906
(303) 577-1000 TELEX #452433 EASYLINK #62926148 FAX #(303) 577-3716
Area Code and Prefix will change, March 1, 1988 to (719) 540-1000/FAX 3716

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## EB103 EVALUATION BOARD, TWO PING-PONGED 8-BIT FLASH A/D CONVERTERS

### FEATURES

- **400 MSPS NOMINAL CONVERSION RATE**
- 100 to 150 MHz Full Scale input Bandwidth
- ½ LSB Integral Linearity (Adjustable with three reference ladder taps)
- Preamp Comparator Design/Optional Input Buffer
- ECL Timing skew clock generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

### GENERAL DESCRIPTION

The EB103 Evaluation Board is intended to show the performance of the HADC77200 flash A/D converter in a ping-ponged mode, and the HDAC51400 Ultra High Speed D/A converter for reconstruction. Included on the unit are two 100K ECL multiplexers for combining the ping-ponged A/D converters' 16 bits of output data into 8 bits at twice the speed. The high speed data is routed between the A/D and D/A, and also off the board as full speed or as divided down data (external clock) for slower speed FFT measurements.

## EB104 EVALUATION BOARD, INCLUDES HADC574Z 12-BIT A/D CONVERTER AND HDAC754A 12-BIT D/A CONVERTER

### FEATURES:

- Provides operating environment for HADC574Z or HADC674Z and HDAC7545A Devices
- Fully Demonstrates Device Function and Resolution
- Eliminates Noisy Breadboard Evaluation Circuitry
- Buffered A/D and D/A Conversion Data Buses
- Includes Sample/Hold Amp and Output Op Amp IC's
- Unipolar or Bipolar Operation

### GENERAL DESCRIPTION

The EB104 Evaluation Board fully demonstrates the capabilities of Honeywell's HADC574/674Z and HDAC7545A 12-bit data conversion products. All of the basic power supply connections, control lines and external components are included. The board can operate in an analog input/output fashion utilizing both A/D and D/A devices, or the devices can be operated separately. Unlike most laboratory breadboarding, the ground-planed PC board provides the necessary low-noise environment essential for 12-bit resolution. The board makes full use of connectors to allow easy hookup and operation.



## EB105 EVALUATION BOARD, INCLUDES HSCF24040 PROGRAMMABLE 7TH ORDER LOW PASS ACTIVE FILTER

### FEATURES

- Complete with Socketed HSCF24040ACD Device
- Demonstrates HSCF24040 Performance and Capabilities
- Toggle Switches for On-Board Control and Programming
- Connectors Allow Easy Interfacing of External Control, Programming, and Analog Signals
- Crystal Time Base
- Leaded Power Supply Connector

### GENERAL DESCRIPTION

The EB105 Evaluation Board allows full exercise of the Honeywell HSCF24040 Programmable 7th Order Low Pass Active Filter. Unlike a handwired breadboard, this ground-planed, printed circuit board provides a high performance, noise-free environment. it provides full demonstration and evaluation of the superb HSCF24040 dynamic characteristics. Programming and control of the device is convenitnely enabled by onboard toggle switches. Alternately, programming and control can be accomplished through the on-board ribbon cable connector. This option allows software control which can aid in system development.

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(303) 577-1000 TELEX #452433 EASYLINK #62926148 FAX #(303) 577-3716
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# Technology Selection Guide

| DEVICE NUMBER | DESCRIPTION | STD | S | LS | FAST | HC | HCT |
|---|---|---|---|---|---|---|---|
| 00 | Quad 2-Input NAND Gate | A | A | A | A | A | A |
| 01 | Quad 2-Input NAND Gate, OC | | | A | | | |
| 02 | Quad 2-Input NOR Gate | A | A | A | A | A | A |
| 03 | Quad 2-Input NAND Gate | A | A | | | A | A |
| 04 | Hex Inverter | A | A | A | A | A | A |
| 05 | Hex Inverter, OC | A | A | A | | | |
| 06 | Hex Inverter Buffer/Driver, OC | A | | | | | |
| 07 | Hex Buffer/Driver, OC | A | | | | | |
| 08 | Quad 2-Input AND Gate | A | A | A | A | A | A |
| 09 | Quad 2-Input AND Gate, OC | | | A | | | |
| 10 | Triple 3-Input NAND Gate | A | A | A | A | A | A |
| 11 | Triple 3-Input AND Gate | A | A | A | A | A | A |
| 13 | Dual 4-Input NAND Schmitt Trigger | A | | A | A | | |
| 14 | Hex Inverter Schmitt Trigger | A | | A | A | A | A |
| 16 | Hex Inverter Buffer/Driver, OC | A | | | | | |
| 17 | Hex Buffer/Driver, OC | A | | | | | |
| 20 | Dual 4-Input NAND Gate | A | A | A | A | A | A |
| 21 | Dual 4-Input AND Gate | A | | A | | Q1 '87 | Q1 '87 |
| 25 | Dual 4-Input NOR with Strobe | A | | | | | |
| 26 | Quad 2-Input NAND Gate, OC | A | | A | | | |
| 27 | Triple 3-Input NOR Gate | A | | A | A | A | A |
| 28 | Quad 2-Input NOR Buffer | A | | | | | |
| 30 | 8-Input NAND Gate | A | | A | A | Q1 '87 | A |
| 32 | Quad 2-Input OR Gate | A | A | A | A | A | A |
| 33 | Quad 2-Input NOR Buffer, OC | A | | A | | | |
| 37 | Quad 2-Input NAND Buffer | A | A | A | A | | |
| 38 | Quad 2-Input NAND Buffer, OC | A | A | A | A | | |
| 39 | Quad 2-Input NAND Buffer, OC | A | | | | | |
| 40 | Dual 4-Input NAND Buffer | A | A | A | A | | |
| 42 | BCD-to-Decimal Decoder | A | | A | | A | A |
| 45 | BCD-to-Decimal Decoder/Driver, OC | A | | | | | |
| 50 | Expandable Dual 2-Wide 2-Input AOI Gate | A | | | | | |
| 51 | Dual 2-Wide 2-Input AOI Gate | A | A | A | A | | |
| 54 | 4-Wide 2-Input AOI Gate | | | A | | | |
| 58 | Dual 4-Input AND/OR Gate | | | | | A | A |
| 64 | 4-2-3-2 Input AOI Gate | | A | | A | | |
| 73 | Dual J-K Master-Slave Flip-Flop | A | | A | | A | A |
| 74 | Dual D-Type Positive Edge-Triggered Flip-Flop | A | A | A* | A | A | A |
| 75 | Quad Bistable Latch | A | | A | | A | A |
| 76 | Dual J-K Master-Slave Flip-Flop | A | | A | | | |
| 83 | 4-Bit Binary Full Adder, Ripple Carry | A | | A* | | | |
| 85 | 4-Bit Magnitude Comparator | A | A | A | A | A | A |
| 86 | Quad 2-Input EXCLUSIVE-OR Gate | A | A | A | A | A | A |
| 90 | Decade Ripple Counter | A | | A | | | |
| 91 | 8-Bit Shift Register | A | | | | | |
| 92 | Divide-by-12 Counter | A | | A | | | |
| 93 | 4-Bit Binary Ripple Counter | A | | A | | A | A |
| 94 | 4-Bit PISO Shift Register | A | | | | | |
| 95 | 4-Bit Shift Register | A | | A** | | | |
| 96 | 5-Bit Shift Register | A | | A | | | |
| 107 | Dual J-K Master-Slave Flip-Flop | A | | A | | A | A |
| 109 | Dual J-K Positive Edge-Triggered Flip-Flop | A | | A* | A | A | A |
| 112 | Dual J-K Negative Edge-Triggered Flip-Flop | | A | A | A | A | A |
| 113 | Dual J-K Negative Edge-Triggered Flip-Flop | | A | A | A | | |
| 114 | Dual J-K Negative Edge-Triggered Flip-Flop | | | | A | | |
| 116 | Dual 4-Bit Latch with Clear | A | | | | | |

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| DEVICE NUMBER | DESCRIPTION | STD | S | LS | FAST | HC | HCT |
|---|---|---|---|---|---|---|---|
| 121 | Monostable Multivibrator | A | | | | | |
| 123 | Quad 3-State Buffer | A | | | | A | A |
| 125 | Quad Retriggerable Monostable Multivibrator | A | | A* | A | A | A |
| 126 | Quad 3-State Buffer | A | | A* | A | A | A |
| 128 | Quad 2-Input NOR Buffer | A | | | | | |
| 132 | Quad 2-Input NAND Schmitt Trigger | A | | A | A | A | A |
| 133 | 13-Input NAND Gate | | A | | | | |
| 134 | 12-Input NAND Gate, 3-State | | A | | | | |
| 135 | Quad EXCLUSIVE-OR/NOR Gate | | A | | | | |
| 136 | Quad EXCLUSIVE-OR, OC | | | A | | | |
| 137 | 3-to-8 Decoder/Demultiplexer, Inverting | | | | | Q1 '87 | Q1 '87 |
| 138 | 3-to-8 Decoder/Demultiplexer | | | | A | A | A |
| 139 | Dual 2-to-4 Decoder/Demultiplexer | | A | A | A | A | A |
| 140 | Dual 4-Input NAND Line Driver | | A | | | | |
| 145 | BCD-to-Decimal Decoder/Driver, OC | A | | | | | |
| 147 | 10-to-4 Priority Encoder | A | | | | A | A |
| 148 | 8-to-3 Priority Encoder | A | | | A | | |
| 150 | 16-to-6 Multiplexer | A | | | | | |
| 151 | 8-to-1 Multiplexer | A | A | A | A | A | A |
| 153 | Dual 4-to-1 Multiplexer | A | A | A | A | A | A |
| 154 | 4-to-16 Decoder/Demultiplexer | A | | A | | A | A |
| 155 | Dual 2-to-4 Decoder/Demultiplexer | A | | A | | | |
| 156 | Dual 2-to-4 Decoder/Demultiplexer, OC | A | | A | | | |
| 157 | Quad 2-to-1 Multiplexer | A | A | A | A | A | A |
| 158 | Quad 2-to-1 Multiplexer | A | A | A | A | A | A |
| 160 | Synchronous 4-Bit Decade Counter | A | | A* | A* | A | A |
| 161 | Synchronous 4-Bit Binary Counter | A | | A* | A* | A | A |
| 162 | Synchronous 4-Bit Decade Counter | | | A* | A* | A | A |
| 163 | Synchronous 4-Bit Binary Counter | A | | A* | A* | A | A |
| 164 | 8-Bit PISO Shift Register | A | | A | | A | A |
| 165 | 8-Bit PISO Shift Register | A | | | | A | A |
| 166 | 8-Bit PISO Shift Register | A | | | A | A | A |
| 168 | Decade Up/Down Counter | | A* | A* | A | | |
| 169 | Binary Up/Down Counter | | A* | A* | A | | |
| 170 | 4 x 4 Register File, OC | A | | A | | | |
| 172 | 16-Bit Multiple Port Register File | | A | | | | |
| 173 | Quad D-Type Flip-Flop, 3-State | A | | A | | A | A |
| 174 | Hex D-Type Flip-Flop with Clear | A | A | A | A | | |
| 175 | Quad D-Type Flip-Flop | A | | | A | A | A |
| 180 | 8-Bit Odd/Even Parity Checker | A | | | | | |
| 181 | 4-Bit Arithmetic Logic Unit | A | A | A | A | Q1 '87 | Q1 '87 |
| 182 | Look-Ahead Carry Generator | | A | | 1H '87 | A | A |
| 189 | 64-Bit Random Access Memory | | | | | | |
| 190 | Decade Up/Down Counter | A | | | A | A | A |
| 191 | Binary Up/Down Counter | A | | A | A | A | A |
| 192 | Decade Up/Down Counter | A | | A | A | Q1 '87 | Q1 '87 |
| 193 | 4-Bit Binary Up/Down Counter | A | | A | A | A | A |
| 194 | 4-Bit Bidirectional Shift Register | A | A | A* | A | A | A |
| 195 | 4-Bit Parallel-Access Shift Register | A | A | A* | A | A | A |
| 197 | Presettable Binary Counter | | | A | | | |
| 198 | 8-Bit Bidirectional Universal Shift Register | | | | A | A | A |
| 199 | 8-Bit Universal Shift Register | A | | | A | | |
| 221 | Dual Monostable Multivibrator | A | | | | | |
| 225 | FIFO Register, 3-State | | A | | | | |
| 227 | 1-to-8 Line Decoder | | | | | A | A |
| 238 | 1-of-8 Decoder/Demultiplexer, True/Inverting | | | | | A | A |
| 240 | Octal Buffer, 3-State | | A | A | A | A | A |
| 241 | Octal Buffer, 3-State | | A | A | A | A | A |

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# Technology Selection Guide

| DEVICE NUMBER | DESCRIPTION | STD | S | LS | FAST | HC | HCT |
|---|---|---|---|---|---|---|---|
| 242 | Quad Inverting Bus Transceiver, 3-State | | A | A | A | A | A |
| 243 | Quad Bus Transceiver, 3-State | | A | A | A | A | A |
| 244 | Octal Buffer, 3-State | | A | A | A | A | A |
| 245 | Octal Bus Transceiver, 3-State | | | A | A | A | A |
| 251 | 8-to-1 Multiplexer, 3-State | | A | A | A | A | A |
| 253 | Dual 4-to-1 Multiplexer, 3-State | | A | A | A | A | A |
| 256 | Dual 4-Bit Addressable Latch | | | A | A | | |
| 257 | Quad 2-to-1 Multiplexer, 3-State | | A | A* | A | A | A |
| 258 | Quad 2-to-1 Multiplexer, 3-State | | A | A* | A | A | A |
| 259 | 8-Bit Addressable Latch | | | A | A | A | A |
| 260 | Dual 5-Input NOR Gate | | A | A | A | | |
| 266 | Quad EXCLUSIVE-OR, OC | | | A | | A | |
| 269 | 8-Bit Up/Down Counter | | | | A | | |
| 273 | Octal D Flip-Flop | | A | A | A | A | A |
| 279 | Quad S-R Latch | A | | | | | |
| 280 | 9-Bit Odd/Even Parity Generator/Checker | | A | | A* | A | A |
| 283 | 4-Bit Adder | | | A | A | A | A |
| 290 | Decade Counter | | | A | | | |
| 293 | 4-Bit Binary Counter | | | A | | | |
| 295 | 4-Bit Shift Register, 3-State | | | A** | | | |
| 297 | Digital Phase-Locked Loop Filter | | | | | A | A |
| 298 | Quad 2-Port Register | A | | A | A | | |
| 299 | Octal Shift/Storage Register, 3-State | | | | A | A | A |
| 322 | Octal Shift/Storage Register | | | | A | | |
| 323 | Octal Shift/Storage Register | | | | A | | |
| 350 | 4-Bit Four-Way Shifter | | A | | A | | |
| 352 | Dual 4-to-1 Multiplexer, Inverting | | | A | A | | |
| 353 | Dual 4-to-1 Multiplexer, Inverting, 3-State | | | A | A | | |
| 354 | 8-Input Multiplexer/Register, 3-State | | | | | Q1 '87 | Q1 '87 |
| 356 | 8-Input Multiplexer/Register, 3-State | | | | | A | A |
| 363 | Octal Latch, 3-State, MOS Compatible Outputs | | | A | | | |
| 364 | Octal D Flip-Flop, 3-State, MOS Compatible Outputs | | | A | | | |
| 365 | Hex Buffer with Common Enable, 3-State | A | | A* | A | A | A |
| 366 | Hex Inverter Buffer/Driver with Common Enable, 3-State | A | | A* | A | A | A |
| 367 | Hex Buffer, 4-Bit and 2-Bit, 3-State | A | | A* | A | A | A |
| 368 | Hex Inverter, 4-Bit and 2-Bit, 3-State | A | | A* | A | A | A |
| 373 | Octal Latch, 3-State | | A | A | A | A | A |
| 374 | Octal D Flip-Flop, 3-State | | A | A | A | A | A |
| 375 | Quad Latch | | | A | | | |
| 377 | Octal D-Type Flip-Flop with Enable | | | A | A | A | A |
| 378 | Hex D Flip-Flop with Enable | | | A | A | | |
| 379 | Quad D Flip-Flop with Enable | | | | A | | |
| 381 | 4-Bit Arithmetic Logic Unit | | | | A | | |
| 382 | 4-Bit Arithmetic Logic Unit | | | | A | | |
| 384 | 8-Bit Serial/Parallel Two's Complement Multiplier | | | | Q1 '87 | | |
| 385 | Quad Serial Adder/Subtractor | | | | 1H '87 | | |
| 390 | Dual Decade Ripple Counter | | | A | | A | A |
| 393 | Dual Binary Ripple Counter | | | A | | A | A |
| 395 | 4-Bit Cascadable Shift Register, 3-State | | | A* | A | | |
| 398 | Quad 2-Port Register with True and Complement Outputs | | | | A | | |
| 399 | Quad 2-Port Register | | | | A | | |
| 412 | Octal Multi-Mode Buffered Latch | | | | 1H '87 | | |
| 423 | Dual Retriggerable Monostable Multivibrator | | | | | A | A |
| 432 | Octal Multi-Mode Buffered Latch | | | | 1H '87 | | |
| 445 | BCD-to-Decimal Decoder with 7V Output | | | A | | | |

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# Technology Selection Guide

| DEVICE NUMBER | DESCRIPTION | STD | S | LS | FAST | HC | HCT |
|---|---|---|---|---|---|---|---|
| 490 | Dual Decade Ripple Counter | | | A | | | |
| 521 | 8-Bit Comparator | | | | A | | |
| 524 | 8-Bit Register Comparator | | | | A | | |
| 533 | Inverting Octal D Latch, 3-State | | | | A | A | A |
| 534 | Octal D Flip-Flop, 3-State | | | | A | A | A |
| 537 | 1-of-10 Decoder, 3-State | | | | A | | |
| 538 | 1-of-8 Decoder, 3-State | | | | A | | |
| 539 | Dual 1-of-4 Decoder, 3-State | | | | A | | |
| 540 | Octal Driver, 3-State | | | A | A | A | A |
| 541 | Octal Driver, 3-State | | | A | A | A | A |
| 543 | Octal Transparent Bidirectional Latch | | | | A | | |
| 544 | Octal Transparent Bidirectional Latch | | | | A | | |
| 545 | Octal Bus Transceiver | | | | A | | |
| 547 | Octal Decoder/Mux w/Addr. Latches and Acknowledge | | | | 1H '87 | | |
| 548 | Octal Decoder/Multiplexer with Acknowledge | | | | 1H '87 | | |
| 550 | Octal Registered Transceiver with Status Flags | | | | 1H '87 | | |
| 551 | Octal Registered Transceiver with Status Flags | | | | 1H '87 | | |
| 557 | 8 x 8 Multiplier with Latch, 3-State | | | | 1H '87 | | |
| 558 | 8 x 8 Multiplier, 3-State | | | | 1H '87 | | |
| 563 | Octal Transparent Inverting Latch, 3-State | | | | 1H '87 | A | A |
| 564 | Octal D-Type Inverting Flip-Flop, 3-State | | | | 1H '87 | A | A |
| 568 | BCD Decade Up/Down Synchronous Counter | | | A* | A | | |
| 569 | 4-Bit Binary Up/Down Synchronous Counter | | | A* | A | | |
| 573 | Octal Transparent Latch, 3-State | | | | 1H '87 | A | A |
| 574 | Octal D-Type Flip-Flop. Positive Edge-Triggered, 3-State | | | | | A | A |
| 579 | 8-Bit Up/Down Counter, Common I/O | | | | A | | |
| 583 | BCD Adder | | | | | Q1 '87 | Q1 '87 |
| 588 | GPIB Compatible Octal Transceiver | | | | A | | |
| 595 | 8-Bit Shift Register with Output Latch | | | | 1H '87 | | |
| 596 | 8-Bit Shift Register with Output Latch | | | | | | |
| 597 | 8-Bit Shift Register with Input Latch | | | | 1H '87 | A | A |
| 598 | 8-Bit Shift Register with Input Latch | | | | 1H '87 | | |
| 604 | Dual 8-Bit Latch, 3-State | | | | A | | |
| 605 | Dual 8-Bit Latch, OC | | | | A | | |
| 620 | Octal Transceiver, 3-State | | | A | A | | |
| 621 | Octal Transceiver, OC | | | A | A | | |
| 622 | Octal Transceiver, OC | | | A | A | | |
| 623 | Octal Transceiver, 3-State | | | A | A | | |
| 630 | Memory Error Detector/Corrector, 3-State | | | | 1H '87 | | |
| 631 | Memory Error Detector/Corrector | | | | 1H '87 | | |
| 640 | Octal Bus Transceiver, 3-State | | | A | A | A | A |
| 640-1 | Octal Bus Transceiver, 3-State 48 mA Sink Capability | | | A | | | |
| 641 | Octal Bus Transceiver, OC | | | A | A | | |
| 641-1 | Octal Bus Transceiver, OC | | | | A | | |
| 642 | Octal Bus Transceiver, OC | | | A | A | | |
| 643 | Octal True/Inverting Transceiver, 3-State | | | | | A | A |
| 645 | Octal Bus Transceiver, 3-State | | | A | | | |
| 645-1 | Octal Bus Transceiver, 3 State | | | A | A | | |
| 646 | Octal Bus Transceiver with Registers, 3-State | | | | A | A | A |
| 647 | Octal Bus Transceiver with Registers, OC | | | | | A | A |
| 648 | Octal Bus Transceiver with Registers, 3-State | | | | A | A | A |
| 649 | Octal Bus Transceiver with Registers, OC | | | | A | | |
| 655 | Octal Buffer with Parity Generator-Checker, 3-State | | | | A* | | |
| 656 | Octal Buffer with Parity Generator-Checker, 3-State | | | | A* | | |
| 657 | Octal Bus Transceiver with Parity Generator-Checker, 3-State | | | | A | | |
| 670 | 4 × 4 Register File, 3-State | | | | | A | A |
| 673 | 16-Bit SIPO Shift Register | | | | A | | |
| 674 | 16-Bit PISO Shift Register | | | | A | | |
| 675 | 16-Bit PISO Shift Register with Serial Output Capability | | | | A | | |
| 676 | 16-Bit PISO Shift Register with Parallel Output Capability | | | | A | | |

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|---|---|---|---|---|---|---|---|
| 688 | 8-Bit Magnitude Comparator | | | | | A | A |
| 764 | Dual Port RAM Controller with DRAM Refresh, with Latch | | | A | 1H '87 | | |
| 765 | 8-Bit Counter | | | | A | | |
| 779 | 8-Bit Counter | | | | A | | |
| 784 | 8-Bit Serial Multiplier and Adder/Subtractor | | | | A | | |
| 786 | 4-Bit Asynchronous Arbiter | | | | | | |
| 821 | 10-Bit Register, Noninverting, 3-State | | | | 1H '87 | | |
| 822 | 10-Bit Register, Inverting, 3-State | | | | 1H '87 | | |
| 823 | 9-Bit Register, Noninverting, 3-State | | | | 1H '87 | | |
| 824 | 9-Bit Register, Inverting, 3-State | | | | 1H '87 | | |
| 825 | 8-Bit Register, Noninverting, 3-State | | | | 1H '87 | | |
| 826 | 8-Bit Register, Inverting, 3-State | | | | 1H '87 | | |
| 827 | 10-Bit Buffer, Noninverting, 3-State | | | | 1H '87 | | |
| 828 | 10-Bit Buffer, Inverting, 3-State | | | | 1H '87 | | |
| 841 | 10-Bit Latch, Noninverting, 3-State | | | | 1H '87 | | |
| 842 | 10-Bit Latch, Inverting, 3-State | | | | 1H '87 | | |
| 843 | 9-Bit Latch, Noninverting, 3-State | | | | 1H '87 | | |
| 844 | 9-Bit Latch, Inverting, 3-State | | | | 1H '87 | | |
| 845 | 8-Bit Latch, Noninverting, 3-State | | | | 1H '87 | | |
| 846 | 8-Bit Latch, Inverting, 3-State | | | | 1H '87 | | |
| 861 | 10-Bit Transceiver, Noninverting, 3-State | | | | 1H '87 | | |
| 862 | 10-Bit Transceiver, Inverting, 3-State | | | | 1H '87 | | |
| 863 | 9-Bit Transceiver, Noninverting, 3-State | | | | | | |
| 864 | 9-Bit Transceiver, Inverting, 3-State | | | | | | |
| 881 | ALU/Function Generator | | | | 1H '87 | | |
| 882 | 32-Bit Carry-Look-Ahead Generator | | | | 1H '87 | | |
| 1240 | Octal Buffer, 3-State | | | | A | | |
| 1241 | Octal Buffer, 3-State | | | | A | | |
| 1242 | Quad Transceiver, Inverting, 3-State | | | | A | | |
| 1243 | Quad Bus Transceiver, 3-State | | | | A | | |
| 1244 | Octal Bus/Line Driver, 3-State | | | | A | | |
| 1245 | Octal Bus Transceiver, 3-State | | | | A | | |
| 3037 | 30 Ohm Transmission Line Driver Quad 2-Input NAND, OC | | | | A | | |
| 3038 | 30 Ohm Transmission Line Driver Quad 2-Input NAND, OC | | | | A | | |
| 3040 | 30 Ohm Transmission Line Driver Dual 4-Input NAND, OC | | | | A | | |
| 30240 | Octal Inverting 30 Ohm Transmission Line Driver, OC | | | | 1H '87 | | |
| 30241 | Octal 30 Ohm Transmission Line Driver | | | | 1H '87 | | |
| 30244 | Octal 30 Ohm Transmission Line Driver | | | | 1H '87 | | |
| 30245 | Octal Transceiver, 30 Ohm Transmission Line Driver | | | | 1H '87 | | |
| 30640 | Octal Transceiver, 30 Ohm Transmission Line Driver, Inverting | | | | 1H '87 | | |
| 4002 | Dual 4-Input NOR Gate | | | | | A | A |
| 4015 | Dual 4-Bit SIPO Shift Register | | | | | A | A |
| 4016 | Quad Bilateral Switch | | | | | A | A |
| 4017 | Johnson Decade Counter with 10 Decoded Outputs | | | | | A | A |
| 4020 | 14-Stage Binary Counter | | | | | A | A |
| 4024 | 7-Stage Binary Counter | | | | | A | A |
| 4040 | 12-Stage Binary Counter | | | | | A | A |
| 4046A | Phase Locked Loop with $V_{CO}$ | | | | | A | A |
| 4049 | Hex Inverting HIGH-to-LOW Level Shifter | | | | | A | |
| 4050 | Hex HIGH-to-LOW Level Shifter | | | | | A | |
| 4051 | 8-Channel Analog MUX/DMUX | | | | | A | A |
| 4052 | Dual 4-Channel Analog MUX/DMUX | | | | | A | A |
| 4053 | Triple 2-Channel Analog MUX/DMUX | | | | | A | A |
| 4059 | Programmable Divide By n Counter | | | | | Q1 '87 | Q1 '87 |
| 4060 | 14-Stage Ripple-Carry Binary Counter | | | | | A | A |
| 4066 | Quad Bilateral Switch | | | | | A | A |
| 4067 | 16-Channel Analog MUX/DMUX | | | | | A | A |

*A Version; **B Version; A = Available; 1H '87 = 1st Half of 1987; Q1 '87 = 1st Quarter of 1987; Q2 '87 = 2nd Quarter of 1987



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| DEVICE NUMBER | DESCRIPTION | STD | S | LS | FAST | HC | HCT |
|---|---|---|---|---|---|---|---|
| 4075 | Tripple 3-Input OR Gate | | | | | A | A |
| 4094 | 8-Stage Shift-And-Store Bus Register | | | | | A | A |
| 4316 | Quad Bilateral Switch | | | | | A | A |
| 4351 | 8-Channel Analog MUX/DMUX with Latch | | | | | A | A |
| 4352 | Dual 4-Channel Analog MUX/DMUX with Latch | | | | | Q1'87 | Q1'87 |
| 4353 | Triple 2-Channel Analog MUX/DMUX with Latch | | | | | A | A |
| 4510 | BCD Up/Down Counter | | | | | Q1'87 | Q1'87 |
| 4511 | BCD to 7-Segment Latch/Decoder/Driver | | | | | A | A |
| 4514 | 1-of-16 Decoder/DMUX with Input Latches | | | | | A | A |
| 4515 | 1-of-16 Decoder/DMUX with Input Latches | | | | | A | A |
| 4516 | Binary Up/Down Counter | | | | | Q1'87 | Q1'87 |
| 4518 | Dual BCD Counter | | | | | A | A |
| 4520 | Dual 4-Bit Binary Counter | | | | | A | A |
| 4538 | Dual Retriggerable Precision Monostable Multivibrator | | | | | A | A |
| 4543 | BCD to 7-Segment Latch/Decoder/Driver for LCDs | | | | | A | A |
| 7030 | 9-Bit x 16 Word Expandable FIFO Register | | | | | Q1'87 | Q1'87 |
| 7046 | Phase-Locked Loop with Lock Detector | | | | | A | A |
| 7597 | 8-Bit Shift Register with Latches | | | | | A | A |
| 40102 | Presettable 2-Decade BCD Down Counter | | | | | Q1'87 | Q1'87 |
| 40103 | 8-Bit Binary Down Counter | | | | | A | A |
| 40104 | 4-Bit Bidirectional Universal Shift Register | | | | | A | A |
| 40105 | 4-Bit x 16-Word FIFO Register | | | | | A | A |

*A Version; **B Version; A = Available; 1H '87 = 1st Half of 1987; Q1 '87 = 1st Quarter of 1987; Q2 '87 = 2nd Quarter of 1987





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# Function Cross Reference Guide

The Function Cross Reference Guide is provided for customer reference only. It does not represent all the devices available from Signetics' Logic Division.
The device number given is a base number. Check the Number Cross Reference Guide for the complete part number and availability.

## GATES

| FUNCTION | DEVICE NO. |
|---|---|
| **Inverters** | |
| Hex Inverter | 04 |
| Hex Inverter, OC | 05 |
| Hex Inverter buffer/Driver, OC (30V) | 06 |
| Hex Inverter Schmitt Trigger | 14 |
| Hex Inverter Buffer/Driver, OC (15V) | 16 |
| Octal Inverting Transmission Line Driver | 30240 |
| Hex Inverter (15V to TTL Levels) | 4049 |
| Hex Inverter Unbuffered Outputs | 4069UB |
| Hex Inverter Schmitt Trigger | 40106 |
| Dual Complementary Pair and Inverter, Unbuffered | 4007UB |
| **NAND** | |
| Quad 2-Input | 00 |
| Quad 2-Input, OC | 01 |
| Quad 2-Input, OC | 03 |
| Quad 2-Input, OC | 26 |
| Quad 2-Input NAND Buffer | 37 |
| Quad 2-Input NAND Buffer, OC | 38 |
| Quad 2-Input NAND Transmission Line Driver, OC | 3037 |
| Quad 2-Input NAND Transmission Line Driver, OC | 3038 |
| Triple 3-Input | 10 |
| Dual 4-Input, Schmitt Trigger | 13 |
| Dual 4-Input | 20 |
| 8-Input | 30 |
| Dual 4-Input NAND Buffer | 40 |
| Dual 4-Input NAND Line Driver | 140 |
| Dual 4-Input NAND Line Driver | 3040 |
| Quad 2-Input, Schmitt Trigger | 132 |
| Quad 2-Input | 4011 |
| Quad 2-Input, Unbuffered Outputs | 4011UB |
| Dual 4-Input | 4012 |
| Triple 3-Input | 4013 |
| 8-Input | 4068 |
| 12-Input | 134 |
| 13-Input | 133 |
| **AND** | |
| Quad 2-Input | 08 |
| Quad 2-Input | 4081 |
| Quad 2-Input, OC | 09 |
| Triple 3-Input | 11 |
| Dual 4-Input | 21 |
| Dual 4-Input | 4082 |
| **NOR** | |
| Quad 2-Input | 02 |
| Quad 2-Input | 28 |

| FUNCTION | DEVICE NO. |
|---|---|
| **NOR (Continued)** | |
| Quad 2-Input | 128 |
| Quad 2-Input | 4001 |
| Quad 2-Input, Unbuffered Output | 4001UB |
| Quad 2-Input, OC | 33 |
| Triple 3-Input | 27 |
| Triple 3-Input | 4025 |
| Dual 3-input, with Inverter | 4000 |
| Dual 4-Input | 4002 |
| Dual 4-Input, with Strobe | 25 |
| Dual 5-Input | 260 |
| 8-Input | 4078 |
| **OR** | |
| Quad 2-Input | 32 |
| Quad 2-Input | 4071 |
| Triple 3-Input | 4075 |
| Dual 4-Input | 4072 |
| **Exclusive-OR** | |
| Quad | 86 |
| Quad | 4030 |
| Quad, OC | 136 |
| Quad | 4070 |
| Quad Exclusive OR-NOR | 135 |
| **Exclusive-NOR** | |
| Quad | 4077 |
| Quad, OC | 266 |
| Quad Exclusive OR-NOR | 135 |
| **Combination Gates** | |
| Expandable Dual 2-Wide 2-Input AND-OR-Invert | 50 |
| Dual 2-Wide 2-Input AND-OR-Invert | 51 |
| 4-Wide 2-Input AND-OR-Invert | 54 |
| Dual 4-Input AND/OR Gate | 58 |
| 4-2-3-2 Input AND-OR-Invert | 64 |
| Dual 3-Input NOR Gate with Inverter | 4000 |
| Dual Complementary Pair and Inverter, Unbuffered | 4007UB |
| Dual 2-Wide 2-Input AND-OR-Invert | 4085 |
| 4-Wide 2-Input AND-OR-Invert | 4086 |

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

# Function Cross Reference Guide

## DUAL FLIP-FLOPS

| FUNCTION | DEVICE NUMBER | CLOCK EDGE | SET | CLEAR |
|---|---|---|---|---|
| D | 74 | ↓ | LOW | LOW |
| D | 4013 | ↓ | HIGH | HIGH |
| JK | 73 | ↓ | | LOW |
| JK | 76 | ↓ | LOW | LOW |
| JK | 107 | ↓ | | LOW |
| JK | 109 | ↓ | LOW | LOW |
| JK | 112 | ↓ | LOW | LOW |
| JK | 113 | ↓ | LOW | |
| JK | 114 | ↓ | LOW | LOW |
| JK | 4027 | ↓ | HIGH | HIGH |

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

## MULTIPLE FLIP-FLOPS

| FUNCTION | DEVICE NUMBER | RESET (LEVEL) | CLOCK EDGE | OUTPUT |
|---|---|---|---|---|
| Quad | 173 | HIGH | ↑ | True |
| Quad D | 175 | LOW | ↑ | True, Comp |
| Quad D | 40175 | LOW | ↑ | True |
| Quad D with Enable | 379 | | ↑ | True, Comp |
| Quad D, 3-State | 4079 | HIGH | ↑ | True |
| Quad D, 3-State | 8T10 | HIGH | ↑ | True |
| Hex D | 174 | LOW | ↑ | True |
| Hex D with Enable | 378 | | ↑ | True |
| Octal D | 273 | LOW | ↑ | True |
| Octal D, 3-State | 374 | | ↑ | True |
| Octal D with Enable | 377 | | ↑ | True |
| Octal D, 3-State | 534 | | ↑ | Comp |
| Octal D, 3-State | 564 | | ↑ | Comp |
| Octal D, 3-State | 574 | | ↑ | True |
| Octal D, 3-State | 40374 | | ↑ | True |
| Octal D, 3-State | 8TS806 | | ↑ | True |
| Octal D, 3-State | 8TS808 | | ↑ | Comp |
| Octal D, 3-State, MOS Compatible Outputs | 364 | | ↑ | True |

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# Function Cross Reference Guide

## OTHER REGISTERS, REGISTER FILES

| FUNCTION | DEVICE NUMBER | BITS | SERIAL ENTRY | PARALLEL ENTRY* | CLOCK |
|---|---|---|---|---|---|
| Quad 2 Port | 298 | 4 x 2 | | 2D (mux) | ⌝⌞ |
| Quad 2 Port | 398 | 4 x 2 | | 2D (mux) | ⌟⌜ |
| Quad 2 Port | 399 | 4 x 2 | | 2D (mux) | ⌟⌜ |
| Register File, OC | 170 | 4 x 4 | | 4A | ⌝⌞ |
| Multiple Port Register File, 3-State | 172 | 16 | | 3D (mux) | ⌝⌞ |
| 4 x 4 Register File, 3-State | 670 | 4 x 4 | | 4A | ⌝⌞ |
| 16 x 5 FIFO, 3-State | 225 | 5 | | 5S | ⌟⌜ |
| 4 x 16 FIFO | 40105 | 4 | D | 4S | |
| 10-Bit Register, Noninverting, 3-State | 821 | 10 | | 2D | ⌟⌜ |
| 10-Bit Register, Inverting, 3-State | 822 | 10 | | 2D | ⌟⌜ |
| 9-Bit Register, Noninverting, 3-State | 823 | 9 | | 2D | ⌟⌜ |
| 9-Bit Register, Inverting, 3-State | 824 | 9 | | 2D | ⌟⌜ |
| 8-Bit Register, Noninverting, 3-State | 825 | 8 | | 2D | ⌟⌜ |
| 8-Bit Register, Inverting, 3-State | 826 | 8 | | 2D | ⌟⌜ |

*D = D type input, A = Asynchronous data input, S = Synchronous data input

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# Function Cross Reference Guide

## SHIFT REGISTERS

S = Synchronous, A = Asynchronous

| FUNCTION | DEVICE NUMBER | BITS | SERIAL ENTRY | PARALLEL ENTRY | CLOCK |
|---|---|---|---|---|---|
| Serial In/Serial Out Shift Register | 91 | 8 | $D_A$ and $D_B$ | | ⌐ |
| Serial In/Serial Out Shift Right | 4006 | (2 × 4) (2 × 5) | D | | ⌐ |
| Serial In/Serial Out Shift Right | 4031 | 64 | $D_A$ + $D_B$ | | ⌐ |
| Dual Serial In/Serial Out Shift Right, 3-State | 4517 | (4 × 16) | D | | ⌐ |
| Quad Serial In/Serial Out Shift Right | 4731 | 64 | D | | ⌐ |
| Serial In/Serial Out Variable Length Shift Right | 4557 | 1 to 64 | $D_A$ + $D_B$ | | ⌐ and ⌐ |
| Serial In/Serial Out Shift Right, 3-State | 4094 | 8 | D | | ⌐ |
| Parallel In/Serial Out | 674 | 16 | D | 16S | ⌐ |
| Serial In/Serial/Parallel Out | 675 | 16 | D | | ⌐ |
| Serial/Parallel In/Serial Out | 676 | 16 | D | 16S | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 94 | 4 | D | 2 × 4A (mux) | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 165 | 8 | D | 8A | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 166 | 8 | D | 8S | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 195 | 4 | J, $\overline{K}$ | 4S | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 199 | 8 | J, K | 8S | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 597 | 8 | D | 8S | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 4014 | 8 | D | 8S | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 4021 | 8 | D | 8A | ⌐ |
| Parallel/Serial In/Serial Out Shift Right | 8274 | 10 | D | 10S | ⌐ |
| Parallel/Serial In/Serial Out Shift Right, 3-State | 598 | 8 | S0, S1 | 8S | ⌐ |
| Serial In/Parallel Out Shift Right | 164 | 8 | $D_0$ and $D_1$ | | ⌐ |
| Serial In/Parallel Out Shift Right, with Reset | 8273 | 10 | D | | ⌐ or ⌐ |
| Dual Serial In/Parallel Out Shift Right | 4015 | 4 | D | | ⌐ |
| Serial In/Parallel Out, 3-State | 595 | 8 | D | | ⌐ |
| Serial In/Parallel Out, OC | 596 | 8 | D | | ⌐ |
| Serial In/Parallel Out | 673 | 16 | D | | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right | 95 | 4 | D | 5A | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right | 96 | 5 | D | 5A | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right | 40195 | 4 | J, $\overline{K}$ | 4S | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right | 8271 | 4 | D | 4S | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right | 82S71 | 4 | D | 4S | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right | 4035 | 4 | J, $\overline{K}$ | 4S | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right, 3-State | 295 | 4 | D | 4S | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right, 3-State | 395 | 4 | D | 4S | ⌐ |
| Parallel In/Serial In/Parallel Out Shift Right, 3-State | 322 | 8 | $D_0$ + $D_1$ | 8S (I/O) | ⌐ |
| Parallel In/Serial In/Parallel Out Bidirectional | 194 | 4 | Dr, $D_L$ | 4S | ⌐ |
| Parallel In/Serial In/Parallel Out Bidirectional | 198 | 8 | Dr, $D_L$ | 8S | ⌐ |
| Parallel In/Serial In/Parallel Out Bidirectional | 40194 | 4 | Dr, $D_L$ | 4S | ⌐ |
| Parallel In/Serial In/Parallel Out Bidirectional, 3-State | 299 | 8 | Dr, $D_L$ | 8S | ⌐ |
| Parallel In/Serial In/Parallel Out Bidirectional, 3-State | 323 | 8 | Dr, $D_L$ | 8S (I/O) | ⌐ |
| Parallel In/Serial In/Parallel Out Bidirectional, 3-State | 40194 | 4 | Dr, $D_L$ | 4S | ⌐ |
| 4-Bit Shifter, 3-State | 350 | 4 | | 4A | |

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# Function Cross Reference Guide

## LATCHES

| FUNCTION | DEVICE NUMBER | COMMON CLEAR (LEVEL) | ENABLE INPUT (LEVEL) | OUTPUT |
|---|---|---|---|---|
| Quad D | 75 | | 2 (H) | True, Comp |
| Quad D | 375 | | 2 (H) | True, Comp |
| Quad D | 4042 | | 2 (H) | True |
| Quad SR | 279 | | | True |
| Quad SR, 3-State | 4043 | | | True |
| Quad SR, 3-State | 4044 | | | True |
| Dual 4-Bit Transparent | 116 | LOW | 2 (L) | True |
| Dual 4-Bit Addressable | 256 | LOW | 1 (L) | True |
| Dual 4-Bit, Strobed | 4508 | HIGH | 1 (L) | True |
| Dual 8-Bit, 3-State | 604 | | | True |
| Dual 8-Bit, OC | 605 | | | True |
| 6-Bit (2-Bit and 4-Bit) | 8T3404 | | 1 (L) | Comp |
| 8-Bit Addressable | 259 | LOW | 1 (H) | True |
| 8-Bit Addressable | 4724 | HIGH | 1 (L) | True |
| 8-Bit Addressable | 9334 | LOW | 1 (L) | True |
| 8-Bit, Noninverting, 3-State | 845 | LOW | 1 (H) | True |
| 8-Bit, Inverting, 3-State | 846 | LOW | 1 (H) | Comp |
| 9-Bit, Noninverting, 3-State | 843 | LOW | 1 (H) | True |
| 9-Bit, Inverting, 3-State | 844 | LOW | 1 (H) | Comp |
| 10-Bit, Noninverting, 3-State | 841 | | 1 (H) | True |
| 10-Bit, Inverting, 3-State | 842 | | 1 (H) | Comp |
| Octal, 3-State | 373 | | 1 (H) | True |
| Octal, Multimode, Buffered | 412 | LOW | | True |
| Octal, Multimode, Buffered | 432 | LOW | | Comp |
| Octal Inverting, 3-State | 533 | | 1 (H) | Comp |
| Octal, Transparent, Bidirectional | 543 | | 4 (L) | True |
| Octal, Transparent, Bidirectional | 544 | | 4 (L) | Comp |
| Octal, Transparent, Inverting, 3-State | 563 | | 1 (H) | Comp |
| Octal, Transparent, 3-State | 573 | | 1 (H) | True |
| Octal Inverting, 3-State | 533 | | 1 (H) | Comp |
| Octal Transparent, 3-State | 40373 | | 1 (H) | True |
| Octal Transparent, 3-State | 8TS805 | | 1 (H) | True |
| Octal Inverting, 3-State | 8TS807 | | 1 (H) | Comp |
| Octal, 3-State with MOS Compatible Outputs | 363 | | 1 (H) | True |

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# Function Cross Reference Guide

## MULTIPLEXERS

| FUNCTION | DEVICE NUMBER | ENABLE INPUT (LEVEL) | SELECT INPUTS | OUTPUT |
|---|---|---|---|---|
| Quad 2-Input | 157 | 1 (L) | 1 | True |
| Quad 2-Input | 158 | 1 (L) | 1 | True |
| Quad 2-Input | 298 | Clocked ⌝L | 1 | True, Latched |
| Quad 2-Input | 398 | 1 (H) | 1 | True, Comp Registered |
| Quad 2-Input | 399 | 1 (H) | 1 | True, Registered |
| Quad 2-Input | 4019 | | 2 | True |
| Quad 2-Input | 4519 | | 2 | True |
| Quad 2-Input | 8266 | | 2 | True |
| Quad 2-Input | 9322 | 1 (L) | 1 | True |
| Quad 2-Input, 3-State | 257 | | 1 | True |
| Quad 2-Input, 3-State | 258 | | 1 | Comp |
| Quad 2-Input, OC | 8234 | | 2 | Comp |
| Dual 4-Input | 153 | 2 (L) | 2 | True, Comp |
| Dual 4-Input | 352 | 2 | 2 | Comp |
| Dual 4-Input | 9309 | | 2 | True, Comp |
| Dual 4-Input | 4539 | 2 (L) | 2 | True |
| Dual 4-Input, 3-State | 253 | | 2 | True |
| Dual 4-Input, 3-State | 353 | 2 | 2 | Comp |
| 8-Input | 9312 | 1 (L) | 3 | True, Comp |
| 8-Input | 151 | 1 (L) | 3 | True, Comp |
| 8-Input, 3-State | 251 | | 1 | True, Comp |
| 8-Input, 3-State | 356 | 1 (L) | 3 | True, Latched |
| 8-Input, 3-State | 354 | 2 (L) | 3 | True, Latched |
| 8-Input, 3-State | 4512 | 1 (L) | 3 | True |
| 16-Input | 150 | 1 (L) | 4 | Comp |

## ANALOG MULTIPLEXERS/DEMULTIPLEXERS AND SWITCHES

| FUNCTION | DEVICE NUMBER |
|---|---|
| Triple 2-Channel Mux/Demux | 4053 |
| Dual 4-Channel Mux/Demux | 4052 |
| 8-Channel Mux/Demux | 4051 |

| FUNCTION | DEVICE NUMBER |
|---|---|
| 16-Channel Mux/Demux | 4066 |
| Quad Bilateral Switches | 4016 |
| Quad Bilateral Switches | 4067 |
| Quad Bilateral Switch | 4316 |
| 8-Channel Analog MUX/DeMUX with Latch | 4351 |
| Dual 4-Channel Analog MUX/DeMUX with Latch | 4352 |
| Triple 2-Channel Analog MUX/DeMUX with Latch | 4353 |

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# Function Cross Reference Guide

## COUNTERS

| FUNCTION | DEVICE NUMBER | MODULUS | PARALLEL ENTRY | PRESETTABLE | CLOCK EDGE |
|---|---|---|---|---|---|
| Asynchronous | 90 | 2 × 5 | | | ↓ |
| Asynchronous | 290 | 2 × 5 | | | ↓ |
| Asynchronous | 92 | 2 × 6 | | | ↓ |
| Asynchronous | 93 | 2 × 8 | | | ↓ |
| Asynchronous | 293 | 2 × 8 | | | ↓ |
| Asynchronous | 176 | 2 × 5 | A | X | ↓ |
| Asynchronous | 177 | 2 × 8 | A | X | ↓ |
| Asynchronous | 197 | 2 × 8 | A | X | ↓ |
| Asynchronous | 290 | 2 × 5 | | | ↓ |
| Asynchronous | 293 | 2 × 8 | | | ↓ |
| Asynchronous | 390 | 2 × 5 | | | ↓ |
| Asynchronous | 393 | 2 × 8 | | | ↓ |
| Asynchronous | 490 | 2 × 5 | | | ↓ |
| Asynchronous | 4020 | 12 | | | ↓ |
| Asynchronous | 4024 | 7 | | | ↓ |
| Asynchronous | 4040 | 14 | | | ↓ |
| Asynchronous with Oscillator | 40b0 | 14 | | | |
| Synchronous | 160 | 10 | S | X | ↑ |
| Synchronous | 161 | 16 | S | X | ↑ |
| Synchronous | 162 | 10 | S | X | ↑ |
| Synchronous | 163 | 16 | S | X | ↑ |
| Synchronous, 3-State | 751 | 256 | S | X | ↑ |
| Synchronous, 3-State | 752 | 100 | S | X | ↑ |
| Synchronous | 4256 | 16 | A | | ↑ or ↓ |
| Synchronous | 40161 | 16 | S | X | ↑ |
| Synchronous | 40163 | 16 | S | X | ↑ |
| Synchronous (Dual) | 4518 | 10 | | | ↑ or ↓ |
| Synchronous (Dual) | 4520 | 16 | | | ↑ or ↓ |
| Up/Down | 168 | 10 | S | X | ↑ |
| Up/Down | 169 | 16 | S | X | ↑ |
| Up/Down | 190 | 10 | A | X | ↑ |
| Up/Down | 191 | 16 | A | X | ↑ |
| Up/Down | 192 | 10 | A | X | ↑ |
| Up/Down | 193 | 16 | A | X | ↑ |
| Up/Down | 269 | 8 | S | X | ↑ |
| Up/Down | 4029 | 10, 16 | A | X | ↑ |
| Up/Down | 4510 | 10 | A | X | ↑ |
| Up/Down | 4516 | 16 | A | X | ↑ |
| Up/Down | 40193 | 16 | A | X | ↑ |
| Up/Down, 3-State | 568 | 10 | S | X | ↑ |
| Up/Down, 3-State | 569 | 16 | S | X | ↑ |
| Up/Down, 3-State | 579 | 8 | S (I/O) | X | ↑ |
| Up/Down, 3-State | 779 | 8 | S (I/O) | X | ↑ |
| Frequency Divider | 4059 | Programmable 3 to 15,999 | | | ↑ |
| Johnson | 4017 | 10 | | | ↑ or ↓ |
| Johnson | 4018 | 5 | A | | |
| Johnson | 4022 | 8 | | | ↑ or ↓ |

S = Synchronous  A = Asynchronous

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

# Function Cross Reference Guide

## TRI-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

| FUNCTION | DEVICE NUMBER | OUTPUT |
|---|---|---|
| Quad Buffer | 125 | True |
| Quad Buffer | 126 | True |
| Quad Bus Driver | 8T09 | |
| Quad Bus Transceiver | 242 | Comp |
| Quad Bus Transceiver | 243 | True |
| Quad Bus Transceiver | 1242 | Comp |
| Quad Bus Transceiver | 1243 | True |
| Quad Bus Transceiver | 8T34 | Comp |
| Quad Bus Transceiver | 8T126 | Comp |
| Quad Bus Transceiver | 8T127 | Comp |
| Quad Bus Transceiver | 8T128 | True |
| Quad Bus Transceiver | 8T129 | True |
| Hex Buffer | 365 | True |
| Hex Inverter | 366 | Comp |
| Hex Buffer, 4-Bit and 2-Bit | 367 | True |
| Hex Inverter, 4-Bit and 2-Bit | 368 | Comp |
| Hex Buffer | 8T95 | True |
| Hex Inverter | 8T96 | Comp |
| Hex Buffer | 8T97 | True |
| Hex Inverter | 8T98 | Comp |
| Hex Buffer | 40097 | True |
| Hex Buffer | 40098 | Comp |
| Octal Buffer | 240 | Comp |
| Octal Buffer | 241 | True |
| Octal Buffer | 244 | True |
| Octal Buffer | 40240 | Comp |
| Octal Buffer | 40244 | True |
| Octal Buffer | 540 | Comp |
| Octal Buffer | 541 | True |
| Octal Buffer with Parity Generator/Checker | 455 | Comp |
| Octal Buffer with Parity Generator/Checker | 456 | True |
| Octal Buffer | 1240 | Comp |
| Octal Buffer | 1241 | True |
| Octal Buffer | 1244 | True |
| Octal Buffer with Parity Generator-Checker | 655 | Comp |
| Octal Buffer with Parity Generator-Checker | 656 | True |
| 10-Bit Buffer | 827 | True |
| 10-Bit Buffer | 828 | Comp |
| Octal Transceiver | 245 | True |
| Octal Transceiver | 545 | True |
| Octal Transceiver with IEEE-488 Termination Resistors | 588 | True |
| Octal Transceiver | 620 | Comp |
| Octal Transceiver | 623 | True |
| Octal Transceiver | 640, 640-1 | Comp |
| Octal Transceiver | 643 | True, Comp |
| Octal Transceiver | 645, 645-1 | True |
| Octal Bus Transceiver with Parity Generator-Checker | 657 | True |
| Octal Bus Transceiver | 1245 | True |
| Octal Transceiver | 40245 | True |
| Octal Transceiver | 8T125 | Comp |
| Octal Transceiver/Register | 646 | True |
| Octal Transceiver/Register | 648 | Comp |
| 10-Bit Transceiver | 861 | True |
| 10-Bit Transceiver | 862 | Comp |
| 9-Bit Transceiver | 863 | True |
| 9-Bit Transceiver | 864 | Comp |

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.





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# Function Cross Reference Guide

## LEVEL TRANSLATORS

| FUNCTION | DEVICE NUMBER |
|---|---|
| Hex Inverting Buffer, Up to 15V Input, TTL Level Output | 4049 |
| Hex Non-Inverting Buffer, Up to 15V Input, TTL Level Output | 4050 |
| Quad Voltage Translator, 3-State, TTL Input, 15V Output | 4104 |
| Quad Transceiver, MOS/CMOS to TTL | 8T26 |
| Quad Transceiver, MOS/CMOS to TTL | 8T28 |

## PRIORITY ENCODERS

| FUNCTION | DEVICE NUMBER | INPUT ENABLE (LEVEL) | INPUT/OUTPUT (LEVEL) |
|---|---|---|---|
| 8-to-3 | 148 | LOW | Active-LOW |
| 8-to-3 | 4532 | HIGH | Active-HIGH |
| 10-to-4 (BCD) | 147 | | Active-LOW |

## DECODERS/DEMULTIPLEXERS

| FUNCTION | DEVICE NUMBER | ADDRESS INPUTS | ENABLE (LEVEL) | OUTPUT (LEVEL) |
|---|---|---|---|---|
| Dual 1 of 4 | 139 | 2 + 2 | 1 (L) + 1 (L) | 4 (L) + 4 (L) |
| Dual 1 of 4 | 155 | 2 | 2 (L) + 1 (L), 1 (H) | 4 (L) + 4 (L) |
| Dual 1 of 4 | 156 | 2 | 2 (L) + 1 (L), 1 (H) | 4 (L) + 4 (L) |
| Dual 1 of 4 | 539 | 2 + 2 | 1 (L) + 1 (L) | 4 (H) + 4 (H) |
| Dual 1 of 4 | 4555 | 2 + 2 | 1 (L) + 1 (L) | 4 (H) |
| Dual 1 of 4 | 4556 | 2 + 2 | 1 (L) + 1 (L) | 4 (L) |
| 1 of 8 | 138 | 3 | 2 (L) 1 (H) | 8 (L) |
| 1 of 8 | 237 | 3 | 1 (L), 1 (H) | 8 (H) |
| 1 of 8 | 238 | 3 | 2 (L), 1 (H) | 8 (H) |
| 1 of 8 | 538 | 3 | 2 (L), 2 (H) | 8 (H) |
| 1 of 8 | 82S50 | 4 (BCD) | | 8 (L) |
| 1 of 10 | 42 | 4 (BCD) | | 10 (L) |
| 1 of 10, OC | 45 | 4 (BCD) | | 10 (L) |
| 1 of 10, OC | 145 | 4 (BCD) | | 10 (L) |
| 1 of 10, OC | 445 | 4 (BCD) | | 10 (L) |
| 1 of 10 | 537 | 4 | 1 (L), 1 (H) | 10 (H) |
| 1 of 10 | 4028 | 4 (BCD) | | 10 (H) |
| 1 of 10 | 9301 | 4 (BCD) | | 10 (L) |
| 1 of 10 | 82S52 | 4 (BCD) | | 10 (L) |
| 1 of 16 | 154 | 4 | 2 (L) | 16 (L) |
| 1 of 16 | 4514 | 4 (Latched) | 1 (L) | 16 (H) |
| 1 of 16 | 4515 | 4 (Latched) | 1 (L) | 16 (L) |
| Octal, with Address Latches and Acknowledge | 547 | 3 | 1 (L), 2 (H) | 8 (L) |
| Octal, with Acknowledge | 548 | 3 | 2 (L), 2 (H) | 8 (L) |
| BCD to 7 Segment Decoder/Driver | 4511 | 4 (Latched) | 1 (L) | 7 (H) |
| BCD to 7 Segment Decoder/Driver | 4543 | 4 (Latched) | | 7 (H) |

## BUFFERS, DRIVERS AND RECEIVERS

| FUNCTION | DEVICE NUMBER | OUTPUT |
|---|---|---|
| Quad 2-Input NOR Buffer | 128 | |
| Quad Buffer | 4041 | True, Comp |
| Hex Buffer | 4049 | Comp |
| Hex Buffer | 4050 | True |
| Strobed Hex Inverter/Buffer | 4502 | Comp |
| Dual 4-Input NAND Line Driver | 140 | |
| Dual Line Driver (AND/OR) | 8T13 | |
| Dual EIA-232B/MIL Line Driver | 8T15 | Comp |
| Dual EIA-232B/MIL Receiver | 8T16 | |
| Dual Line Driver for IBM 360/370 Interface | 8T23 | |
| Dual Line Receiver for IBM 360/370 Interface | 8T24 | |
| Hex Bus Receiver (DM8837) | 8T37 | |

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.



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# Function Cross Reference Guide

## OPEN COLLECTOR, BUFFERS, DRIVERS, AND TRANSCEIVERS

| FUNCTION | DEVICE NUMBER | OUTPUT |
|---|---|---|
| Quad Bus Transceiver | 8T38 | |
| Quad Bus Transceiver | 8T26 | Comp |
| Quad Bus Transceiver | 8T28 | True |
| Hex Inverter | 05 | Comp |
| Hex Inverter/Driver | 06 | Comp |
| Hex Buffer/Driver | 07 | True |
| Hex Buffer/Driver | 16 | Comp |
| Hex buffer/Driver | 17 | True |
| Octal Transceiver | 621 | True |
| Octal Transceiver | 622 | Comp |
| Octal Transceiver | 641, 641-1 | True |
| Octal Transceiver | 642, 642-2 | Comp |
| Octal Transceiver and Registers | 647 | True |
| Octal Transceiver and Registers | 649 | Comp |
| BCD to Decimal Decoder/Driver | 45 | Active-LOW |
| BCD to Decimal Decoder/Driver | 145 | Active-LOW |

## MULTIVIBRATORS AND PHASE LOCKED LOOPS

| FUNCTION | DEVICE NUMBER |
|---|---|
| Monostable Multivibrator | 121 |
| Dual Retriggerable Monostable Multivibrator | 123 |
| Dual Monostable Multivibrator | 221 |
| Dual Retriggerable Monostable Multivibrator | 423 |
| Dual Monostable Multivibrator | 4528 |
| Dual Retriggerable Monostable Multivibrator | 4538 |
| Monostable/Astable Multivibrator | 4047 |
| Digital Phase Locked Loop Filter | 297 |
| Phase Locked Loop | 4046 |

## COMPARATORS

| FUNCTION | DEVICE NUMBER |
|---|---|
| 4-Bit Comparator | 85 |
| 4-Bit Comparator | 4585 |
| 5-Bit Comparator | 9324 |
| 8-Bit Comparator | 521 |
| 8-Bit Comparator | 688 |

## PARITY

| FUNCTION | DEVICE NUMBER |
|---|---|
| 8-Bit Odd/Even Parity Checker | 180 |
| 8-Bit Parity Generator/Checker | 8262 |
| 8-Bit Parity Generator/Checker | 82S62 |
| 9-Bit Odd/Even Parity Generator/Checker | 280 |
| 13-Bit Parity Generator/Checker | 4531 |

## ARITHMETIC FUNCTIONS

| FUNCTION | DEVICE NUMBER |
|---|---|
| 4-Bit Binary Full Adder, Ripple Carry | 83 |
| 4-Bit Binary Full Adder, Fast Carry | 283 |
| 4-Bit Binary Full Adder | 4008 |
| 4-Bit BCD Full Adder | 82S83 |
| 4-Bit ALU | 181 |
| 4-Bit ALU | 381 |
| 4-Bit ALU | 382 |
| 4-Bit ALU | 82S83 |
| Look Ahead Carry Generator | 182 |
| 8-Bit Serial/Parallel Two's Complement Multiplier | 384 |
| 8 x 8 Multiplier w/Latch | 557 |
| 8 x 8 Multiplier | 558 |
| BCD Adder | 583 |
| 8-Bit Serial Multiplier Adder, Subtractor | 784 |
| ALU Function Generator | 881 |
| 32-Bit Look-Ahead-Carry Generator | 882 |

## SPECIAL FUNCTIONS

| FUNCTION | DEVICE NUMBER |
|---|---|
| 64-Bit FAST Random Access Memory | 189 |
| Memory Error Detector/Corrector, 3-State | 630 |
| Memory Error Detector/Corrector, OC | 631 |
| Dual-Port RAM Controller with Dynamic Memory Refresh | 764 |
| Dual Port RAM Controller without Latch | 765 |
| IEC/IEEE Bus Interface | 4738 |
| Frequency Synthesizer | 4750 |
| A.C. Motor Control Circuit | 4752 |
| 18-Element Bar Graph LCD Driver | 4754 |

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.





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# Family Characteristic Specifications

## INTERFACING COMMON LOGIC FAMILIES

| From | To | ECL | | TTL | | | | CMOS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 4000B | |
| | | 10K | 100K | STD | S | FAST | LS | HC | HCT | $V_{DD} = 5V$ | $V_{DD} > 5V$ |
| ECL | 10K | D | D | T | T | T | T | T | T | T | T |
| | 100K | D | D | T | T | T | T | T | T | T | T |
| TTL | STD | T | T | D | D | D | D | P | D | P | T |
| | S | T | T | D | D | D | D | P | D | P | T |
| | FAST | T | T | D | D | D | D | P | D | P | T |
| | LS | T | T | D | D | D | D | P | D | P | T |
| CMOS | HC | T | T | D | D | D | D | D | D | D | T |
| | HCT | T | T | D | D | D | D | D | D | D | T |
| | 4000B at 5V | T | T | D | D | D | D | D | D | D | T |
| | 4000B $V_{DD} > 5V$ | T | T | T | T | T | T | T | T | T | D |

D — Direct interface
P — Pullup resistor required
T — Level translator required



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# 10K & 100K ECL Product List

## 10K ECL

| DEVICE TYPE | DESCRIPTION |
|---|---|
| 10100 | Quad 2-Input NOR Gate |
| 10101 | Quad OR/NOR Gate |
| 10102 | Quad 2-Input NOR Gate |
| 10103 | Quad 2-Input OR Gate |
| 10104 | Quad 2-Input AND Gate |
| 10105 | Triple 2-3-2-Input OR/NOR Gate |
| 10106 | Triple 4-3-3-Input NOR Gate |
| 10107 | Triple 2-Input Exclusive-OR/Exclusive-NOR Gate |
| 10108 | Dual 3-Input AND/NAND Gate |
| 10109 | Dual 4-5-Input OR/NOR Gate |
| 10110 | Dual 3-Input/3-Output OR Gate (Line Driver) |
| 10111 | Dual 3-Input/3-Output NOR Gate (Line Driver) |
| 10113 | Quad Exclusive-OR Gate with Enable |
| 10114 | Triple Line Receiver |
| 10115 | Quad Line Receiver |
| 10116 | Triple Line Receiver |
| 10117 | Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate |
| 10118 | Dual 2-Wide 3-Input OR-AND Gate |
| 10119 | 4-Wide 4-3-3-3-Input OR-AND Gate |
| 10121 | 4-Wide OR-AND/OR-AND-INVERT Gate |
| 10123 | Triple 4-3-3-Input Bus Driver |
| 10124 | Quad TTL to ECL Translator |
| 10125 | Quad ECL to TTL Translator |
| 10130 | Dual D-Type Latch |
| 10131 | Dual D-Type Master-Slave Flip-Flop |
| 10132 | Dual 2-Input Multiplexer with Clocked D-Type Latches and Common Reset |
| 10133 | Quad Latch with D-Type Inputs and Enable Outputs |
| 10134 | Dual 2-Input Multiplexer with Clocked D-Type Latches |

| DEVICE TYPE | DESCRIPTION |
|---|---|
| 10135 | Dual J-K Master-Slave Flip-Flop |
| 10136 | Universal Hexadecimal Counter |
| 10137 | Universal Decade Counter |
| 10141 | 4-Bit Universal Shift Register |
| 10149 | 1024-Bit, 4 Bits per Word PROM |
| 10149A | 1024-Bit, 4 Bits per Word PROM |
| 10158 | Quad 2-to-1 Multiplexer (Non-Inverting) |
| 10159 | Quad 2-to-1 Multiplexer (Inverting) |
| 10160 | 12-Bit Parity Generator/Checker |
| 10161 | 3-Bit Decoder with 2 Enable Inputs (1-of-8 LOW) |
| 10162 | 3-Bit Decoder with 2 Enable Inputs (1-of-8 HIGH) |
| 10164 | 8-Input Multiplexer with Enable Input |
| 10165 | 8-Input Priority Encoder |
| 10171 | Dual 2-Bit Decoder (1-of-4 Lines LOW) |
| 10172 | Dual 2-Bit Decoder (1-of-4 Lines HIGH) |
| 10173 | Quad 2-Input Multiplexer with Latched Outputs |
| 10174 | Dual 4-to-1 Multiplexer with Enable |
| 10175 | Quint D-Latch w/Common Reset & 2 Wire-OR Common Clock Inputs |
| 10176 | Hex D-Type Master-Slave Flip-Flop |
| 10179 | Look-Ahead Carry Block-Arithmetic Functions |
| 10180 | Dual High-Speed Adder/Subtractor |
| 10181 | 4-Bit Logic Unit/Function Generator |
| 10188 | Hex Buffer (Non-Inverting) |
| 10189 | Hex Inverter |
| 10192 | Quad Differential Line Driver |
| 10210 | Dual 3-Input/3-Output (High-Speed) OR Gate |
| 10211 | Dual 3-Input/3-Output (High-Speed) NOR Gate |
| 10216 | Triple Differential OR/NOR Line Receiver (High-Speed) |
| 10231 | Dual D-Type Master-Slave Flip-Flop (High-Speed) |

## 100K ECL

| DEVICE TYPE | DESCRIPTION |
|---|---|
| 100101 | Triple 5-Input Gate |
| 100102 | Quint 2-Input Gate |
| 100107 | Quint Exclusive-OR/NOR |
| 100112 | Quad Driver |
| 100113 | Line Driver |
| 100114 | Line Receiver |
| 100117 | Triple AOI |
| 100118 | 5-Wide AOI |
| 100122 | 9-Bit Buffer Gate |
| 100123 | Hex Bus Driver |
| 100124 | TTL-to-ECL Translator |
| 100125 | ECL-to-TTL Translator |
| 100126 | Back Plane Driver |
| 100131 | Triple D Flip-Flop (2ns) |
| 100136 | Multipurpose Counting Register |
| 100141 | 8-Bit Universal Shift Register |
| 100145 | 16 × 4 Register File |
| 100149 | 1024-Bit, 4 Bits per Word PROM |
| 100149A | 1024-Bit, 4 Bits per Word PROM |
| 100150 | Hex D-Latch |
| 100151 | Hex D Flip-Flop |

| DEVICE TYPE | DESCRIPTION |
|---|---|
| 100155 | Quad Multiplexer/Latch |
| 100158 | Shift Matrix |
| 100160 | Dual 9-Bit Parity |
| 100163 | Dual 8-Input Multiplexer |
| 100164 | 16-Input Multiplexer |
| 100165 | Universal Priority Encoder |
| 100166 | 9-Bit Comparator |
| 100170 | Universal Decoder |
| 100171 | Triple 4-Input Multiplexer |
| 100175 | 100K–10K Translator |
| 100179 | Carry Look-Ahead Generator |
| 100180 | Fast 6-Bit Adder |
| 100181 | 4-Bit ALU Binary/Decimal |
| 100231 | Triple D Flip-Flop (1.8ns) |
| 100255 | TTL–100K Translator/Bidirectional |
| 100310 | 28-Bit ALU (144-Pin) |
| 100330 | 4 Byte MUX (64-Pin) |
| 100331 | 16-to-8 Connection Matrix (64-Pin) |
| 100340 | 4 Byte Comparator w/MUX (64-Pin) |
| 100380 | FIFO RAM Controller (144-Pin) |





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# 10K & 100K ECL Selection Guide

| DEVICE TYPE | DESCRIPTION |
|---|---|
| **OR/NOR Gates** | |
| 10100 | Quad 2-Input NOR Gate |
| 10101 | Quad OR/NOR Gate |
| 10102 | Quad 2-Input NOR Gate |
| 10103 | Quad 2-Input OR Gate |
| 10105 | Triple 2-3-2-Input OR/NOR Gate |
| 10106 | Triple 4-3-3-Input NOR Gate |
| 10109 | Dual 4-5-Input OR/NOR Gate |
| 10110 | Dual 3-Input/3-Output OR Gate (Line Driver) |
| 10111 | Dual 3-Input/3-Output NOR Gate (Line Driver) |
| 10210 | Dual 3-Input/3-Output (High-Speed) OR Gate |
| 10211 | Dual 3-Input/3-Output (High-Speed) NOR Gate |
| 100101 | Triple 5-Input Gate |
| 100102 | Quint 2-Input Gate |
| **Exclusive OR/NOR Gates** | |
| 10107 | Triple 2-Input Exclusive-OR/Exclusive-NOR Gate |
| 10113 | Quad Exclusive-OR Gate with Enable |
| 100107 | Quint Exclusive-OR/NOR |
| **AND, AND/NAND Gates** | |
| 10104 | Quad 2-Input AND Gate |
| 10108 | Dual 3-Input AND/NAND Gate |
| **AND-OR-Invert Combination Gates** | |
| 10117 | Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate |
| 10118 | Dual 2-Wide 3-Input OR-AND Gate |
| 10119 | 4-Wide 4-3-3-3-Input OR-AND Gate |
| 10121 | 4-Wide OR-AND/OR-AND-INVERT Gate |
| 100117 | Triple AOI |
| 100118 | 5-Wide AOI |
| **Buffer Gates** | |
| 10188 | Hex Buffer (Non-Inverting) |
| 10189 | Hex Inverter |
| 100122 | 9-Bit Buffer Gate |
| **Flip-Flops** | |
| 10131 | Dual D-Type Master-Slave Flip-Flop |
| 10135 | Dual J-K Master-Slave Flip-Flop |
| 10176 | Hex D-Type Master-Slave Flip-Flop |
| 10231 | Dual D-Type Master-Slave Flip-Flop (High-Speed) |
| 100131 | Triple D Flip-Flop (2ns) |
| 100151 | Hex D Flip-Flop |
| 100231 | Triple D Flip-Flop (1.8ns) |
| **Latch** | |
| 10130 | Dual D-Type Latch |
| 10133 | Quad Latch with D-Type Inputs and Enable Outputs |
| 10175 | Quint D-Latch w/Common Reset & 2 Wire-OR Common Clock Inputs |
| 100150 | Hex D-Latch |
| **Registers/Shift Registers** | |
| 10141 | 4-Bit Universal Shift Register |
| 10175 | Quint D-Latch w/Common Reset & 2 Wire-OR Common Clock Inputs |
| 100136 | Multipurpose Counting Register |
| 100141 | 8-Bit Universal Shift Register |
| 100145 | 16 × 4 Register File |
| 100158 | Shift Matrix |
| 100150 | Hex D-Latch |
| 100331 | 16-to-8 Connection Matrix (64-Pin) |
| **Counters** | |
| 10136 | Universal Hexadecimal Counter |
| 10137 | Universal Decade Counter |
| 100136 | Multipurpose Counting Register |

| DEVICE TYPE | DESCRIPTION |
|---|---|
| **Multiplexers/Encoders** | |
| 10132 | Dual 2-Input Multiplexer with Clocked D-Type Latches and Common Reset |
| 10134 | Dual 2-Input Multiplexer with Clocked D-Type Latches |
| 10158 | Quad 2-to-1 Multiplexer (Non-Inverting) |
| 10159 | Quad 2-to-1 Multiplexer (Inverting) |
| 10164 | 8-Input Multiplexer with Enable Input |
| 10165 | 8-Input Priority Encoder |
| 10173 | Quad 2-Input Multiplexer with Latched Outputs |
| 10174 | Dual 4-to-1 Multiplexer with Enable |
| 100155 | Quad Multiplexer/Latch |
| 100163 | Dual 8-Input Multiplexer |
| 100164 | 16-Input Multiplexer |
| 100165 | Universal Priority Encoder |
| 100171 | Triple 4-Input Multiplexer |
| 100330 | 4 Byte MUX (64-Pin) |
| 100340 | 4 Byte Comparator w/MUX (64-Pin) |
| **Decoders/Demuliplexer** | |
| 10161 | 3-Bit Decoder with 2 Enable Inputs (1-of-8 LOW) |
| 10162 | 3-Bit Decoder with 2 Enable Inputs (1-of-8 HIGH) |
| 10171 | Dual 2-Bit Decoder (1-of-4 Lines LOW) |
| 10172 | Dual 2-Bit Decoder (1-of-4 Lines HIGH) |
| 100170 | Universal Decoder |
| **Arithmetic Operators** | |
| 10160 | 12-Bit Parity Generator/Checker |
| 10179 | Look-Ahead Carry Block-Arithmetic Functions |
| 10180 | Dual High-Speed Adder/Subtractor |
| 10181 | 4-Bit Logic Unit/Function Generator |
| 100160 | Dual 9-Bit Parity |
| 100166 | 9-Bit Comparator |
| 100179 | Carry Look-Ahead Generator |
| 100180 | Fast 6-Bit Adder |
| 100181 | 4-Bit ALU Binary/Decimal |
| 100310 | 28-Bit ALU (144-Pin) |
| **Bus and Line Drivers** | |
| 10110 | Dual 3-Input/3-Output OR Gate (Line Driver) |
| 10111 | Dual 3-Input/3-Output NOR Gate (Line Driver) |
| 10123 | Triple 4-3-3-Input Bus Driver |
| 10192 | Quad Differential Line Driver |
| 100112 | Quad Driver |
| 100113 | Line Driver |
| 100123 | Hex Bus Driver |
| 100126 | Back Plane Driver |
| **Receivers** | |
| 10114 | Triple Line Receiver |
| 10115 | Quad Line Receiver |
| 10116 | Triple Line Receiver |
| 10216 | Triple Differential OR/NOR Line Receiver (High-Speed) |
| 100114 | Line Receiver |
| **Translators** | |
| 10124 | Quad TTL to ECL Translator |
| 10125 | Quad ECL to TTL Translator |
| 100124 | TTL-to-ECL Translator |
| 100125 | ECL-to-TTL Translator |
| 100175 | 100K–10K Translator |
| 100255 | TTL–100K Translator/Bidirectional |
| **Memories** | |
| 10149 | 1024-Bit, 4 Bits per Word PROM |
| 10149A | 1024-Bit, 4 Bits per Word PROM |
| 100380 | FIFO RAM Controller (144-Pin) |

# 8T/8200/82S00/9300/9600 Availability Guide

| DEVICE | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|
| 8234 | 2-Input, 4-Bit Digital Multiplexer | A |
| 82S41 | Quad Exclusive-OR Gate | A |
| 8242 | Quad Exclusive-NOR Gate | A |
| 82S50 | Binary-to-Octal Decoder | A |
| 82S52 | BCD-to-Decimal Decoder | A |
| 8262 | 8-Bit Parity Generator/Checker | A |
| 82S62 | 8-Bit Parity Generator/Checker | A |
| 8266 | 2-Input, 4-Bit Digital Multiplexer | A |
| 8271 | 4-Bit Shift Register | A |
| 8273 | 10-Bit SIPO Shift Register | A |
| 8274 | 10-Bit PISO Shift Register | A |
| 82S82 | 4-Bit Arithmetic Unit | A |
| 82S83 | 4-Bit BCD Adder | A |
| 8881 | Quad 2-Input NAND (O/C) | A |
| 8890 | Hex Inverter | A |
| 8891 | Hex Inverter | A |
| 9309 | Dual 4-Input Multiplexer | A |
| 9310 | 4-Bit Decade Counter | A |
| 9316 | 4-Bit Binary Counter | A |
| 9322 | Data Selector/Multiplexer | A |
| 9324 | 5-Bit Comparator | A |
| 9334 | 8-Bit Addressable Latch | A |
| 9386 | Quad Exclusive-NOR | A |
| 9602 | Dual Monostable Multivibrator | A |
| 8T09 | Quad Bus Driver (3-State) | A |
| 8T10 | Quad D-Type Bus Latch | A |
| 8T13 | Dual Line Driver | A |
| 8T15 | Dual EIA/MIL Line Receiver | A |
| 8T16 | Dual Communications EIA/MIL Line Receiver | A |
| 8T20 | Bidirectional Monostable Multivibrator | A |

A = Available

| DEVICE | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|
| 8T23 | Dual Line Driver for IBM 360/370 Interface (75123) | A |
| 8T24 | Triple Line Receiver for IBM 360/370 Interface (75124) | A |
| 8T26A | Quad Bus Driver/Receiver | A |
| 8T28 | Quad Bus Driver/Receiver (Non-Inverting) | A |
| 8T34 | Quad Bus Transceiver (DM8834) | A |
| 8T37 | Hex Bus Receiver (DM8837) | A |
| 8T38 | Quad Bus Transceiver (DM8838) | A |
| 8T95 | Hex Buffer | A |
| 8T96 | Hex Inverter | A |
| 8T97 | Hex Buffer | A |
| 8T98 | Hex Inverter | A |
| 8T125 | Octal Transceiver (Inverting) | A |
| 8T126 | Quad Bus Driver/Receiver (Inverting) | A |
| 8T127 | Quad Bus Driver/Receiver (Inverting) | A |
| 8T129 | Quad Bus Driver/Receiver (Non-Inverting) | A |
| 8T245 | Octal Transceiver | A |
| 8T380 | Quad Bus Receiver | A |
| 8T3404 | 6-Bit Latch | A |
| 8TS805 | Octal Transparent Latch | A |
| 8TS806 | Octal Clocked D-Latch | A |
| 8TS807 | Octal Transparent Latch, Inverting Outputs | A |
| 8TS808 | Octal Clocked D-Latch, Inverting Outputs | A |





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# FAST™ Product Availability Guide

| DEVICE | PIN | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|---|
| 74F00 | 14 | Quad 2-Input NAND Gate | A |
| 74F02 | 14 | Quad 2-Input NOR Gate | A |
| 74F04 | 14 | Hex Inverter | A |
| 74F08 | 14 | Quad 2-Input NAND Gate | A |
| 74F10 | 14 | Triple 3-Input NAND Gate | A |
| 74F11 | 14 | Triple 3-Input AND Gate | A |
| 74F13 | 14 | Dual 4-Input Schmitt Trigger | A |
| 74F14 | 14 | Hex Schmitt Trigger | A |
| 74F20 | 14 | Dual 4-Input NAND Gate | A |
| 74F27 | 14 | Triple 3-Input NOR Gate | A |
| 74F30 | 14 | 8-Input NAND Gate | A |
| 74F32 | 14 | Quad 2-Input OR Gate | A |
| 74F37 | 14 | Quad 2-Input NAND Buffer | A |
| 74F38 | 14 | Quad 2-Input NAND Buffer (O/C) | A |
| 74F40 | 14 | Dual 4-Input NAND Buffer | A |
| 74F51 | 14 | Dual 3-Wide 2-Input AND-NOR | A |
| 74F64 | 14 | AND/OR Invert Gate | A |
| 74F74 | 14 | Dual D-Type Flip-Flop | A |
| 74F83 | 16 | 4-Bit Full Adder | P |
| 74F85 | 16 | 4-Bit Magnitude Comparator | A |
| 74F86 | 14 | Quad 2-Input Exclusive-OR Gate | A |
| 74F109 | 16 | Dual J-K Flip-Flop | A |
| 74F112 | 16 | Dual J-K Flip-Flop | A |
| 74F113 | 16 | Dual J-K Flip-Flop | A |
| 74F114 | 16 | Dual J-K Flip-Flop | A |
| 74F125 | 14 | Quad Buffer (3-State) | A |
| 74F126 | 14 | Quad Buffer (3-State) | A |
| 74F132 | 14 | Quad 2-Input Schmitt Trigger | A |
| 74F138 | 16 | 1-of-8 Decoder/Demultiplexer | A |
| 74F139 | 16 | Dual 1-of-4 Decoder/Demultiplexer | A |
| 74F148 | 16 | 8-Bit Priority Encoder | A |
| 74F151 | 16 | 8-Input Multiplexer | A |
| 74F153 | 16 | Dual 4-Input Multiplexer | A |
| 74F154 | 24 | 1-of-16 Decoder/Demultiplexer | Q1 '87 |
| 74F157/A | 16 | Quad 2-Input Multiplexer NINV | A |
| 74F158/A | 16 | Quad 2-Input Multiplexer INV | A |
| 74F160A | 16 | BCD Decade Counter, Asynchronous Reset | A |
| 74F161A | 16 | 4-Bit Binary Counter, Asychronous Reset | A |
| 74F162A | 16 | BCD Decade Counter, Synchronous Reset | A |
| 74F163A | 16 | 4-Bit Binary Counter, Synchronous Reset | A |
| 74F164 | 14 | 8-Bit PISO Shift Register | A |
| 74F166 | 16 | 8-Bit Serial/Parallel-In Serial Out | A |
| 74F168 | 16 | 4-Bit BCD Decade Up/Down Counter | A |
| 74F169 | 16 | 4-Bit Binary Up/Down Counter | A |
| 74F174 | 16 | Hex D Flip-Flop w/Common Master Reset | A |

| DEVICE | PIN | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|---|
| 74F175 | 16 | Quad D Flip-Flop w/Common Master Reset | A |
| 74F181 | 24 | Arithmetic Logic Unit | A |
| 74F182 | 16 | Carry Look-Ahead Generator | A |
| 74F189 | 16 | 64-Bit RAM | Q1 '87 |
| 74F190 | 16 | Up/Down Decade Counter | Q4 '86 |
| 74F191 | 16 | Up/Down Binary Counter | Q4 '86 |
| 74F192 | 16 | Up/Down Decade Counter | Q4 '86 |
| 74F193 | 16 | Up/Down Binary Counter | Q4 '86 |
| 74F194 | 16 | 4-Bit Bidirectional Universal Shift Register | A |
| 74F195 | 16 | 4-Bit Parallel Access Shift Register | A |
| 74F198 | 24 | 8-Bit Bidirectional Universal Shift Register | Q4 '86 |
| 74F199 | 24 | 8-Bit Parallel-Access Shift Register | Q4 '86 |
| 74F240 | 20 | Octal Inverting Bus/Line Driver | A |
| 74F241 | 20 | Octal Bus/Line Driver | A |
| 74F242 | 14 | Quad Bus Transceiver | A |
| 74F243 | 14 | Quad Bus Transceiver | A |
| 74F244 | 20 | Octal Bus/Line Driver | A |
| 74F245 | 20 | Octal Bus Transceiver | A |
| 74F251 | 16 | 8-Input Multiplexer (3-State) | A |
| 74F253 | 16 | Dual 4-Input Multiplexer (3-State) | A |
| 74F256 | 16 | Dual 4-Bit Addressable Latch | A |
| 74F257/A | 16 | Quad 2-Input Multiplexer NINV (3-State) | A |
| 74F258/A | 16 | Quad 2-Input Multiplexer INV (3-State) | A |
| 74F259 | 16 | 8-Bit Addressable Latch | A |
| 74F260 | 14 | Dual 5-Input NOR | A |
| 74F269 | 24 | 8-Bit Up/Down Counter | A |
| 74F273 | 20 | Octal D Flip-Flop | A |
| 74F280A/B | 14 | 9-Bit Parity Generator/Checker | A |
| 74F283 | 16 | 4-Bit Adder | A |
| 74F298 | 16 | Quad 2-Input Multiplexer w/Storage | A |
| 74F299 | 20 | Octal Shift/Storage Register (3-State) | A |
| 74F322 | 20 | Octal Shift/Storage Register (3-State) | Q4 '86 |
| 74F323 | 20 | Octal Shift/Storage Register (3-State) | Q4 '86 |
| 74F350 | 16 | 4-Bit Shifter (3-State) | A |
| 74F352 | 16 | Dual 4-Input Multiplexer (Inverted '153) | A |
| 74F353 | 16 | Dual 4-Input Multiplexer (Inverted '253) | A |
| 74F365 | 16 | Hex Buffer with Common Enable (3-State) | A |
| 74F366 | 16 | Hex Inverter with Common Enable (3-State) | A |
| 74F367 | 16 | Hex Buffer, 4-Bit and 2-Bit (3-State) | A |
| 74F368 | 16 | Hex Inverter, 4-Bit and 2-Bit (3-State) | A |
| 74F373 | 20 | Octal D-Latch (3-State) | A |
| 74F374 | 20 | Octal D Flip-Flop (3-State) | A |
| 74F377 | 20 | Octal D-Type Flip-Flop with Enable | A |
| 74F378 | 16 | Hex D Flip-Flop with Enable | A |
| 74F379 | 16 | Quad D Flip-Flop with Enable | A |

A = Available *no SMD yet.
Q1' 86 = 1st Quarter of 1986 Q2 '86 = 2nd Quarter of 1986 Q3 '86 = 3rd Quarter of 1986



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| DEVICE | PIN | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|---|
| 74F381 | 20 | 4-Bit Arithmetic Logic Unit | A |
| 74F382 | 20 | 4-Bit Arithmetic Logic Unit | A |
| 74F384 | 16 | 8-Bit Serial/Parallel Two's Complement Multiplier | Q1 '87 |
| 74F385 | 20 | Quad Serial Adder/Subtractor | Q4 '86 |
| 74F393 | 14 | Dual Binary Ripple Counter | Q4 '86 |
| 74F395 | 16 | 4-Bit Cascadable S/R (3-State) | A |
| 74F398 | 20 | 4-Bit Flip-Flop, Complementary Outputs | A |
| 74F399 | 16 | 4-Bit Flip-Flop, True Outputs | A |
| 74F412 | 24 | Multi-Mode Buffered Latch | Q4 '86 |
| 74F432 | 24 | Multi-Mode Buffered Latch | Q4 '86 |
| 74F455 | 24 | Octal Buffer w/Parity Generator/Checker | A |
| 74F456 | 24 | Octal Buffer w/Parity Generator/Checker | A |
| 74F521 | 20 | Octal Comparator | A |
| 74F524 | 20 | 8-Bit Register Comparator | Q4 '86 |
| 74F533 | 20 | Inverting Octal D-Latch (3-State) | A |
| 74F534 | 20 | Inverting Octal D Flip-Flop (3-State) | A |
| 74F537 | 20 | 1-of-10 Decoder (3-State) | A |
| 74F538 | 20 | 1-of-8 Decoder (3-State) | Q4 '86 |
| 74F539 | 20 | Dual 1-of-4 Decoder (3-State) | Q4 '86 |
| 74F540 | 20 | Octal Buffer/Line Driver (3-State) | A |
| 74F541 | 20 | Octal Buffer/Line Driver (3-State) | A |
| 74F543 | 24 | Octal Registered Transceiver | Q4 '86 |
| 74F544 | 24 | Octal Registered Transceiver | A |
| 74F545 | 20 | Octal Bus Transceiver | A |
| 74F547 | 20 | Octal Decoder/MUX w/Addressable Latches | Q4 '86 |
| 74F548 | 20 | Octal Decoder/Multiplier w/Acknowledge | Q4 '86 |
| 74F550 | 28 | Octal Registered XCVR w/Flags NINV (3-State) | Q4 '86 |
| 74F551 | 28 | Octal Registered XCVR w/Flags INV (3-State) | Q4 '86 |
| 74F552 | 28 | Octal Registered XCVR w/Flags INV (3-State) | Q4 '86 |
| 74F563 | 20 | Octal D-Latch, Broadside Pinout 'F533 | Q4 '86 |
| 74F564 | 20 | Octal D Flip-Flop, Broadside Pinout 'F534 | Q4 '86 |
| 74F568 | 20 | 4-Bit BCD Decade Up/Down Counter (3-State) | Q4 '86 |
| 74F569 | 20 | 4-Bit Binary Up/Down Counter (3-State) | Q4 '86 |
| 74F573 | 20 | Octal D-Latch, Broadside Pinout 'F373 | Q4 '86 |
| 74F574 | 20 | Octal D Flip-Flop, Broadside Pinout 'F374 | Q4 '86 |
| 74F579 | 20 | 8-Bit Up/Down Counter, Common I/O | A |
| 74F582 | 24 | 4-Bit BCD ALU | Q4 '86 |
| 74F583 | 16 | 4-Bit BCD Adder | Q4 '86 |
| 74F588 | 20 | GPIB Compatible Octal Transceiver | A |
| 74F595 | 16 | 8-Bit Shift Register w/Output Latch | Q4 '86 |

| DEVICE | PIN | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|---|
| 74F597 | 16 | 8-Bit Shift Register w/Input Latch | Q4 '86 |
| 74F598 | 16 | 8-Bit Shift Register w/Input Latch | Q4 '86 |
| 74F604 | 28 | Dual 8-Bit Latch (3-State) | A |
| 74F605 | 28 | Dual 8-Bit Latch (O/C) | A |
| 74F620 | 20 | Octal Bus Transceiver (3-State) | A |
| 74F621 | 20 | Octal Bus Transceiver (O/C) | A |
| 74F622 | 20 | Octal Bus Transceiver (O/C) | A |
| 74F623 | 20 | Octal Bus Transceiver (3-State) | A |
| 74F640 | 20 | Octal Bus Transceiver, Inverting (3-State) | A |
| 74F641 | 20 | Octal Bus Transceiver (O/C) | A |
| 74F642 | 20 | Octal Bus Transceiver, Inverting (O/C) | A |
| 74F646 | 24 | Octal Bus XCVR/Register INV (3-State) | A |
| 74F647 | 24 | Octal Bus XCVR/Register NINV (O/C) | A |
| 74F648 | 24 | Octal Bus XCVR/Register INV (3-State) | A |
| 74F649 | 24 | Octal Bus XCVR/Register NINV (O/C) | A |
| 74F651 | 24 | Octal XCVR/Register INV (3-State) | A |
| 74F652 | 24 | Octal XCVR/Register NINV (3-State) | A |
| 74F653 | 24 | Octal XCVR/Register INV (O/C) | A |
| 74F654 | 24 | Octal XCVR/Register NINV (O/C) | A |
| 74F655A | 24 | Octal Inverting Buffer w/Parity Generator/Checker | A |
| 74F656A | 24 | Octal Buffer w/Parity Generator/Checker | A |
| 74F657 | 24 | Octal Bus Transceiver w/Parity Generator/Checker | A |
| 74F670 | 16 | 4 × 4 Register File | Q4 '86 |
| 74F673A | 24 | 16-Bit Serial-In/Parallel-Out Shift Register | Q4 '86 |
| 74F674 | 24 | 16-Bit Parallel-In/Serial-Out Shift Register | Q4 '86 |
| 74F675 | 24 | 16-Bit SIPO Shift Register w/SO Capability | Q4 '86 |
| 74F676 | 24 | 16-Bit SIPO Shift Register w/SO Capability | Q4 '86 |
| 74F711 | 20 | Quint 2-Input Multiplexer | Q1 '87 |
| 74F712 | 24 | Quint 3-Input Multiplexer | Q1 '87 |
| 74F723 | 24 | Quad 3-Input Multiplexer | Q1 '87 |
| 74F725 | 24 | Quad 3-Input Multiplexer | Q1 '87 |
| 74F732 | 20 | Quad Data Multiplexer | Q1 '87 |
| 74F733 | 20 | Quad Data Multiplexer | Q1 '87 |
| 74F764 | 40 | Dual Port RAM Controller with Latch | A |
| 74F765 | 40 | Dual Port RAM Controller without Latch | A |
| 74F779 | 16 | 8-Bit Counter w/Common I/O (3-State) | A |
| 74F784 | 20 | 8-Bit Serial Multiplier and Adder/Subtractor | Q4 '86 |
| 74F804 | 20 | Hex 2-Input NAND Driver | Q4 '86 |
| 74F805 | 20 | Hex 2-Input NOR Driver | Q4 '86 |
| 74F808 | 20 | Hex 2-Input AND Driver | Q4 '86 |

A = Available *no SMD yet.
Q1' 86 = 1st Quarter of 1986 Q2 '86 = 2nd Quarter of 1986 Q3 '86 = 3rd Quarter of 1986





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# FAST™ Product Availability Guide

| DEVICE | PIN | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|---|
| 74F821 | 24 | 10-Bit Register, Non-Inverting (3-State) | Q1 '87 |
| 74F822 | 24 | 10-Bit Register, Inverting (3-State) | Q1 '87 |
| 74F823 | 24 | 9-Bit Register, Non-Inverting (3-State) | Q1 '87 |
| 74F824 | 24 | 9-Bit Register, Inverting (3-State) | Q1 '87 |
| 74F825 | 24 | 8-Bit Register, Non-Inverting (3-State) | Q1 '87 |
| 74F826 | 24 | 8-Bit Register, Inverting (3-State) | Q1 '87 |
| 74F827 | 24 | 10-Bit Buffer, Non-Inverting (3-State) | A |
| 74F828 | 24 | 10-Bit Buffer, Inverting (3-State) | A |
| 74F832 | 20 | Hex 2-Input OR Driver | Q1 '87 |
| 74F841 | 24 | 10-Bit Latch, Non-Inverting (3-State) | Q4 '86 |
| 74F842 | 24 | 10-Bit Latch, Inverting (3-State) | Q4 '86 |
| 74F843 | 24 | 9-Bit Latch, Non-Inverting (3-State) | Q4 '86 |
| 74F844 | 24 | 9-Bit Latch, Inverting (3-State) | Q4 '86 |
| 74F845 | 24 | 8-Bit Latch, Non-Inverting (3-State) | Q4 '86 |
| 74F846 | 24 | 8-Bit Latch, Inverting (3-State) | Q4 '86 |
| 74F861 | 24 | 10-Bit Transceiver, Non-Inverting (3-State) | Q4 '86 |
| 74F862 | 24 | 10-Bit Transceiver, Inverting (3-State) | Q4 '86 |
| 74F863 | 24 | 9-Bit Transceiver, Non-Inverting (3-State) | Q4 '86 |
| 74F864 | 24 | 9-Bit Transceiver, Inverting (3-State) | Q4 '86 |
| 74F881 | 24 | ALU/Function Generator | A |
| 74F882 | 24 | 32-Bit Look-Ahead Carry Generator | A |
| 74F1240 | 20 | Octal Buffer, Light Load 'F240 | A |
| 74F1241 | 20 | Octal Buffer, Light Load 'F241 | A |
| 74F1242 | 14 | Quad Transceiver, Light Load 'F242 | A |
| 74F1243 | 14 | Quad Transceiver, Light Load 'F243 | A |

| DEVICE | PIN | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|---|
| 74F1244 | 20 | Octal Driver, Light Load 'F244 | A |
| 74F1245 | 20 | Octal Bus Transceiver, Light Load 'F245 | A |
| 74F1764 | 48 | 1MBit DRAM Dual Ported Controller w/Latch | P |
| 74F1765 | 48 | 1MBit DRAM Dual Ported Controller w/o Latch | P |
| 74F2952 | 24 | Octal Transceiver, Non-Inverting (3-State) | P |
| 74F2953 | 24 | Octal Transceiver, Inverting (3-State) | P |
| 74F3037 | 16 | 30Ω Transmission Line Driver (Quad 2-Input NAND) | A |
| 74F3038 | 16 | 30Ω Transmission Line Driver (Quad 2-Input NAND, O/C) | A |
| 74F3040 | 16 | 30Ω Transmission Line Driver (Dual 4-Input NAND) | A |
| 74F30240 | 24 | Octal Inverting 30Ω Transmission Line Driver (O/C) | A |
| 74F30244 | 24 | Octal 30Ω Transmission Line/Backplane Driver | Q4 '86 |
| 74F30245 | 24 | Octal Transceiver 30Ω Transmission Line Driver (O/C) | A |
| 74F30640 | 24 | Octal Transceiver 30Ω Transmission Line Driver Inverting (O/C) | A |

A = Available *no SMD yet.
Q1' 86 = 1st Quarter of 1986 Q2 '86 = 2nd Quarter of 1986 Q3 '86 = 3rd Quarter of 1986

**FAST ORDERING INFORMATION**

| PACKAGES | COMMERCIAL RANGES $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74F--N |
| Plastic SO[1] | N74F--D |

**NOTE:**
1. SO package is surface-mounted micro-miniature DIP.

# FAST™ Family Characteristics

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | | 74F | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | | −0.5 to $V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in LOW output state | Standard outputs | 40 | mA |
| | | 3-State outputs | 48 | mA |
| | | Buffer outputs | 128 | mA |
| $T_A$ | Operating free-air temperature range | | 0 to 70 | °C |

**NOTE:**

1. For 3-State outputs, $V_{OUT} = -0.5\,V$ to $5.5\,V$ with $V_{CC} = 0\,V$.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | 74F | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | −18 | mA |
| $V_{OH}$ | HIGH-level output voltage | Open collector | | | 4.5 | V |
| $I_{OH}$ | HIGH-level output current | Standard outputs | | | −1 | mA |
| | | 3-State outputs | | | −3 | mA |
| | | Buffer outputs | | | −15 | mA |
| $I_{OL}$ | LOW-level output current | Standard outputs | | | 20 | mA |
| | | 3-State outputs | | | 24 | mA |
| | | Buffer outputs | | | 64 | mA |
| $T_A$ | Operating free-air temperature range | | 0 | | 70 | °C |





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# FAST™ Family Characteristics

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | | | LIMITS[2] Min | LIMITS[2] Typ[3] | LIMITS[2] Max | UNITS | $V_{CC}$[4] | CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | | V | | Recognized as a HIGH Signal over Recommended $V_{CC}$ and $T_A$ Range |
| $V_{IL}$ | Input LOW Voltage | | | | | 0.8 | V | | Recognized as a LOW Signal over Recommended $V_{CC}$ and $T_A$ Range |
| $V_{IK}$ ($V_{DC}$) | Input Clamp Diode Voltage | | | | | −1.2 | V | Min | $I_{IN} = -18$mA |
| $V_{OH}$ | Output HIGH Voltage | Std[5] | ±10% | 2.5 | 3.4 | | V | Min | $I_{OH} = -1$mA |
| | | | ±5% | 2.7 | 3.4 | | V | Min | $I_{OH} = -1$mA |
| | | 3-State | ±10% | 2.4 | 3.3 | | V | Min | $I_{OH} = -3$mA |
| | | | ±5% | 2.7 | 3.3 | | V | Min | $I_{OH} = -3$mA |
| | | Buffers | ±10% | 2.0 | 3.1 | | V | Min | $I_{OH} = -15$mA |
| | | | ±5% | 2.0 | 3.1 | | V | Min | $I_{OH} = -15$mA |
| $V_{OL}$ | Output LOW Voltage | Std[5] | ±10% | | 0.35 | 0.5 | V | Min | $I_{OL} = 20$mA |
| | | | ±5% | | 0.35 | 0.5 | V | Min | $I_{OL} = 20$mA |
| | | 3-State | ±10% | | 0.35 | 0.5 | V | Min | $I_{OL} = 24$mA |
| | | | ±5% | | 0.35 | 0.5 | V | Min | $I_{OL} = 24$mA |
| | | Buffers | ±10% | | 0.35 | 0.5 | V | Min | $I_{OL} = 48$mA |
| | | | ±5% | | 0.40 | 0.55 | V | Min | $I_{OL} = 84$mA |
| $I_I$ | Input HIGH Current Breakdown Test | Diode inputs[6] | | | | 100 | μA | Max | $V_{IN} = 7.0$V |
| | | NPN inputs | | | | 100 | μA | 0.0V | $V_{IN} = 7.0$V |
| | | Transceiver I/O pins | | | | 1.0 | mA | 5.5V | $V_{IN} = 5.5$V |
| $I_{IH}$ | Input HIGH Current | | | | | n(28) | μA | Max | $V_{IH} = 2.7$V (20μA × n HIGH U.L.) |
| $I_{IL}$ | Input LOW Current | Diode inputs[6] | | | | n(−600) | μA | Max | $V_{IL} = 0.5$V (−600μA × n LOW U.L.) |
| | | NPN inputs | | | | n(−20) | μA | Max | $V_{IL} = 0.5$V (−20μA × n LOW U.L.) |
| $I_{IH}$ + $I_{OZH}$ | Input HIGH Current (I/O pins) | | | | | n(20) +50 | μA | Max | $V_{IH} = 2.7$V (20μA × n HIGH U.L.) |
| $I_{IL}$ + $I_{OZL}$ | Input LOW Current (I/O pins) | Diode inputs[6] | | | | n(−0.6) | μA | Max | $V_{IL} = 0.5$V (−0.5μA × n LOW U.L.) |
| | | NPN inputs | | | | n(−20) +50 | μA | Max | $V_{IL} = 0.5$V (−20μA × n LOW U.L.) |
| $I_{OZH}$ | 3-State OFF Current HIGH | | | | | 50 | μA | Max | $V_{OUT} = 2.7$V |
| $I_{OZL}$ | 3-State OFF Current LOW | | | | | −50 | μA | Max | $V_{OUT} = 0.5$V |
| $I_{OH}$ | Open-Collector Output Leakage | | | | | 250 | μA | Min | $V_{OH} = 4.5$V |
| $I_{OS}$[7] | Output Short-Circuit Current | Std.[5] 3-State | | −80 | | −158 | μA | Max | $V_{OUT} = 0$V |
| | | Buffer Driver | | −100 | | −225 | μA | Max | $V_{OUT} = 0$V |

**NOTE:**

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to $T_A = +25°C$ and $V_{CC} = +5.0$V.
4. Min and Max refer to the values listed in the data sheet table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
6. On certain part types, Signetics uses a high impedance NPN base input structure to enhance device performance. Parts which have this structure are indicated in the FAST Data Manual. NPN inputs are tested with $V_{CC} = 0$V and 7.0V at the input. It is necessary to turn $V_{CC}$ off for the NPN input test to measure leakage. Otherwise, the current source is on and the leakage is undetectable.
7. For testing $I_{OS}$, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operation values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{OS}$ test should be performed last.

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Signetics

# FAST 74F455, 74F456
## Buffers/Drivers

**'F455 Octal Buffer/Line Driver with Parity, Inverting (3-State)**
**'F456 Octal Buffer/Line Driver with Parity, Inverting (3-State)**
***Product Specification***

**Logic Products**

### FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **'F455 combines 'F240 and 'F280A functions in one package**
- **'F456 combines 'F241 and 'F280A functions in one package**
- **'F455A and 'F456A are center pin versions of the 'F655A and 'F656A respectively**
- **'F455 Inverting**
  **'F456 Non-inverting**
- **3-State outputs sink 64mA and source 15mA**
- **24-pin plastic slim DIP (300 mil) package**
- **Inputs on one side and outputs on the other side simply PC board layout**

### DESCRIPTION

The 'F455 and 'F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F455 | 3.5ns | 70mA |
| 74F456 | 4.5ns | 70mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F455N, N74F456N |
| Plastic SOL-24 | N74F455D, N74F456D |

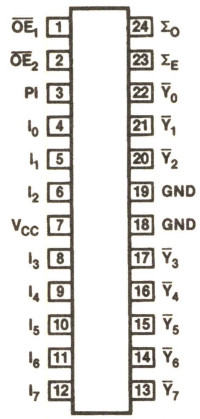
**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $I_n$ | Data inputs | 1.0/0.033 | 20μA/20μA |
| PI | Parity input | 1.0/0.033 | 20μA/20μA |
| $\overline{OE}_1$, $\overline{OE}_2$ | 3-State output enable inputs (active LOW) | 1.0/0.033 | 20μA/20μA |
| $\overline{Y}_n$ | Data outputs ('F455) | 750/106.7 | 15mA/64mA |
| $Y_n$ | Data outputs ('F456) | 750/106.7 | 15mA/64mA |
| $\Sigma_E$, $\Sigma_O$ | Parity outputs | 750/106.7 | 15mA/64mA |

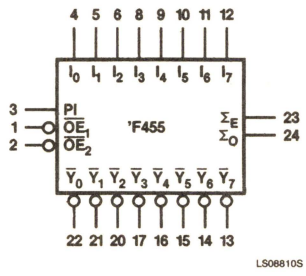
### PIN CONFIGURATION

'F455




### LOGIC SYMBOL

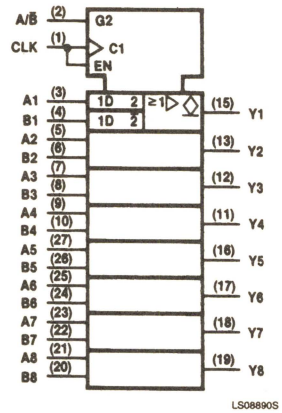
'F455




$V_{CC}$ = Pin 16
GND = Pin 18 and 19

### LOGIC SYMBOL (IEEE/IEC)

'F455

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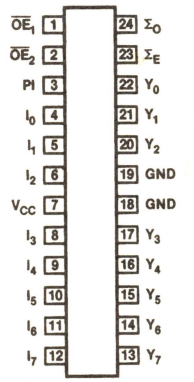
# Buffers/Drivers

# FAST 74F455, 74F456

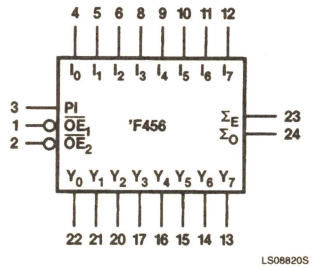
## PIN CONFIGURATION

'F456




## LOGIC SYMBOL

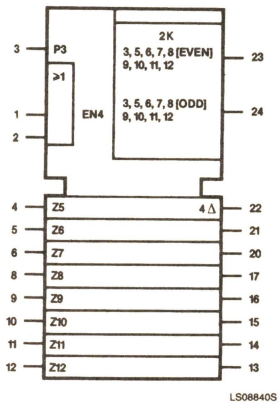
'F456




$V_{CC}$ = Pin 16
GND = Pin 18 and 19

## LOGIC SYMBOL (IEEE/IEC)

'F456




## FUNCTION TABLES

| INPUTS | | | DATA OUTPUTS | |
|---|---|---|---|---|
| $\overline{OE}_1$ | $\overline{OE}_2$ | $I_n$ | 'F455 | 'F456 |
| L | L | L | H | L |
| L | L | H | L | H |
| H | X | X | (Z) | (Z) |
| X | H | X | (Z) | (Z) |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance level

| INPUTS | PARITY OUTPUTS | |
|---|---|---|
| Number of inputs HIGH (PI, $I_0 - I_7$) | $\Sigma_E$ | $\Sigma_O$ |
| Even – 0, 2, 4, 6, 8 | H | L |
| Odd – 1, 3, 5, 7, 9 | L | H |
| Any $\overline{OE}$ = HIGH | (Z) | (Z) |

Signetics

# FAST 74F646, 74F648
## Transceivers/Registers

**'F646 — Octal Transceiver/Register, Non-Inverting (3-State)**
**'F648 — Octal Transceiver/Register, Inverting (3-State)**
***Preliminary Specification***

**Logic Products**

### FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-State outputs**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F646 | 7.5ns | 115mA |
| 74F648 | 7.5ns | 115mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F646N, N74F648N |
| Plastic SOL-24 | N74F646D, N74F648D |

**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### DESCRIPTION

These devices consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable $\overline{G}$ and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (S) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Enable $\overline{G}$ is active (LOW). In the isolation mode (Enable G, HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed with the 'F646 and 'F648.

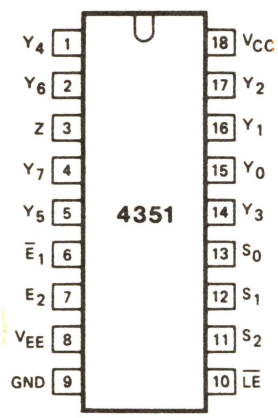
### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $A_1 - A_8$, $B_1 - B_8$ | A and B inputs | 1/0.033 | 20μA/20μA |
| CPAB, CPBA | Clock pulse input | 1/0.033 | 20μA/20μA |
| SAB, SBA | Transmit/receive input | 1/0.033 | 20μA/20μA |
| DIR, $\overline{G}$ | Output enable inputs | 1/0.033 | 20μA/20μA |
| $A_1 - A_8$, $B_1 - B_8$ | A and B outputs | 150/33.3 | 3mA/20mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

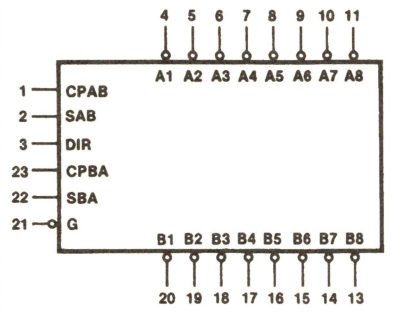
### PIN CONFIGURATION

'F646




### LOGIC SYMBOL

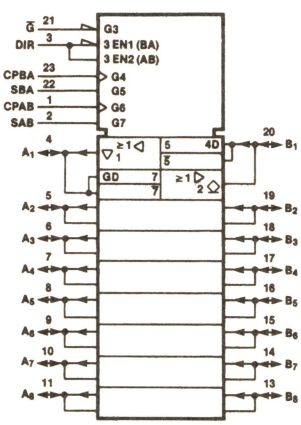
'F646




$V_{CC}$ = Pin 24
GND = Pin 12

### LOGIC SYMBOL (IEEE/IEC)

'F646





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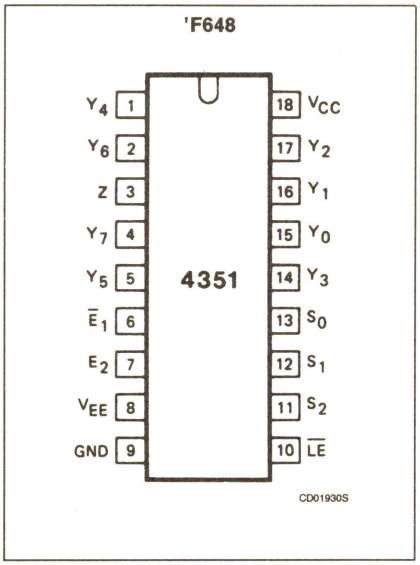
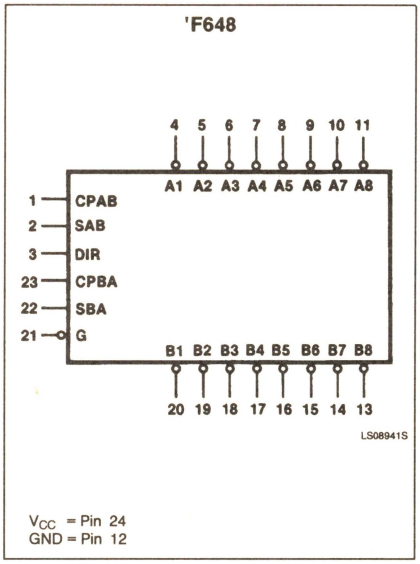
# Transceivers/Registers

# FAST 74F646, 74F648

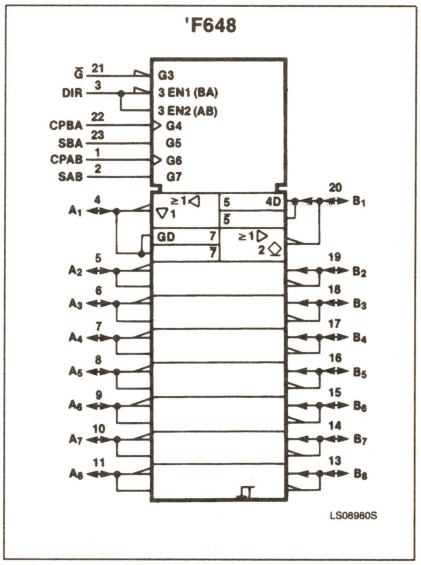
## PIN CONFIGURATION




## LOGIC SYMBOL




## LOGIC SYMBOL (IEEE/IEC)



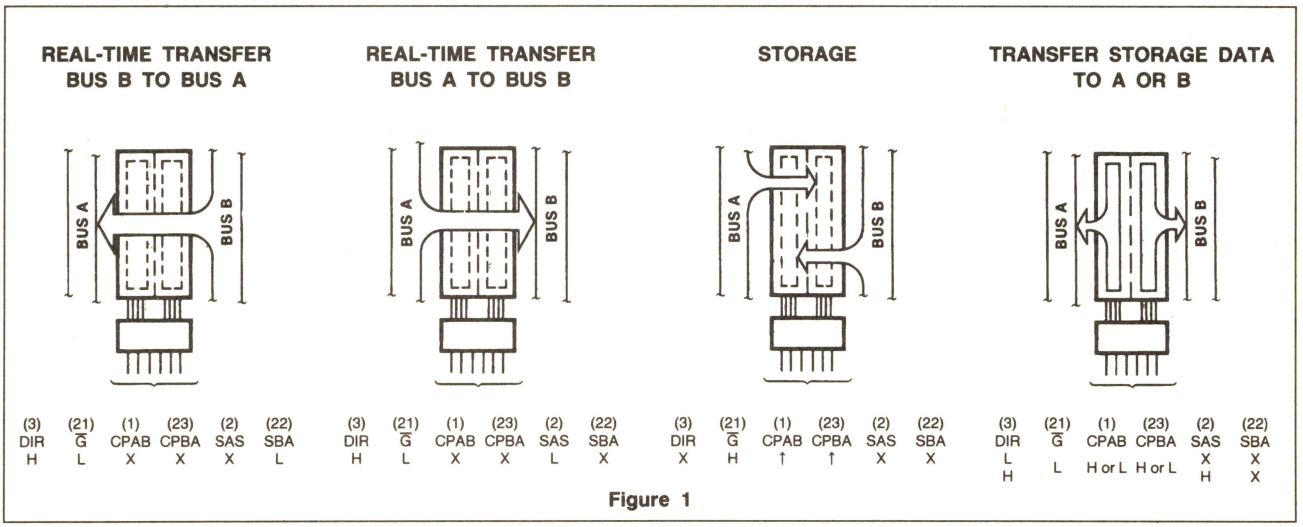




Figure 1

## FUNCTION TABLE

| INPUTS | | | | | | DATA I/O* | | OPERATION OR FUNCTION | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{G}$ | DIR | CPAB | CPBA | SAB | SBA | $A_1 - A_8$ | $B_1 - B_8$ | 'F646, 'F647 | 'F648, 'F649 |
| H<br>H | X<br>X | H or L<br>↑ | H or L<br>↑ | X<br>X | X<br>X | Input | Input | Isolation<br>Store A and B data | Isolation<br>Store A and B data |
| L<br>L | L<br>L | X<br>X | X<br>X | X<br>X | L<br>H | Output | Input | Real time B data to A bus<br>Stored B data to A bus | Real time $\overline{B}$ data to A bus<br>Stored $\overline{B}$ data to A bus |
| L<br>L | H<br>H | X<br>H or L | X<br>X | L<br>H | X<br>X | Input | Output | Real time A data to B bus<br>Stored A data to B bus | Real time $\overline{A}$ data to B bus<br>Stored $\overline{A}$ data to B bus |

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

H = high level  X = irrelevant
L = low level  ↑ = low-to-high level transition

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# FAST 74F655A, 74F656A
## Buffers/Drivers

**Octal Buffer/Line Driver with Parity**
**('F655A — Inverting 3-State)**
**('F656A — Non-Inverting 3-State)**
***Product Specification***

### FEATURES

- **Significantly improved AC performance over 'F655 and 'F656**
- **High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **Ideal in applications where high output drive and light bus loading are required ($I_{IL}$ is 20μA vs FAST std of 600μA)**
- **'F655A combines 'F240 and 'F280 functions in one package**
- **'F656A combines 'F244 and 'F280A functions in one package**
- **'F655A Inverting**
  **'F656A Non-inverting**
- **3-State outputs sink 64mA**
- **Inputs source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Inputs on one side and outputs on the other side simplify PC board layout**
- **Combined functions reduce part count and enhance system performance**

### DESCRIPTION

The 'F655A and 'F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F655A | 6.5ns | 64mA |
| 74F656A | 6.5ns | 64mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F655AN, N74F656AN |
| Plastic SOL-24 | N74F655AD, N74F656AD |

**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $I_n$ | Data inputs | 1.0/0.033 | 20μA/20μA |
| PI | Parity input | 1.0/0.033 | 20μA/20μA |
| $\overline{OE}_1$, $\overline{OE}_2$ $\overline{OE}_3$ | 3-State output enable inputs (active LOW) | 1.0/0.033 | 20μA/20μA |
| $\overline{Y}_n$ | Data outputs ('F655A) | 750/106.7 | 15mA/64mA |
| $Y_n$ | Data outputs ('F656A) | 750/106.7 | 15mA/64mA |
| $\Sigma_E$, $\Sigma_0$ | Parity outputs | 750/106.7 | 15mA/64mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.



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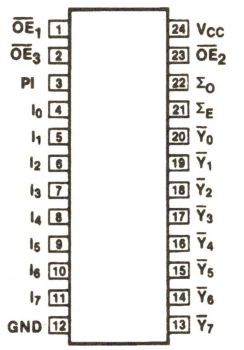
# Buffers/Drivers

# FAST 74F655A, 74F656A

## PIN CONFIGURATION

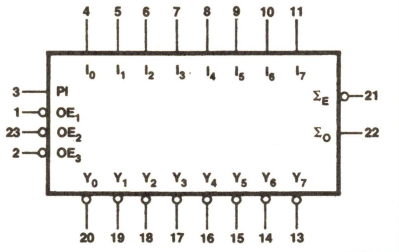
'F655A




CD08061S

## LOGIC SYMBOL

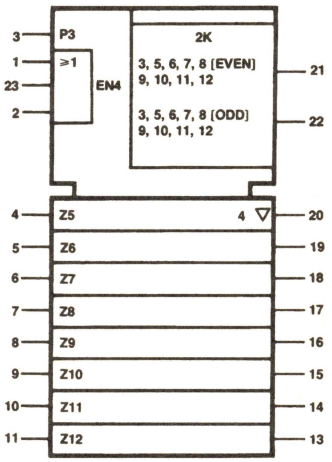
'F655A




LS10340S

## LOGIC SYMBOL (IEEE/IEC)

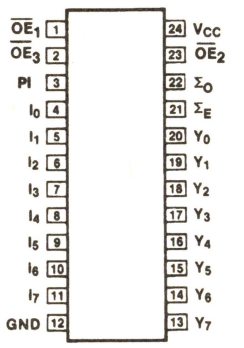
'F655A




LS10310S

## PIN CONFIGURATION

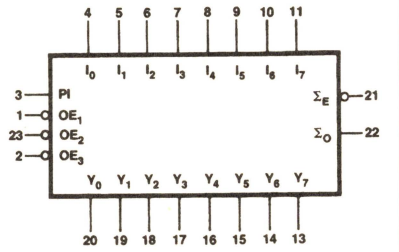
'F656A




CD08071S

## LOGIC SYMBOL

'F656A




LS10330S

## LOGIC SYMBOL (IEEE/IEC)

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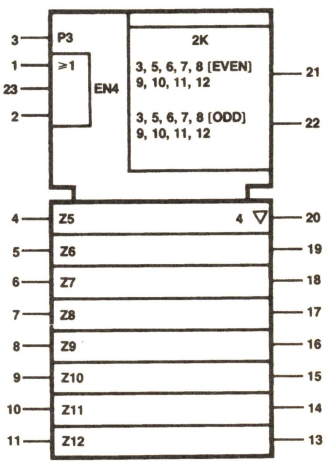


LS10320S

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# FAST 74F657
## Transceiver

**Octal Bidirectional Transceiver With 8-Bit Parity Generator/Checker (3-State Outputs)**
***Product Specification***

**Logic Products**

### FEATURES

- **High-impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **Ideal in applications where high output drive and light bus loading are required ($I_{IL}$ is 20μA Vs FAST std of 600μA)**
- **24-pin plastic slim dip (300-mil) package**
- **Combines 'F245 and 'F280A functions in one package**
- **3-State outputs**
- **Outputs sink 64mA**
- **15mA source current**
- **Input diodes for termination effects**

### DESCRIPTION

The 'F657 contains eight non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 20mA at the A ports and 64mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F657 | 5ns | 120mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F657N |
| Plastic SOL-24 | N74F657D |

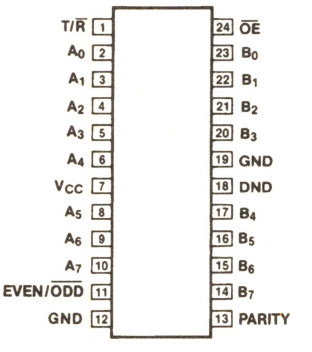
**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

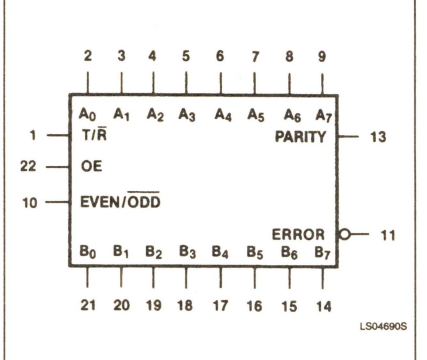
| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $A_0 - A_7$ | A ports 3-State inputs | 5.0/0.167 | 100μA/100μA |
| $B_0 - B_7$ | B ports 3-State inputs | 3.5/0.117 | 70μA/70μA |
| PARITY | Parity input | 3.5/0.117 | 70μA/70μA |
| T/$\overline{R}$ | Transmit/receive input | 2.0/0.066 | 40μA/40μA |
| EVEN/$\overline{ODD}$ | EVEN/ODD input | 1.0/0.033 | 20μA/20μA |
| $\overline{OE}$ | Output enable input (active LOW) | 2.0/0.066 | 40μA/40μA |
| $A_0 - A_7$ | A ports 3-State outputs | 150/40 | 3mA/24mA |
| $B_0 - B_7$ | B ports 3-State outputs | 750/106.7 | 15mA/64mA |
| PARITY | Parity output | 150/40 | 3mA/24mA |
| $\overline{ERROR}$ | Error output | 150/40 | 3mA/24mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

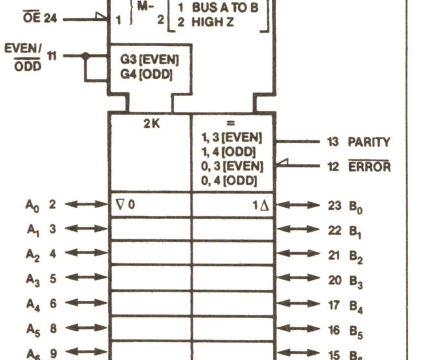
### PIN CONFIGURATION




### LOGIC SYMBOL




### LOGIC SYMBOL (IEEE/IEC)

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# FAST 74F1240, F1241
## Buffers

**'F1240 Octal Inverter Buffer (3-State)**
**'F1241 Octal Buffer (3-State)**
***Product Specification***

**Logic Products**

### FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Low power, light bus loading**
- **Functional pin for pin equivalent of 'F240 and 'F241**
- **1/30th the bus loading of 'F240 or 'F241**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

### DESCRIPTION

The 'F1240 and 'F1241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_n$, each controlling four of the 3-State outputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F1240 | 3.5ns | 40mA |
| 74F1241 | 4.5ns | 46mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F1240N, N74F1241N |
| Plastic SOL-20 | N74F1240D, N74F1241D |

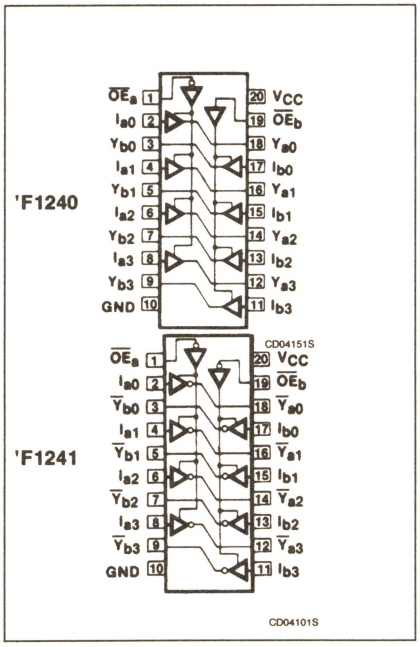
**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

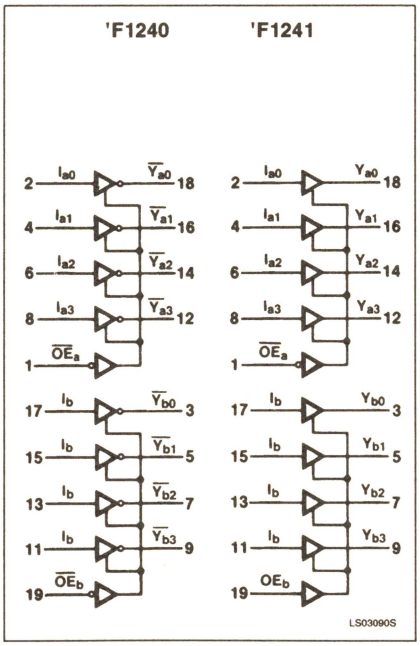
| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $\overline{OE}_a$, $\overline{OE}_b$ | 3-State output enable input (active LOW) | 1.0/0.033 | 20μA/20μA |
| $OE_b$ | 3-State output enable input (active HIGH) | 1.0/0.033 | 20μA/20μA |
| $I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$ | Data inputs | 1.0/0.033 | 20μA/20μA |
| $\overline{Y}_{a0} - \overline{Y}_{a3}$, $\overline{Y}_{b0} - \overline{Y}_{b3}$ 'F1240 | Data outputs | 750/106.7 | 15mA/64mA |
| $Y_{a0} - Y_{a3}$, $Y_{b0} - Y_{b3}$ 'F1241 | Data outputs | 750/106.7 | 15mA/64mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

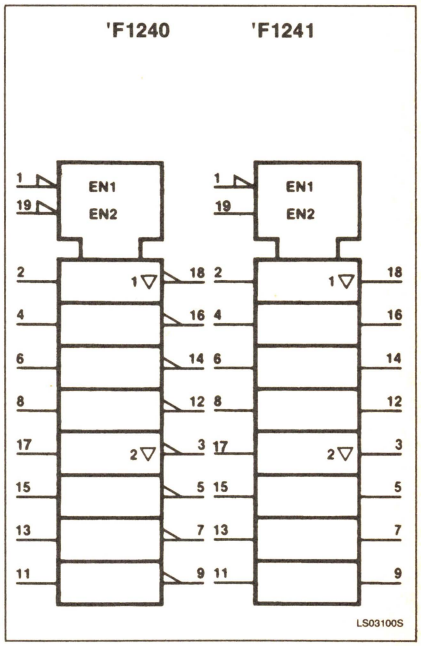
### PIN CONFIGURATION




### LOGIC SYMBOL




### LOGIC SYMBOL (IEEE/IEC)

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### FUNCTION TABLE for 'F1240

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{OE}_a$ | $I_a$ | $\overline{OE}_b$ | $I_b$ | $\overline{Y}_{an}$ | $\overline{Y}_{bn}$ |
| L | L | L | L | H | H |
| L | H | L | H | L | L |
| H | X | H | X | (Z) | (Z) |

### FUNCTION TABLE for 'F1241

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{OE}_a$ | $I_a$ | $OE_b$ | $I_b$ | $Y_{an}$ | $Y_{bn}$ |
| L | L | H | L | L | L |
| L | H | H | H | H | H |
| H | X | L | X | (Z) | (Z) |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

### ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| | PARAMETER | 74F | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | −0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in LOW output state | 128 | mA |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

### RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74F | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −15 | mA |
| $I_{OL}$ | LOW-level output current | | | 64 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |





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# FAST 74F166
## Shift Register

**8-Bit Serial/Parallel-In, Serial Out Shift Register**
***Product Specification***

**Logic Products**

### FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Synchronous parallel to serial applications**
- **Synchronous serial data input for easy expansion**
- **Clock enable for "do nothing" mode**
- **Asynchronous Master Reset**
- **Exandable to 16-bits in 8-bit increments**

### DESCRIPTION

The 166 is a high speed 8-bit shift register that has fully synchronous serial parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one set-up time before the LOW-to-HIGH clock transistion, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position $Q_0$ from Serial Data Input ($D_s$), and the remaining bits are shifted one place to the right ($Q_0 - Q_1 - Q_2$, etc.), with each positive-going clock transition.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F166 | 175MHz | 41mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F166N |
| Plastic SO-16 | N74F166D |

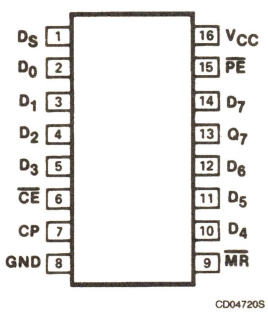
**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

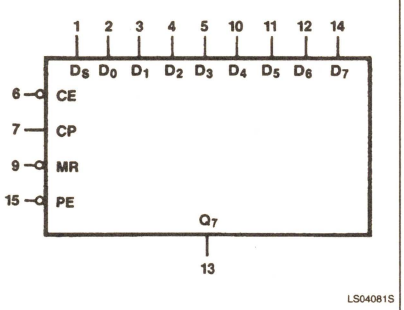
| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $\overline{PE}$ | Parallel enable input | 1/0.033 | 20μA/20μA |
| $\overline{CE}$ | Clock enable input | 1/0.033 | 20μA/20μA |
| CP | Clock input (active rising edge) | 1/0.033 | 20μA/20μA |
| $D_s$ | Serial data input | 2/0.066 | 40μA/40μA |
| $D_0 - D_7$ | Parallel data input | 1/0.033 | 20μA/20μA |
| $\overline{MR}$ | Master Reset input (active LOW) | 2/0.066 | 40μA/40μA |
| $Q_7$ | Output | 50/33 | 1.0mA/20mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

### PIN CONFIGURATION

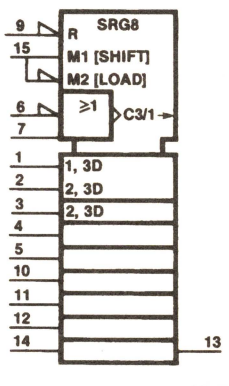



### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC SYMBOL (IEEE/IEC)

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# FAST 74F269
## 8-Bit Counter

**8-Bit Bidirectional Binary Counter**
***Product Specification***

**Logic Products**

### FEATURES
- **Synchronous counting and loading**
- **Built-in lookahead carry capability**
- **Count frequency 115MHz typ**
- **Supply current 95mA typ**

### DESCRIPTION
The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F269 | 115MHz | 95mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F269N |
| Plastic SOL-24 | N74F269D |

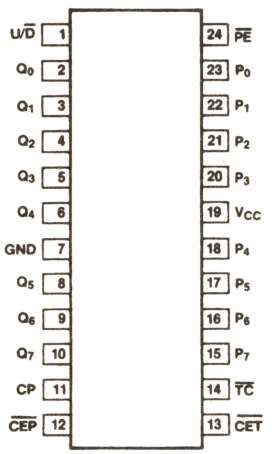
**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

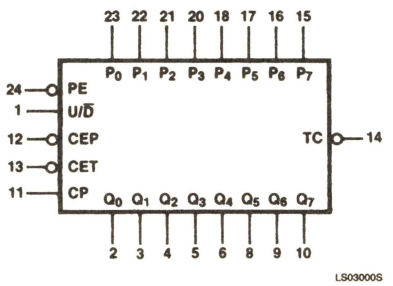
| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $P_0 - P_7$ | Parallel data inputs | 1.0/1.0 | 20μA/0.6mA |
| $\overline{PE}$ | Parallel enable input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| U/$\overline{D}$ | Up-Down count control input | 1.0/1.0 | 20μA/0.6mA |
| $\overline{CEP}$ | Count enable parallel input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{CET}$ | Count enable trickle input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| CP | Clock input | 1.0/1.0 | 20μA/0.6mA |
| $\overline{TC}$ | Terminal count output (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $Q_0 - Q_7$ | Flip-flop outputs | 50/33 | 1mA/20mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

### PIN CONFIGURATION

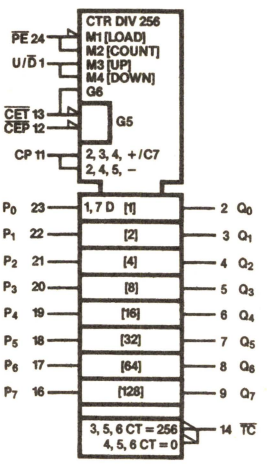



### LOGIC SYMBOL




$V_{CC}$ = Pin 19
GND = Pin 7

### LOGIC SYMBOL (IEEE/IEC)

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# FAST 74F579
## Counter

**8-Bit Bidirectional Binary Counter (3-State)**
***Product Specification***

**Logic Products**

## FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Built-in cascading carry capability**
- **Count frequency 115MHz typ**
- **Supply current 100mA typ**
- **Fully synchronous operation**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous Reset**
- **Center power pins to reduce effects of package inductance**
- **See 'F269 for 24-pin separate I/O port version**
- **See 'F779 for 16-pin version**

## DESCRIPTION

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look–ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock.

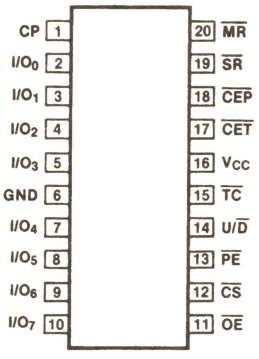
| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F579 | 115MHz | 100mA |

## ORDERING CODE

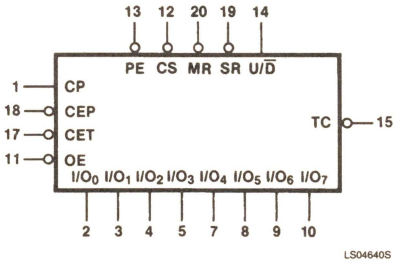
| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F579N |
| Plastic SOL-20 | N74F579D |

**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## PIN CONFIGURATION

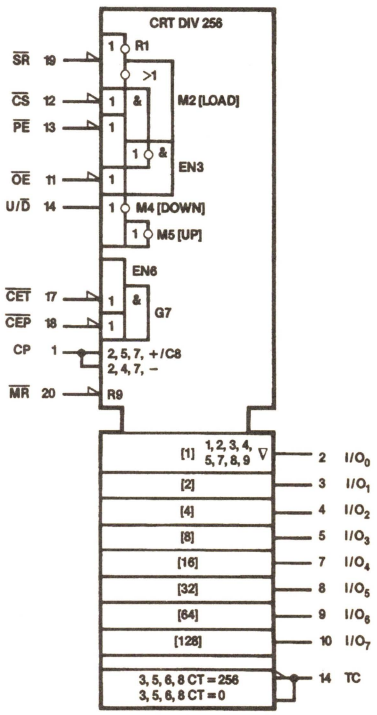



## LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 18 and 19

## LOGIC SYMBOL (IEEE/IEC)

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# Counter

# FAST 74F579

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $I/O_0 - I/O_7$ | Data inputs | 1.0/1.0 | 20μA/0.6mA |
| | Data outputs | 150/40 | 3mA/24mA |
| $\overline{PE}$ | Parallel enable input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $U/\overline{D}$ | Up-down count control input | 1.0/1.0 | 20μA/0.6mA |
| $\overline{MR}$ | Master reset input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{SR}$ | Synchronous reset input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{CEP}$ | Count enable parallel input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{CET}$ | Count enable trickle input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{CS}$ | Chip select input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{OE}$ | Output enable input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| CP | Clock pulse input (active rising edge) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{TC}$ | Terminal count output (active LOW) | 150/33 | 3mA/20mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

## FUNCTION TABLE

| $\overline{MR}$ | $\overline{SR}$ | $\overline{CS}$ | $\overline{PE}$ | $\overline{CEP}$ | $\overline{CET}$ | $U/\overline{D}$ | $\overline{OE}$ | CP | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| X | X | H | X | X | X | X | X | X | I/Oa to I/Oh in High-Z ($\overline{PE}$ disabled) |
| X | X | L | H | X | X | X | H | X | I/Oa to I/Oh in High-Z |
| X | X | L | H | X | X | X | L | X | Flip-flop outputs appear on I/O lines |
| L | X | X | X | X | X | X | X | X | Asynchronous reset for all flip-flops |
| H | L | X | X | X | X | X | X | ↑ | Synchronous reset for all flip-flops |
| H | H | L | L | X | X | X | X | ↑ | Parallel load all flip-flops |
| H | H | (not LL) | | H | X | X | X | ↑ | Hold |
| H | H | (not LL) | | X | H | X | X | ↑ | Hold ($\overline{TC}$ held high) |
| H | H | (not LL) | | L | L | H | X | ↑ | Count up |
| H | H | (not LL) | | L | L | L | X | ↑ | Count down |

H = HIGH voltage level
L = LOW voltage level
X = Don't Care
↑ = LOW-to-HIGH clock transition not LL means $\overline{CS}$ and $\overline{PE}$ should never both be LOW voltage level at the same time.





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# FAST 74F779
## 8-Bit Counter

**8-Bit Bidirectional Binary Counter (3-State)**
***Product Specification***

**Logic Products**

### FEATURES
- **Multiplexed 3-State I/O ports**
- **Built-in lookahead carry capability**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24-pin separate I/O port version**
- **See 'F579 for 20-pin version**

### DESCRIPTION
The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins ($S_0$, $S_1$). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F779 | 145MHz | 90mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F779N |
| Plastic SOL-16 | N74F779D |

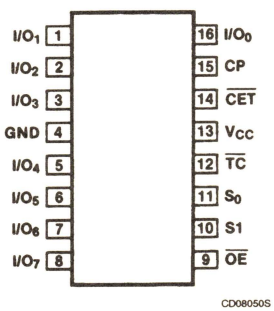
**NOTES:**
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

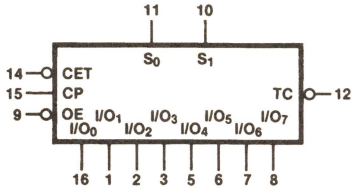
| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $I/O_0 - I/O_7$ | Data inputs | 3.5/1.0 | 70μA/0.6mA |
| | Data outputs | 150/40 | 3mA/24mA |
| $S_0$, $S_1$ | Select inputs | 1.0/1.0 | 20μA/0.6mA |
| $\overline{OE}$ | Output enable input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{CET}$ | Count enable trickle input (active LOW) | 1.0/1.0 | 20μA/0.6mA |
| CP | Clock input pulse (active rising edge) | 1.0/1.0 | 20μA/0.6mA |
| $\overline{TC}$ | Terminal count output (active LOW) | 50/33 | 1mA/20mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

### PIN CONFIGURATION

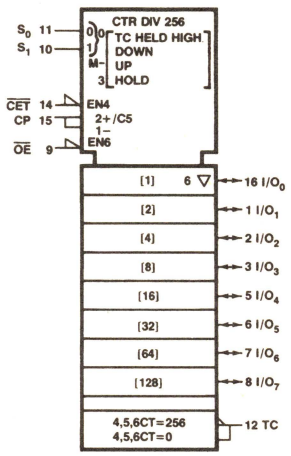



### LOGIC SYMBOL




$V_{CC}$ = Pin 13
GND = Pin 4

### LOGIC SYMBOL (IEEE/IEC)

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# 8-Bit Counter

# FAST 74F779

## FUNCTION TABLE

| INPUTS | | | | | OPERATING MODE |
|---|---|---|---|---|---|
| S1 | S0 | $\overline{CET}$ | $\overline{OE}$ | CP | |
| X | X | X | H | X | I/Oa to I/Oh in HIGH Z |
| X | X | X | L | X | Flip-flop outputs appear on I/O lines |
| L | L | X | X | ↑ | Parallel load all flip-flops |
| (not LL) | | H | X | ↑ | Hold ($\overline{TC}$ held HIGH) |
| H | L | L | X | ↑ | Count up |
| L | H | L | X | ↑ | Count down |

H = HIGH voltage level
L = LOW voltage level
X = don't care
not LL means S0 and S1 should never both be LOW level at the same time.
↑ = LOW-to-HIGH clock transition





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# FAST 74F3037
## 30Ω Line Driver

**Quad 2-Input NAND 30Ω Line Driver**
***Product Specification***

**Logic Products**

### FEATURES

- **30Ω line driver**
- **160mA output drive capability in the LOW state**
- **67mA output drive capability in the HIGH state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on $V_{CC}$ and GND when both side pins are used**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F3037 | 3.8ns | 15mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74F3037N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| A, B | Data inputs | 1.0/1.0 | 20μA/0.6mA |
| $\overline{Y}$ | Data outputs | 3350/266 | 67mA/160mA |

**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

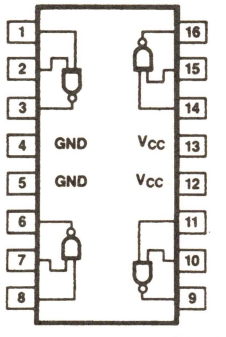
### DESCRIPTION

The F3037 is a high current Line driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the F3037 is 67mA source and 160mA sink with a $V_{CC}$ as low as 4.5 volts. This guarantees incident wave switching with $V_{OH}$ not less than 2.0V and $V_{OL}$ not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

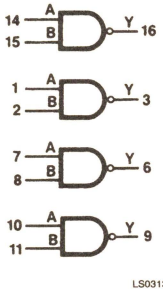
The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

### PIN CONFIGURATION



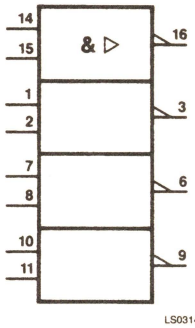
CD04120S

### LOGIC SYMBOL



LS03130S

### LOGIC SYMBOL (IEEE/IEC)



LS03140S

853-0021 76480

Signetics

# 30Ω Line Driver

# FAST 74F3037

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | $\overline{Y}$ |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| | PARAMETER | 74F | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | −0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in LOW output state | 320 | mA |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74F | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | HIGH level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | HIGH level output current | | | −67 | mA |
| $I_{OL}$ | LOW level output current | | | 160 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |





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Signetics

# SCN2674
# Advanced Video Display Controller (AVDC)

***Product Specification***

**Microprocessor Products**

## DESCRIPTION

The Signetics SCN2674 Advanced Video Display Controller (AVDC) is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The AVDC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. It provides consecutive addressing to a user-specified display buffer memory domain and controls the CPU display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the AVDC.

A minimum CRT terminal system configuration consists of an AVDC, an SCN2671 Keyboard and Communication Controller (PKCC), an SCN2670 Display Character and Graphics Generator (DCGG), an SCB2675 Color/Monochrome Attributes Controller (CMAC), a single-chip microcomputer such as the 8048, a display buffer RAM, and a small amount of TTL for miscellaneous address decoding, interface, and control. Typically, the package count for a minimum system is between 15 and 20 devices; system complexity can be enhanced by upgrading the microprocessor and expanding via the system address and data buses.

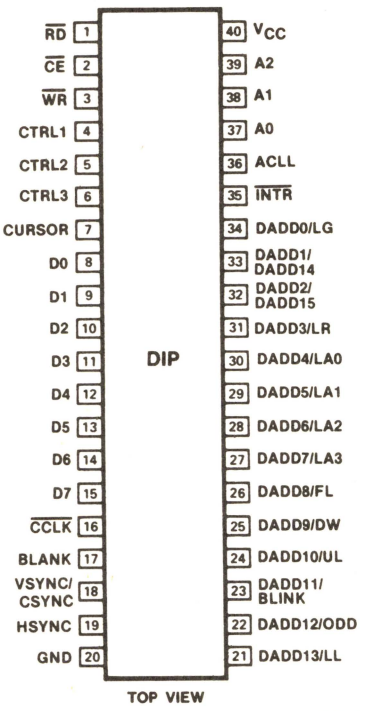
## FEATURES

- **2.7MHz and 4MHz character rates**
- **1 to 256 characters per row**
- **1 to 16 raster lines per character row**
- **1 to 128 character rows per frame**
- **Bit-mapped graphics mode**
- **Programmable horizontal and vertical sync generators**
  - **RS-170 compatible sync**
- **Interlaced or non-interlaced operation**
- **Up to 64k RAM addressing for multiple page operation**
- **Readable, writable and incrementable cursor**
  - **Programmable cursor size and blink**
- **AC line lock**
- **Automatic wraparound of RAM**
- **Automatic split screen**
- **Automatic bidirectional soft scrolling**
  - **Programmable scan line increment**
- **Row table addressing mode**
- **Double height tops and bottoms**
- **Double width control output**
- **Selectable buffer interface modes**
- **Dynamic RAM refresh**
- **Completely TTL compatible**
- **Single +5V power supply**
- **Power-on reset circuit**

## APPLICATIONS

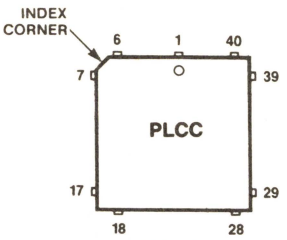
- **CRT terminals**
- **Word processing systems**
- **Small business computers**
- **Home computers**

## PIN CONFIGURATIONS




TOP VIEW

CD00500S




TOP VIEW

CD0044PS

| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | NC | 17 | D7 | 31 | DADD6/LA2 |
| 2 | $\overline{RD}$ | 18 | $\overline{CCLK}$ | 32 | DADD5/LA1 |
| 3 | $\overline{CE}$ | 19 | BLANK | 33 | DADD4/LA0 |
| 4 | $\overline{WR}$ | 20 | VSYNC | 34 | NC |
| 5 | CTRL1 | | CSYNC/ | 35 | DADD3/LR |
| 6 | CTRL2 | 21 | HSYNC | 36 | DADD2/ |
| 7 | CTRL3 | 22 | GND | | DADD15 |
| 8 | CURSOR | 23 | NC | 37 | DADD1/ |
| 9 | D0 | 24 | DADD13/LL | | DADD14 |
| 10 | D1 | 25 | DADD12/ | 38 | DADD0/LG |
| 11 | D2 | | ODD | 39 | $\overline{INTR}$ |
| 12 | NC | 26 | DADD11/ | 40 | ACLL |
| 13 | D3 | | BLINK | 41 | A0 |
| 14 | D4 | 27 | DADD10/UL | 42 | A1 |
| 15 | D5 | 28 | DADD9/DW | 43 | A2 |
| 16 | D6 | 29 | DADD8/FL | 44 | $V_{CC}$ |
| | | 30 | DADD7/LA3 | | |

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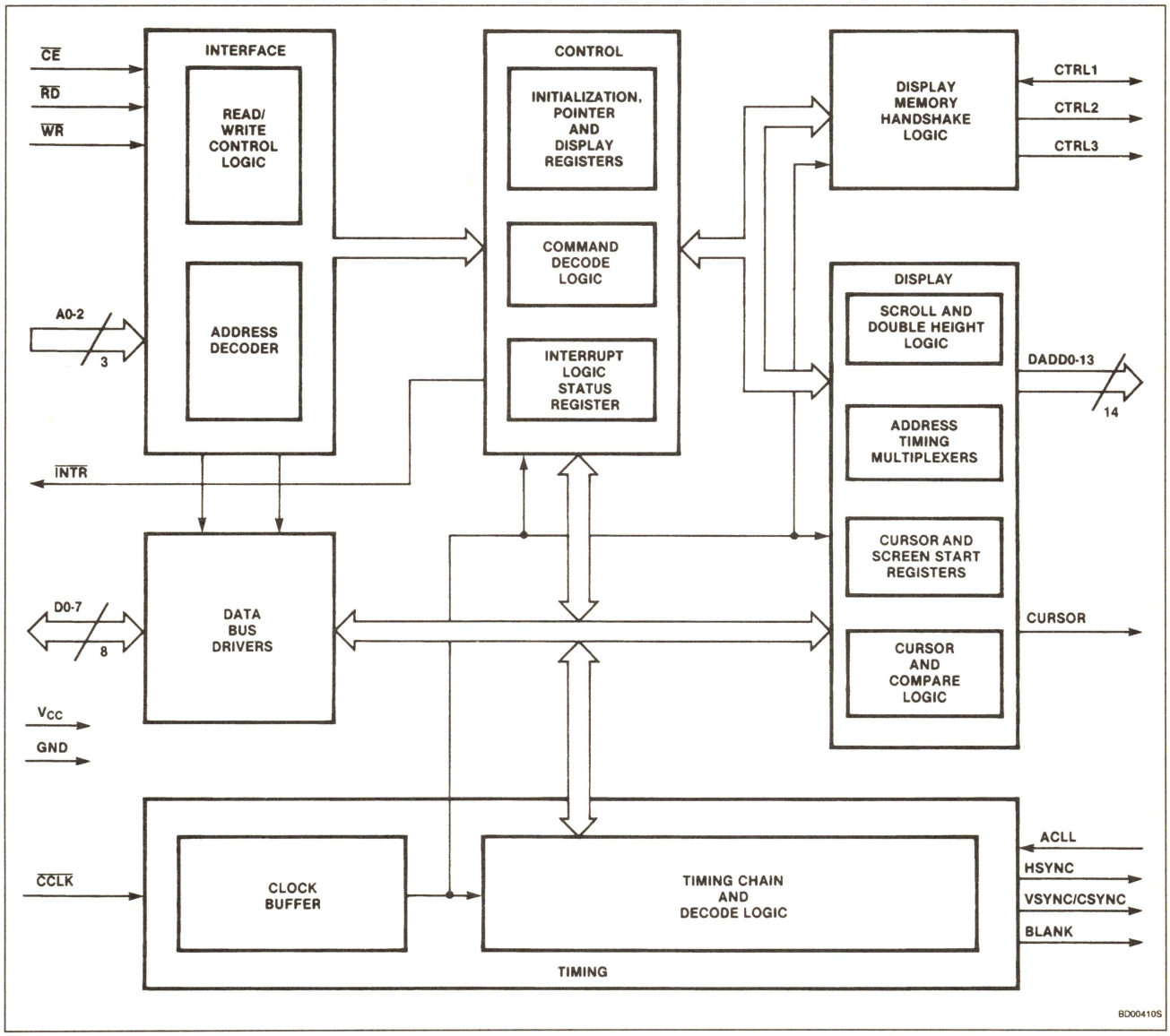
# Advanced Video Display Controller (AVDC) SCN2674

## ORDERING CODE

| PACKAGES | $V_{CC}$ = +5V ±5%, $T_A$ = 0°C to +70°C | |
|---|---|---|
| | 4MHz | 2.7MHz |
| Ceramic DIP | SCN2674BC4I40 | SCN2674BC3I40 |
| Plastic DIP | SCN2674BC4N40 | SCN2674BC3N40 |
| Plastic LCC | SCN2674BC4A44 | SCN2674BC3A44 |

## BLOCK DIAGRAM




Signetics

Signetics

# SCB2675T

## Turbo Color/Monochrome Attributes Controller (Turbo-CMAC)

**Microprocessor Products**

***Preliminary Specification***

### DESCRIPTION

HThe Signetics SCB2675T Turbo Color/Monochrome Attributes Controller (Turbo-CMAC) is a bipolar LSI device designed for CRT terminals and display systems that employ raster scan techniques. It contains a programmable dot clock divider to generate a character clock, a high speed shift register to serialize input dot data into a video stream, latches and logic to apply visual attributes to the resulting display, and logic to display a cursor on the display.

The Turbo-CMAC provides control of visual attributes on a character by character basis for two operating modes: monochrome and color. The monochrome mode provides reverse video, blank, highlight and two general purpose user definable attributes. In this mode, the display characters can be specified to appear on either a light or dark screen background. Retrace video suppression can be automatically or externally controlled. The color mode provides eight colors for foreground (character) video and eight colors for background video together with a luminance output for external color set selection or to simultaneously drive a monochrome monitor. Additionally, both modes provide double width, underline, blink, dot stretching and dot width attributes. In monochrome mode, the SCB2675T emulates the attribute characteristics of Digital Equipment Corporation's VT100 terminal.

The horizontal dot frequency is the basic timing input to the Turbo-CMAC. This clock is divided internally to provide a character clock output for system synchronization. Up to nine bits of dot data are parallel loaded into the video shift register on each character boundary. The two TTL video data outputs in monochrome mode are encoded to provide four video intensities (black, gray, white and highlight). The video data in color mode is encoded to provide eight foreground colors and shifted out on three TTL outputs, together with the luminance output.

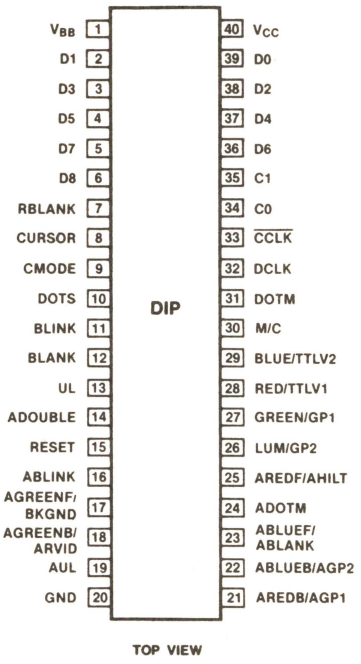
### FEATURES

- **40MHz video dot rate version**
- **Four video intensities encoded on two TTL outputs (monochrome mode)**
- **Eight foreground and background colors encoded on three TTL outputs (color mode)**
- **Internally latched character attributes:**
  - **Reverse video**
  - **Blank**
  - **Blink**
  - **Underline**
  - **Highlight**
  - **Two general purpose**
  - **Eight foreground colors**
  - **Eight background colors**
  - **Dot width control**
  - **Double width characters**
- **VT100 compatible attributes**
- **Reverse video cursor with optional white cursor in color mode**
- **Up to 10 dots per character**
- **Light or dark background in monochrome mode**
  - **Automatic retrace blanking**
- **Programmable dot stretching**
- **Compatible with SCN2674 AVDC and SCN2670 DCGG**
- **TTL compatible**
- **40-pin dual in-line package**

### APPLICATIONS

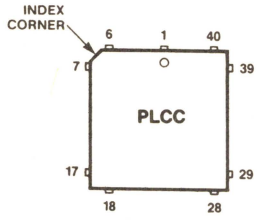
- **CRT terminals**
- **Word processing systems**
- **Small business computers**

### PIN CONFIGURATION




TOP VIEW

CD00430S




TOP VIEW

CD0044PS

| Pin | Function | Pin | Function |
|---|---|---|---|
| 2 | $V_{BB}$ | 24 | AREDB/AGP1 |
| 3 | D1 | 25 | ABLUEB/AGP2 |
| 4 | D3 | 26 | ABLUEF/ABLANK |
| 5 | D5 | 27 | ADOTM |
| 6 | D7 | 28 | AREDF/AHILT |
| 7 | D8 | 29 | LUM/GP2 |
| 8 | RBLANK | 30 | GREEN/GP1 |
| 9 | CURSOR | 31 | RED/TTLV1 |
| 10 | CMODE | 32 | BLUE/TTLV2 |
| 11 | DOTS | 33 | M/C |
| 13 | BLINK | 35 | DOTM |
| 14 | BLANK | 36 | DCLK |
| 15 | UL | 37 | $\overline{CCLK}$ |
| 16 | ADOUBLE | 38 | C0 |
| 17 | RESET | 39 | C1 |
| 18 | ABLINK | 40 | D6 |
| 19 | AGREENF/BKGND | 41 | D4 |
| 20 | AGREENB/ARVID | 42 | D2 |
| 21 | AUL | 43 | D0 |
| 22 | GND | 44 | $V_{CC}$ |





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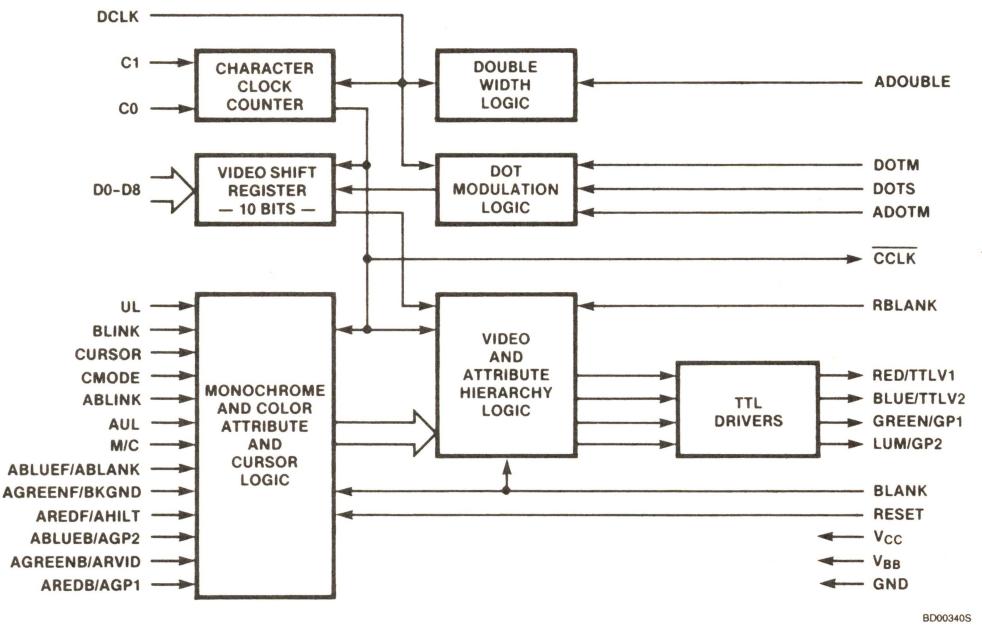
# Turbo Color/Monochrome Attributes Controller (Turbo-CMAC) SCB2675T

## ORDERING CODE

| PACKAGES | DOTS PER CHARACTER | $V_{CC}$ = 5V ± 5%, 0°C to +70°C |
|---|---|---|
| | | 40MHz |
| Plastic DIP<br>Plastic LCC | 7, 8, 9, 10 | SCB2675TC4N40<br>SCB2675TC4A44 |

## BLOCK DIAGRAM



Signetics

# SCC63484
# Advanced CRT Controller (ACRTC)

*Objective Specification*

**Microprocessor Products**

## DESCRIPTION

The Signetics SCC63484 Advanced CRT Controller (ACRTC) is a CMOS VLSI microcomputer peripheral device capable of controlling raster scan type CRTs to display both graphics and characters. The ACRTC is a new generation CRT controller that is based on a bit-mapped technology and has more display control functions than those of an SCN2674 Advanced Video Display Controller (AVDC).

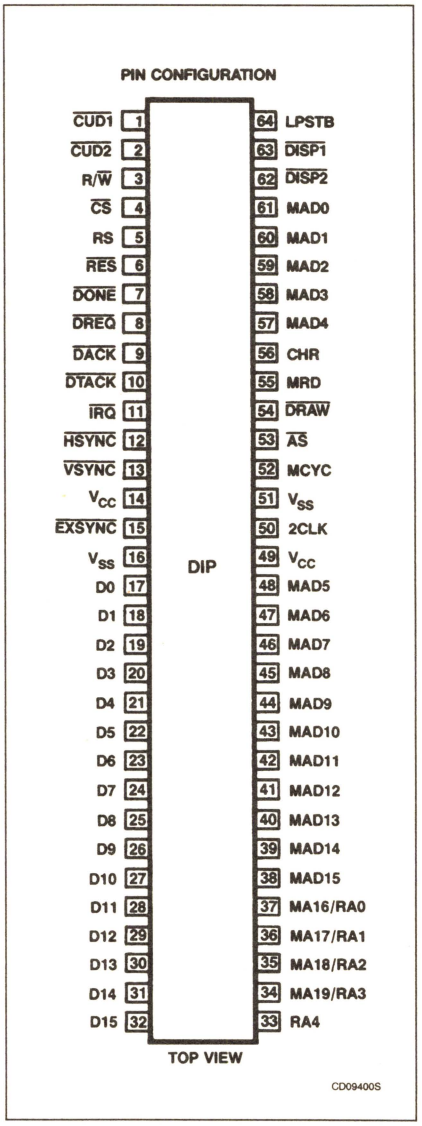
The ACRTC prepares the mechanisms to use in one of three modes; character only, graphic only and multiplexed character/graphic modes. Therefore, the ACRTC can be applied to many applications, from character-only display devices to large full-graphic systems.

The ACRTC can reduce CPU software overhead and enhance system throughput.

## FEATURES

- **High-speed graphic drawings**
  - **Drawing rate: maximum 500ns/pixel (color drawing)**
  - **Drawn graphics: Dot, line, rectangle, polyline, polygon, circle, ellipse, paint, copy, etc.**
  - **Drawn colors: 16 bits/word, 1, 2, 4, 8, 16 bits/pixel (5 types) monochrome to max 64k colors**
- **Large frame memory space**
  - **Maximum 2Mbytes graphic memory**
  - **Maximum 128-byte character memory separated from the MPU memory**
  - **Available to maximum 4096 × 4096 high-resolution CRT (1 bit/pixel mode)**
- **Various CRT display controls**
  - **Split screens (3 displays and 1 window)**
  - **Zooming up (1 to 16 times)**
  - **Scroll (vertical and horizontal)**
- **External synchronization**
  - **Synchronization between ACRTCs or between the ACRTC and external device, e.g. TV system or other controller**
- **DMA interface**
- **Two programmable cursors**
- **Three scan modes**
  - **Non-interlace, interlace sync., and interlace sync. and video modes**
- **Interrupt request to MPU**
- **256 characters/line, 32 rasters/line, 4096 rasters/screen**
- **Maximum clock frequency 8MHz**
- **CMOS, +5V single power supply**

## PIN CONFIGURATION







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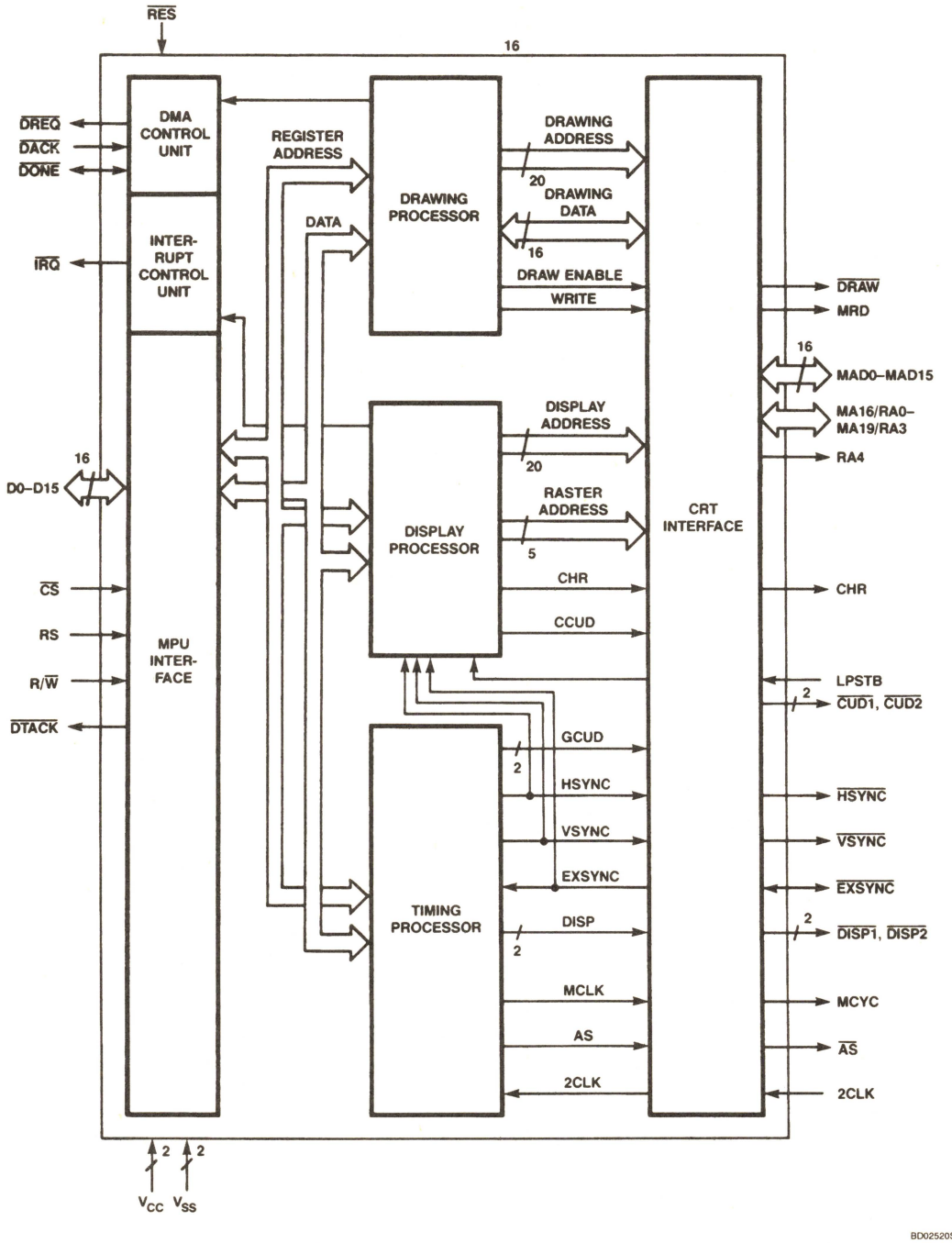
# Advanced CRT Controller (ACRTC)

# SCC63484

## ORDERING CODE

| PACKAGE | $V_{CC}$ = 5V ± 5%, $T_A$ = 0°C to +70°C | | |
|---|---|---|---|
| | | | 8MHz |
| Plastic DIP | | | SCC63484C8A64 |
| Ceramic DIP | | | SCC63484C8I64 |

## BLOCK DIAGRAM



Signetics

# SCN2681
# Dual Asynchronous Receiver/ Transmitter (DUART)

*Product Specification*

**Microprocessor Products**

## DESCRIPTION

The Signetics SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

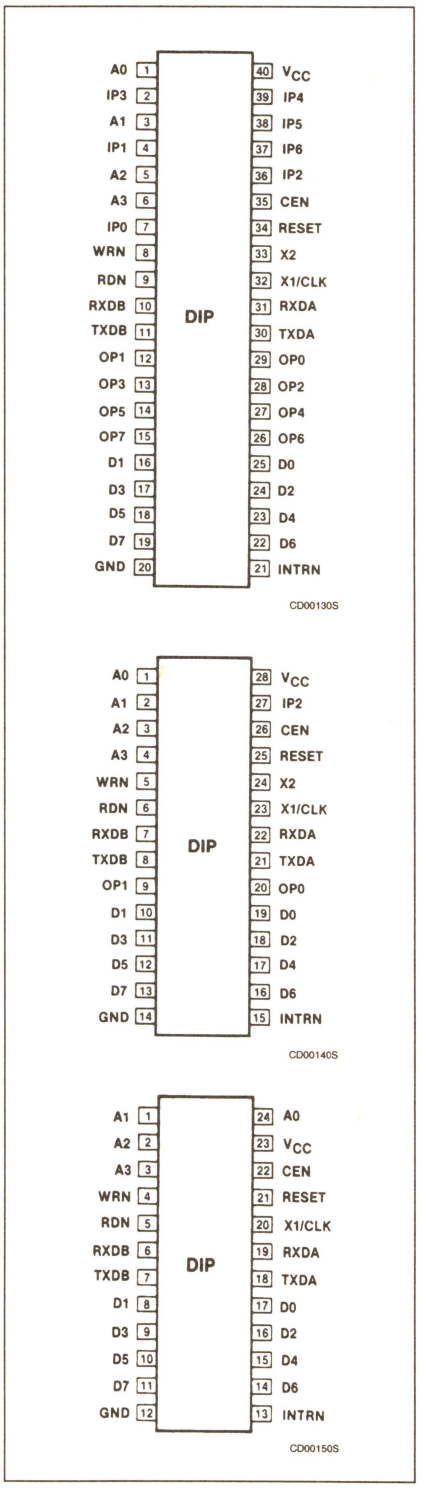
The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

## FEATURES

- **Dual full-duplex asynchronous receiver/transmitter**
- **Quadruple buffered receiver data registers**
- **Programmable data format**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in 1/16-bit increments**
- **Programmable baud rate for each receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4k baud**
  - **One user-defined rate derived from programmable timer/counter**
  - **External 1× or 16× clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex)**
  - **Automatic echo**
  - **Local loopback**
  - **Remote loopback**
- **Multi-function programmable 16-bit counter/timer**
- **Multi-function 7-bit input port**
  - **Can serve as clock or control inputs**
  - **Change of state detection on four inputs**
- **Multi-function 8-bit output port**
  - **Individual bit set/reset capability**
  - **Outputs can be programmed to be status/interrupt signals**
- **Versatile interrupt system**
  - **Single interrupt output with eight maskable interrupting conditions**
  - **Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs**
- **Maximum data transfer: 1× – 1MB/s, 16× – 125kB/s**
- **Automatic wake-up mode for multidrop applications**
- **Start-end break interrupt/status**
- **Detects break which originates in the middle of a character**
- **On-chip crystal oscillator**
- **TTL compatible**
- **Single +5V power supply**

## PIN CONFIGURATIONS

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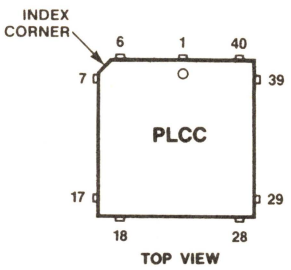
# Dual Asynchronous Receiver/Transmitter (DUART) SCN2681

## PIN CONFIGURATIONS (Continued)




CD0044PS

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | A0 | 24 | INTRN |
| 3 | IP3 | 25 | D6 |
| 4 | A1 | 26 | D4 |
| 5 | IP1 | 27 | D2 |
| 6 | A2 | 28 | D0 |
| 7 | A3 | 29 | OP6 |
| 8 | IP0 | 30 | OP4 |
| 9 | WRN | 31 | OP2 |
| 10 | RDN | 32 | OP0 |
| 11 | RXDB | 33 | TXDA |
| 12 | NC | 34 | NC |
| 13 | TXDB | 35 | RXDA |
| 14 | OP1 | 36 | X1/CLK |
| 15 | OP3 | 37 | X2 |
| 16 | OP5 | 38 | RESET |
| 17 | OP7 | 39 | CEN |
| 18 | D1 | 40 | IP2 |
| 19 | D3 | 41 | IP6 |
| 20 | D5 | 42 | IP5 |
| 21 | D7 | 43 | IP4 |
| 22 | GND | 44 | $V_{CC}$ |

## ORDERING CODE

| PACKAGES | $V_{CC}$ = +5V ±5%, $T_A$ = 0°C to +70°C | | | |
|---|---|---|---|---|
| | 24-Pin[1] | 28-Pin[2] | 40-Pin[2] | 44-Pin |
| Ceramic DIP | Not available | SCN2681AC1I28 | SCN2681AC1I40 | Not available |
| Plastic DIP | SCN2681AC1N24 | SCN2681AC1N28 | SCN2681AC1N40 | Not available |
| Plastic LCC | Not available | Not available | Not available | SCN2681AC1A44 |

**NOTES:**
1. [1]400 mil wide DIP
2. [2]600 mil wide DIP

Also provided on the SCN2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCN2681 is available in four package versions: 40-pin and 28-pin, both 0.6″ wide DIPs; a compact 24-pin 0.4″ wide DIP; and a 44-pin PLCC.

Signetics

# SCN68681
# Dual Asynchronous Receiver/ Transmitter (DUART)

*Product Specification*

**Microprocessor Products**

## DESCRIPTION

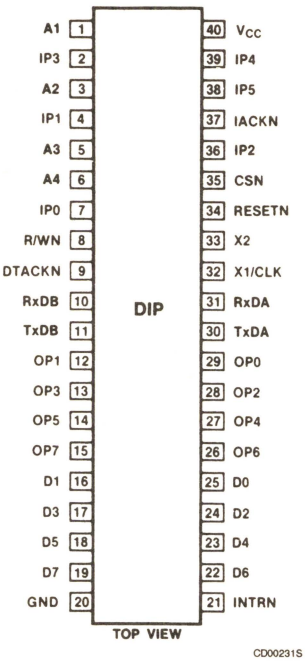
The Signetics SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices, and can also interface easily with other microprocessors. The DUART can be used in polled or interrupt driven systems.

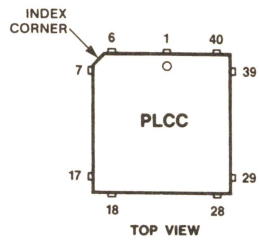
The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

## FEATURES

- **S68000 bus compatible**
- **Dual full-duplex asynchronous receiver/transmitter**
- **Quadruple buffered receiver data registers**
- **Programmable data format**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in 1/16-bit increments**
- **Programmable baud rate for each receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4K baud**
  - **One user-defined rate derived from programmable timer/ counter**
  - **External 1× or 16× clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex)**
  - **Automatic echo**
  - **Local loopback**
  - **Remote loopback**
- **Multi-function programmable 16-bit counter/timer**
- **Multi-function 6-bit input port**
  - **Can serve as clock or control inputs**
  - **Change-of-state detection on four inputs**
- **Multi-function 8-bit output port**
  - **Individual bit set/reset capability**
  - **Outputs can be programmed to be status/interrupt signals**
- **Versatile interrupt system**
  - **Single interrupt output with eight maskable interrupting conditions**
  - **Interrupt vector output on interrupt acknowledge**
  - **Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs**
- **Maximum data transfer: 1× – 1MB/sec, 16× – 125kB/sec**
- **Automatic wake-up mode for multidrop applications**
- **Start-end break interrupt/status**
- **Detects break which originates in the middle of a character**
- **On-chip crystal oscillator**
- **TTL compatible**
- **Single +5V power supply**

## PIN CONFIGURATIONS




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | A1 | 24 | INTRN |
| 3 | IP3 | 25 | D6 |
| 4 | A2 | 26 | D4 |
| 5 | IP1 | 27 | D2 |
| 6 | A3 | 28 | D0 |
| 7 | A4 | 29 | OP6 |
| 8 | IP0 | 30 | OP4 |
| 9 | R/WN | 31 | OP2 |
| 10 | DTACKN | 32 | OP0 |
| 11 | RxDB | 33 | TxDA |
| 12 | NC | 34 | NC |
| 13 | TxDB | 35 | RxDA |
| 14 | OP1 | 36 | X1/CLK |
| 15 | OP3 | 37 | X2 |
| 16 | OP5 | 38 | RESET |
| 17 | OP7 | 39 | CSN |
| 18 | D1 | 40 | IP2 |
| 19 | D3 | 41 | IACKN |
| 20 | D5 | 42 | IP5 |
| 21 | D7 | 43 | IP4 |
| 22 | GND | 44 | $V_{CC}$ |

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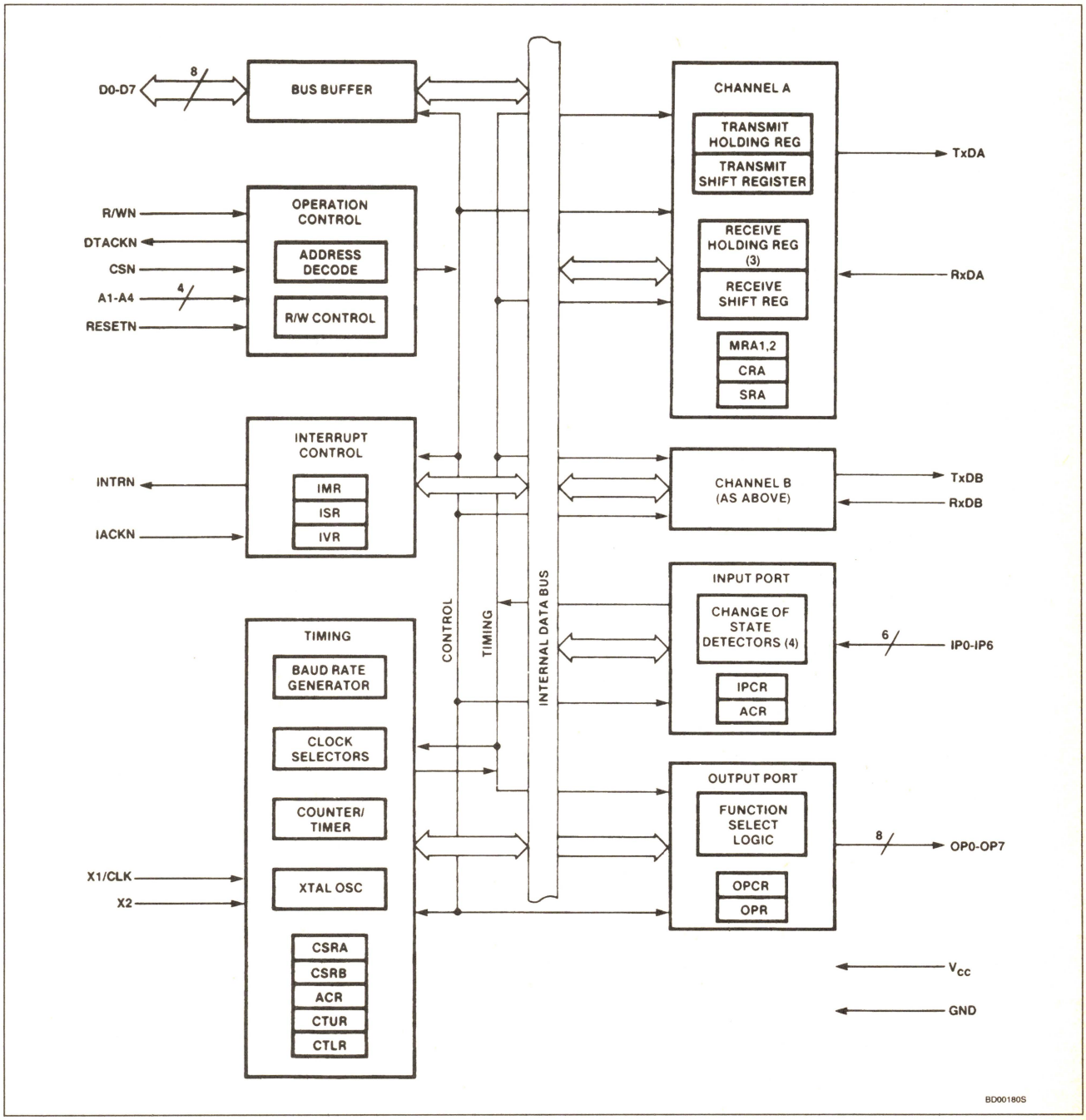
# Dual Asynchronous Receiver/Transmitter (DUART) SCN68681

## ORDERING CODE

| PACKAGES | $V_{CC}$ = +5V ±5%, $T_A$ = 0°C to +70°C |
|---|---|
| Ceramic DIP | SCN68681C1I40 |
| Plastic DIP | SCN68681C1N40 |
| Plastic LCC | SCN68681CIA44 |

## BLOCK DIAGRAM



Signetics

# SCC2691
# Universal Asynchronous Receiver/Transmitter (UART)

*Objective Specification*

**Microprocessor Products**

## DESCRIPTION

The Signetics SCC2691 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter in a single 24-pin DIP. It is fabricated with Signetics CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of the receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

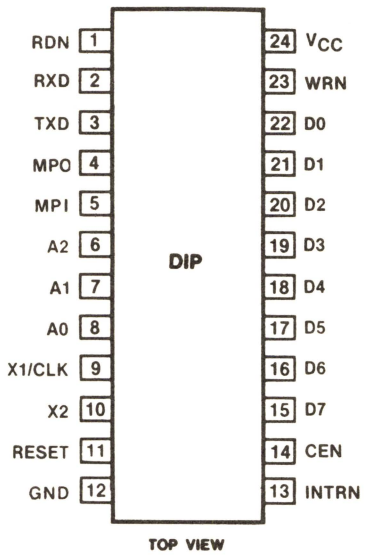
The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes.

The UART is fully TTL compatible and operates from a single +5V power supply.

## FEATURES

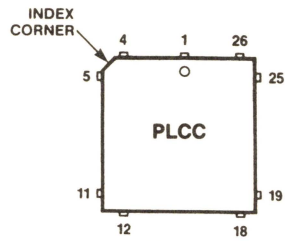
- **Full-duplex asynchronous receiver/transmitter**
- **Quadruple buffered receiver data register**
- **Programmable data format:**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in $^{1}/_{16}$-bit increments**
- **Baud rate for the receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4k baud**
  - **One user-defined rate derived from programmable timer/counter**
  - **External 1× or 16× clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex)**
  - **Automatic echo**
  - **Local loopback**
  - **Remote loopback**
- **Multi-function programmable 16-bit counter/timer**
- **Single interrupt output with seven maskable interrupting conditions**
- **On-chip crystal oscillator**
- **Low power mode**
- **TTL compatible**
- **Single +5V power supply**

## PIN CONFIGURATIONS




TOP VIEW

CD00011S




TOP VIEW

CD0028PS

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 15 | NC |
| 2 | RDN | 16 | INTRN |
| 3 | RXD | 17 | CEN |
| 4 | TXD | 18 | D7 |
| 5 | MPO | 19 | D6 |
| 6 | MPI | 20 | D5 |
| 7 | NC | 21 | D4 |
| 8 | A2 | 22 | D3 |
| 9 | A1 | 23 | NC |
| 10 | A0 | 24 | D2 |
| 11 | X1/CLK | 25 | D1 |
| 12 | X2 | 26 | D0 |
| 13 | RESET | 27 | WRN |
| 14 | GND | 28 | $V_{CC}$ |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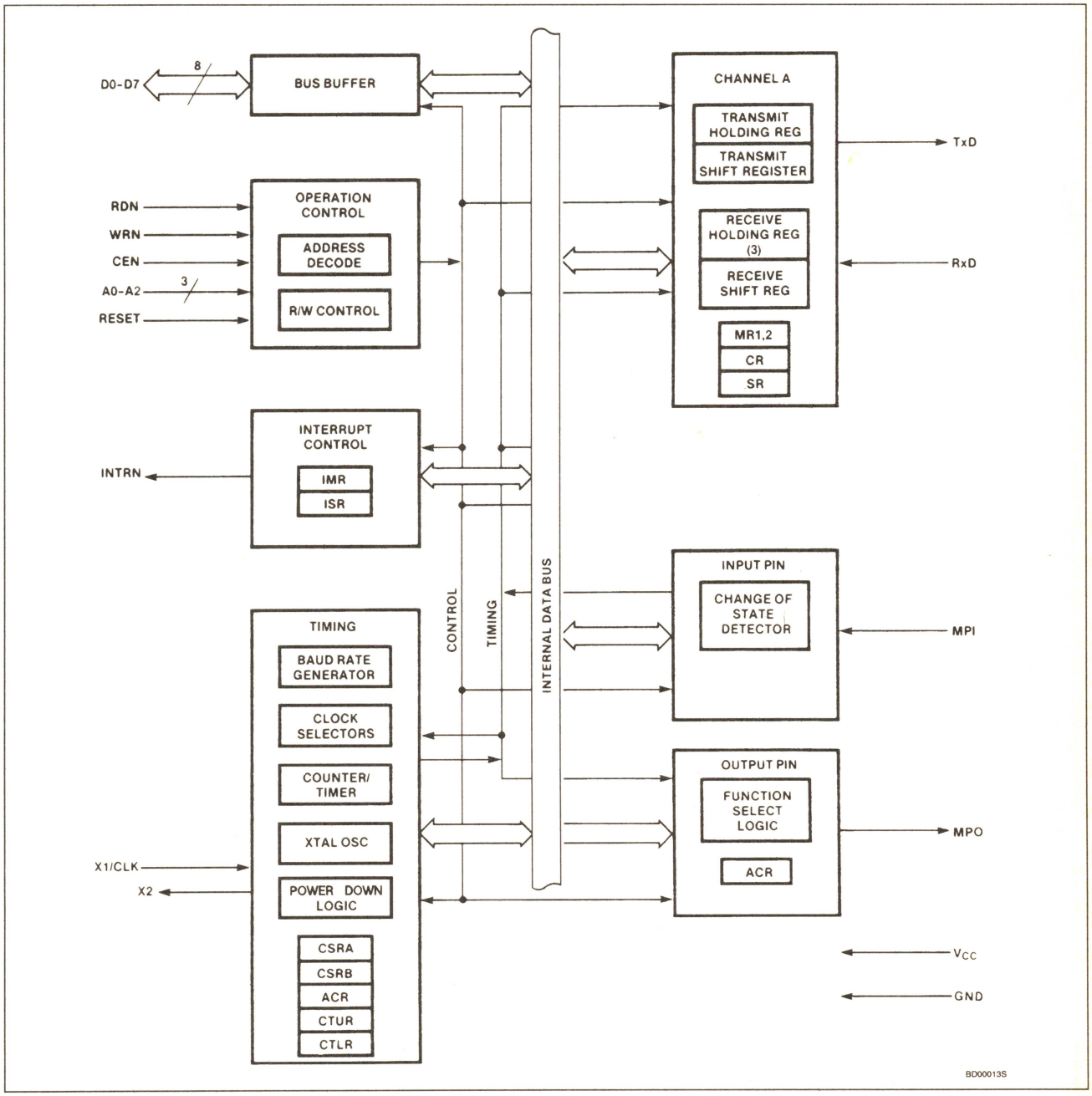
# Universal Asynchronous Receiver/Transmitter (UART) SCC2691

## ORDERING CODE

| PACKAGES | $V_{CC}$ = +5V ± 10%, $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | SCC2691AC1N24 |
| Plastic LCC | SCC2691AC1A28 |

## BLOCK DIAGRAM



Signetics

# SCC2698

# Octal Universal Asynchronous Receiver/Transmitter (Octal-UART)

**Microprocessor Products**

***Preliminary Specification***

## DESCRIPTION

The Signetics SCC2698 Octal Universal Asynchronous Receiver/Transmitter (Octal-UART) is a single-chip MOS-LSI communications device that provides an eight-channel full-duplex asynchronous receiver/transmitter in a single package. It is fabricated with Signetics' CMOS technology, which combines the benefits of high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the Octal-UART particularly functional for dual-speed channel applications such as clustered terminal systems.

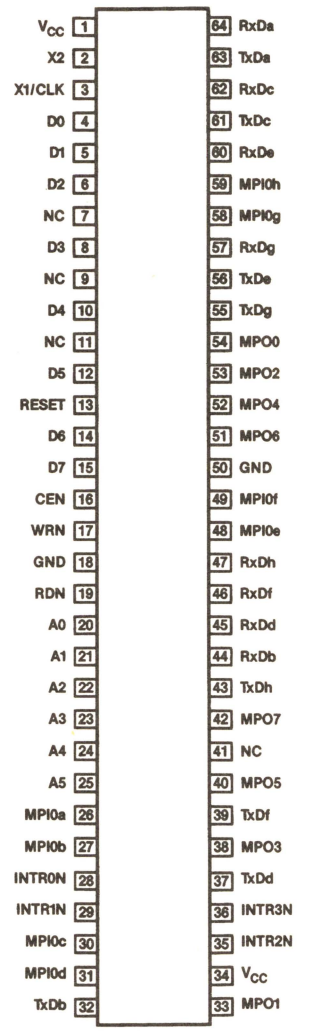
The receiver is quadruply buffered to minimize the potential of receiver overrun, or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

The Octal-UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The Octal-UART is fully TTL compatible and operates from a single +5V power supply.

## FEATURES

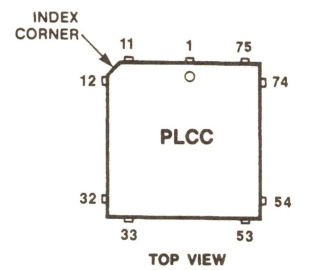
- **Eight full-duplex asynchronous receiver/transmitters**
- **Quadruple buffered receiver data register**
- **Programmable data format:**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in 1/16-bit increments**
- **Baud rate for the receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4k baud**
  - **One user-defined rate derived from programmable counter/timer**
  - **External 1× or 16× clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex), automatic echo, local loopback, remote loopback**
- **Four multi-function programmable 16-bit counter/timers**
- **Single interrupt output with eight maskable interrupting conditions**
- **On-chip crystal oscillator**
- **TTL compatible**
- **Single +5V power supply with low power mode**

## PIN CONFIGURATIONS




TOP VIEW

CD09380S




TOP VIEW

CD0045PS

PLCC Pin Functions (Next Page)



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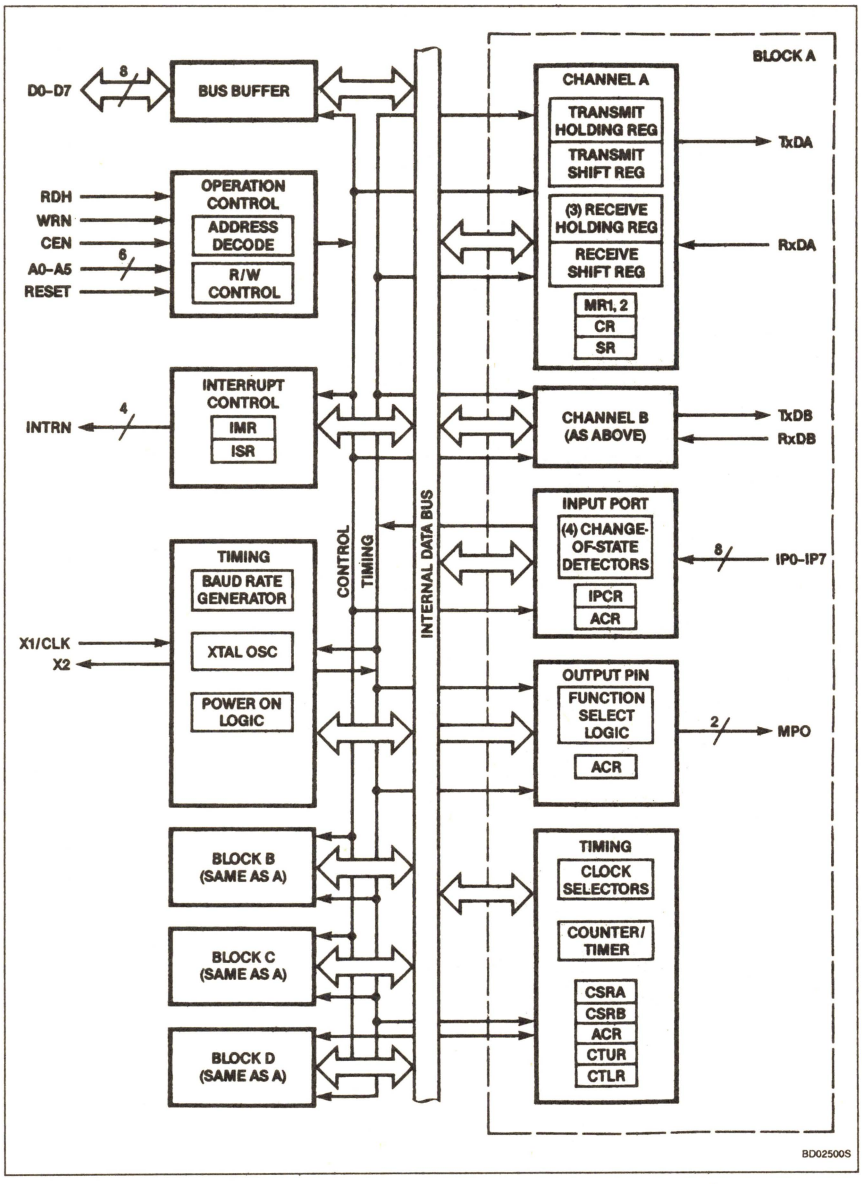
# Octal Universal Asynchronous Receiver/Transmitter (Octal-UART)

# SCC2698

## ORDERING CODE

| PACKAGES | $V_{CC}$ = +5V ± 5%, $T_A$ = 0 to +70°C |
|---|---|
| Plastic DIP | SCC2698AC1N64 |
| Plastic LCC | SCC2698AC1A84 |

## BLOCK DIAGRAM




## PIN CONFIGURATION (Continued)

PLCC

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | TxDa | 43 | MPO1 |
| 2 | MPI13g | 44 | MPI2d |
| 3 | RxDa | 45 | $V_{CC}$ |
| 4 | MPI13h | 46 | INTR2N |
| 5 | $V_{CC}$ | 47 | INTR3N |
| 6 | X2 | 48 | MPI3c |
| 7 | X1/CLK | 49 | TxDd |
| 8 | D0 | 50 | MPI3d |
| 9 | D1 | 51 | MPO3 |
| 10 | D2 | 52 | TxDf |
| 11 | D3 | 53 | MPO5 |
| 12 | D4 | 54 | MPO7 |
| 13 | D5 | 55 | TxDh |
| 14 | MPI1a | 56 | RxDb |
| 15 | RESET | 57 | RxDd |
| 16 | D6 | 58 | RxDf |
| 17 | D7 | 59 | RxDh |
| 18 | CEN | 60 | MPI1e |
| 19 | WRN | 61 | MPI0e |
| 20 | GND | 62 | MPI1f |
| 21 | MPI1b | 63 | MPI0f |
| 22 | RDN | 64 | MPI2e |
| 23 | A0 | 65 | GND |
| 24 | MPI2a | 66 | MPI2f |
| 25 | A1 | 67 | MPO6 |
| 26 | MPI2b | 68 | MPI3e |
| 27 | A2 | 69 | MPO4 |
| 28 | MPI3a | 70 | MPI3f |
| 29 | A3 | 71 | MPO2 |
| 30 | MPI3b | 72 | MPO0 |
| 31 | A4 | 73 | TxDg |
| 32 | A5 | 74 | TxDe |
| 33 | MPI0a | 75 | RxDg |
| 34 | MPI0b | 76 | MPI0g |
| 35 | INTR0N | 77 | MPI0h |
| 36 | INTR1N | 78 | MPI1g |
| 37 | MPI0c | 79 | RxDe |
| 38 | MPI1c | 80 | MPI1h |
| 39 | MPI0d | 81 | TxDc |
| 40 | MPI1d | 82 | MPI2g |
| 41 | TxDb | 83 | RxDc |
| 42 | MPI2c | 84 | MPI2h |



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Signetics

# SCN68562
# Dual Universal Serial Communications Controller (DUSCC)

**Products**

***Preliminary Specification***

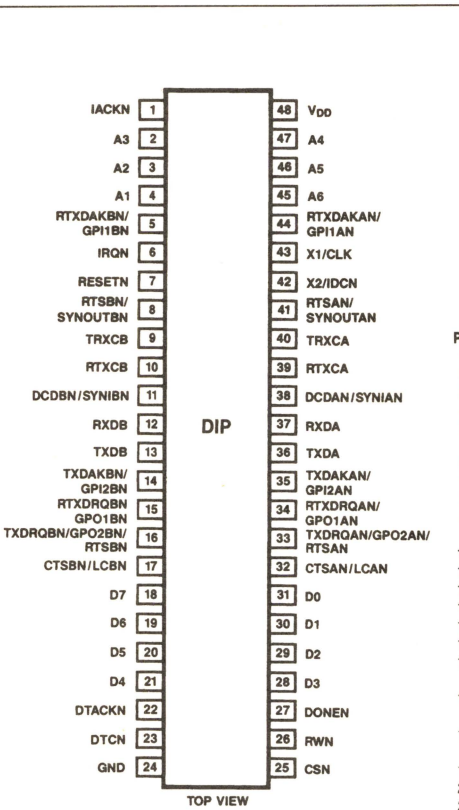
## DESCRIPTION

The Signetics SCN68562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN68562 interfaces to the 68000 MPU via asynchronous bus control signals and is capable of program-polled, interrupt-driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1× or 16× clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

## PIN CONFIGURATIONS




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | IACKN | 27 | CSN |
| 2 | A3 | 28 | R/WN |
| 3 | A2 | 29 | DONEN |
| 4 | A1 | 30 | D3 |
| 5 | RTxDAKBN/ GPI1BN | 31 | D2 |
| | | 32 | D1 |
| 6 | IRQN | 33 | D0 |
| 7 | NC | 34 | NC |
| 8 | RESETN | 35 | CTSAN/LCAN |
| 9 | RTSBN/ SYNOUTBN | 36 | TxDRQAN/ GPO2AN/RTSAN |
| 10 | TRxCB | 37 | RTxDRQAN/ GPO1AN |
| 11 | RTxCB | | |
| 12 | DCDBN/SYNIBN | 38 | TxDAKAN/GPI2AN |
| 13 | NC | 39 | TxDA |
| 14 | RxDB | 40 | RxDA |
| 15 | TxDB | 41 | NC |
| 16 | TxDAKBN/ GPI2BN | 42 | DCDAN/SYNIAN |
| | | 43 | RTxCA |
| 17 | RTxDRQBN/ GPO1BN | 44 | TRxCA |
| | | 45 | RTSAN/ SYNOUTAN |
| 18 | TxDRQBN/ GPO2BN/RTSBN | 46 | X2/IDCN |
| | | 47 | X1/CLK |
| 19 | CTSBN/LCBN | 48 | RTxDAKAN/ GPI1AN |
| 20 | D7 | | |
| 21 | D6 | 49 | A6 |
| 22 | D5 | 50 | A5 |
| 23 | D4 | 51 | A4 |
| 24 | DTACKN | 52 | $V_{DD}$ |
| 25 | DTCN | | |
| 26 | GND | | |

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.





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# Dual Universal Serial Communications Controller (DUSCC) SCN68562

## FEATURES

### General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multi-protocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, e tc.
  - COP: BISYNC, DDCMP, X.21
  - ASYNC: 5 – 8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4K baud
  - One user-defined rate derived from programmable counter/timer
  - External 1× or 16× clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/ decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full-half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with Signetics' SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
  - 68000 compatible
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

### Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in $\frac{1}{16}$- bit increments
- 1× or 16× Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search $\frac{1}{2}$ bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match

### Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection
- BISYNC Features
  - EBCDIC or ASCII header, text and control messages
  - SYN, DLE stripping
  - EOM (end of message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text

### Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0 – 7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS-FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

## ORDERING CODE

| PACKAGES | $V_{CC}$ = +5V± 10%, $T_A$ = 0 to +70°C |
|---|---|
| Ceramic DIP | SCN68562C4I48 |
| Plastic DIP | SCN68562C4N48 |
| Plastic LCC | SCN68562C4A52 |



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Signetics

# SCN68454
# Intelligent Multiple Disk Controller (IMDC)

***Preliminary Specification***

**Products**

## DESCRIPTION

The SCN68454 Intelligent Multiple Disk Controller (IMDC) provides the traditional and advanced features required to control Winchester type rigid disks and floppy disks. It can control up to four rigid or floppy disk drives, in any combination. It can be used to control, with a minimum of external hardware, any drive that has an SA1000 interface standard or an ST506 Seagate interface standard.

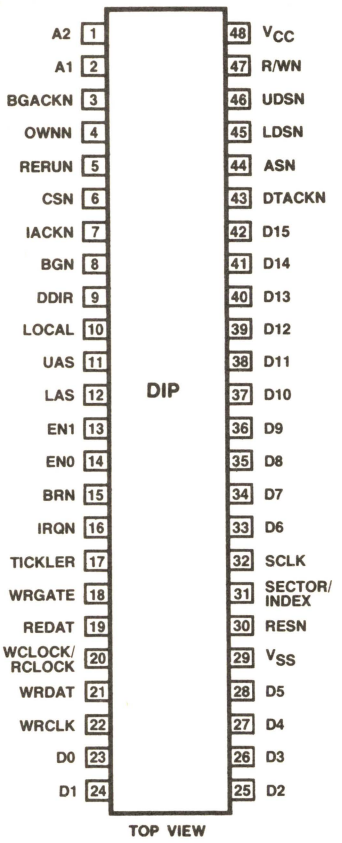
The IMDC supports soft or hard sectored disk track format and standard IBM track formats for floppy disks (both single and double density).

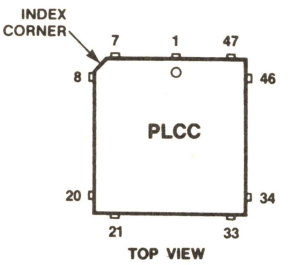
The controller is programmable via an external host processor by the use of high level commands. Data transfer on the host data bus can be 8 or 16-bit in parallel. The IMDC is capable of handling a serial data rate of up to 10Mbits per second. The SCN68454 is constructed using Signetics MOS-VLSI technology.

## FEATURES

- **Bus compatible with SCN68000 microprocessor**
- **Automatic rerun on bus error**
- **Supports SCN68000 vectored interrupts**
- **31-bit address counter**
- **16/8-bit data transfers**
- **Supports up to 4 rigid disks and floppy disks in any combination**
- **Supports SA1000 and ST506 Winchester interfaces**
- **Data rates up to 10Mbits per second for MFM**
- **Data rates up to 2Mbits per second for FM**
- **Handles FM and MFM data encoding/decoding**
- **On chip DMA controller and FIFO buffer (128 bytes)**
- **Multiple sector read/write with implied seek**
- **Automatic bad sector handling**
- **32 and 40-bit ECC programmable polynomials**
- **Supports computer generated ECC polynomials**

## PIN CONFIGURATION




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 27 | NC |
| 2 | A2 | 28 | D2 |
| 3 | A1 | 29 | D3 |
| 4 | BGACKN | 30 | D4 |
| 5 | OWNN | 31 | D5 |
| 6 | RERUNN | 32 | $V_{SS}$ |
| 7 | CSN | 33 | RESN |
| 8 | IACKN | 34 | SECTOR/INDEX |
| 9 | BGN | 35 | SCLK |
| 10 | DDIR | 36 | D6 |
| 11 | LOCAL | 37 | D7 |
| 12 | UAS | 38 | D8 |
| 13 | LAS | 39 | D9 |
| 14 | NC | 40 | NC |
| 15 | EN1 | 41 | D10 |
| 16 | EN0 | 42 | D11 |
| 17 | BRN | 43 | D12 |
| 18 | IRQN | 44 | D13 |
| 19 | TICKLER | 45 | D14 |
| 20 | WRGATE | 46 | D15 |
| 21 | REDAT | 47 | DTACKN |
| 22 | WCLOCK/RCLOCK | 48 | ASN |
| 23 | WRDAT | 49 | LDSN |
| 24 | WRCLK | 50 | UDSN |
| 25 | D0 | 51 | R/WN |
| 26 | D1 | 52 | $V_{CC}$ |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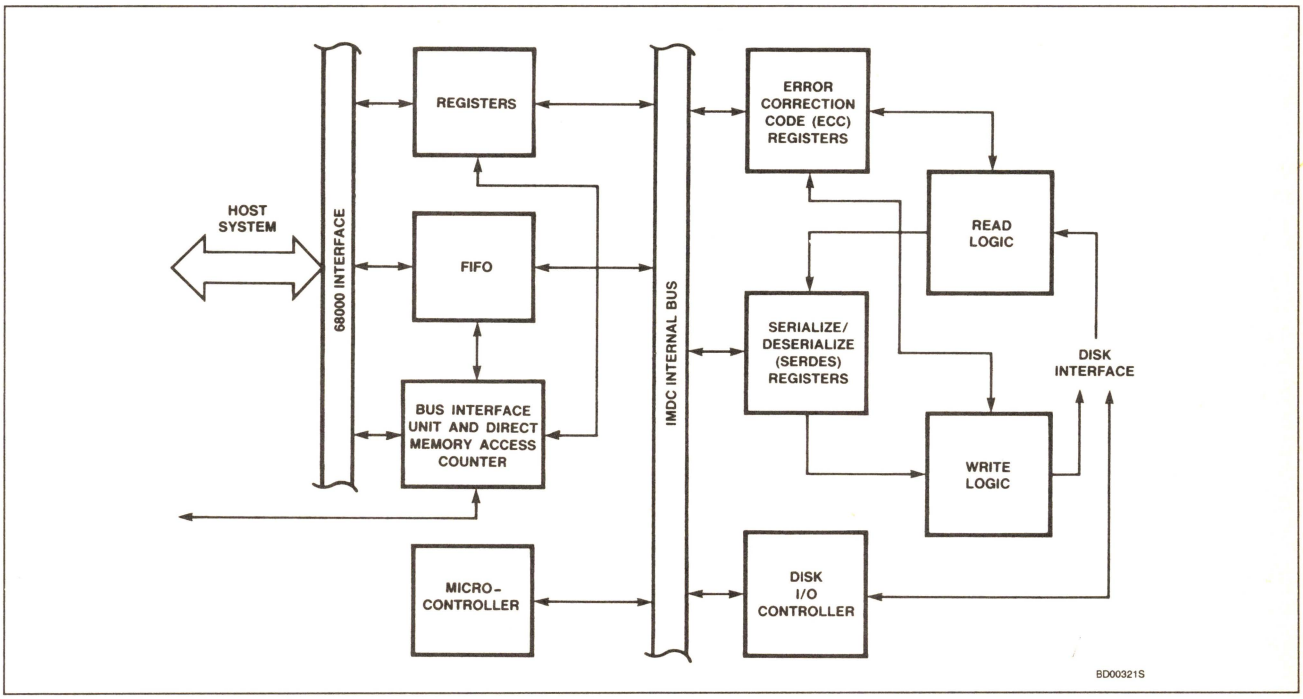
# Intelligent Multiple Disk Controller (IMDC) SCN68454

## ORDERING CODE

| PACKAGES | $V_{CC}$ = 5V ± 5%, $T_A$ = 0 to 70°C |
|---|---|
| Ceramic DIP | SCN68454C6I48 |
| Plastic DIP | SCN68454C6N48 |
| Plastic LCC | SCN68454C6A52 |

## BLOCK DIAGRAM



Signetics

# SCB68459
# Disk Phase-Locked Loop (DPLL)

***Product Specification***

**Microprocessor Products**

## DESCRIPTION

The SCB68459 Disk Phase-Locked Loop (DPLL) is a bipolar device that complements the SCN68454 Intelligent Multiple Disk Controller (IMDC). Together, with an external voltage controlled oscillator (VCO), the DPLL and IMDC provide all the functions required to control up to four disks with SA800, ST500, or SA1000 type interfaces.

The DPLL uses an external VCO for the variable clock rate which tracks the read data from the disk unit. This VCO can be any device that can interface to the DPLL. The IMDC can control up to four disks; if these are all the same, only one DPLL is needed. If different disk types are driven by the same IMDC, then a DPLL is required for each disk drive type.

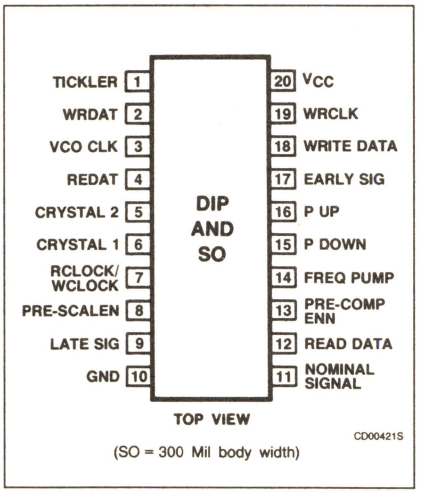
The SCB68459 DPLL operates by producing an oscillator frequency to match the frequency of an input signal. In this locked condition, any slight change in the input frequency (called jitter) will appear as a change in phase between the input frequency and the VCO frequency. This phase shift then acts as an error signal to change the frequency of the local DPLL VCO to match the input frequency.

The SCB68459 is constructed using Signetics extended performance logic (EPL) bipolar technology.

## FEATURES

- **Supports composite data rate of 100kHz to 10MHz**
- **On-chip multiplexer for read and write clock**
- **Supports MFM and FM data formats**
- **Generates synchronous clock for read data**
- **Built-in pre-compensation circuit**
- **Phase detector and frequency detection for improved operation**
- **External loop gain control**
- **Minimal amount of external components required for operation**
- **Single +5V power supply**
- **Crystal-controlled write clock**

## PIN CONFIGURATION

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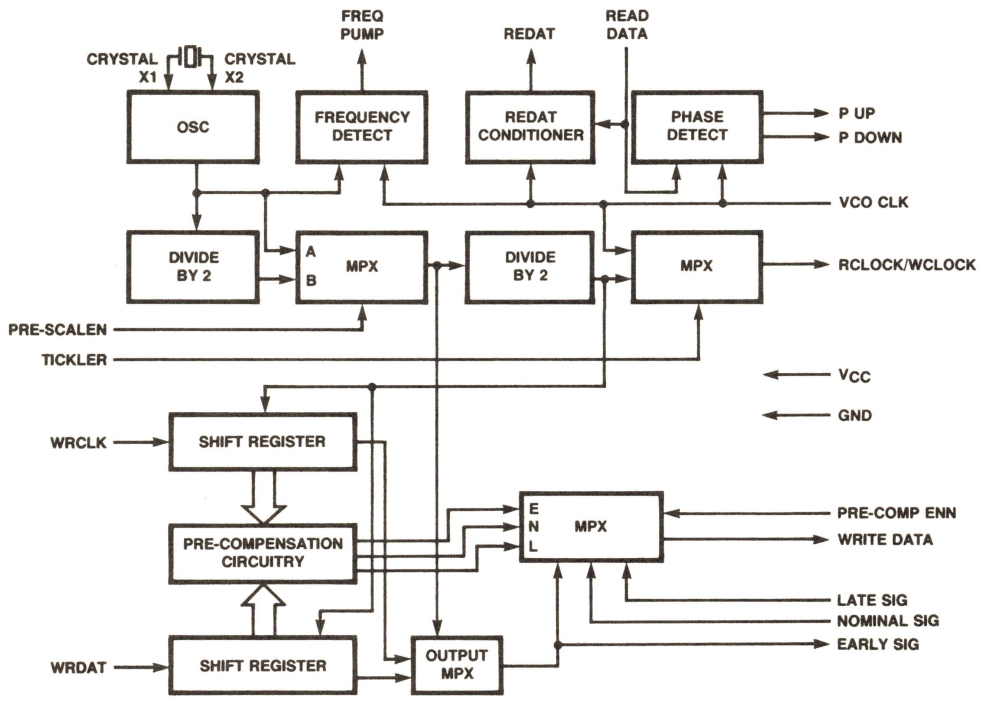
# Disk Phase-Locked Loop (DPLL) SCB68459

## ORDERING CODE

| PACKAGES | $V_{CC}$ = +5V ±5%, $T_A$ = 0 to +70°C |
|---|---|
| Ceramic DIP | SCB68459CAI20 |
| Plastic DIP | SCB68459CAN20 |
| Small Outline | SCB68459CAD20 |

## BLOCK DIAGRAM



Signetics

# SCB68172
# VMEbus Controller (BUSCON)

***Objective Specification***

**Microprocessor Products**

## DESCRIPTION

The Signetics SCB68172 VMEbus Controller (BUSCON) is an interface device for the VMEbus. It can be used in three different configurations: master-only, slave-only, and master/slave. The SCB68172 can be used with a processor-type interface or with a DMA controller-type interface. In all configurations, it handles the VMEbus signaling protocol in compliance with revisions B and C of the VMEbus Specification.

## CONFIGURATION/VERSION

Applications of the BUSCON are identified as follows (see Figures 1 through 4):

| VERSION | APPLICATION |
|---|---|
| PMS | Processor-type master/slave |
| DMAC | DMA controller-type master/slave |
| MS | Either PMS or (DMAC) |
| M | Master-only |
| S | Slave-only |

All of these applications are handled by the SCB68172, with unused pins tied to stated logic levels in some of the applications.

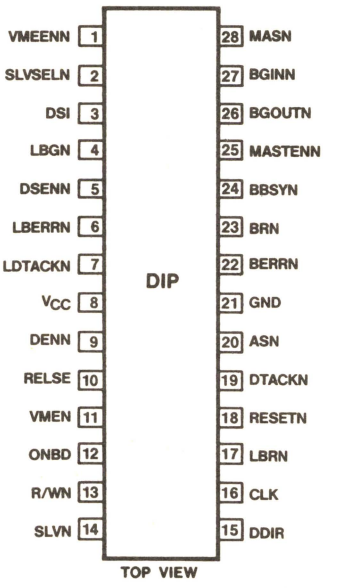
Figure 5 shows a functional model of the SCB68172 logic. The ASN, MASN, LBRN, BGINN, and RELSE inputs are internally synchronized to CLK before being presented to the state machine which determines the major functions of the device. The SLVN, ONBD, and VMEN signals are used directly in the state machine, although they are highly qualified to prevent metastable conditions on the state machine outputs. The BRN, BBSYN and LBGN signals are direct state machine outputs, while ASN, MASTENN, VMEENN, SLVSELN, and BGOUTN are derived from the state machine outputs plus some combinatorial qualification.

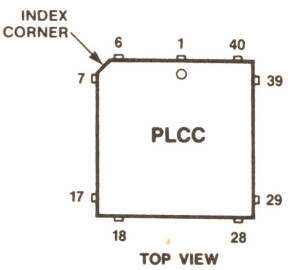
The DSI, R/WN, DTACKN, BERRN, LDTACKN, and LBERRN inputs function largely as direct combinatorial inputs. The DDIR, DTACKN, BERRN, LDTACKN, LBERRN, and (when applicable) MASN outputs are largely derived directly from these direct inputs, with some qualification from the state machine outputs. The DENN and DSENN outputs have complex multi-case logic which uses both the direct inputs and the state machine outputs.

## FEATURES

- **Master, slave, or master/slave (dual ported) applications**
- **Helps assure VMEbus compatibility**
- **Allows for address decoding time**
- **Processor or DMA controller interface for master/requester**
- **Master/requester logic allows release on request (ROR) or release when done (RWD) operation, early or intercycle release**
- **Supports and exploits address lookahead**

## PIN CONFIGURATIONS




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | VMEENN | 24 | DDIR |
| 3 | SLVSELN | 25 | CLK |
| 4 | DSI | 26 | LBRN |
| 5 | LBGN | 27 | RESETN |
| 6 | NC | 28 | NC |
| 7 | NC | 29 | NC |
| 8 | DSENN | 30 | DTACKN |
| 9 | LBERRN | 31 | ASN |
| 10 | NC | 32 | NC |
| 11 | LDTACKN | 33 | GND |
| 12 | NC | 34 | NC |
| 13 | $V_{CC}$ | 35 | BERRN |
| 14 | NC | 36 | NC |
| 15 | DENN | 37 | BRN |
| 16 | RELSE | 38 | BBSYN |
| 17 | NC | 39 | NC |
| 18 | NC | 40 | NC |
| 19 | VMEN | 41 | MASTENN |
| 20 | ONBD | 42 | BGOUTN |
| 21 | R/WN | 43 | BGINN |
| 22 | SLVN | 44 | MASN |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# VMEbus Controller (BUSCON) SCB68172

## ORDERING CODE

| PACKAGES | $V_{CC}$ = 5V± 5%, $T_A$ = 0°C to 70°C |
|---|---|
| CERDIP | SCB68172C2F28 |
| Plastic DIP | SCB68172C2N28 |
| Plastic LCC | SCB68172C2A44 |

## PIN DESCRIPTION

| MNEMONIC | PIN NO. | | TYPE | CONFIG | NAME AND FUNCTION |
|---|---|---|---|---|---|
| | DIP | PLCC | | | |
| CLK | 16 | 25 | I | All | **Clock:** User-supplied clock signal. |
| SLVN | 14 | 22 | I | S,MS | **Slave:** Active-low decode of the VMEbus address and address modifier lines indicating that the current cycle is for this board. SLVN should not be qualified with ASN nor VMEENN. It is first sampled on the rising clock edge after the rising edge on which ASN is first detected. It must remain valid until after the next low-going edge on DTACKN or BERRN. In a master-only application, SLVN should be pulled up to $V_{CC}$. |
| ASN | 20 | 31 | I/O<br>I | M,MS<br>S | **Address Strobe:** Direct connect to VMEbus ASN. |
| VMEN | 11 | 19 | I | M,MS | **VME Decode:** Active-low decode of the master's address lines, indicating that the master's current cycle is for a slave on the VMEbus. VMEN should not be qualified with MASN nor MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until MASN goes false (high). In a slave-only configuration, VMEN should be pulled up to $V_{CC}$. |
| LBRN | 17 | 26 | I | M,MS | **Local Bus Request:** Connected to the low-active bus request output of a DMA controller. Typically tied to a high logic level in processor-type interfaces. |
| ONBD | 12 | 20 | I | MS | **Onboard:** Active-high decode of the master's address lines, indicating that the master's current cycle is for an onboard slave that is dual-ported with the VMEbus. ONBD should not be qualified with MASN or MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until after MASN goes false (high). In a master-only or slave-only application, ONBD should be grounded. If a master/slave configuration does not contain "local slaves" as shown in figure 3, VMEN and ONBD should both be connected to an active-low "VME decode". A cycle between the onboard master and a local slave (VMEN high, ONBD low) is ignored by BUSCON, and can proceed concurrently with a cycle between another VMEbus master and an onboard dual-ported slave. |
| MASN | 28 | 44 | I<br>I/O | M,PMS<br>DMAC | **Master's Address Strobe:** RMW and Sequential VMEbus master cycles are accomplished by holding MASN low across several data strobes. If LBGN is high at the end of the RESETN low time, the state of ASN is driven onto MASN whenever BUSCON does not have control of the VMEbus. In a slave-only application, MASN should be pulled up to $V_{CC}$. |
| MASTENN | 25 | 41 | O | MS | **Master Enable:** In a master/slave application, the low state of this signal enables the master onto the shared bus and enables shared-bus responses back to the master. MASTENN also provides the direction control for the VMEbus address transceivers. |
| VMEENN | 1 | 2 | O | M,MS | **VME Enable:** Active-low enable for the VMEbus address drivers (master-only) or transceivers (master/slave). |
| SLVSELN | 2 | 3 | O | S,MS | **Slave Select:** Active-low select for the onboard slave resources (the shared/dual ported slaves in a master/slave application). Derived from MASN and ONBD, or from ASN and SLVN. If necessary, MASTENN and VMEENN are cycled to provide address setup time before SLVSELN is asserted. |
| BRN | 23 | 37 | O | M,MS | **Bus Request:** Active-low, open collector VMEbus request. Direct connect to the selected level among VMEbus BR0* – BR3*. |
| BGINN | 27 | 43 | I | M,MS | **Bus Grant In:** Direct connect to the selected level among VMEbus BG0IN* – BG3IN*. |



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Signetics

# SCC80C451/SCC83C451
## I/O Expanded CMOS Microcontroller

***Preliminary Specification***

**Products**



### DESCRIPTION

The Signetics SCC80C451/SCC83C451 is an I/O expanded, single-chip microcontroller fabricated with Signetics' high-density epitaxial CMOS technology. It is offered in a 68-pin PLCC and a 64-pin DIP. The Signetics CMOS technology combines the high-speed and high-density characteristics of HMOS with the low power of CMOS. Signetics' epitaxial substrate minimizes latch-up sensitivity.

The SCC80C451/SCC83C451 is a functional extension of the SCC80C31/SCC80C51 microcontroller with three additional I/O ports and four I/O control lines. The PLCC version has a total of 68 pins. The DIP version has a total of 64 pins. The four added control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

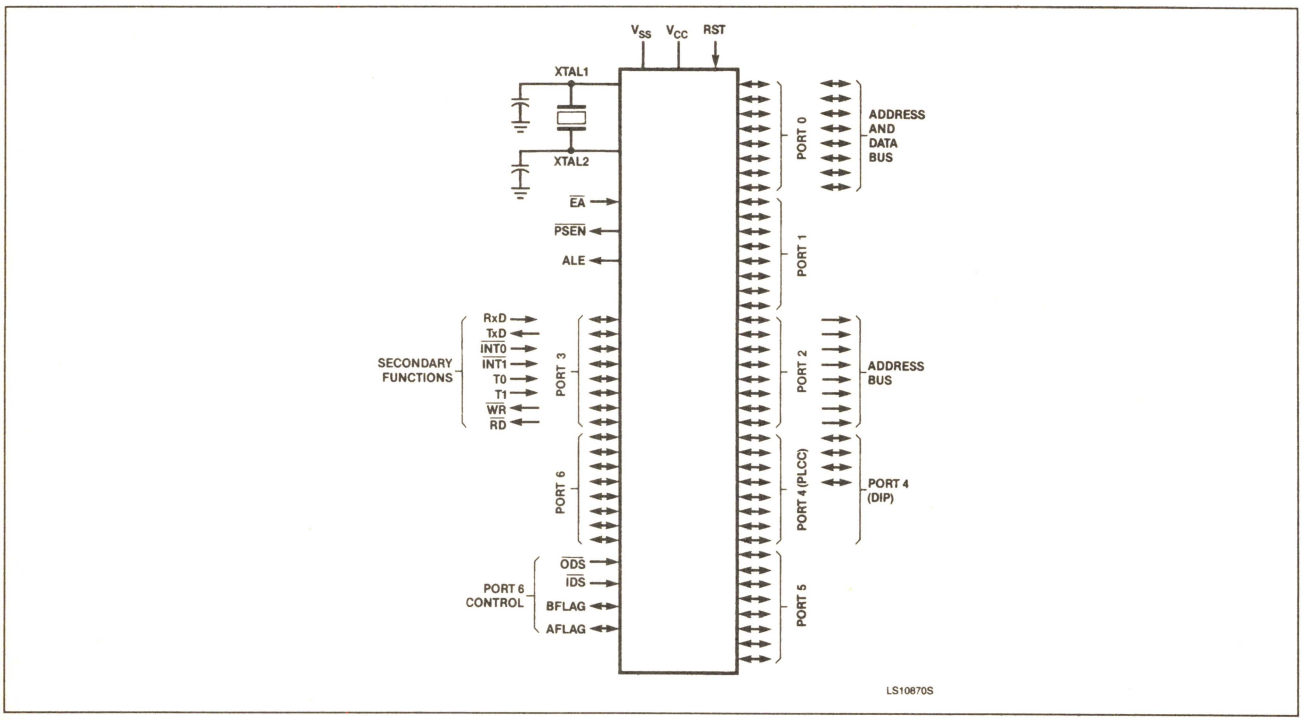
The SCC80C451/SCC83C451 includes a 4k × 8 ROM; a 128 × 8 RAM; 56 (PLCC) or 52 (DIP) I/O lines; two 16-bit timer/counters; a five source, two priority level, nested interrupt structure; a serial I/O port for either a full-duplex UART, I/O expansion, or multiprocessor communications; and on-chip oscillator and clock circuits.

The SCC80C451/SCC83C451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

### FEATURES

- **SCC80C451 — CPU with RAM and I/O**
- **SCC83C451 — 80C451 with mask-programmable ROM**
- **68-pin PLCC and 64-pin DIP packages**
  - **Seven 8-bit I/O ports (PLCC version)**
  - **Six 8-bit ports and one 4-bit port (DIP version)**
- **Port 6 features:**
  - **8 data pins**
  - **4 control pins**
  - **Direct MPU bus interface**
  - **Parallel printer interface**
- **Pin compatible with 87C451 microcontroller**
- **On the microcontroller:**
  - **SCC80C51 CPU**
  - **4k × 8 ROM (SCC83C451 only)**
  - **128 × 8 RAM**
  - **Two 16-bit timer/counters**
  - **Full-duplex serial I/O**
  - **Two external interrupts**
- **External memory addressing capability:**
  - **64k ROM and 64k RAM**
- **Low power consumption:**
  - **Normal operation: 24mA typical @ 5V, 12MHz**
  - **Idle mode: 3mA typical @ 5V, 12MHz**
  - **Power-down mode: 50μA typical @ 2V**

### LOGIC SYMBOL



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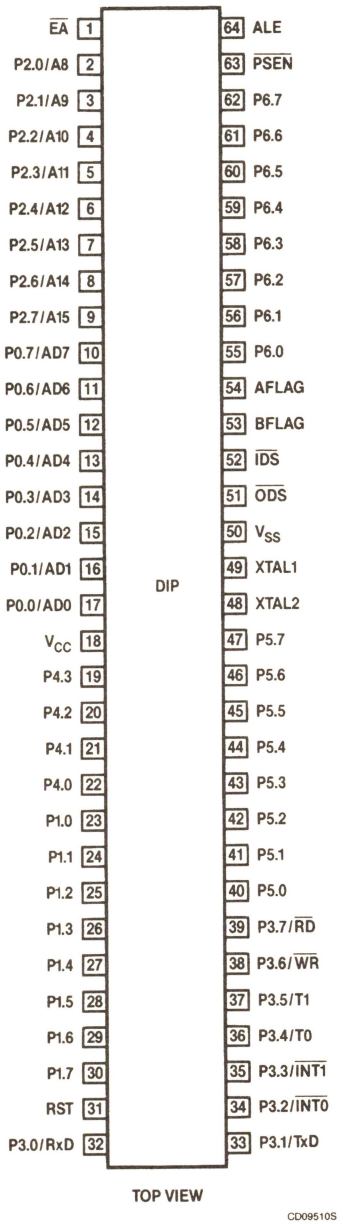
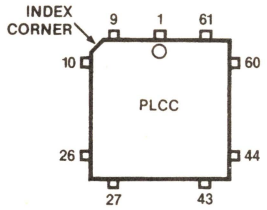
# I/O Expanded CMOS Microcontroller — SCC80C451/SCC83C451

## PIN CONFIGURATION




TOP VIEW

CD09510S




TOP VIEW

CD09520S

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | $\overline{EA}$ | 35 | RST |
| 2 | P2.0/A8 | 36 | P3.0/R × D |
| 3 | P2.1/A9 | 37 | P3.1/T × D |
| 4 | P2.2/A10 | 38 | P3.2/$\overline{INT0}$ |
| 5 | P2.3/A11 | 39 | P3.3/$\overline{INT1}$ |
| 6 | P2.4/A12 | 40 | P3.4/T0 |
| 7 | P2.5/A13 | 41 | P3.5/T1 |
| 8 | P2.6/A14 | 42 | P3.6/$\overline{WR}$ |
| 9 | P2.7/A15 | 43 | P3.7/$\overline{RD}$ |
| 10 | P0.7/AD7 | 44 | P5.0 |
| 11 | P0.6/AD6 | 45 | P5.1 |
| 12 | P0.5/AD5 | 46 | P5.2 |
| 13 | P0.4/AD4 | 47 | P5.3 |
| 14 | P0.3/AD3 | 48 | P5.4 |
| 15 | P0.2/AD2 | 49 | P5.5 |
| 16 | P0.1/AD1 | 50 | P5.6 |
| 17 | P0.0/AD0 | 51 | P5.7 |
| 18 | $V_{CC}$ | 52 | XTAL2 |
| 19 | P4.7 | 53 | XTAL1 |
| 20 | P4.6 | 54 | $V_{SS}$ |
| 21 | P4.5 | 55 | $\overline{ODS}$ |
| 22 | P4.4 | 56 | $\overline{IDS}$ |
| 23 | P4.3 | 57 | BFLAG |
| 24 | P4.2 | 58 | AFLAG |
| 25 | P4.1 | 59 | P6.0 |
| 26 | P4.0 | 60 | P6.1 |
| 27 | P1.0 | 61 | P6.2 |
| 28 | P1.1 | 62 | P6.3 |
| 29 | P1.2 | 63 | P6.4 |
| 30 | P1.3 | 64 | P6.5 |
| 31 | P1.4 | 65 | P6.6 |
| 32 | P1.5 | 66 | P6.7 |
| 33 | P1.6 | 67 | $\overline{PSEN}$ |
| 34 | P1.7 | | |
| 68 | ALE | | |

Signetics

# SC84C00/20/40
## CMOS Single-Chip 8-Bit Microcontroller

*Objective Specification*

**Microprocessor Products**

### DESCRIPTION

The SC 84CXX family are a low cost, reduced pin count, CMOS derivative of the 8048 family. The family consists of three devices of different memory configurations, including the SC 84C00 piggyback EPROM version for prototyping and small runs.

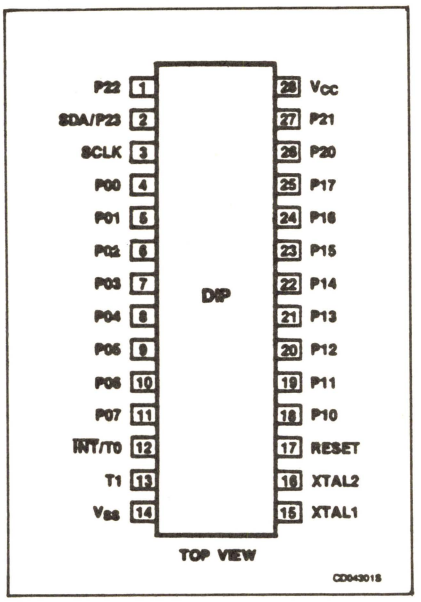
The Inter-Integrated Circuit serial bus interface ($I^2C$ bus) facilitates I/O and Ram expansion; access to EEPROM memory and other dedicated $I^2C$ peripherals, as well as processor to processor communication.

Members of the SC 84CXX family have the following 20 I/O lines: an Inter-Integrated Circuit serial bus interface, ($I^2C$ bus); an 8-bit timer/counter; a three source, single level, fixed priority interrupt structure; and an on chip oscillator.

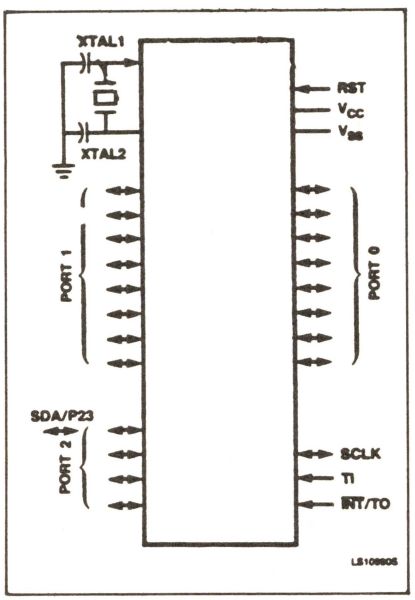
### FEATURES

- Inter-Integrated Circuit ($I^2C$) serial bus interface
- Broad power supply voltage range: 2.5 to 5.5 volts
- Broad oscillator frequency range: .1 to 10MHz
- Low power consumption;
  - Idle mode, Stop mode
- 2K or 4K bytes of ROM plus piggyback EPROM version for prototypes
- 64 or 128 bytes of RAM
- 8-bit counter/timer
- CMOS and TTL compatible
- 20 quasi-bidirectional I/O lines
- Three vectored interrupts
  - external, $I^2C$ counter/timer
- 40 to 85°C temperature range
- Internal power on reset and low voltage detection circuits
- Choice of DIP or SOL packages

### PIN CONFIGURATION




### LOGIC SYMBOL

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# CMOS Single-Chip 8-Bit Microcontroller — SC84C00/20/40

## ORDERING

SC 84C□□ □ □ □ 28 (CPxxxx)

**ROM/RAM (bytes)**
20 = 2K/64
40 = 4K/128
00 = Ext/256

*Blank = POR 1.9VMax
A = 3.5V± .5V

**OPERATING TEMPERATURE RANGE**
C = 0°C to +70°C

**SPEED**
A = 10MHz clock
6 = 16MHz

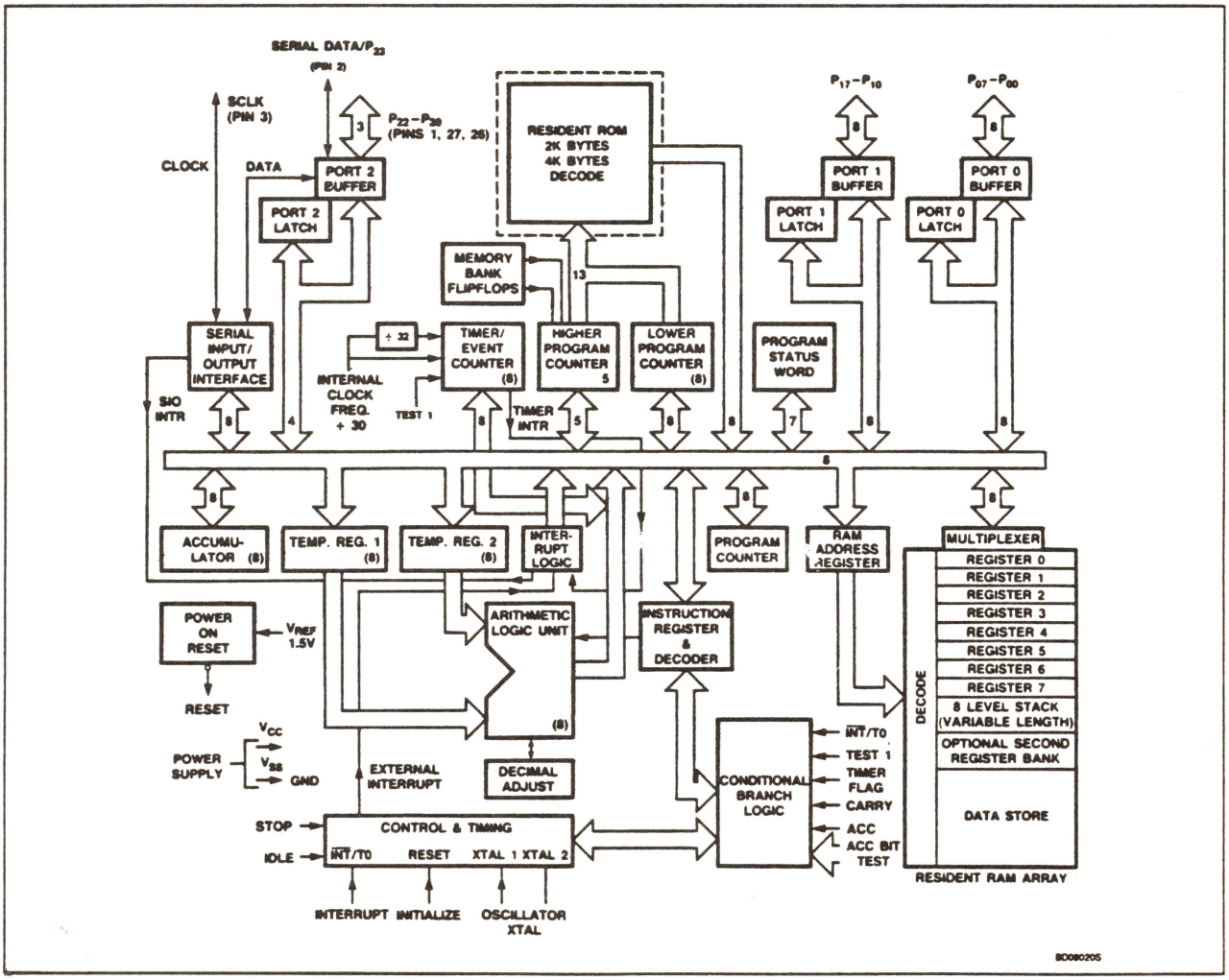
**28-Pin**

**PACKAGE**
N = Plastic DIP
I = Ceramic DIP
D = Plastic SOL

**CUSTOM ROM PATTERN NUMBER**
Applies to masked ROM versions only. Number will be assigned by Signetics. Contact Signetics sales office for ROM pattern submission requirements.

NOTE:
*See DC Electrical Characteristics "RESET"

## BLOCK DIAGRAM




Signetics

# Signetics

# SC80C31B/SC80C51B
## CMOS Single-Chip 8-Bit Microcontroller

***Preliminary Specification***

**Microprocessor Products**



## DESCRIPTION

The Signetics SC80C31B/SC80C51B is a high-performance microcontroller fabricated with Signetics' high-density CMOS technology. The CMOS 80C31/80C51 is functionally compatible with the NMOS 8031/8051 microcontroller. The Signetics CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Signetics' epitaxial substrate minimizes latch-up sensitivity.

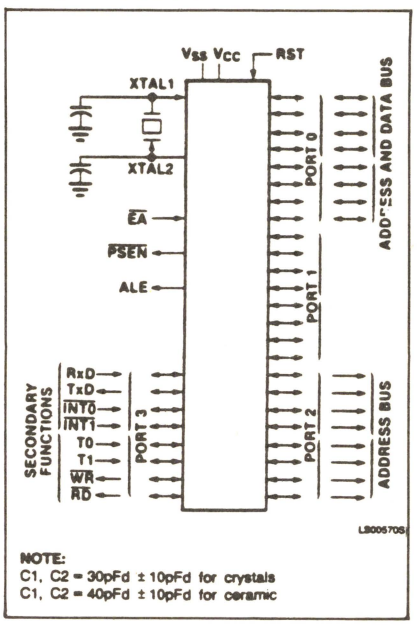
The SC80C31B/SC80C51B contains a 4K × 8 ROM; a 128 × 8 RAM; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion or full duplex UART; and on-chip oscillator and clock circuits. In addition, the SC80C31B/80C51B has two software selectable modes of reduced activity for further power reduction – idle mode and power-down mode.

Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

## FEATURES

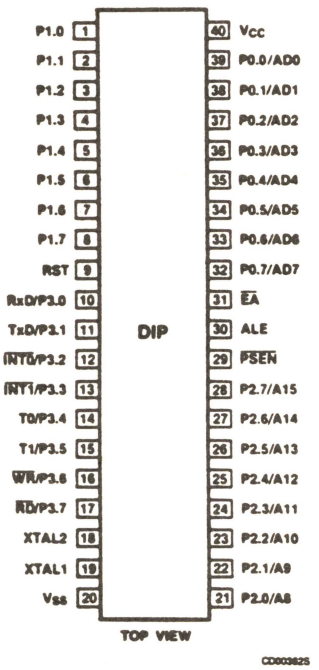
- **SC80C31 microcontroller without ROM**
- **SC80C51 control-oriented microcontroller**
- **SC8031/8051 compatible**
  - **4K × 8 ROM**
  - **128 × 8 RAM**
  - **Two 16-bit timer/counters**
  - **Full duplex serial channel**
  - **Boolean processor**
- **Memory addressing capability**
  - **64K ROM and 64K RAM**
- **Power control modes:**
  - **Idle mode**
  - **Power-down mode**
- **CMOS and TTL compatible**
- **Three speed ranges at $V_{CC}$ = 5V ±20%**
  - **3.5 to 12 MHz**
  - **3.5 to 16 MHz**
  - **.5 to 12 MHz**

## LOGIC SYMBOL

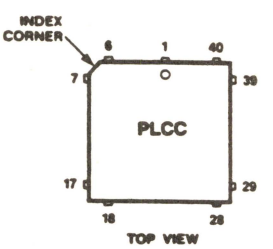



**NOTE:**
C1, C2 = 30pFd ± 10pFd for crystals
C1, C2 = 40pFd ± 10pFd for ceramic

## PIN CONFIGURATIONS




CD00362S




CD0044PS

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | P1.0 | 24 | A8/P2.0 |
| 3 | P1.1 | 25 | A9/P2.1 |
| 4 | P1.2 | 26 | A10/P2.2 |
| 5 | P1.3 | 27 | A11/P2.3 |
| 6 | P1.4 | 28 | A12/P2.4 |
| 7 | P1.5 | 29 | A13/P2.5 |
| 8 | P1.6 | 30 | A14/P2.6 |
| 9 | P1.7 | 31 | A15/P2.7 |
| 10 | RST | 32 | PSEN |
| 11 | RxD/P3.0 | 33 | ALE |
| 12 | NC | 34 | NC |
| 13 | TxD/P3.1 | 35 | EA |
| 14 | $\overline{INT0}$/P3.2 | 36 | P0.7/AD7 |
| 15 | $\overline{INT1}$/P3.3 | 37 | P0.6/AD6 |
| 16 | T0/P3.4 | 38 | P0.5/AD5 |
| 17 | T1/P3.5 | 39 | P0.4/AD4 |
| 18 | $\overline{WR}$/P3.6 | 40 | P0.3/AD3 |
| 19 | $\overline{RD}$/P3.7 | 41 | P0.2/AD2 |
| 20 | XTAL2 | 42 | P0.1/AD1 |
| 21 | XTAL1 | 43 | P0.0/AD0 |
| 22 | $V_{SS}$ | 44 | $V_{CC}$ |



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# CMOS Single-Chip 8-Bit Microcontroller | SC80C31B/SC80C51B

## ORDERING

SC80C□□ B □ □ □ □□ (CPxxxx)

**ROM/RAM (bytes)**
31 = EXT/128
51 = 4K/128

**OPERATING TEMPERATURE RANGE**
A = 40°C to +85°C
C = 0°C to +70°C

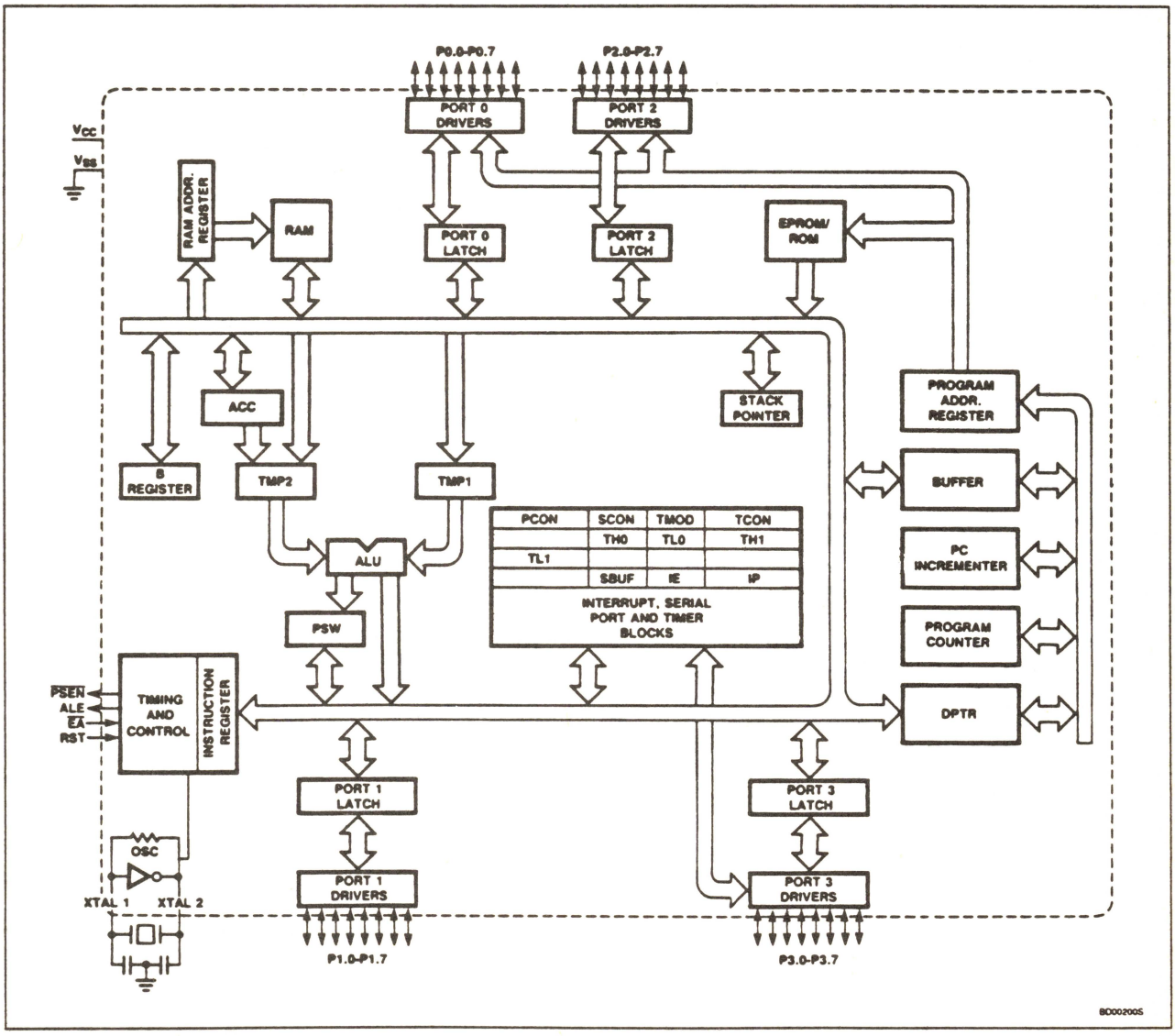
**SPEED**
0 = 3.5 to 12MHz
1 = 3.5 to 16MHz
2 = 0.5 to 12MHz

**CUSTOM ROM PATTERN NUMBER**
Applies to masked ROM versions only. Number will be assigned by Signetics. Contact Signetics sales office for ROM pattern submission requirements.

**40=Pin DIP**
**44=Pin LCC**

**PACKAGE**
N = Plastic DIP
I = Ceramic DIP
A = Plastic LCC

## BLOCK DIAGRAM




Signetics

Signetics

# SCN8032AH, SCN8052AH
## Single-chip 8-Bit Microcontroller

***Preliminary Specification***

**Microprocessor Products**



## DESCRIPTION

The Signetics SCN8032AH/SCN8052AH 8-bit Microcontroller is a high-performance single-chip computer, fabricated with Signetics' highly-reliable +5 volt, depletion-load, N-Channel, silicon-gate MOS technology. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications.

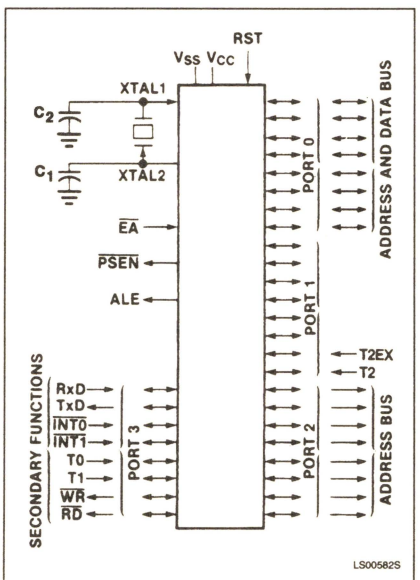
The SCN8032AH contains 256 bytes of read/write data memory; 32 I/O lines configured as four 8-bit ports; three 16-bit timer/counters; a six-source, two-priority level nested interrupt structure; a programmable serial I/O port; and an on-chip oscillator with clock circuitry. The SCN8052AH has all of these features plus 8K bytes of nonvolatile read-only program memory. Both microcontrollers have memory expansion capabilities of up to 64K bytes of data storage and 64K bytes of program memory that may be realized with standard TTL compatible memories.

Because of its' extensive BCD/binary arithmetic and bit-handling facilities, the SCN8032AH/SCN8052AH microcontroller is efficient at both computational and control-oriented tasks. Efficient use of program memory is also achieved by using the familiar compact instruction set of the 8031/8051. Forty-four percent of the instructions are one-byte, 41% two-byte and 15% three-byte. The majority of the instructions execute in just 1.0$\mu$s at 12MHz operation. The longest instructions, multiply and divide, require only 4$\mu$s at 12MHz.

## FEATURES

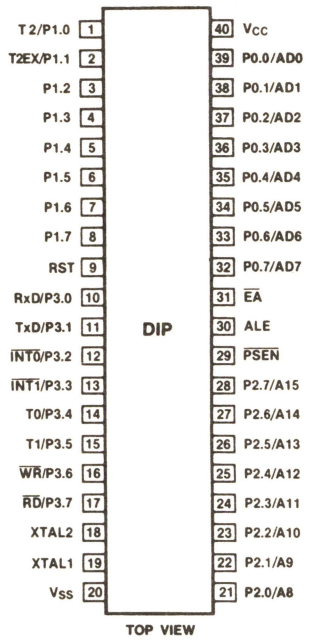
- **SCN8032AH – control-oriented CPU with RAM and I/O**
- **SCN8052AH – an SCN8032AH with factory mask-programmable ROM**
- **8K × 8 ROM (SCN8052AH only)**
- **256 × 8 RAM**
- **32 I/O lines (four 8-bit ports)**
- **Three 16-bit timer/counters**
- **Programmable full-duplex serial channel**
- **Variable transmit/receive baud rate capability**
- **Timer 2 capture capability**
- **128K accessible external memory**
- **Boolean processor**
- **128 user bit-addressable locations**
- **Upward compatible with SCN8031AH/SCN8051AH**

## LOGIC SYMBOL



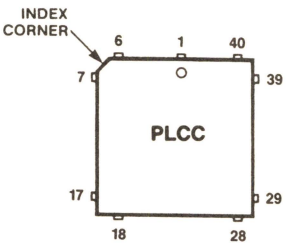

**NOTES:**
C1, C2 = 30 pfd. ±10pfd for crystals
= 40 pfd ±10pfd for ceramic resonators

## PIN CONFIGURATIONS




TOP VIEW

CD00361S




TOP VIEW

CD0044PS

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | T2/P1.0 | 24 | A8/P2.0 |
| 3 | T2EX/P1.1 | 25 | A9/P2.1 |
| 4 | P1.2 | 26 | A10/P2.2 |
| 5 | P1.3 | 27 | A11/P2.3 |
| 6 | P1.4 | 28 | A12/P2.4 |
| 7 | P1.5 | 29 | A13/P2.5 |
| 8 | P1.6 | 30 | A14/P2.6 |
| 9 | P1.7 | 31 | A15/P2.7 |
| 10 | RST | 32 | PSEN |
| 11 | RXD/P3.0 | 33 | ALE |
| 12 | NC | 34 | NC |
| 13 | TXD/P3.1 | 35 | EA |
| 14 | INT0/P3.2 | 36 | AD7/P0.7 |
| 15 | INT1/P3.3 | 37 | AD6/P0.6 |
| 16 | T0/P3.4 | 38 | AD5/P0.5 |
| 17 | T1/P3.5 | 39 | AD4/P0.4 |
| 18 | WR/P3.6 | 40 | AD3/P0.3 |
| 19 | RD/P3.7 | 41 | AD2/P0.2 |
| 20 | XTAL2 | 42 | AD1/P0.1 |
| 21 | XTAL1 | 43 | AD0/P0.0 |
| 22 | VSS | 44 | VCC |



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# Single-chip 8-Bit Microcontroller

# SCN8032AH, SCN8052AH

## ORDERING CODE

**SCN80□□ H □ □ □ □□ (CPxxxx)**

**ROM/RAM (bytes)**
32 = EXT/256
52 = 8K/256

**POWER CONSUMPTION**
H = Reduced Power AH

**OPERATING TEMPERATURE RANGE**
A = −40°C to +85°C
C = 0°C to +70°C

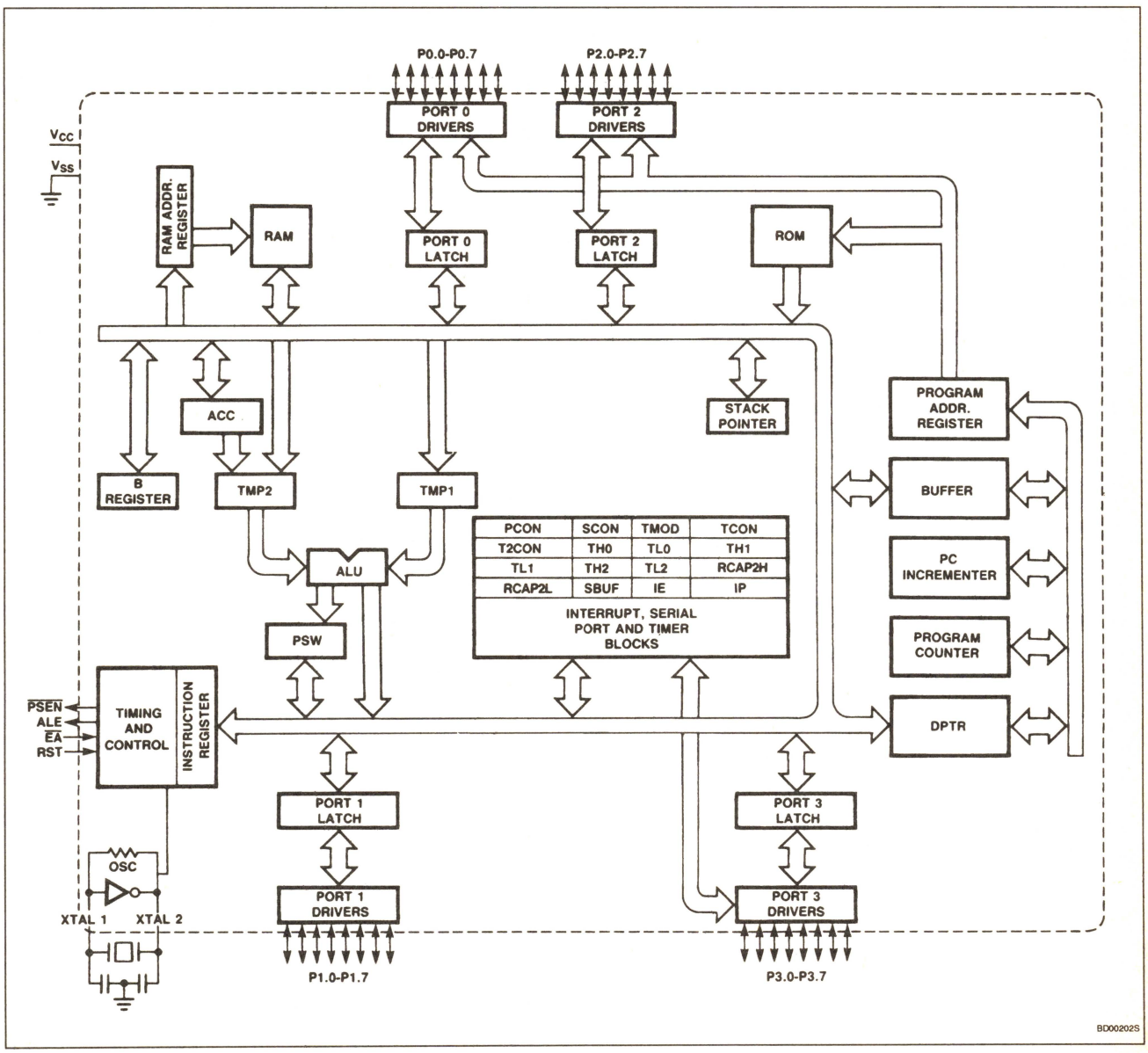
**SPEED**
C = 12MHz clock

**PACKAGE**
N = Plastic DIP
I = Ceramic DIP
A = Plastic LCC

**40 = PIN DIP**
**44 = PIN PLCC**

**CUSTOM ROM PATTERN NUMBER**
Applies to masked ROM versions only. Number will be assigned by Signetics. Contact Signetics sales office for ROM pattern submission requirements.

## BLOCK DIAGRAM



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# Signetics

# SCN8049
# Single-Chip 8-Bit Microcontroller

***Product Specification***

**Microprocessor Products**

## DESCRIPTION

The Signetics SCN80 Series microcontrollers are self-contained, 8-bit processors which contain the system timing, control logic, RAM data memory, ROM program memory (8048/49/50 only), and I/O lines necessary to implement dedicated control functions. All SCN80 Series devices are pin and program compatible, differing only in the size of the on-board program ROM and data RAM, as follows:

| TYPE | RAM SIZE | ROM SIZE |
|---|---|---|
| SCN8049 | 128 × 8 | 2K × 8 |
| SCN8050 | 256 × 8 | 4K × 8 |
| SCN8039 | 128 × 8 | — |
| SCN8040 | 256 × 8 | — |

Program memory can be expanded externally up to a maximum total of 4K bytes without paging. Data memory can also be expanded externally. I/O capabilities can be expanded using standard devices or the 8243 I/O expander.

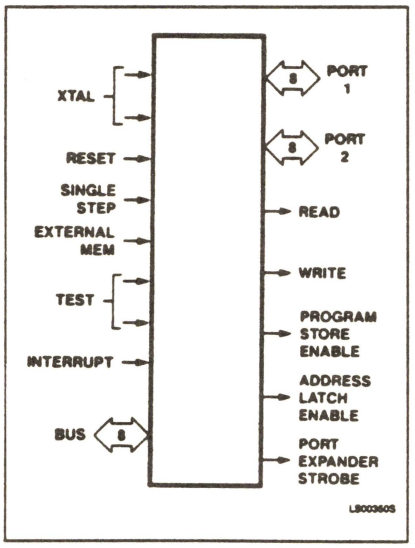
The SCN80 Series processors are designed to be efficient control processors as well as arithmetic processors. They provide an instruction set which allows the user to directly set and reset individual lines within its I/O ports as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions make these processors very efficient in implementing standard logic functions. Also, special attention has been given to code efficiency. Over 70% of the instructions are a single byte long and all others are only 2 bytes long.

An on-chip 8-bit counter is provided which can count, under program control, either internal clock pulses (with a divide by 32 prescaler) or external events. The counter can be programmed to cause an interrupt on terminal count.

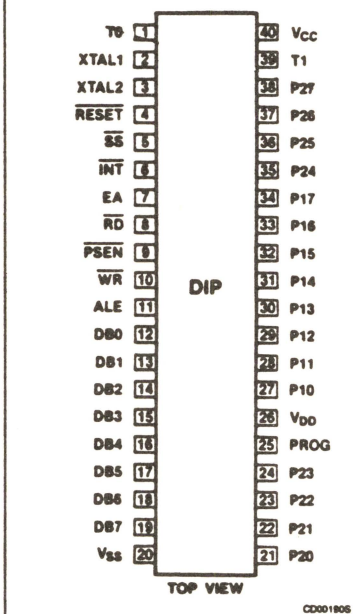
## FEATURES

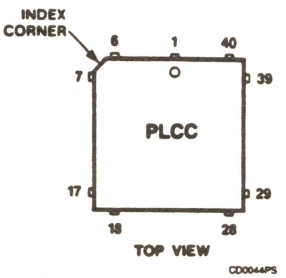
- **8-bit CPU, ROM, RAM, I/O in a 40-pin package**
- **24 quasi bidirectional I/O lines**
- **Two test inputs**
- **Internal counter/timer**
- **Single-level vectored interrupts: external, counter/timer**
- **Over 90 instructions, 70% single byte**
- **1.36μs or 2.5μs instruction cycle, all instructions one or two cycles**
- **Expandable memory and I/O**
- **Low voltage standby**
- **TTL compatible inputs and outputs**
- **Single +5V power supply**

## LOGIC SYMBOL




## PIN CONFIGURATIONS




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | T0 | 24 | P20 |
| 3 | XTAL1 | 25 | P21 |
| 4 | XTAL2 | 26 | P22 |
| 5 | $\overline{\text{RESET}}$ | 27 | P23 |
| 6 | $\overline{\text{SS}}$ | 28 | PROG |
| 7 | $\overline{\text{INT}}$ | 29 | $V_{DD}$ |
| 8 | EA | 30 | P10 |
| 9 | $\overline{\text{RD}}$ | 31 | P11 |
| 10 | $\overline{\text{PSEN}}$ | 32 | P12 |
| 11 | $\overline{\text{WR}}$ | 33 | P13 |
| 12 | NC | 34 | NC |
| 13 | ALE | 35 | P14 |
| 14 | DB0 | 36 | P15 |
| 15 | DB1 | 37 | P16 |
| 16 | DB2 | 38 | P17 |
| 17 | DB3 | 39 | P24 |
| 18 | DB4 | 40 | P25 |
| 19 | DB5 | 41 | P26 |
| 20 | DB6 | 42 | P27 |
| 21 | DB7 | 43 | T1 |
| 22 | $V_{SS}$ | 44 | $V_{CC}$ |





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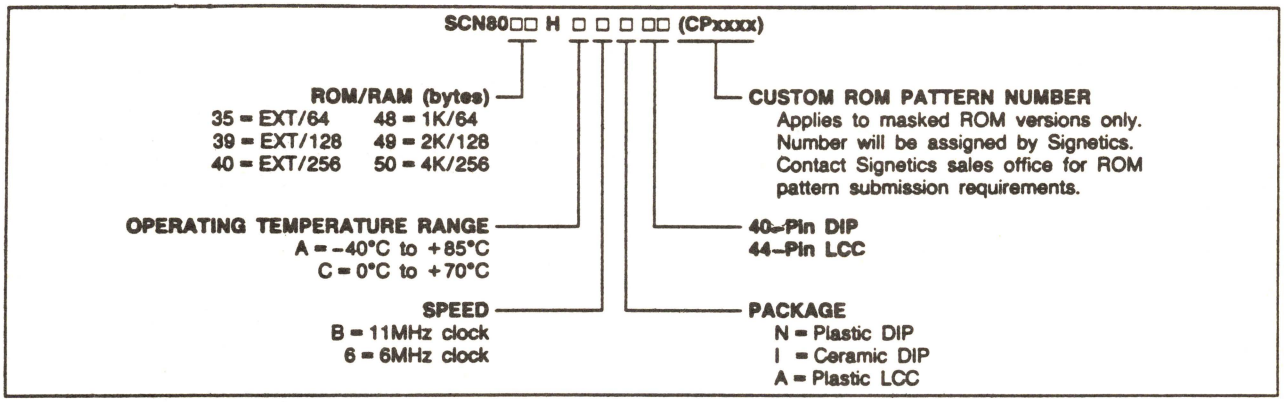
# Single-Chip 8-Bit Microcontroller — SCN8049

## ORDERING




## PIN DESCRIPTION

| MNEMONIC | PIN NO. DIP | PIN NO. PLCC | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| $V_{SS}$ | 20 | 22 | | Circuit ground potential. |
| $V_{DD}$ | 26 | 29 | | Low power standby. |
| $V_{CC}$ | 40 | 44 | | **Main Power Supply:** +5V during operation. |
| PROG | 25 | 28 | O | Output strobe for 8243 I/O expander. |
| P10 – P17 | 27 – 34 | 30 – 33, 35 – 38 | I/O | **Port 1:** 8-bit quasi-bidirectional port. |
| P20 – P27 | 21 – 24, 35 – 38 | 24 – 27, 39 – 42 | I/O | **Port 2:** 8-bit quasi-bidirectional port. P20-23 contain the four high-order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243. |
| DB0 – DB7 | 12 – 19 | 14 – 21 | I/O | **Data Bus:** True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the eight low-order program counter bits during an external program memory fetch and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ and $\overline{WR}$. |
| T0 | 1 | 2 | I | Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 and be designated as a clock output using the ENT0 CLK instruction. |
| T1 | 39 | 43 | I | Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction. |
| XTAL1 | 2 | 3 | I | **Crystal 1:** One side of the crystal input for internal oscillator. Also input for external source (non-TTL $V_{IH}$). |
| XTAL2 | 3 | 4 | I | **Crystal 2:** Other side of crystal input. |
| $\overline{INT}$ | 6 | 7 | I | **Interrupt:** Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. Interrupt must remain low for at least three machine cycles for proper operation. |
| $\overline{RESET}$ | 4 | 5 | I | **Reset:** Used to initialize the microcomputer. Active low. Internal pullup ~75KΩ. During program verification the address is latched by a "0" to "1" transition on $\overline{RESET}$ and the data at the addressed location is output on BUS. |
| $\overline{RD}$ | 8 | 9 | O | **Read:** Output strobe activated during a bus read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. |
| $\overline{WR}$ | 10 | 11 | O | **Write:** Output strobe during a bus write. Used as write strobe to external data memory. |
| ALE | 11 | 13 | O | **Address Latch Enable:** Occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory. |
| $\overline{PSEN}$ | 9 | 10 | O | **Program Store Enable:** Output occurs only during a fetch to external program memory. |
| $\overline{SS}$ | 5 | 6 | I | **Single Step:** Can be used in conjunction with ALE to "single step" the processor through each instruction. |
| EA | 7 | 8 | I | **External Access:** Forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. |

**NOTE:**
Each pin on these ports can be assigned, under program control, to be an input or an output. A pin is designated as an input by writing a logic "1" to the pin. $\overline{RESET}$ sets all pins to the input mode. Each pin has an internal pullup of approximately 50kΩ.



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# 8X401
# Microcontroller

***Product Specification***

**Microprocessor Products**

## DESCRIPTION

The Signetics 8X401 Microcontroller is a very high-speed bipolar microprocessor implemented with internal ECL technology. The 8X401 Microcontroller combines speed, flexibility, and a bit-oriented instruction set to accommodate many sophisticated applications. It excels in systems that require high-speed bit or byte manipulations, such as high-speed controllers and data communications.

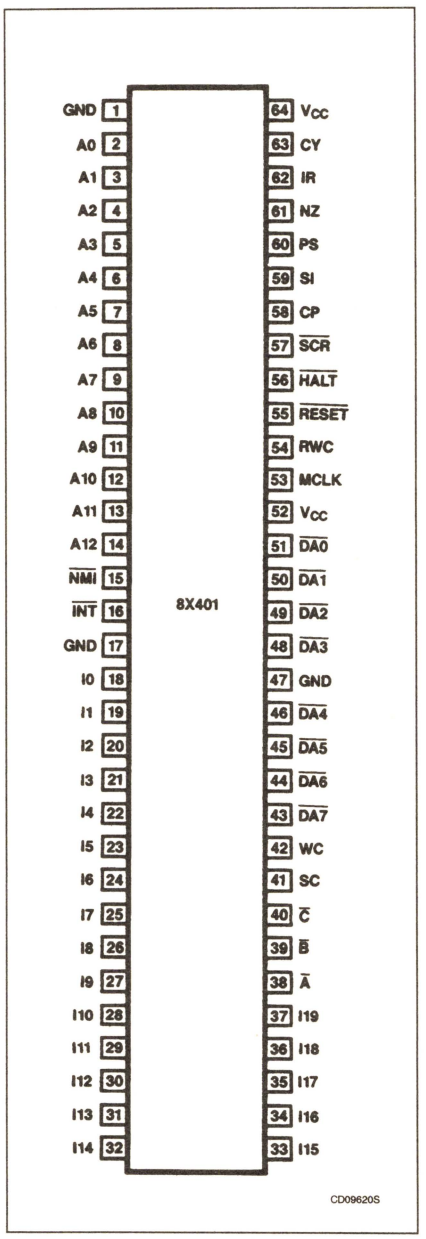
The 8X401 can fetch, execute, and generate the next instruction address for a 20-bit instruction in a minimum of 150ns. Within one instruction cycle, the 8X401 can be programmed to input, right-rotate and mask single or multiple bit subfields, perform an ALU operation, left-rotate, merge the subfield into the destination, and output.

To interface with program memory, the 8X401 uses a 13-bit address bus and a 20-bit instruction bus. An 8-bit bidirectional data/address bus, and an I/O control and timing bus is used to access external peripheral devices.

## FEATURES

- **Fetches and executes all instructions in a minimum of 150ns**
- **Bit manipulation-oriented instruction set**
- **Separate buses for instruction, instruction address and I/O**
- **Sixteen 8-bit registers**
- **On-chip interrupt control**
- **TTL compatible I/O**
- **Single +5V supply**
- **0.9-inch 64-pin DIP, 68-pin plastic leaded chip carrier**
- **Two user-definable status flags**
- **Single TTL clock input**
- **Three independent I/O banks**
- **On-board control sequencer**
- **On-chip subroutine capabilities**
- **Fixed instruction set — 32 instructions**
- **Complete development support**

## PIN CONFIGURATION




## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| 64-pin CERAMIC DIP 900 Mil Wide | N8X401I |

Signetics

853-0843 83744



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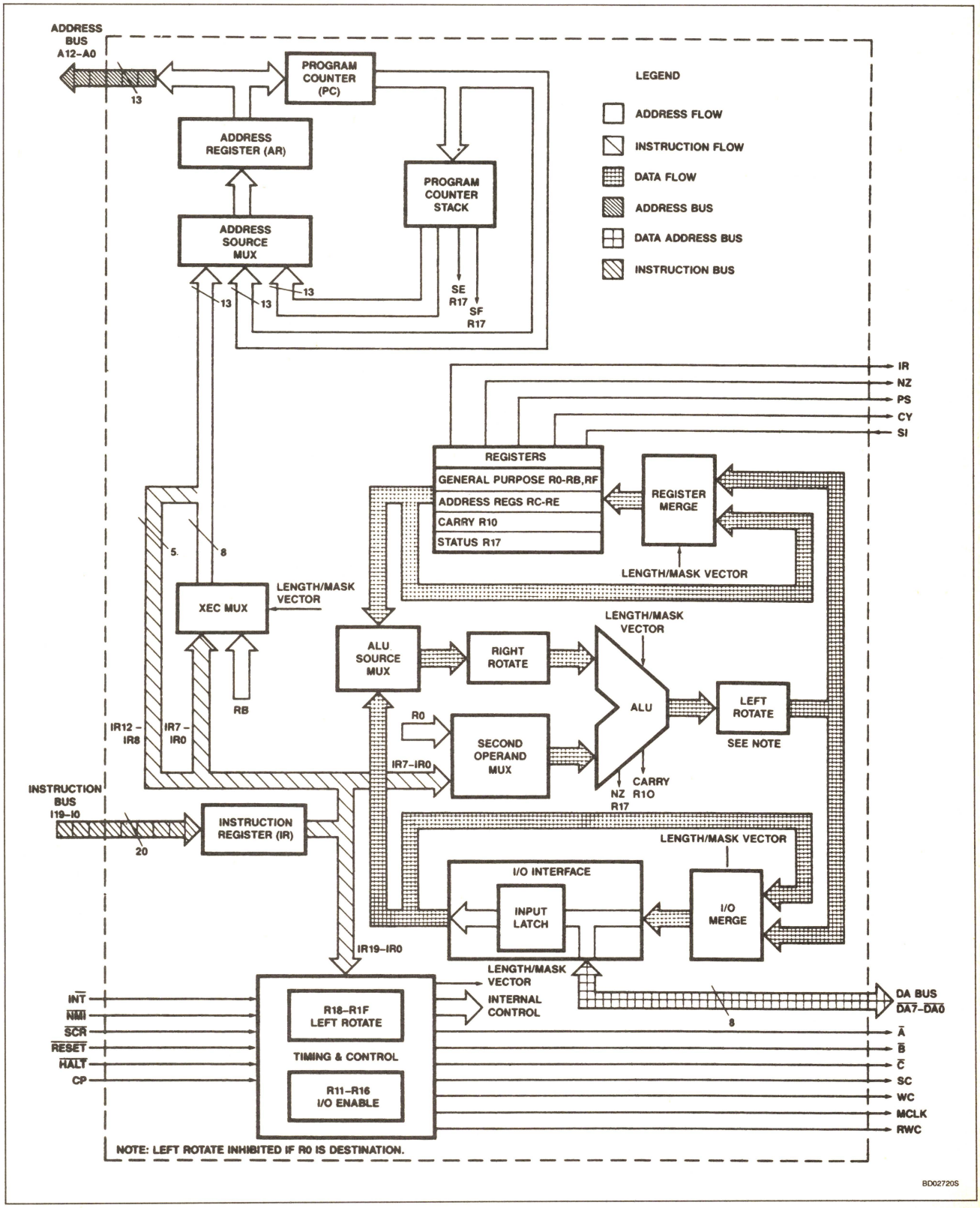
## BLOCK DIAGRAM OF THE 8X401




Signetics

Signetics

# 8X450
# RAM

***Product Specification***

**Microprocessor Products**

## DESCRIPTION

The 8X450 is a 256-byte RAM designed primarily as a working storage element for 8X305 based systems. The 8X450 can be used as a dedicated RAM or in groups of RAMs to form a customized memory stack.

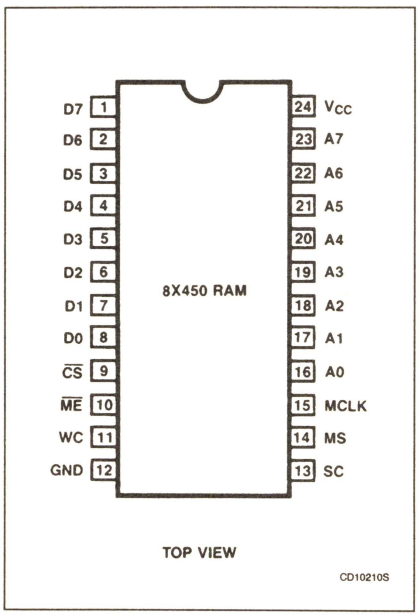
## FEATURES

- **256-byte RAM**
- **Two modes of operation**
- **Paged RAM capability**
- **On-chip address latches**
- **Directly bus compatible with the 8X305 microcontroller**
- **24-pin slim line package**
- **Single + 5-volt supply**

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| 24-Pin Ceramic DIP 400 Mil Wide | N8X450I |

## PIN CONFIGURATION

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## FUNCTIONAL OPERATION

The 8X450 can be used in either of two operating modes — conventional DA select or fast select. Each mode supports either single or multiple RAM applications. The mode of operation is selected by the MS pin.

### Conventional $\overline{DA}$ Select (MS = 1)

When MS is tied high, the conventional $\overline{DA}$ addressing mode is selected; in this mode, the 8X450 data and address lines are tied together. For applications that use a single RAM, the chip select ($\overline{CS}$) input is grounded. To prevent bus contention in applications that use multiple RAMs, the $\overline{CS}$ input is driven by an external source. Examples of both configurations (single and multiple RAMs) are shown in the Application Diagrams at the rear of this data sheet. Control signals and operating conditions for conventional $\overline{DA}$ addressing are summarized in Table 1.

### Fast Select Operations (MS = 0)

When MS is tied low, the fast select addressing mode is invoked; in this mode, the 8X450 address lines are driven by an external source and the 8X450 data lines are tied to the 8X305 $\overline{IV}$ bus. The $\overline{CS}$ input is treated exactly the same as in conventional $\overline{DA}$ addressing; examples of single and multiple RAM configurations are shown at the rear of this data sheet. Control signals and operating conditions for fast select addressing are summarized in Table 2.

## PIN CONFIGURATION AND DECRIPTIONS

| PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|
| 1 – 8 | D7 – D0 | Bidirectional data bus, D0 is LSB |
| 9 | $\overline{CS}$ | Chip Select, active low |
| 10 | $\overline{ME}$ | Master Enable, active low |
| 11 | WC | Write Control, active high |
| 12 | GND | Ground |
| 13 | SC | Select Control, active high |
| 14 | MS | Mode Select |
| 15 | MCLK | Master Clock, active high |
| 16 – 23 | A0 – A7 | Address lines, A0 is LSB |
| 24 | $V_{CC}$ | Power supply |

**Table 1. Conventional $\overline{DA}$ Select (MS = 1)**

| SC | WC | $\overline{ME}$ | MCLK | FUNCTION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Read from RAM |
| 0 | 0 | 1 | X | None |
| 0 | 1 | 0 | 1 | Write data to RAM |
| 0 | 1 | 1 | 1 | None |
| 1 | 0 | 0 | 1 | Conventional $\overline{DA}$ select (write address to RAM) |
| 1 | 0 | 1 | 1 | None |

**NOTES:**
1. Other states are not generated by the 8X305 and are not defined for operation in this mode.
2. Table 1 is valid only if the chip select ($\overline{CS}$) is low; if $\overline{CS}$ is high, the 8X450 is disabled.

**Table 2. Fast Select (MS = 0)**

| SC | WC | $\overline{ME}$ | MCLK | FUNCTION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Read from RAM |
| 0 | 0 | 1 | 0 | None |
| X | X | 1 | 1 | Write address to RAM |
| 0 | 1 | 0 | 1 | Write data to RAM |

**NOTES:**
1. Other states are not generated by the 8X305 and are not defined for operation in this mode.
2. Table 2 is valid only if the chip select ($\overline{CS}$) is low. If $\overline{CS}$ is high, the 8X450 is disabled.

Signetics

# 8X470
# I/O Port

***Product Specification***

**Microprocessor Products**

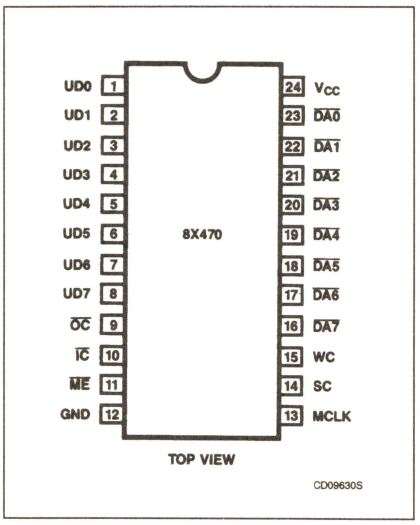
## DESCRIPTION

The 8X470 I/O Port (Figure 1) is a fuse-programmable device designed to interface a user system with a Signetics 8X401 Microcontroller. The 8X470 has three internal registers — a data register and two status registers. The data register is shared between the two systems, while each system has its own dedicated status register. The 8X470 can be programmed to provide a bidirectional or unidirectional user interface with the user data entry being either synchronous or asynchronous with the 8X401.

## FEATURES

- **Two independent 8-bit busses**
- **Fast polling**
- **Directly bus-compatible with the 8X401, 8X305 Microcontrollers**
- **256 Data Addresses**
- **Separate Controller and User status registers**
- **16 Status Addresses**
- **Positionable Controller Status Register output**
- **Bidirectional or unidirectional I/O capability**
- **Synchronous or asynchronous user data entry**
- **Conventional $\overline{DA}$ or Fast select addressing techniques**
- **24-pin slimline package**
- **Single +5V supply**

## PIN CONFIGURATION

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# I/O Port

# 8X470

## PIN DESCRIPTION

| PIN | IDENTIFIER | FUNCTION |
|---|---|---|
| 1 – 8 | UD0 – UD7 | User port data lines. Active high. |
| 9 | $\overline{OC}$ | **Output Control:** An active low signal which controls reading into the I/O port from the UD bus. |
| 10 | $\overline{IC}$ | **Input Control:** An active low signal which controls writing into the I/O port from the UD bus. |
| 11 | $\overline{ME}$ | **Master Enable:** The $\overline{ME}$ pin depends upon the addressing mode for its function.<br>Conventional $\overline{DA}$ select: $\overline{ME}$ is an active low signal which allows read or write or address operations from the $\overline{DA}$ bus.<br>Fast select: $\overline{ME}$ is an active high signal which allows the controller status register to be read on the $\overline{DA}$ bus. |
| 12 | GND | **Ground.** |
| 13 | MCLK | **Master Clock:** Input from the 8X401. |
| 14 | SC | **Select Command:** The SC pin depends upon the addressing mode for its function.<br>Conventional $\overline{DA}$ select: An active high signal which compares the 8X401 $\overline{DA}$ bus and the address. An address match selects the 8X470.<br>Fast select: SC is an active high signal which outputs the contents of the data register on the $\overline{DA}$ bus while clearing the control status register. |
| 15 | WC | **Write Command:** An active high signal which controls the writing of data into the I/O port from the 8X401 $\overline{DA}$ bus. |
| 16 – 23 | $\overline{DA7}$ – $\overline{DA0}$ | Controller Data/Address ($\overline{DA}$) lines. Active low. |
| 24 | $V_{CC}$ | +5V power supply. |

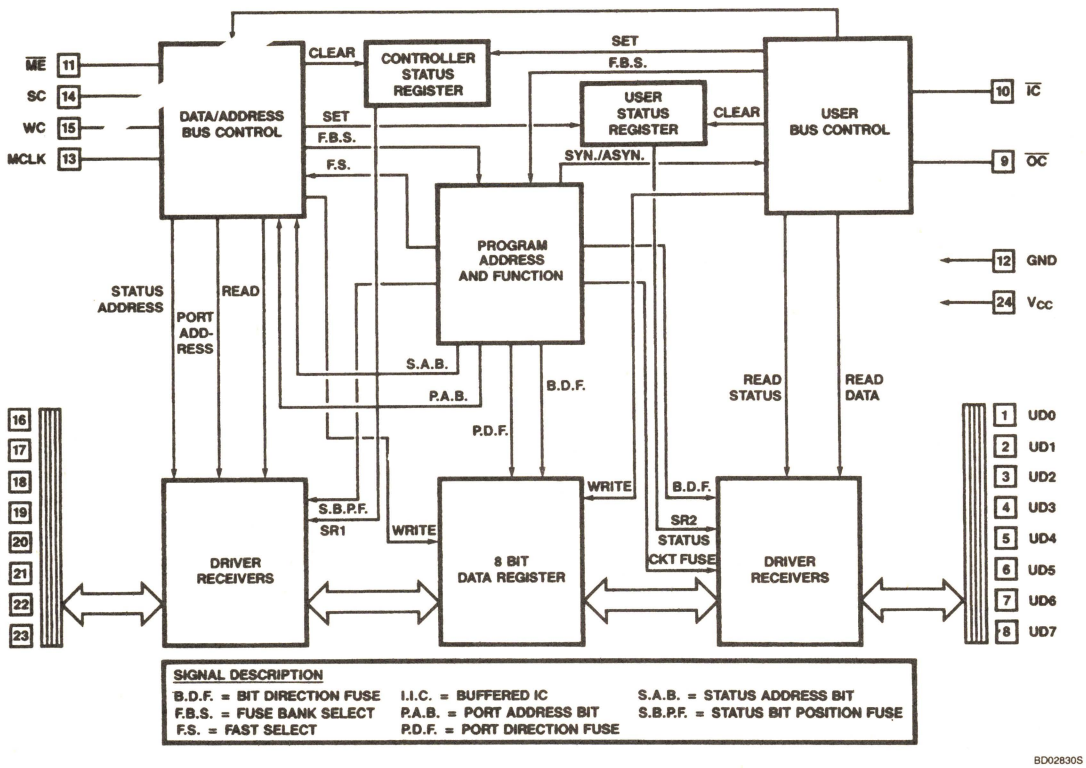


**Figure 1 8x470 Block Diagram**

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Products

# 2960
# Error Detection and Correction (EDC) Unit

***Product Specification***

## FEATURES

- **Boosts Memory Reliability — Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold.**
- **Very High Speed — Perfect for MOS microprocessor, minicomputer and mainframe systems.**
  - **Data In to error detect: 32ns worst case.**
  - **Data In to corrected data out: 65ns worst case.**
- **High-performance systems can use the Signetics EDC in the check-only mode to avoid memory system slowdown.**
- **Replaces 25 to 50 MSI chips — All necessary features are built-in to the Signetics 2960, including diagnostics, data in, data out and check bit latches.**
- **Handles Data Words From 8 to 64 Bits — The Signetics 2960 is cascadable: 1 EDC for 8 or 16 bits, 2 for 32 bits, 4 for 64 bits.**
- **Easy Byte Operations — Separate byte enables on the data out latch simplify the steps and cuts the time required by byte writes.**
- **Built-In Diagnostics — The processor may completely exercise the EDC under software control to check for proper operation.**

## DESCRIPTION

The Signetics 2960 Error Detection and Correction Unit (EDC) (Figure 1) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the EDC will correct any single-bit error and will detect all double- and some triple-bit errors. For 16-bit words, 6 check bits are used. The 2960 can be expanded to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Signetics 2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions.

The product is supplied in a 48-lead hermetic DIP package and a 48-pin plastic package.

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## BLOCK DIAGRAM

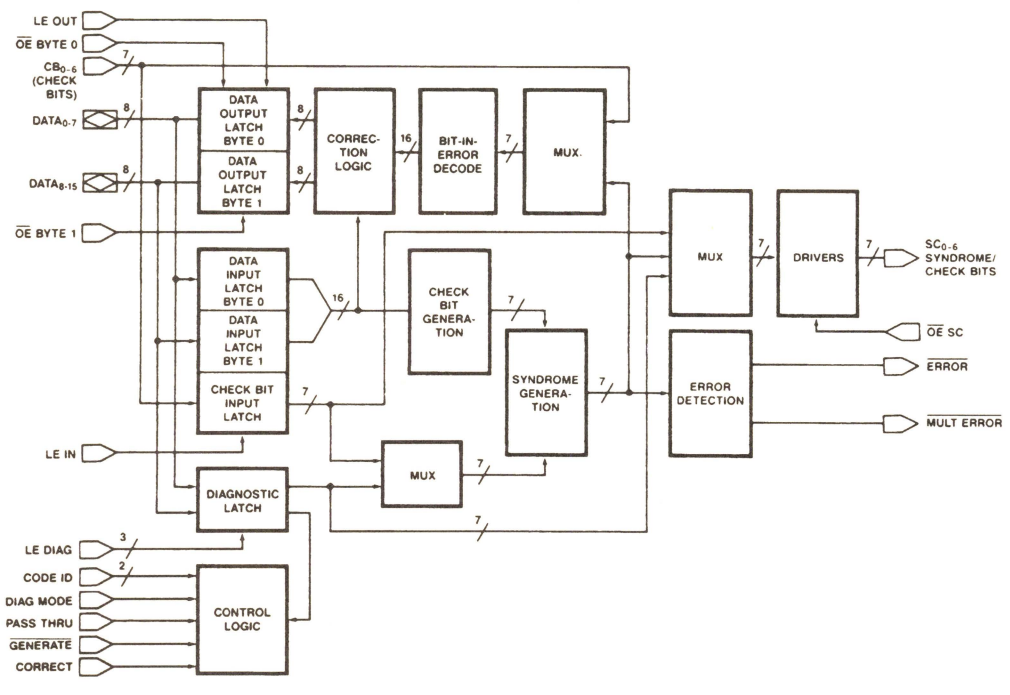


**Figure 1**

853-0065 82174

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# NE5205
# Wideband High Frequency Amplifier

***Product Specification***

**Linear Products**

## DESCRIPTION

The NE5205 is a High Frequency Amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz. This performance makes the amplifier ideal for cable TV applications. The NE5205 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE5205 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 600MHz operating range.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 650MHz. The metal can is hermetically sealed, and can operate over the full −55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE5205s in series as required, without any degradation in amplifier stability.

## FEATURES

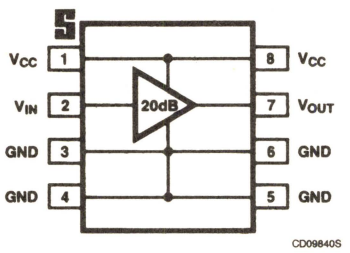
- **650MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface Mount package available**
- **Excellent performance in cable TV 75Ω systems**

## APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **CB radio**
- **Telecommunications**

## PIN CONFIGURATIONS

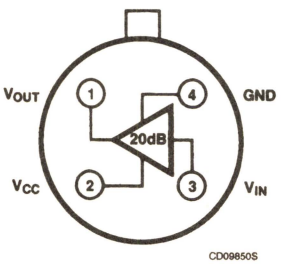
**N, FE, D Packages**




TOP VIEW

NOTE:
Signetics designates Pin 1.

**EC Package**




NOTE:
Tab denotes Pin 1.

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# SE/NE5539
## Ultra-High Frequency Operational Amplifier

**Linear Products**

### DESCRIPTION

The Signetics SE/NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

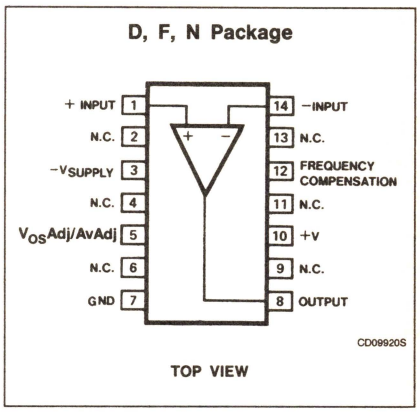
### FEATURES

- **Gain bandwidth product: 1.2GHz at 17dB**
- **Slew rate: 600/V$\mu$s**
- **Full power response: 48MHz**
- **$A_{VOL}$: 52dB typical**
- **350MHz unity gain**

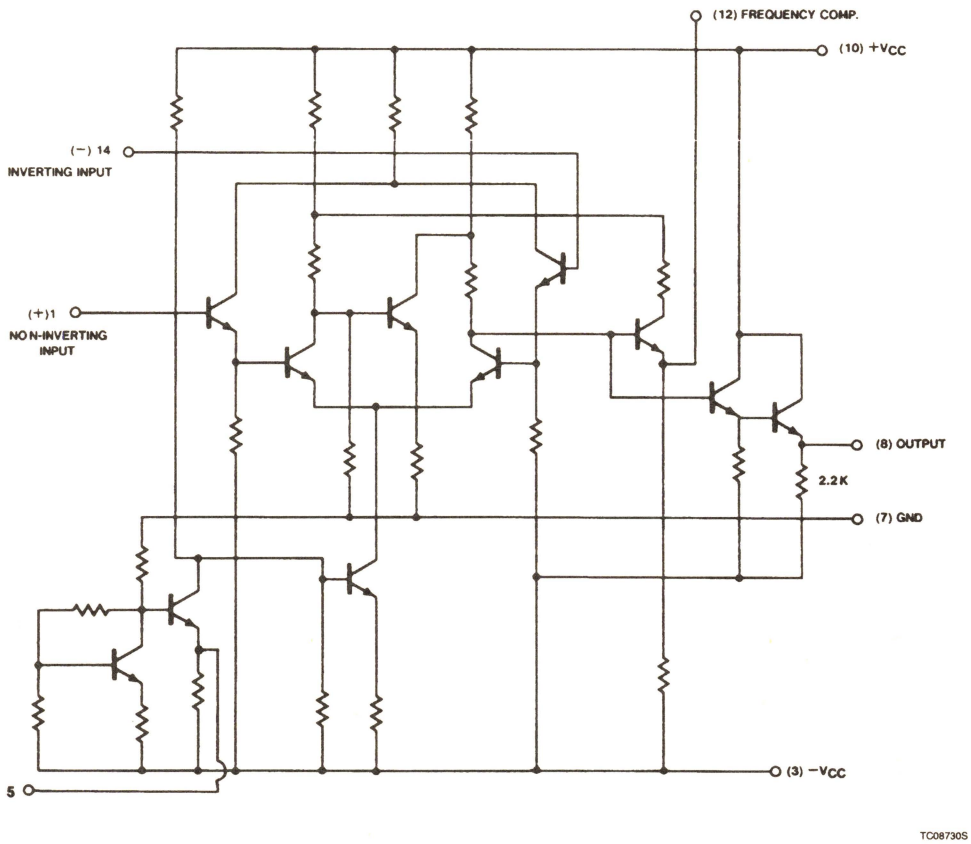
### APPLICATIONS

- **Switch mode power supplies**
- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

### PIN CONFIGURATION




### EQUIVALENT CIRCUIT

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# NE5592
## Video Amplifier

**Linear Products**

### DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

### FEATURES

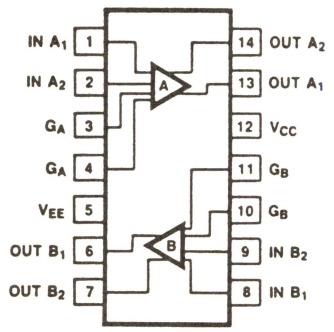
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

### APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

### PIN CONFIGURATION

**D, N Package**

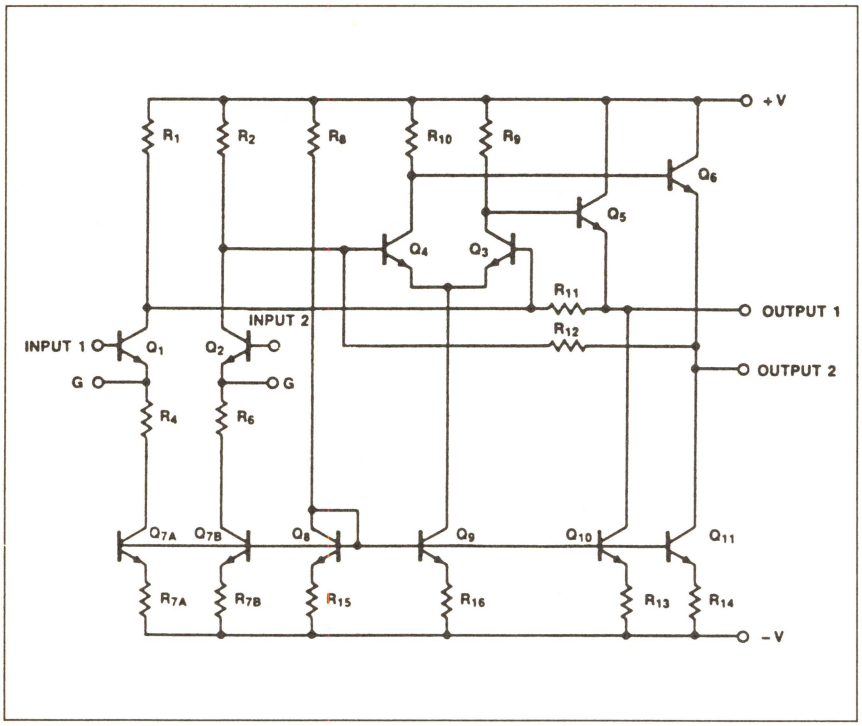



TOP VIEW

### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 14-pin plastic DIP | | NE5592N |
| 14-pin SO DIP | | NE5592D |

### EQUIVALENT CIRCUIT



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# SA/SE/NE5230
## Low Voltage Operational Amplifier

*Product Specification*

**Linear Products**

### DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 115dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 23nV/$\sqrt{Hz}$ noise specification.

### FEATURES

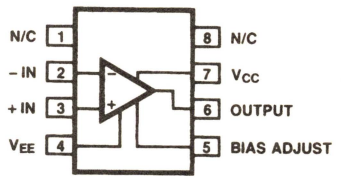
- **Works down to 1.8V supply voltages**
- **Adjustable supply current**
- **Low noise**
- **Common-mode includes both rails**
- **$V_{OUT}$ within 100mV of both rails**

### APPLICATIONS

- **Portable precision instruments**
- **Remote transducer amplifier**
- **Portable audio equipment**
- **Rail-to-Rail comparators**
- **Half-wave rectification without diodes**
- **Remote temperature transducer with 4 to 20mA output transmission**

### PIN CONFIGURATION

**N, FE & D Packages**




**TOP VIEW**

CD11070S

### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 8-pin Plastic DIP | 0 to +70°C | NE5230D |
| 8-pin Ceramic DIP | 0 to +70°C | NE5230FE |
| 8-pin Plastic DIP | 0 to +70°C | NE5230N |
| 8-pin Plastic DIP | −40 to +85°C | SA5230D |
| 8-pin Plastic DIP | −40 to +85°C | SA5230N |
| 8-pin Ceramic DIP | −55 to +125°C | SE5230FE |
| 8-pin Plastic DIP | −55 to +125°C | SE5230N |



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# SE/NE5532/5532A
## Internally Compensated Dual Low Noise OP Amp

*Product Specification*

**Linear Products**

### DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

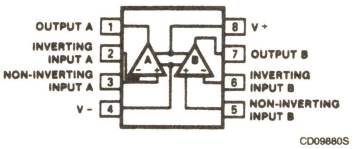
This makes the device especially suitable for application in high-quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise voltage specifications.

### FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms)**
- **Input noise voltage: 5nV/√Hz (typical)**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew-rate: 9V/μs**
- **Large supply voltage range: ±3 to ±20V**
- **Compensated for unity gain**

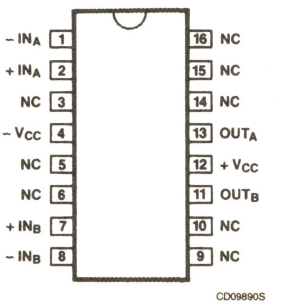
### PIN CONFIGURATIONS

**FE, N Packages**



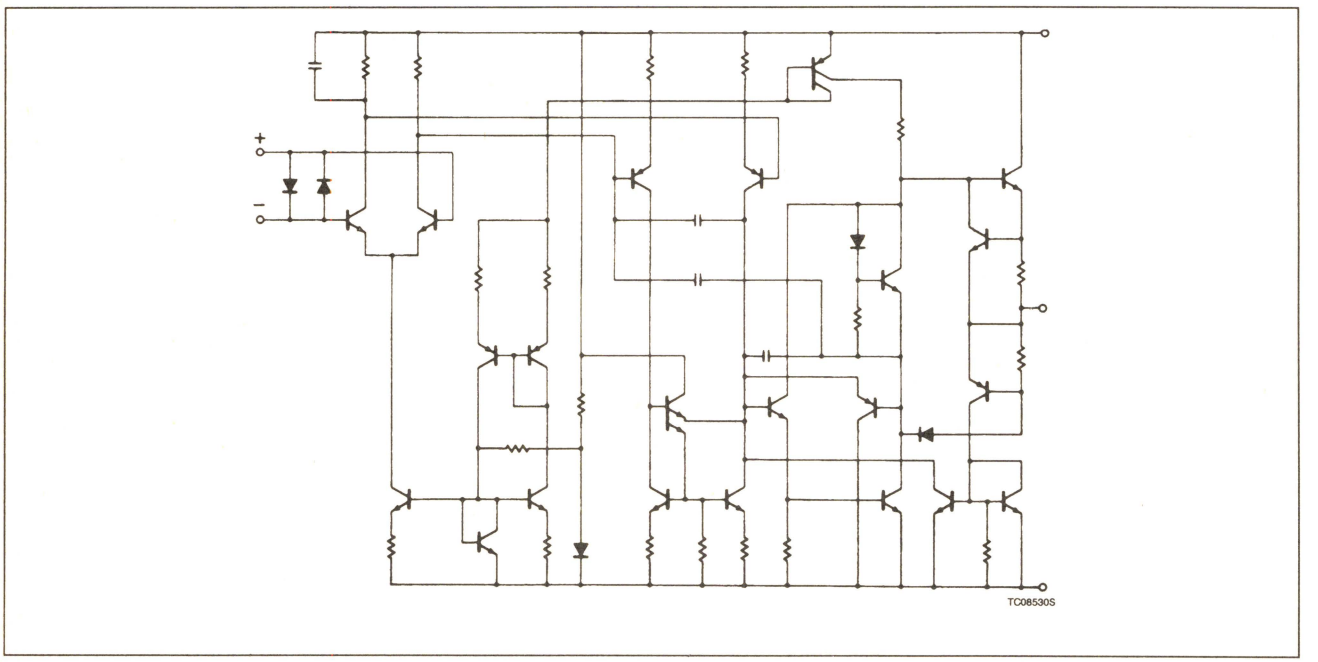

TOP VIEW

**D Package[2]**




TOP VIEW

### EQUIVALENT SCHEMATIC (EACH AMPLIFIER)





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# NE/SA/SE5534
## Single and Dual Low Noise Op Amp

**Linear Products**

*Preliminary Specification*

### DESCRIPTION

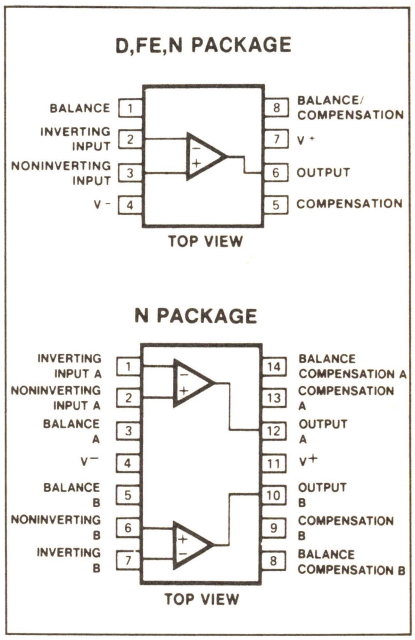
The 5534 is a dual and single high-performance low noise operational amplifier. compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5534A version be used which has guaranteed noise specifications.

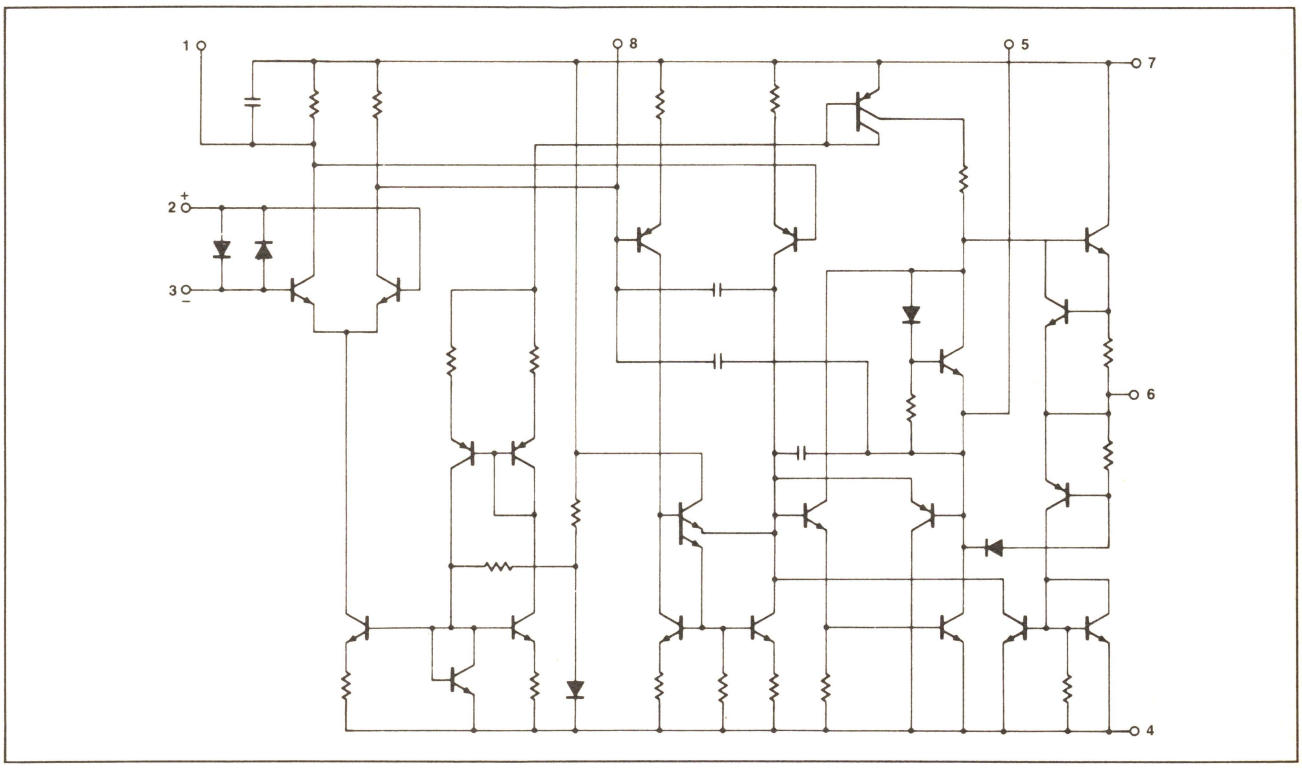
### FEATURES

- **Small-signal bandwidth: 10 MHz**
- **Output drive capability: 600Ω, 10 V (rms) at $V_S = \pm 18$ V**
- **Input noise voltage: 4nV/√Hz**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10 kHz**
- **Power bandwidth: 200 kHz**
- **Slew rate: 13 V/μs**
- **Large supply voltage range: ±3 to ±20 V**

### PIN CONFIGURATIONS




### BLOCK DIAGRAM

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# SE/NE5212
# Transimpedance Amplifier

***Preliminary Specification***

**Linear Products**

## DESCRIPTION

The NE/SE5212 is a low noise differential amplifier, particularly suitable for signal recovery in fiber-optic receivers and in any other applications where very low signal levels obtained from high impedance sources need to be amplified.

## FEATURES

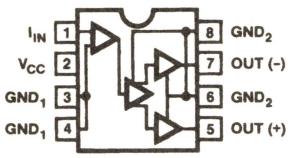
- **Extremely low noise 2.5pA/$\sqrt{Hz}$**
- **Single 5V supply**
- **Large bandwidth: 150MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High power supply rejection ratio**
- **14k$\Omega$ differential transresistance**

## APPLICATIONS

- **Fiber-optic receivers**
- **Wideband gain block**
- **General purpose instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**

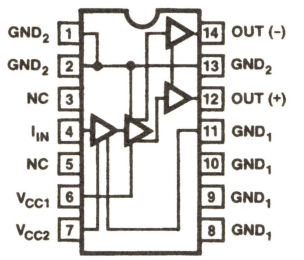
## PIN CONFIGURATIONS

**N, FE, D-8 Packages**




CD10450S

**D-14 Package**




CD10440S

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 8-pin Plastic DIP | 0°C to +70°C | NE5212N |
| 8-pin Plastic SO | 0°C to +70°C | NE5212D8 |
| 8-pin Ceramic DIP | 0°C to +70°C | NE5212FE |
| 14-pin Plastic SO | 0°C to +70°C | NE5212D14 |
| 8-pin Plastic SO | −40°C to +85°C | SA5212D8 |
| 14-pin Plastic SO | −40°C to +85°C | SA5212D14 |
| 8-pin Plastic DIP | −40°C to +85°C | SA5212N |
| 8-pin Ceramic DIP | −40°C to +85°C | SA5212FE |
| 8-pin Plastic DIP | −55°C to +125°C | SE5212N |
| 8-pin Ceramic DIP | −55°C to +125°C | SE5212FE |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | | | UNIT |
|---|---|---|---|---|---|
| | | NE5212 | SA5212 | SE5212 | |
| | Temperature Range | | | | |
| $T_A$ | Operating ambient | 0 to 70 | −40 to 85 | −55 to 125 | °C |
| $T_J$ | Operating junction | −55 to 150 | −55 to 150 | −55 to 150 | °C |
| $T_{STG}$ | Storage | −65 to 150 | −65 to 150 | −65 to 150 | °C |
| $V_{CC}$ | Power Supply | 6 | 6 | 6 | V |

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# TDA7050
# Low Voltage Mono/Stereo Power Amplifier

*Product Specification*

## DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

## APPLICATIONS

- **Portable Radio**
- **Personal Computer**
- **Speech Synthesis**
- **Telephone Modem**

## FEATURES

- **Limited to battery supply application only (Typ. 3 and 4V)**
- **Operates with supply voltage down to 1.6V**
- **No external components required**
- **Very low quiescent current**
- **Fixed integrated gain of 26dB, floating differential input**
- **Flexibility in use — mono BTL as well as stereo**
- **Small dimension of encapsulation (see package design example)**

## ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 8-pin Plastic SO DIP | 0°C to +70°C | TDA7050D |
| 8-pin Plastic DIP | 0°C to +70°C | TDA7050N |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_P$ | Supply voltage | 6 | V |
| $I_{OM}$ | Peak output current | 150 | mA |
| $P_{TOT}$ | Total power dissipation | see derating curve, Figure 1 | |
| $T_{stg}$ | Storage temperature range | −55 to +150 | °C |
| $T_C$ | Crystal temperature | 100 | °C |
| $t_{sc}$ | AC and DC short-circuit duration at $V_P$ = 3.0 V (during mishandling) | 5 | s |

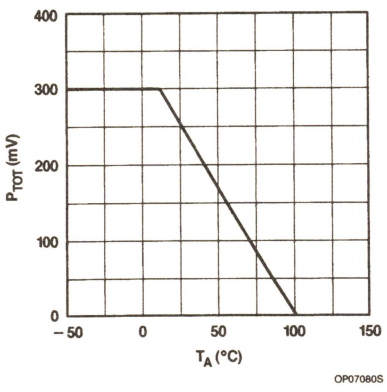


**Figure 1. Power Derating Curve**

## SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{J\ MAX} - T_A}{R_{TH\ J\text{-}A}} = \frac{100 - 60}{300} = 0.1\ W$$

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# TDA1510
## 2 × 12W Audio Amplifier

*Product Specification*

**Linear Products**

### DESCRIPTION

The TDA1510 is a monolithic integrated class B output amplifier in a 13-pin single in-line (SIP) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1.6Ω). At a supply voltage $V_P = 14.4V$, an output power of 24W can be delivered into a 4Ω BTL (Bridge-Tied Load), or, when used as stereo amplifier, it delivers 2 × 12W into 2Ω or 2 × 7W into 4Ω.

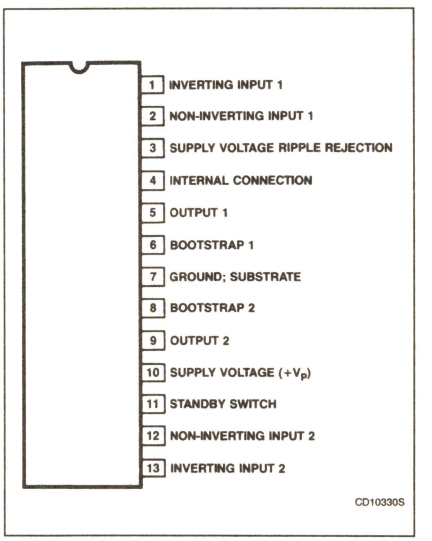
### FEATURES

- **Flexibility in use — stereo as well as mono BTL**
- **High output power**
- **Low offset voltage at the output (important for BTL)**
- **Large useable gain variation**
- **Very good ripple rejection**
- **Load dump protection**
- **AC short-circuit safe to ground**
- **Thermal protection**
- **Internal limited bandwidth for high frequencies**
- **Low standby current possibility, to simplify required switches**
- **Low number and small sized external components**
- **High reliability**

### APPLICATIONS

- **Car radios**
- **Low-impedance loads**
- **Stereo amplifiers**

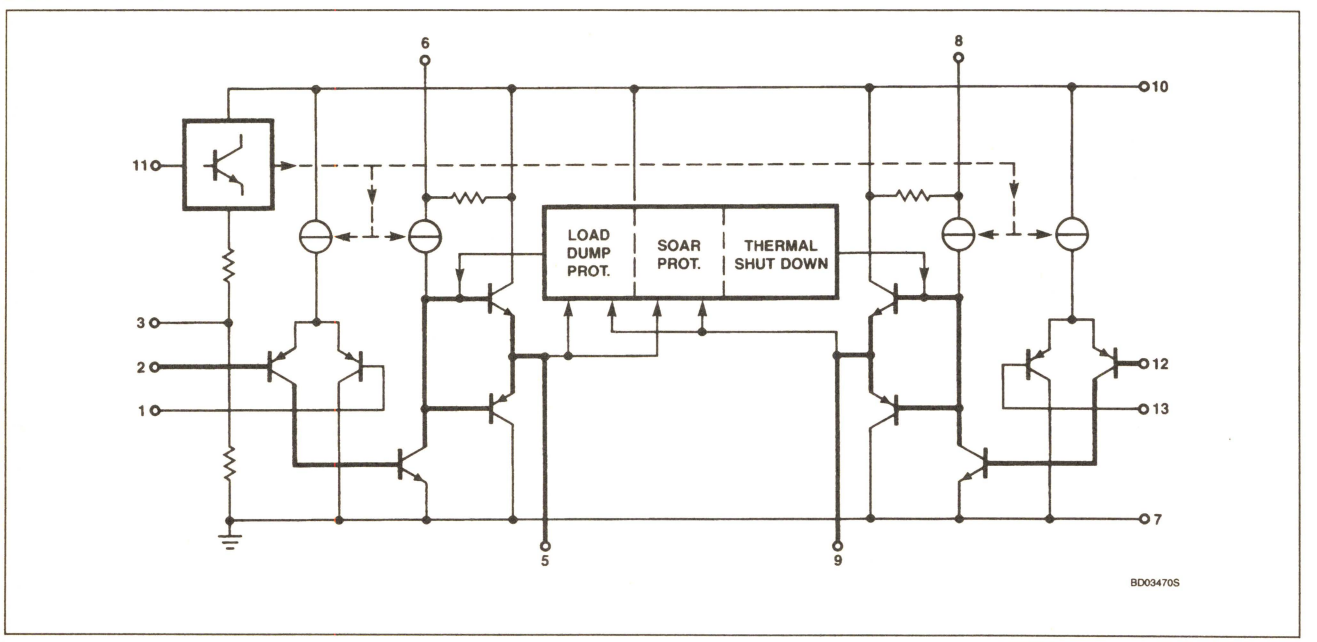
### PIN CONFIGURATION




### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 13-Pin Plastic Power SIP | 0 to +70°C | TDA1510U |

### BLOCK DIAGRAM





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# TDA1515A
## 24W BTL Audio Amplifier

***Product Specification***

**Linear Products**

### DESCRIPTION

The TDA1515 is a monolithic integrated class-B output amplifier in a 13 pin single in-line (SIP) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1.6Ω). At a supply voltage $V_{CC}$ = 14.4V, an output power of 21W can be delivered into a 4Ω BTL (Bridge-Tied Load), or, when used as stereo amplifier, it delivers 2 × 11W into 2Ω or 2 × 6.5W into 4Ω.

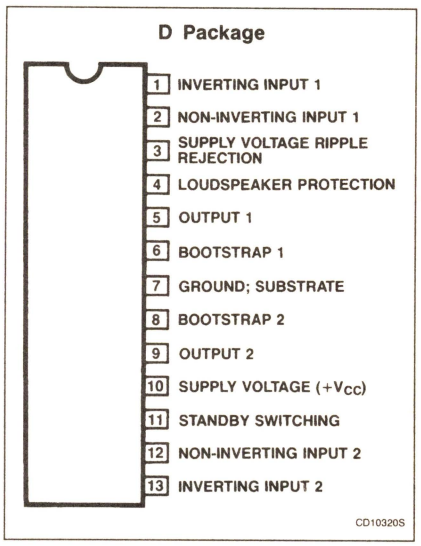
### FEATURES

- **Flexibility in use — mono BTL as well as stereo**
- **High output power**
- **Low offset voltage at the output (important for BTL)**
- **Large usable gain variation**
- **Very good ripple rejection**
- **Internal limited bandwidth for high frequencies**
- **Low standby current possibility (typ. 1μA), to simplify required switches; TTL drive possible**
- **Low number and small-sized external components**
- **High reliability**
- **Load dump protection**
- **AC and DC short-circuit safe to ground up to $V_{CC}$ = 18V**
- **Thermal protection**
- **Speaker protection in bridge configuration**
- **SOAR protection**
- **Outputs short-circuit safe to ground in BTL**
- **Reverse-polarity safe**

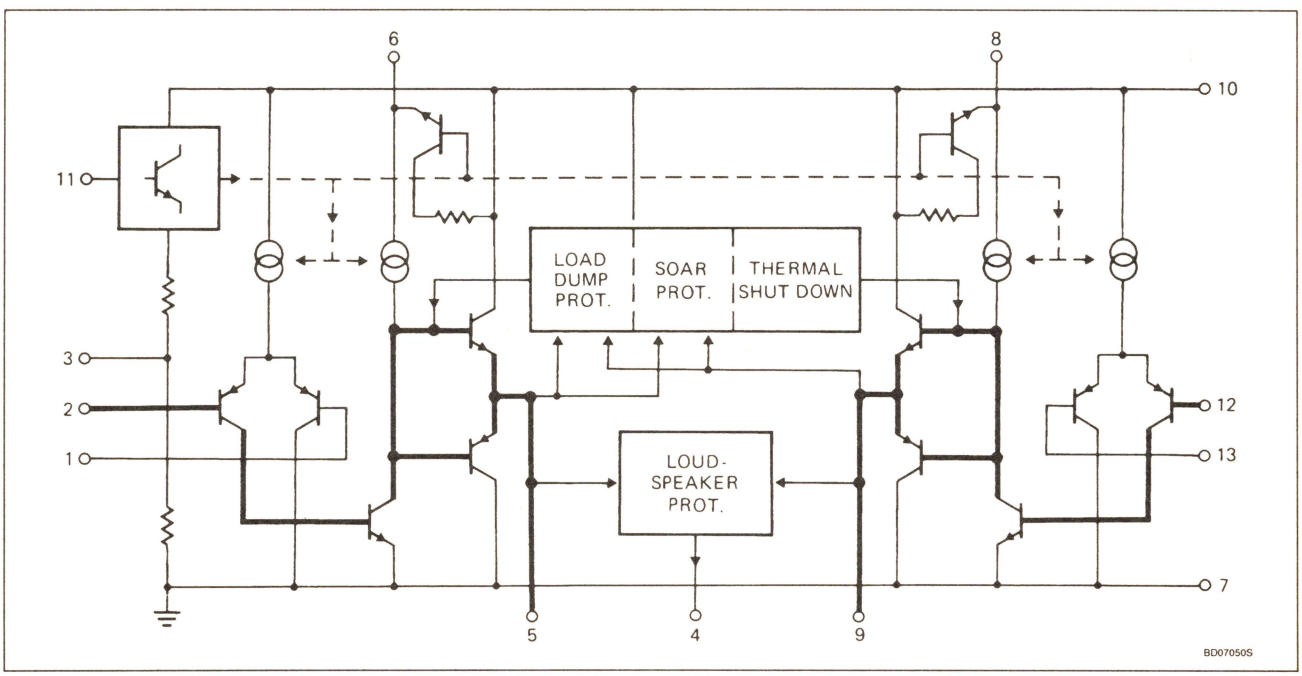
### APPLICATIONS

- **Car radio applications**
- **Drive low impedance loads**
- **Stereo amplifier**

### PIN CONFIGURATION




### BLOCK DIAGRAM

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# TDA1512
# 12 to 20W Audio Amplifier

***Product Specification***

**Linear Products**

## DESCRIPTION

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies.

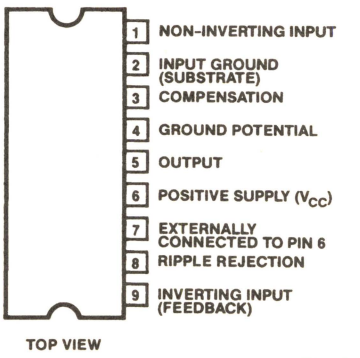
## FEATURES

- **Thermal protection**
- **Low intermodulation distortion**
- **Low transient intermodulation distortion**
- **Built-in output current limiter**
- **Low input offset voltage**
- **Output stage with low cross-over distortion**
- **Single in-line (SIP) power package**

## APPLICATIONS

- **Television**
- **Radio receivers**
- **Hi-Fi power amp**

## PIN CONFIGURATION




## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 9-Pin Plastic SIP (SOT-131B) | −25°C to +150°C | TDA1512U |
| 9-Pin Plastic SIP-bent-to DIP plastic power (SOT-157B) | −25°C to +150°C | TDA1512QU |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 35 | V |
| $I_{ORM}$ | Repetitive peak output current | 3.2 | A |
| $I_{OSM}$ | Non-repetitive peak output current | 5 | A |
| $P_{TOT}$ | Total power dissipation | see derating curve Figure 1 | |
| $T_{STG}$ | Storage temperature | −55 to +150 | °C |
| $T_A$ | Operating ambient temperature | −25 to +150 | °C |
| $t_{SC}$ | AC short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_{CC} = 30V$ with $R_I = 4\Omega$ | 100 | hours |
| $\theta_{JMB}$ | Thermal resitance From junction to mounting base | typ. 3<br>$\leqslant 4$ | °C/W<br>°C/W |



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# NE5050
## Power Line Modem

**Linear Products**

### DESCRIPTION

The NE5050 a is a modem for power line and twisted-pair communications. The modem incorporates features to overcome power line impulse noise and line impedance modulation. The modem transmitter section has a Colpitts oscillator, positive logic carrier on/off switch, and driver. The receiver has an amplifier, limiter, amplitude detector, amplitude modulation cancelling stage, impulse filter, and SR flip-flop. One NE5050 can be used to transmit Amplitude Shift Key (ASK carrier on/off) modulation. With two NE5050s, Frequency Shift Key Modulation (FSK) can be implemented. The modem accepts and sends out TTL or CMOS compatible serial data information.

### FEATURES

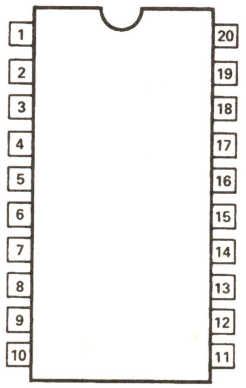
- **High receiver sensitivity — 1mV**
- **Limiter protects overload for signals up to $70V_{P-P}$**
- **High data rates — 300k bit/s over twisted-pair**
- **Has CSMA/CD carrier-sense, multiple access/collision detection capability**
- **Useful balanced interstage ports are available for bandpass filter**
- **Colpitts oscillator tank can be made with crystal or LC network**
- **Receiver signals are processed in real-time making this device suitable for repeater applications**

### APPLICATIONS

- **Power line data communications**
- **Twisted-pair data communications**

### PIN CONFIGURATION

**D[1] and N Packages**




CD05031S

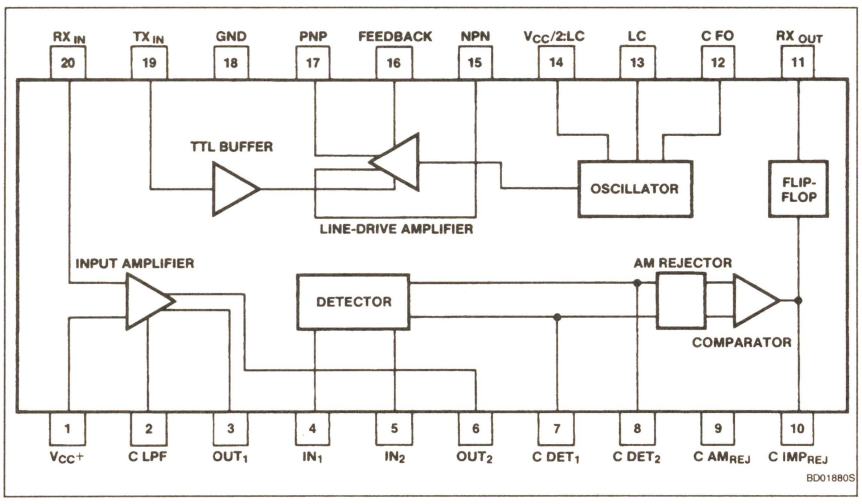
| PIN | NAME AND FUNCTION |
|---|---|
| 1 | $+V_{CC}$ |
| 2 | Low-pass filter |
| 3 | Amplifier output (+) |
| 4 | Detector input (+) |
| 5 | Detector input (+) |
| 6 | Amplifier output (−) |
| 7 | Detector output (−) |
| 8 | Detector output (−) |
| 9 | AM rejection |
| 10 | Impulse filter |
| 11 | Receiver output (data out) |
| 12 | Oscillator feedback |
| 13 | Oscillator I/O |
| 14 | Oscillator bias ($+V_{CC}/2$) |
| 15 | Transmit carrier (NPN base) |
| 16 | Line-drive feedback |
| 17 | Transmit carrier (PNP base) |
| 18 | Ground |
| 19 | Transmitter input (data in) |
| 20 | Receiver input (carrier in) |

**NOTE:**
1. SOL — Released in large SO package only.

### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 20-Pin Plastic SOL package | 0 to 70°C | NE5050D |
| 20-Pin Plastic DIP | 0 to 70°C | NE5050N |

### BLOCK DIAGRAM

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# NE5080
# High-Speed FSK Modem Transmitter

***Preliminary Specification***

**Linear Products**

## DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single Channel Phase-Continuous-FSK Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies remains fixed at 1.67 to 1.00 at any center frequency.

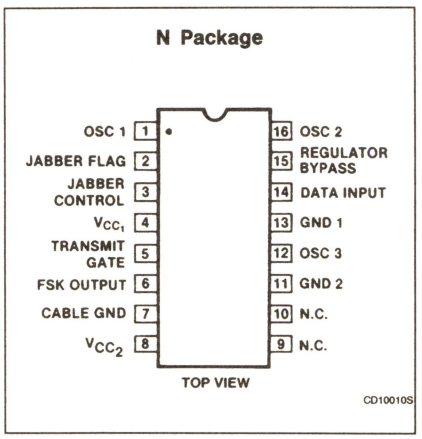
## FEATURES

- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half-or full-duplex operation**
- **Jabber function on-chip**

## APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

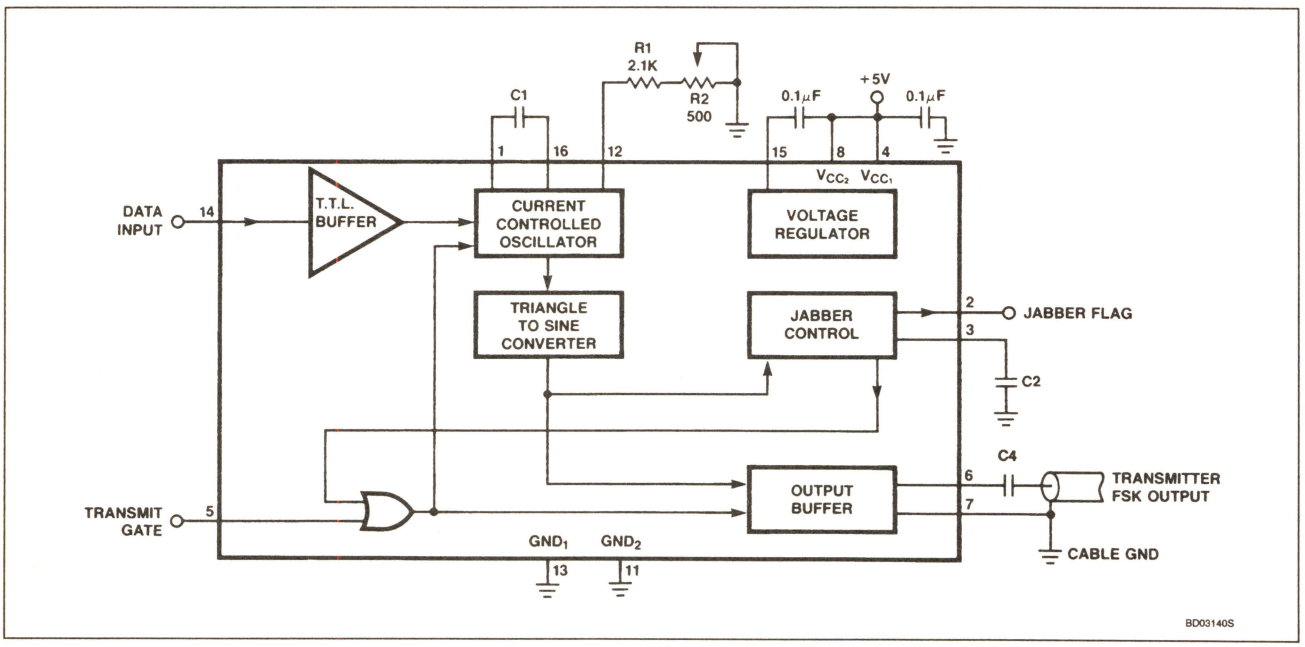
## PIN CONFIGURATION




## ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-Pin Plastic DIP | | NE5080N |

## BLOCK DIAGRAM





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# NE570/571/SA571
# Compandor

***Product Specification***

**Linear Products**

## DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal; a linerarized, temperature-compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

## CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at $V_{REF}$. The rectified current is averaged on an external filter capacitor tied to the $C_{RECT}$ terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1$\mu$A.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg.}}{R_1}$$

## FEATURES

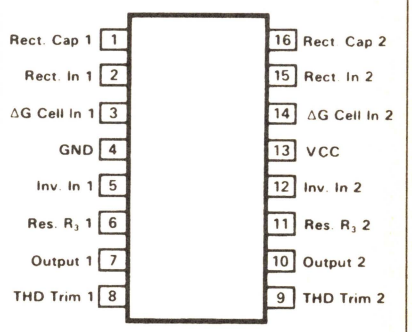
- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to $6V_{DC}$**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

## APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor — 570**
- **Telephone subscriber compandor — 571**
- **High level limiter**
- **Low level expandor — noise gate**
- **Dynamic noise reduction systems**
- **Voltage-controlled amplifier**
- **Dynamic filters**

## PIN CONFIGURATION

**D[1], F, N Packages**



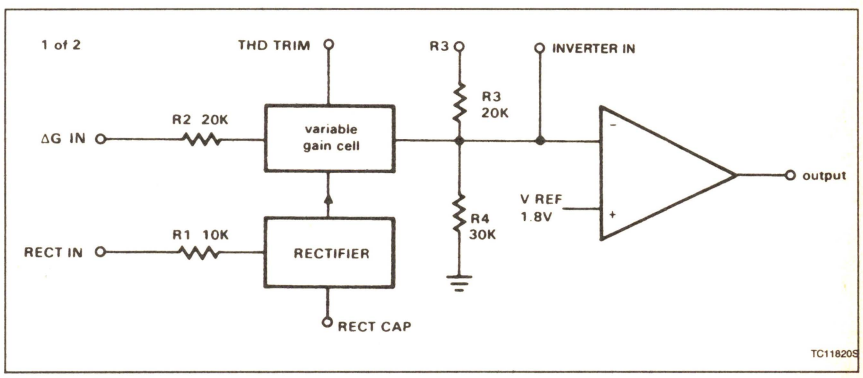

CD10500S

**NOTES:**
1. SOL - Released in Large SO Package Only.
2. SOL and Non-Standard Pinout.
3. SO and Non-Standard Pinouts.

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-pin Hermetic Cerdip | 0 to +70°C | NE570F |
| 16-pin Plastic DIP | 0 to +70°C | NE570N |
| 16-pin Plastic SOL | 0 to +70°C | NE571D |
| 16-pin Hermetic Cerdip | 0 to +70°C | NE571F |
| 16-pin Plastic Cerdip | 0 to +70°C | NE571N |
| 16-pin Hermetic Cerdip | −40 to +85°C | SA571F |
| 16-pin Plastic DIP | −40 to +85°C | SA571N |

## BLOCK DIAGRAM




TC11820S

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# SA/NE572

# Programmable Analog Compandor

*Objective Specification*

**Linear Products**

## DESCRIPTION

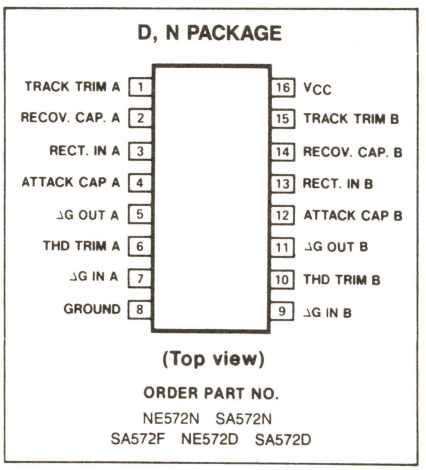
The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell ($\Delta G$) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

## FEATURES

- **Independent control of attack and recovery time.**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external Op Amp**
- **Wide dynamic range—greater than 110dB**
- **Temperature compensated gain control**
- **Low distortion gain cell**
- **Low noise—6$\mu$V typical**
- **Wide supply voltage range—6V–22V**
- **System level adjustable with external components.**

## PIN CONFIGURATION



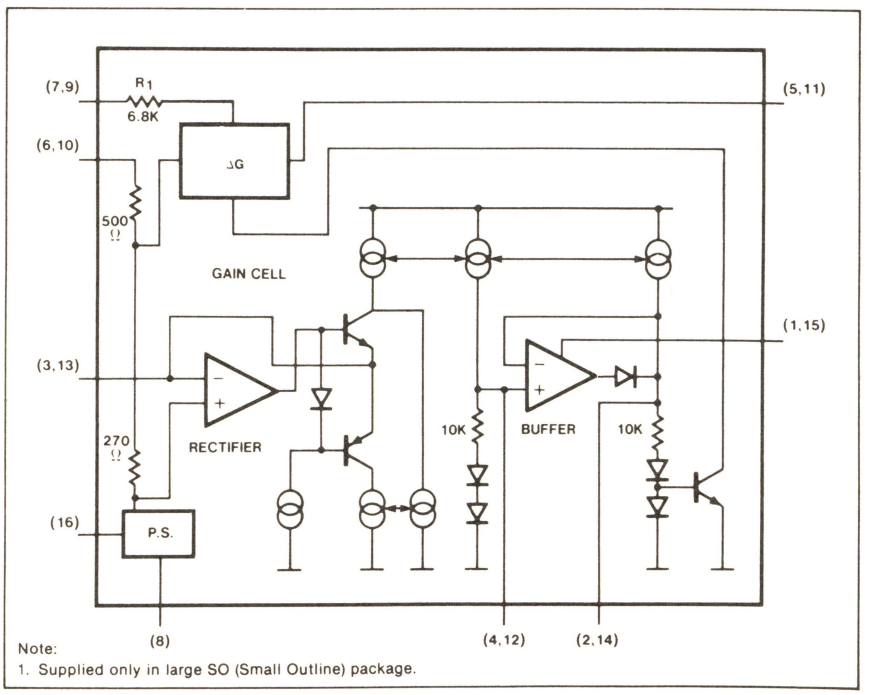

## APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High level limiter**
- **Low level noise gate**
- **State variable filter**

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 22 | VDC |
| $T_A$ | Operating temperature range NE572 | 0 to 70 | °C |
| | Operating temperature range SA572 | -40 to +85 | °C |
| $P_D$ | Power dissipation | 500 | mW |

## BLOCK DIAGRAM




Note:
1. Supplied only in large SO (Small Outline) package.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# SA/NE602
# Double Balanced Mixer And Oscillator

*Product Specification*

**Linear Products**

## DESCRIPTION

The SA/NE602 is a low-power VHF monolithic double balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA/NE602 a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual-in-line plastic package and an 8-lead SO (surface-mount miniature package).

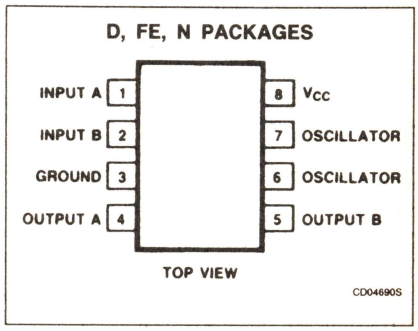
## FEATURES

- **Low current consumption: 2.4mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA602 meets cellular radio specifications**

## APPLICATIONS

- **Cellular radio mixer/oscillator**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LAN's**

## PIN CONFIGURATION

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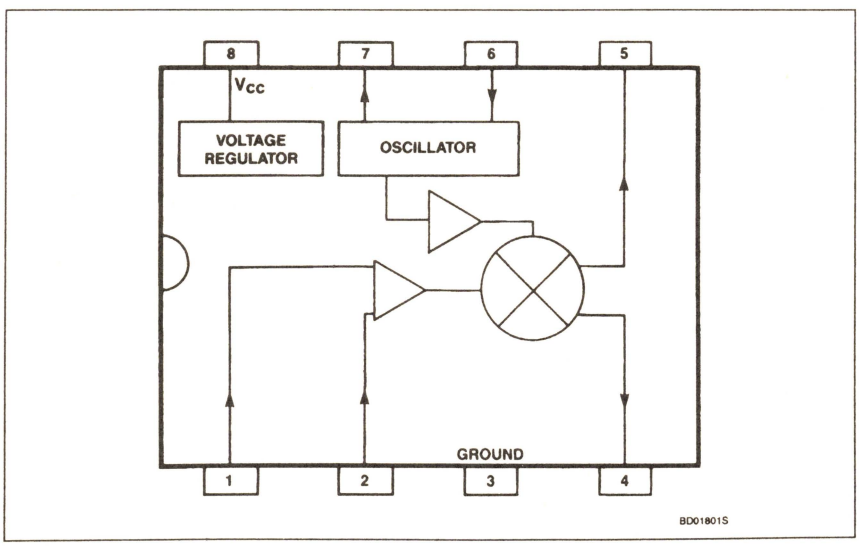


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# NE612
# Double Balanced Mixer And Oscillator

*Product Specification*

**Linear Products**

## DESCRIPTION

The NE612 is a low-power VHF monolithic double balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8- lead dual-in-line plastic package and an 8-lead SO (surface mounted miniature package).

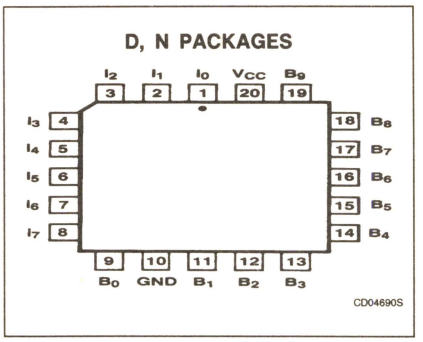
## FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

## APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LAN's**
- **HF and VHF frequency conversion**

## PIN CONFIGURATION

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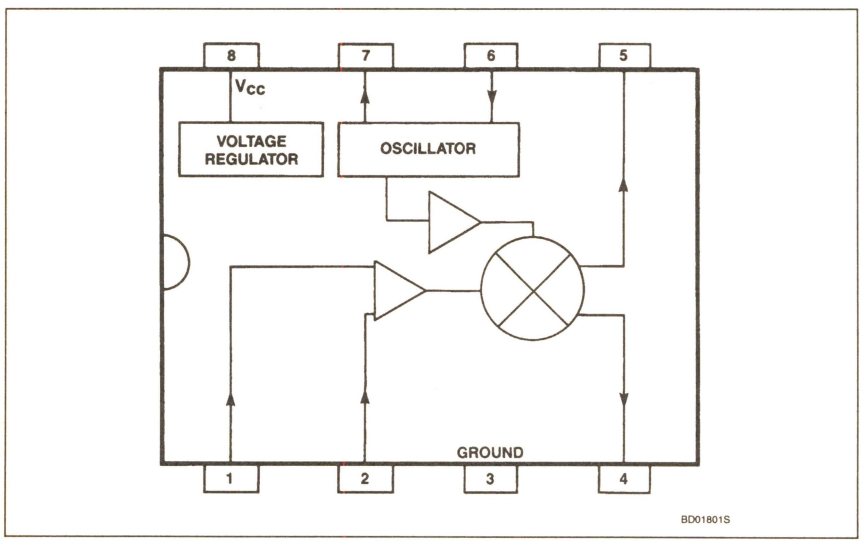


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# SA/NE 604
## Low Power FM IF System

*Product Specification*

**Linear Products**

### DESCRIPTION

The SA/NE604 is a monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The SA/NE604 is available in a 16-lead dual-in-line plastic and Cerdip packages and 16-lead SO (surface-mounted miniature package).

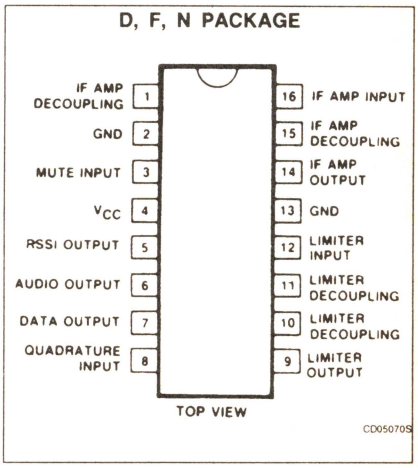
### FEATURES

- Low-power consumption: 2.3mA typical
- Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Separate data output
- Audio output with muting
- Low external count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5$\mu$V across input pins (0.27$\mu$V into 50$\Omega$ matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA604 meets cellular radio specifications

### APPLICATIONS

- Cellular Radio FM IF
- Communications receivers
- Intermediate frequency amplification and detection up to 15MHz
- RF level meter
- Spectrum analyzer
- Instrumentation

### PIN CONFIGURATION

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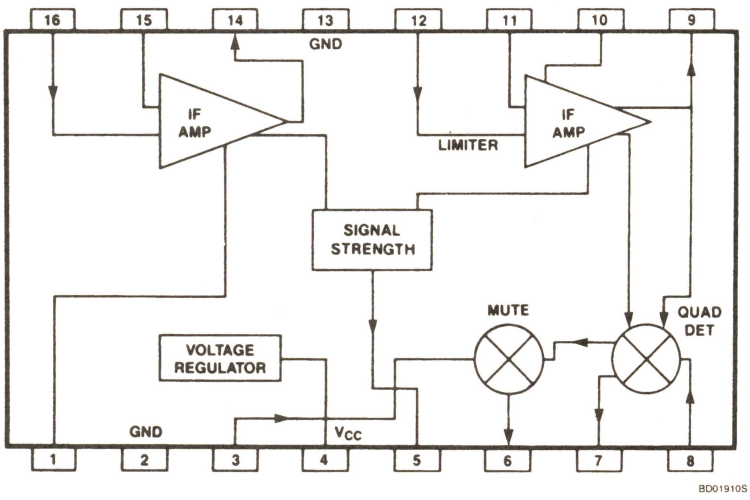


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# NE614
# Low Power FM IF System

*Product Specification*

**Linear Products**

## DESCRIPTION

The NE614 is a monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE614 is available in a 16-lead dual-in-line plastic package and 16-lead SO (surface-mounted miniature package).

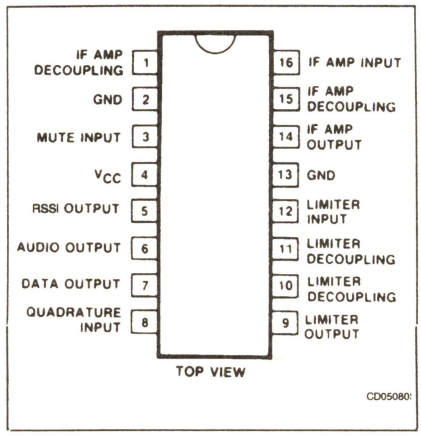
## FEATURES

- **Low-power consumption**
- **Logarithmic signal strength indicator**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity**

## APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Cordless telephone**
- **Remote control**

## PIN CONFIGURATION

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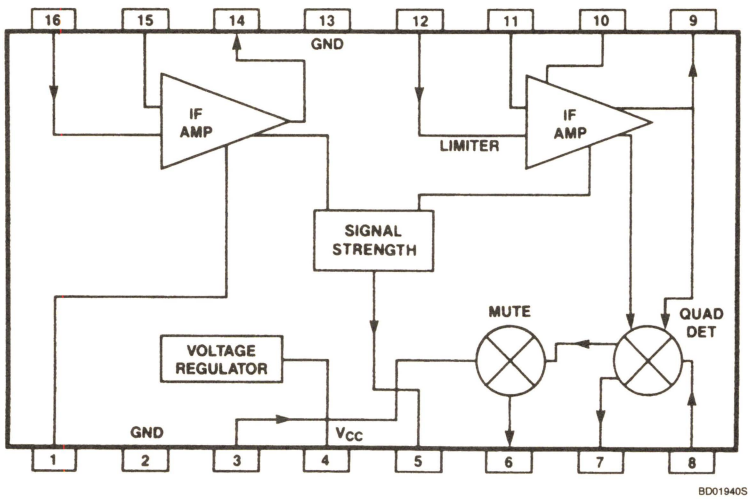


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# TDA5030T
## VHF Mixer/Oscillator

**Linear Products**

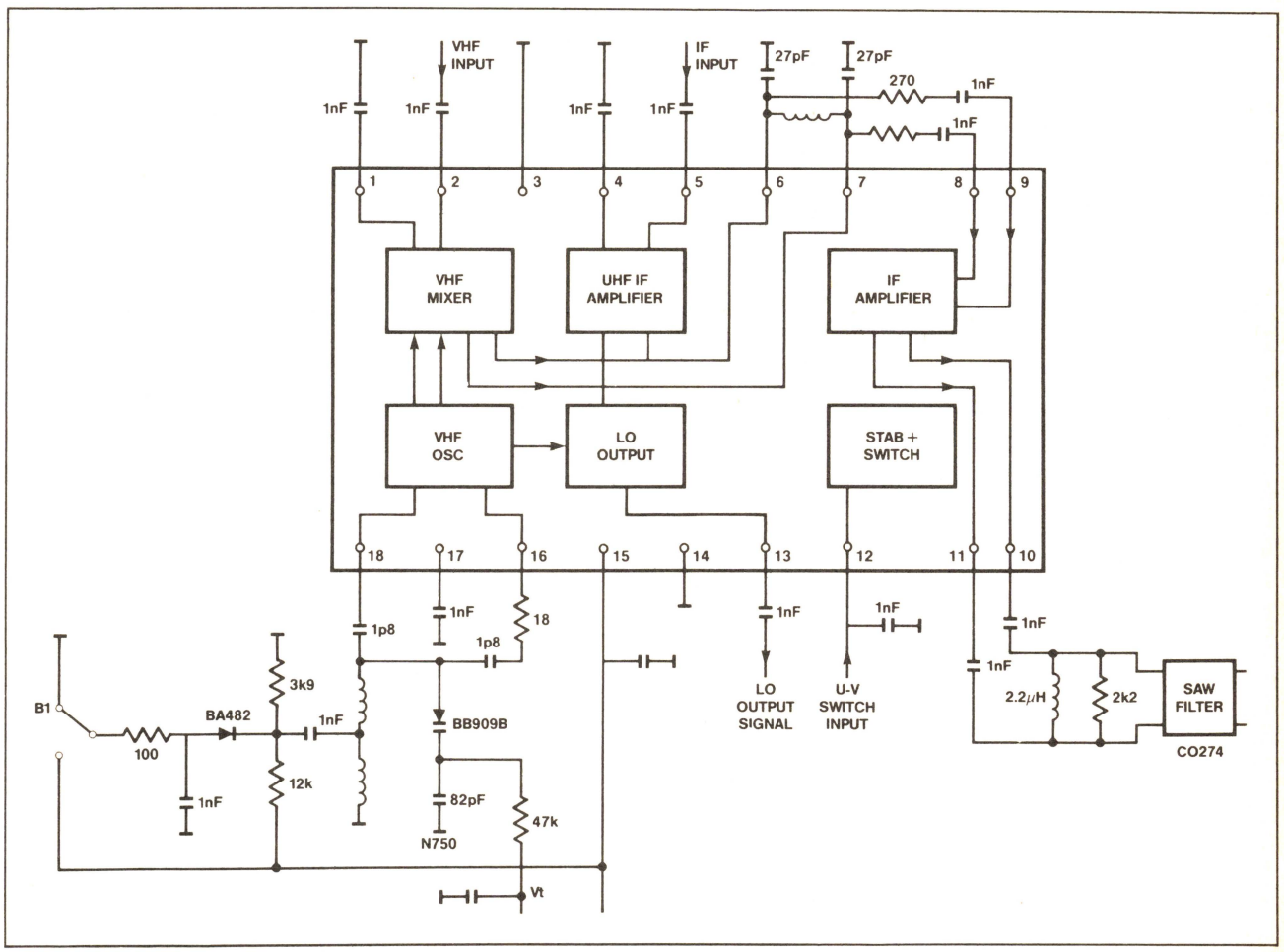
***Preliminary Specification***

### DESCRIPTION
The TDA5030T is a monolithic IC for the VHF mixer/oscillator function in TV tuners.

### FEATURES
- **Balanced mixer**
- **Amplitude controlled oscillator**
- **SAW filter preamplifier**
- **UHF IF preamplifier**
- **Buffered stage for drive of a prescaler with the oscillator signal**
- **Voltage stabilizer**
- **U-V switching circuit**

### APPLICATIONS
- **Mixer/oscillator**
- **RF receiver**
- **Tuners**
- **CATV**

### BLOCK DIAGRAM

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# TDD1742T
# CMOS Frequency Synthesizer (Lopsy)

***Advance Information***

**Linear Products**

## DESCRIPTION

The TDD1742T is an oxide-isolated CMOS (LOCMOS) circuit designed specifically for Low Power Frequency Synthesizer applications, especially for VHF and UHF portables.

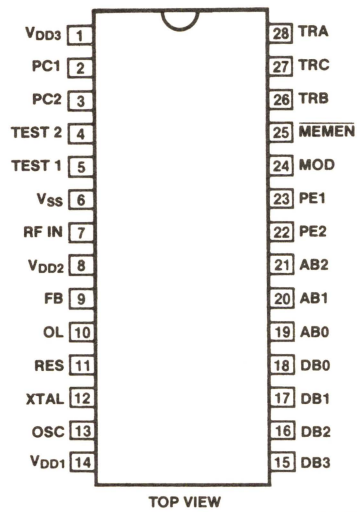
## FEATURES

- **Single chip with on-board sample and hold capacitor**
- **Low power requirements**
- **High performance phase comparator with low phase noise and spurious response**
- **Auxiliary digital phase comparator for fast locking**
- **On-board phase modulator**
- **Simple interface to memory**
- **Microprocessor controllable**
- **Power-on reset circuitry**

## APPLICATIONS

- **Frequency synthesizers**
- **Radio/TV LO circuit**

## PIN CONFIGURATION




TOP VIEW

CD01350S

| PIN | SYMBOL | FUNCTION |
|---|---|---|
| 1 | $V_{DD3}$ | Main power supply; +7 to +10V |
| 2 | PC1 | High-gain phase comparator (analogue) |
| 3 | PC2 | Low-gain phase comparator (digital) |
| 4 | Test 2 | Not connected |
| 5 | Test 1 | Not connected |
| 6 | $V_{SS}$ | Positive power supply |
| 7 | RF IN | RF input |
| 8 | $V_{DD2}$ | Power supply for TTL-compatible stages; +5V ± 10% |
| 9 | FB | Feedback to pre-scaler |
| 10 | OL | Out-of-lock indication |
| 11 | RES | Power-on-reset |
| 12 | XTAL | Reference oscillator/buffer output |
| 13 | OSC | Reference oscillator/buffer input |
| 14 | $V_{DD1}$ | Main power supply; +7 to +10V |
| 15 | DB3 | Data bus inputs |
| 16 | DB2 | Data bus inputs |
| 17 | DB1 | Data bus inputs |
| 18 | DB0 | Data bus inputs |
| 19 | AB0 | Address bus |
| 20 | AB1 | Address bus |
| 21 | AB2 | Address bus |
| 22 | PE2 | Program enable 2 |
| 23 | PE1 | Program enable 1 |
| 24 | $\overline{MOD}$ | Phase modulation input |
| 25 | $\overline{MEMEN}$ | Memory enable |
| 26 | TRB | Bias resistor $R_B$ |
| 27 | TRC | Bias resistor $R_C$ |
| 28 | TRA | Bias resistor $R_A$ |





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# TDA7000
## Single-Chip FM Radio Circuit

***Preliminary Specification***

**Linear Products**

### DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked Loop) system with an intermediate frequency of 70kHz. The IF selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too-noisy input signals. Special precautions are taken to meet the radiation requirements.

### FEATURES

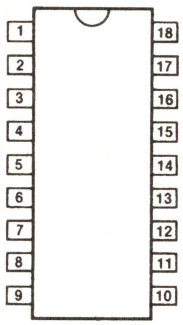
- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

### APPLICATIONS

- **Mono FM Portable Radio**
- **Wireless Telephone**
- **LAN**
- **Data Receivers**
- **SCA Receiver**

### PIN CONFIGURATION

**N Package**




TOP VIEW

CD10150S

### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 18-pin Plastic DIP | 0°C to +70°C | TDA7000N |

### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage (Pin 5) | 12 | V |
| $V_{6-5}$ | Oscillator voltage (Pin 6) | $V_{CC}-0.5$ to $V_{CC}+0.5$ | V |
| $P_{TOT}$ | Total power dissipation | See derating curve Figure 2 | |
| $T_{STG}$ | Storage temperature range | −55 to +150 | °C |
| $T_A$ | Operating ambient temperature range | 0 to +60 | °C |

### PIN DESCRIPTION

| PIN NO. | NAME AND FUNCTION |
|---|---|
| 1 | Muting capacitor |
| 2 | Audio frequency output |
| 3 | Noise source |
| 4 | Loop filter capacitor |
| 5 | Supply Voltage |
| 6 | VCO |
| 7 | 1st integrator capacitor (to Pin 9) |
| 8 | 2nd integrator capacitor |
| 9 | 1st integrator capacitor (to Pin 7) |
| 10 | IF filter capacitor (to Pin 11) |
| 11 | If filter capacitor |
| 12 | If limiter capacitor |
| 13 | RF input |
| 14 | Mixer |
| 15 | Current source capacitor |
| 16 | Ground |
| 17 | Demodulator capacitor |
| 18 | Correlator capacitor |

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# TDA7010T
# FM Radio Circuit (SO Package)

***Product Specification***

**Linear Products**

## DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked Loop) system with an intermediate frequency of 70kHz. The IF selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

## FEATURES

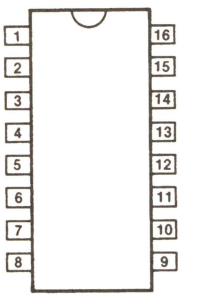
- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

## APPLICATIONS

- **Mono FM Portable Radio**
- **Wireless Telephone**
- **LAN**
- **Data Recievers**
- **SCA Receivers**

## PIN CONFIGURATION

**D Package**




TOP VIEW

CD10160S

## ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-Pin Plastic SO DIP | 0°C to +70°C | TDA7010TD |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage (Pin 4) | 12 | V |
| $V_{6-5}$ | Oscillator voltage (Pin 5) | $V_{CC}-0.5$ to $V_{CC}+0.5$ | V |
| | Total power dissipation | See derating curve Figure 2 | |
| $T_{STG}$ | Storage temperature range | −55 to +150 | °C |
| $T_A$ | Operating ambient temperature range | 0 to +60 | °C |

## PIN DESCRIPTION

| PIN NO. | NAME AND FUNCTION |
|---|---|
| 1 | Muting capacitor |
| 2 | Audio frequency output |
| 3 | Loop filter capacitor |
| 4 | Supply Voltage |
| 5 | VCO |
| 6 | 1st integrator capacitor (to Pin 7) |
| 7 | 2nd integrator capacitor |
| 8 | 1st integrator capacitor (to Pin 8) |
| 9 | IF filter capacitor (to Pin 11) |
| 10 | If limiter capacitor |
| 11 | RF input |
| 12 | Mixer |
| 13 | Current source capacitor |
| 14 | Ground |
| 15 | Demodulator capacitor |
| 16 | Correlator capacitor |





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# TDA7020T
## FM Radio Circuit

*Product Specification*

**Linear Products**

### DESCRIPTION

The TDA7020T integrated circuit is for FM portable radios, stereo as well as mono, where a minimum periphery is important in terms of small dimensions and low cost. The IC has a FLL (Frequency-Locked Loop) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant circuit of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MPX signal is required to avoid noise when receiving stereo. 50kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field strength detector enables field strength dependent channel separation control.

### FEATURES

- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Frequency detector**
- **Mute circuit**
- **RF input frequency range to 110MHz**
- **Loop amplifier**
- **Internal reference circuit**
- **LF amplifier for:**
  - **— mono earphone amplifier or**
  - **— MPX filter**
- **Field strength dependent channel separation control facility**

### APPLICATIONS

- **FM radios**
- **Stereo**
- **Mono**

### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-Pin Plastic SO DIP | 0°C to +70°C | TDA7020TD |

### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_P$ | Supply voltage (Pin 4) | 7 | V |
| $V_{6-5}$ | Oscillator voltage (Pin 5) | $V_p$–0.5 to $V_p$+0.5 | V |
| $P_{TOT}$ | Total power dissipation (see derating curve, Figure 2) | | |
| $T_{STG}$ | Storage temperature range | –55 to +150 | °C |
| $T_A$ | Operating temperature range | –10 to +70 | °C |



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# NE5900
# Call Progress Decoder

***Product Specification***

**Linear Products**

## DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder provides information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ringback, busy signal, or reorder tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS, and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

## FEATURES

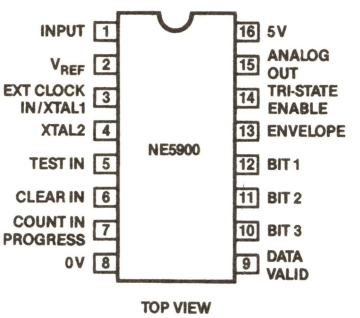
- **Fully decoded tri-state call progress status output**
- **Works with traditional, precision, or PBX call progress tones**
- **Low power consumption**
- **Low cost 3.58MHz crystal or clock**
- **No calibration or adjustment**
- **Interfaces with LSTLL, CMOS, NMOS**
- **Easy application**

## APPLICATIONS

- **Modems**
- **PBXs**
- **Security equipment**
- **Auto dialers**
- **Answering machines**
- **Remote diagnostics**
- **Pay telephones**

## PIN CONFIGURATION

**D[1] and N Packages**

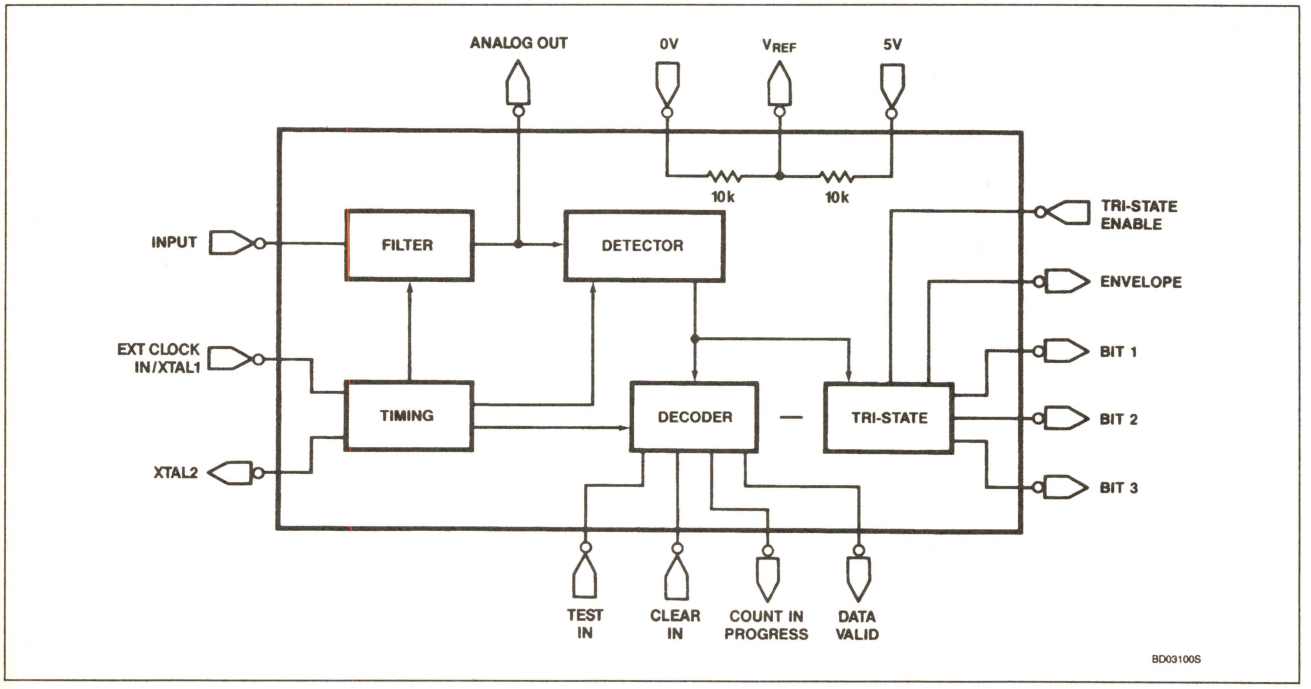



TOP VIEW

CD09970S

NOTES:
1. SOL — Released in large SO package only.

## BLOCK DIAGRAM CPD




BD03100S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# PCD3310
## Pulse and DTMF Dialer with Redial

*Advance Information*

**Linear Products**

### DESCRIPTION

The PCD3310 is a single-chip silicon-gate CMOS integrated circuit with an on-chip oscillator for a 3.58MHz crystal. It is a dual-standard dialing circuit for either pulse dialing (PD) or dual tone multi-frequency (DTMF) dialing.

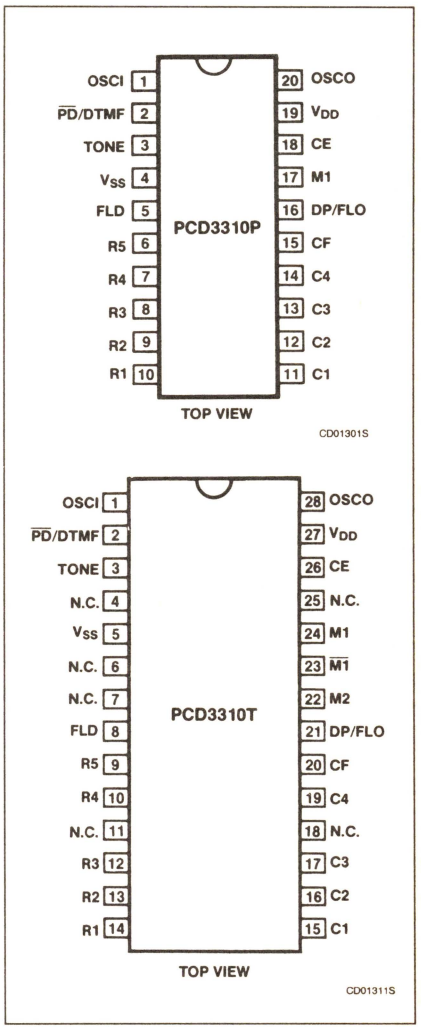
Input data is derived from any standard matrix keypad for dialing in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode, bursts as well as pauses are timed to a minimum in manual dialing, the maximum depending on the key depression time.

### FEATURES

- **PD and DTMF dialing.**
- **23-digit capacity for redial operation (cursor method)**
- **Memory clear and electronic notepad**
- **Mixed mode dialing (start with DP and end with DTMF dialing**
- **Dual redial buffers for PABX and public calls**
- **Four extra function keys: program, flash, redial and PD to DTMF (mixed dialing)**
- **DTMF timing:**
  - **manual dialing-minimum duration for bursts and pauses**
  - **redialing-calibrated timing**
- **On-chip voltage reference for supply and temperature independent tone output**
- **On-chip filtering for low output distortion (CEPT CS 203 compatible)**
- **On-chip oscillator with low cost 3.58MHz TV color-burst crystal**
- **Uses standard single-contact or double-contact (common left open) keypad**
- **Keyboard entries fully debounced at both edges**
- **Flash (register recall) output**

### PIN CONFIGURATION



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# TEA1067
# Low Voltage Transmission IC With Dialer Interface

*Advance Information*

**Linear Products**

## DESCRIPTION

The TEA1067 is a low-voltage bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. The TEA1067 operates down to 2.0V which facilitates the use of telephone sets in parallel operation. Electronic switching between dialing and speech is performed by internal circuitry. Other specifications similar to TEA1060/61.

## FEATURES

- **Low DC line voltage; operates down to 2V excluding polarity guard.**
- **Minimum instantaneous line voltage 0.9V excluding polarity guard.**
- **Voltage regular with adjustable static resistance.**
- **Provides supply with limited current for external circuitry.**
- **Symmetrical high-impedance inputs (64kohm) for dynamic, magnetic or piezoelectric microphones.**
- **Asymmetrical high-impedance input (32kohm) for electret microphone.**
- **DTMF signal input.**
- **Mute input for pulse or DTMF dialing.**
- **Power down input for pulse dial or register recall.**
- **Receiving amplifier for magnetic, dynamic or piezoelectric earpieces.**
- **Large amplification setting range on microphone and earpiece amplifiers.**
- **Line loss compensation facility, line current dependent.**
- **Gain control adaptable to exchange supply.**
- **Possibility to adjust the DC line voltage.**

## APPLICATIONS

- **Telephone handsets requiring low operating voltage.**





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# TEA1080

## Supply IC for Telephone Set Peripherals

*Product Specification*

**Linear Products**

### DESCRIPTION

The TEA1080 is a bipolar integrated circuit intended for use in line-powered telephone sets to supply peripheral circuits for extended dialing and/or loudspeaking facilities.

The IC uses a part of the surplus of the line current sinked normally in the voltage regulator of the applied speech/transmission circuit.

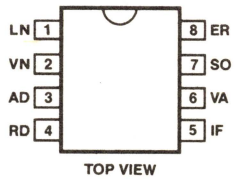
### FEATURES

- **High input impedance for audio signals**
- **High output current**
- **Large audio signal handling**
- **Low distortion**
- **Two modes of operation:**
  - **regulated output voltage**
  - **constant DC voltage drop in series with a resistor between line and output terminal**
- **Low number of external components**

### APPLICATION

- **Telephone hand sets**

### PIN CONFIGURATION




TOP VIEW

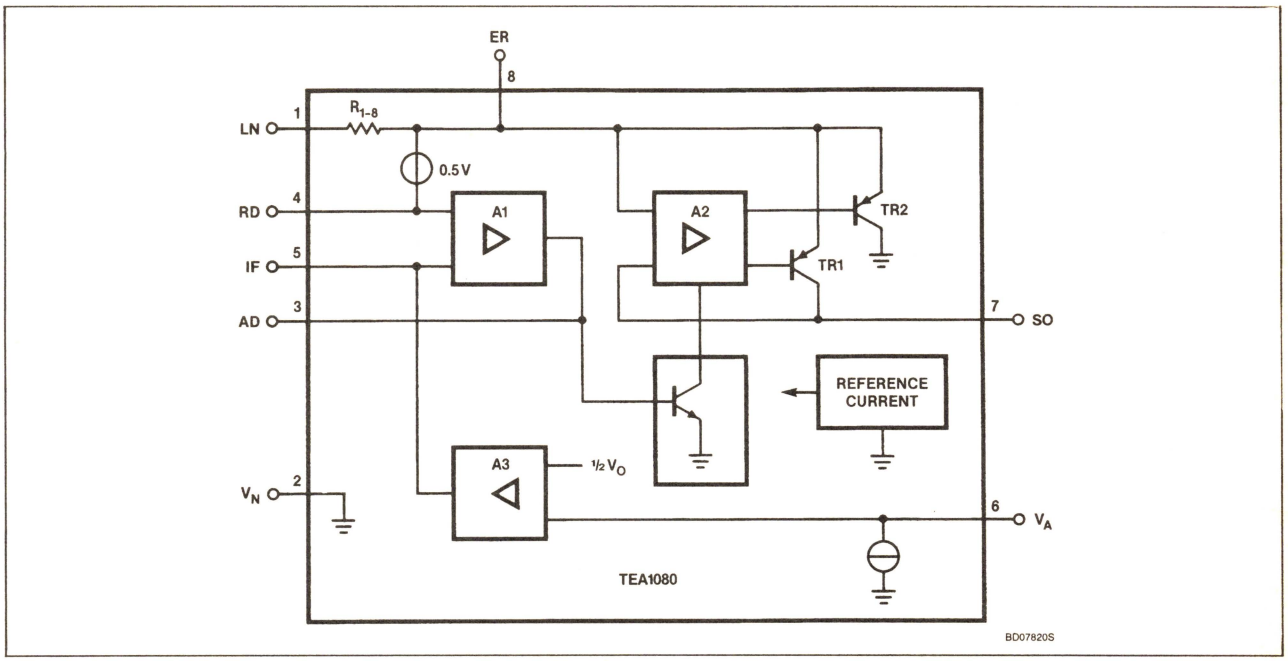
CD01371S

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | LN | Positive line terminal |
| 2 | VN | Negative line terminal |
| 3 | AD | Amplifier decoupling |
| 4 | RD | Regulator input |
| 5 | IF | Input low-pass filter |
| 6 | VA | Output voltage adjustment |
| 7 | SO | Supply output |
| 8 | ER | Supply terminal of the internal circuit |

### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 8-Pin Plastic DIP (SOT-97A) | −25°C to +70°C | TEA1080PN |

### BLOCK DIAGRAM

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# MEA8000
## Voice Synthesizer

**Linear Products**

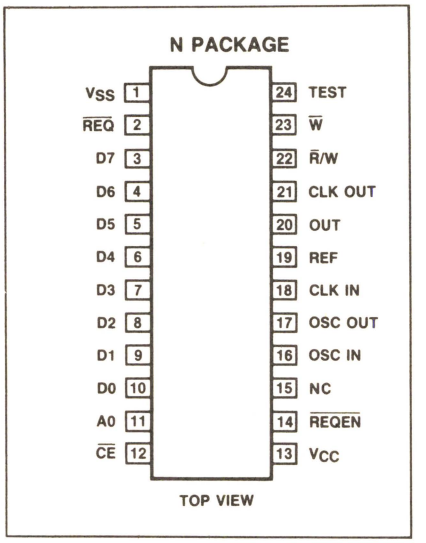
***Preliminary Specification***

### DESCRIPTION
The MEA8000 is a 24-pin N MOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately in a Read-Only Memory. An efficient, easy-to-use speech editing and encoding system with EPROM programming capability, has been specially developed.

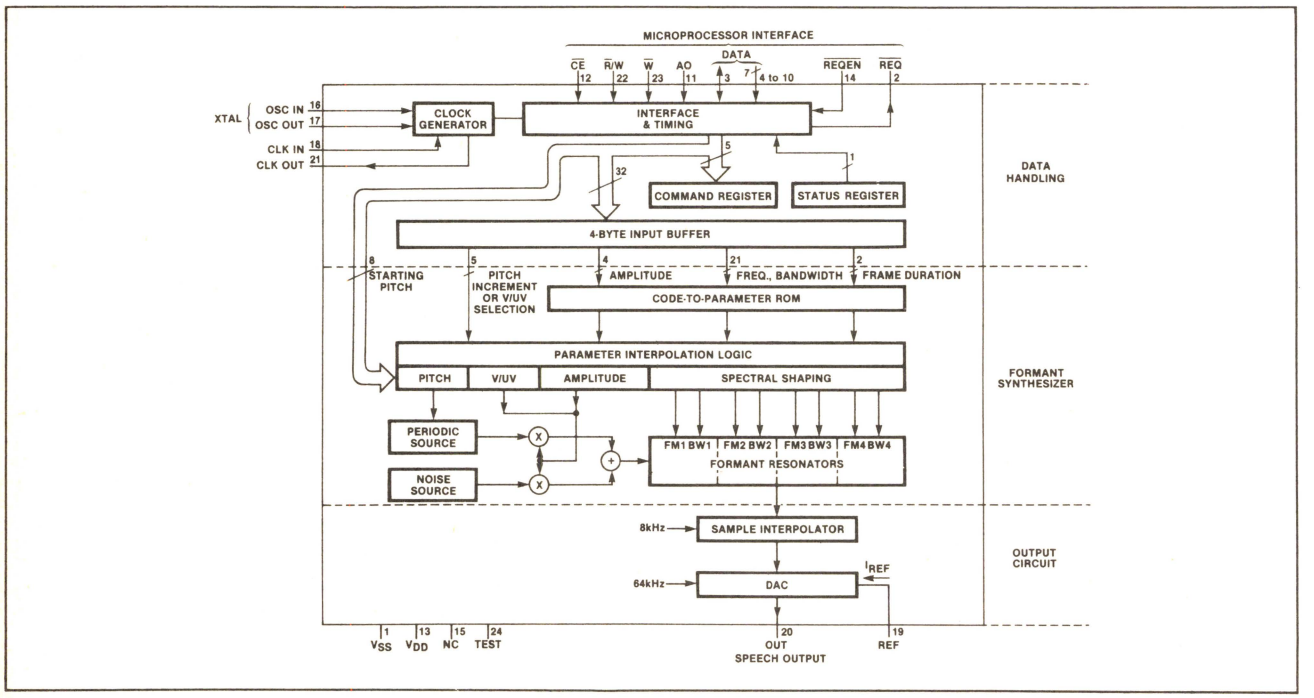
### APPLICATIONS
- **Telephony**
- **Automotive**
- **Computer response/prompt.**
- **Video games.**
- **General industrial.**

### FEATURES
- **Microprocessor interface capability including an 8-bit data bus, an enable and a read/write input control signals.**
- **32-bit data buffer holding speech frame codes.**
- **Digital filter of 8th order with 3 programmable formant frequencies, one fixed formant frequency, and 4 programmable formant bandwidths. 4 kHz bandwidth.**
- **Programmable amplitudes.**
- **Programmable duration of each frame: 8, 16, 32, or 64 milliseconds.**
- **Low data rate: average 1000 bits/sec.**
- **Operates from standard EPROMs/ROMs.**
- **Minimal external audio filter requirement.**
- **Crystal controlled oscillator or external (TTL) clock.**
- **Single +5 V power supply.**

### PIN CONFIGURATION




### BLOCK DIAGRAM





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# NE5150/5151/5152
## Triple 4-Bit RGB D/A Converter with Memory
## Triple 4-Bit RGB D/A Converter

**Linear Products**

***Preliminary Specification***

### DESCRIPTION

The NE5150/5151/5152 are triple 4-bit DACs intended for use in graphic display systems. They are a high performance — yet cost effective — means of interfacing digital memory and a CRT. The NE5150/5152 are single integrated circuit chips containing special input buffers, an ECL static RAM, high-speed latches, and three 4-bit DACs. The input buffers are user-selectable as either ECL or TTL compatible for the NE5150. The NE5152 is similar to the NE5150, but is TTL compatible only, and operates off of a single +5V supply. The RAM is organized as 16 × 12, so that 16 "color words" can be down loaded from the pixel memory into the chip memory. Each 12-bit word represents 4 bits of red, 4 bits of green and 4 bits of blue information. This system gives 4096 possible colors. The RAM is fast enough to completely reload during the horizontal retrace time. The latches resynchronize the digital data to the DACs to prevent glitches. The DACs include all the composite video functions to make the output waveforms meet RS-170 and RS-343 standards, and produce $1V_{P-P}$ into 75Ω. The composite functions (reference white, bright, blank, and sync) are latched to prevent screen-edge distortions generally found on "video DACs." External components are kept to an absolute minimum (bypass capacitors only as needed) by including all reference generation circuitry and termination resistors on-chip, by building in high-frequency PSRR (eliminating separate $V_{EE}$s and costly power supplies and filtering), and by using a single-ended clock. The guaranteed maximum operating frequency for the NE5150/5152 is 110MHz over the commercial termperature range. The devices are housed in a standard 24-pin package and consume less than 1W of power.

The NE5151 is a simplified version of the NE5150, including all functions except the memory. Maximum operating frequency is 150MHz.

### FEATURES

- **Single-chip**
- **On-board ECL static RAM**
- **4096 colors**
- **ECL and TTL compatible**
- **110MHz update rate (NE5150, 5152)**
- **150MHz update rate (NE5151)**
- **Low power and cost**
- **Drives 75Ω cable directly**
- **Internal reference**
- **40dB PSRR**
- **No external components necessary**

### APPLICATIONS

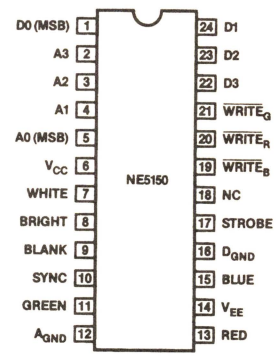
- **Bit-mapped graphics**
- **Super high-speed DAC**
- **Home computers**
- **Raster-scan displays**

### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDE CODE |
|---|---|---|
| 24-Pin Ceramic DIP | 0°C to +70°C | NE5150F |
| 24-Pin Ceramic DIP | 0°C to +70°C | NE5151F |
| 24-Pin Ceramic DIP | 0°C to +70°C | NE5152F |

### PIN CONFIGURATIONS

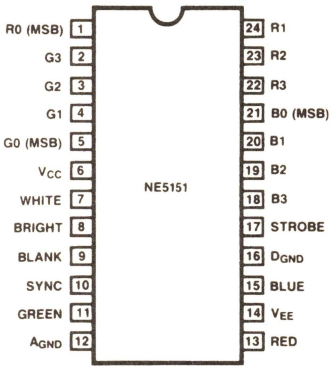
**NE5150 F Package**




CD09550S

TOP VIEW

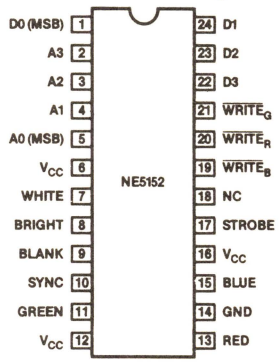
**NE5151 F Package**




CD09560S

TOP VIEW

**NE5152 F Package**



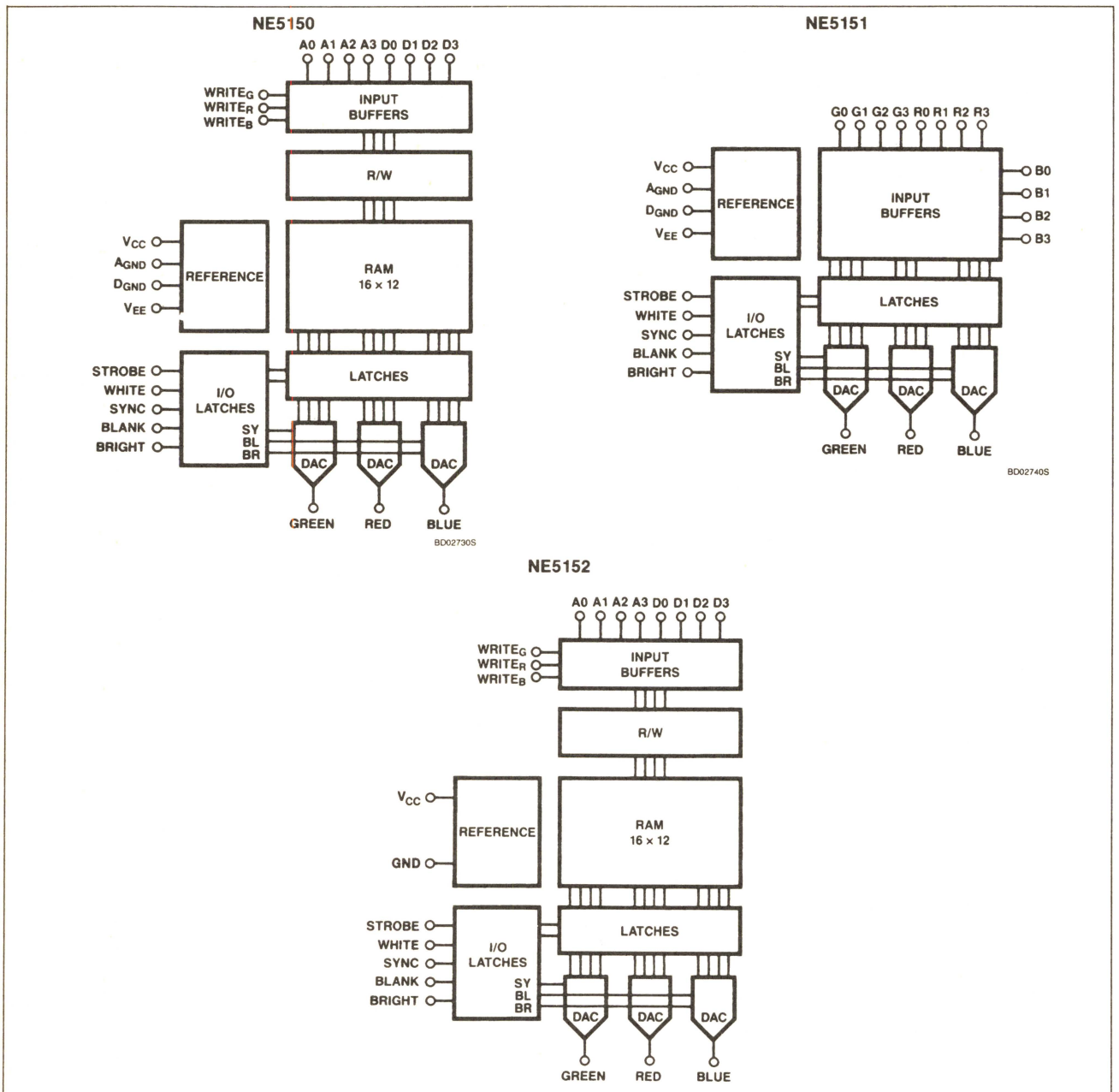

CD09570S

TOP VIEW

Signetics

# Triple 4-Bit RGB D/A Converter with Memory
# NE5150/5151/5152

## BLOCK DIAGRAMS





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# SE/NE5018
# 8-Bit μP-Compatible D/A Converter

***Product Specification***

**Linear Products**

## DESCRIPTION

The NE5018 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultralow loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew ratre buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale, while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

## FEATURES

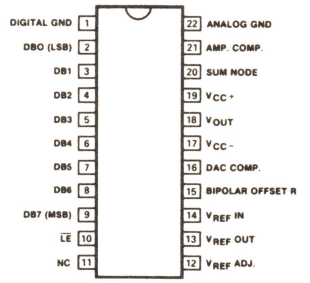
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± ½ LSB (0.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both shortcircuit protected**
- **Compatible with 8085, 6800 and many other μPs**

## APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog – digital multiplication**

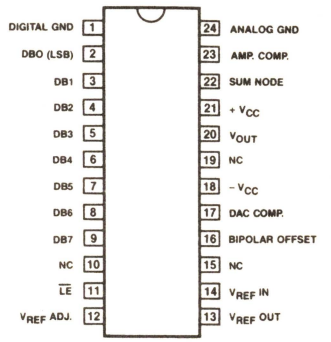
## PIN CONFIGURATIONS

**F, N Package**




CD09820S

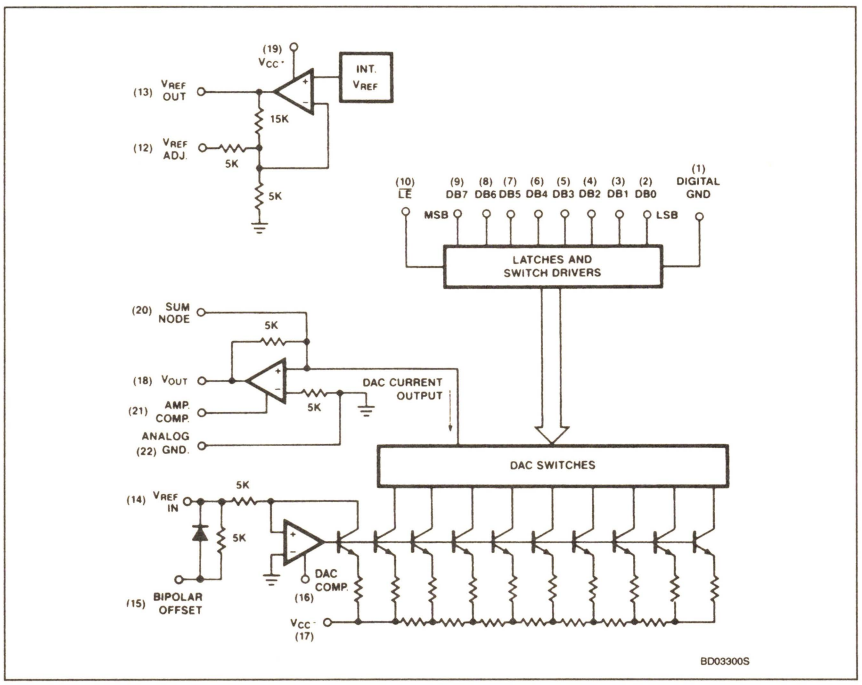
**D Package** [2]




CD09830S

**NOTES:**
1. SOL-released in large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

## BLOCK DIAGRAM




BD03300S

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# PNA7518
## 8-Bit Multiplying DAC

***Product Specification***

**Linear Products**

### DESCRIPTION

The PNA7518 is an NMOS 8-bit multiplying digital-to-analog converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analog output at a sampling rate of 30MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analog signal from a resistor chain. Two external reference voltages supply the resistor chain.

The input latches are positive edge-triggered. The output impedance is approximately 0.5kΩ depending on the applied digital code. An additional operational amplifier is required for the full bandwidth. Two's complement is selected when STC (Pin 11) is HIGH or is not connected.

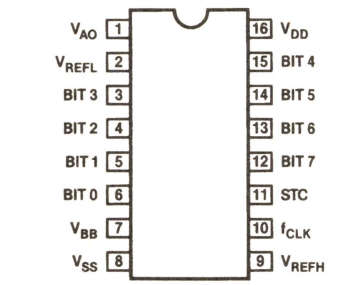
### FEATURES

- **TTL input levels**
- **Positive edge-triggered**
- **Analog voltage output at 30MHz sampling rate**
- **Binary or two's complement input**
- **Output voltage accuracy to within ± ½ of the input**

### APPLICATIONS

- **Video data conversion**
- **CRT displays**
- **Waveform/test signal generation**
- **Color/black-and-white graphics**

### PIN CONFIGURATION




TOP VIEW

CD10200S

| | | |
|---|---|---|
| 1 | $V_{AO}$ | analog output voltage |
| 2 | $V_{refL}$ | reference voltage LOW |
| 3 | bit 3 | digital voltage inputs ($V_I$) |
| 4 | bit 2 | |
| 5 | bit 1 | |
| 6 | bit 0 | least-significant bit (LSB) |
| 7 | $V_{BB}$ | back bias |
| 8 | $V_{SS}$ | ground |
| 9 | $V_{refH}$ | reference voltage HIGH |
| 10 | $f_{CLK}$ | clock input |
| 11 | STC | select two's complement |
| 12 | bit 7 | most-significant bit (MSB) |
| 13 | bit 6 | |
| 14 | bit 5 | digital voltage inputs ($V_I$) |
| 15 | bit 4 | |
| 16 | $V_{DD}$ | positive supply voltage |

### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-pin Plastic DIP | 0°C to +70°C | PNA7518N |





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# TDA5702
## 8-Bit Digital-To-Analog Converter

*Preliminary Specification*

**Linear Products**

### DESCRIPTION

The TDA5702 is an 8-bit digital to analog converter (DAC) designed for video and professional applications. The TDA5702 converts the 8-bit binary-coded digital words into an analog output signal at a sampling rate of 25MHz. The design of the TDA5702 has eliminated the need for an operational amplifier, buffer and deglitching circuit at the analog output.

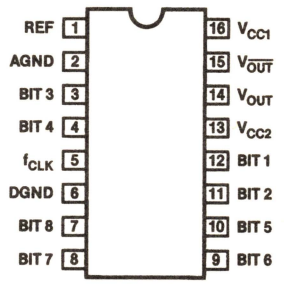
### FEATURES

- **8-bit accuracy**
- **Internal input register**
- **TTL compatible digital signals**
- **Two voltage supply connections:**
  **analog +5V**
  **digital +5V**
- **Two complementary outputs ($V_{OUT}$, $V_{\overline{OUT}}$)**
- **No deglitching circuit required**
- **Low power consumption; typically 300 mW**
- **16-lead plastic DIP**

### APPLICATIONS

- **Video data conversion**
- **Color/black-and-white graphics**
- **Waveform/test signal generation**
- **Waveform/test signal generation**

### PIN CONFIGURATION




TOP VIEW

CD10840S

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | REF | current reference loop decoupling |
| 2 | AGND | analog ground |
| 3 | Bit 3 | |
| 4 | Bit 4 | |
| 5 | $f_{CLK}$ | 25MHz clock input |
| 6 | DGND | digital ground |
| 7 | Bit 8 | most significant bit (MSB) |
| 8 | Bit 7 | |
| 9 | Bit 6 | |
| 10 | Bit 5 | |
| 11 | Bit 2 | |
| 12 | Bit 1 | least significant bit (LSB) |
| 13 | $V_{P2}$ | digital supply voltage |
| 14 | $V_{OUT}$ | analog voltage output |
| 15 | $V_{\overline{OUT}}$ | complementary analog voltage output |
| 16 | $V_{P1}$ | analog supply voltage |

### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-Pin Plastic DIP | 0 to +70°C | TDA5702N |

### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| | Supply voltages | | |
| $V_{P2}$ | at Pin 13 | 8 | V |
| $V_{P1}$ | at Pin 16 | 8 | V |
| | Input voltage | | |
| | at Pins 3, 4, 5, 7 | | |
| $V_{IN}$ | 8, 9, 10, 11 and 12 | 8 | V |
| $T_{STG}$ | Storage temperature range | −55 to +150 | °C |
| $T_J$ | Junction temperature | +125 | °C |
| $T_A$ | Operating temperature range | 0 to +70 | °C |



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# TDA5703
## Analog To Digital Converter

***Preliminary Specification***

**Linear Products**

### DESCRIPTION

The TDA5703 is an 8-bit analog to digital converter (ADC) designed for video and professional applications. The TDA5703 converts the analog input signal into 8-bit binary coded digital words at a sampling rate of up to 25MHz.

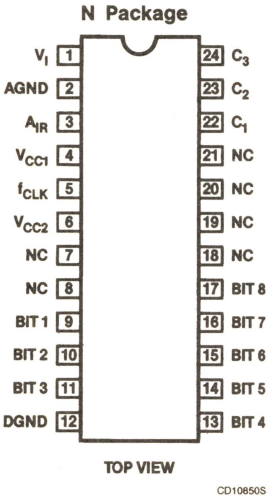
### FEATURES

- **8-bit binary coded resolution**
- **Digitizing rates up to 25MHz**
- **Internal reference**
- **Only 3 external capacitors required**
- **Two voltage supply connections: analog +5V digital +5V**
- **1V full-scale analog input (75 Ω external resistor tied to $V_{P1}$)**
- **Full-scale bandwidth; 10.5 MHz at 3 dB**
- **Low power consumption; typically 250 mW**
- **24-lead plastic DIP**

### APPLICATIONS

- **Video data conversion**

### PIN CONFIGURATION




| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | $V_I$ | Analog voltage input |
| 2 | A GND | Analog ground |
| 3 | $A_{IR}$ | Analog input reference |
| 4 | $V_{P1}$ | Analog supply voltage |
| 5 | $f_{CLK}$ | Clock input |
| 6 | $V_{P2}$ | Digital supply voltage |
| 7 | NC | Not connected |
| 8 | NC | Not connected |
| 9 | Bit 1 | Least significant bit (LSB) |
| 10 | Bit 2 | |
| 11 | Bit 3 | |
| 12 | D GND | Digital ground |
| 13 | Bit 4 | |
| 14 | Bit 5 | |
| 15 | Bit 6 | |
| 16 | Bit 7 | |
| 17 | Bit 8 | Most significant bit (MSB) |
| 18 | NC | Not connected |
| 19 | NC | Not connected |
| 20 | NC | Not connected |
| 21 | NC | Not connected |
| 22 | $C_1$ | |
| 23 | $C_2$ | Decoupling for internal reference |
| 24 | $C_3$ | |

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# PNA7509
# 7-Bit Analog-to-Digital Converter

***Preliminary Specification***

**Linear Products**

## DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analog-to-digital converter designed for video applications. The device converts the analog input signal into 7-bit binary coded digital words at a sampling rate of 22MHz.

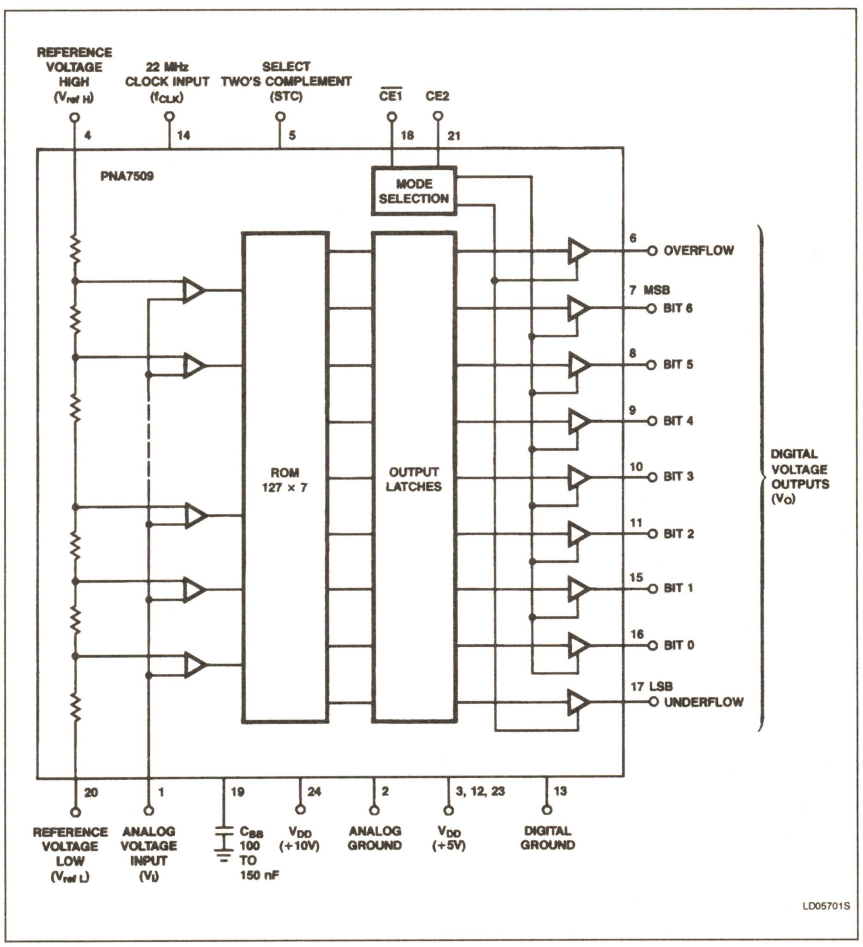
The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge-triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

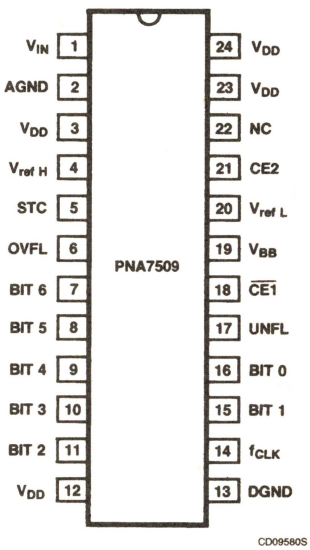
## FEATURES

- **7-bit resolution**
- **22MHz clock frequency**
- **No external sample and hold required**
- **High input impedance**
- **Binary or two's complement 3-state TTL outputs**
- **Overflow and underflow 3-state TTL outputs**
- **Low reference current (250$\mu$A typ.)**
- **Positive supply voltages (+5V, +10V)**
- **Low power consumption (400mW typ.)**
- **Available in SO Package**

## BLOCK DIAGRAM




## PIN CONFIGURATION




CD09580S

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | $V_{IN}$ | analog voltage input |
| 2 | AGND | analog ground |
| 3 | $V_{DD}$ | positive supply voltage (+5V) |
| 4 | $V_{refH}$ | reference voltage HIGH |
| 5 | STC | select two's complement |
| 6 | OVFL | overflow |
| 7 | bit 6 | most-significant bit (MSB) |
| 8 | bit 5 | |
| 9 | bit 4 | |
| 10 | bit 3 | |
| 11 | bit 2 | |
| 12 | $V_{DD}$ | positive supply voltage (+5V) |
| 13 | DGND | digital ground |
| 14 | $f_{CLK}$ | 22MHz clock input |
| 15 | bit 1 | |
| 16 | bit 0 | least-significant bit (LSB) |
| 17 | UNFL | underflow |
| 18 | $\overline{CE1}$ | chip enable input 1 |
| 19 | $V_{BB}$ | back bias output |
| 20 | $V_{refL}$ | reference voltage LOW |
| 21 | CE2 | chip enable input 2 |
| 22 | n.c. | not connected |
| 23 | $V_{DD}$ | positive supply voltage (+5V) |
| 24 | $V_{DD}$ | positive supply voltage (+10V) |

## APPLICATIONS

- **High-speed A/D conversion**
- **Video signal digitizing**
- **Radar pulse analysis**
- **High energy physics research**
- **Transient signal analysis**

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# SE/NE521
# High-Speed Dual Differential Comparator/Sense AMP

***Preliminary Specification***

**Linear Products**

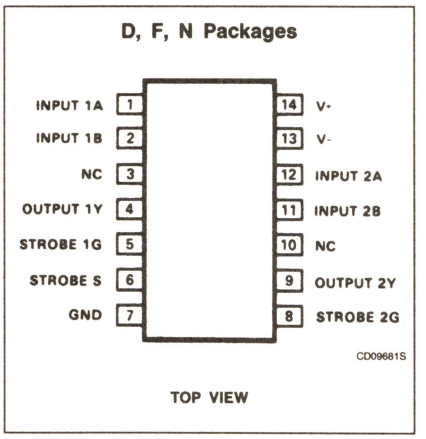
## FEATURES

- 12ns max. guaranteed propagation delay
- 20μA max. input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

## APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

## PIN CONFIGURATION




## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 14-pin Plastic DIP | | NE521N |
| 14-pin SO DIP | | NE521D |
| 14-pin Cerdip | | NE521F |
| 14-pin Cerdip | | SE521F |

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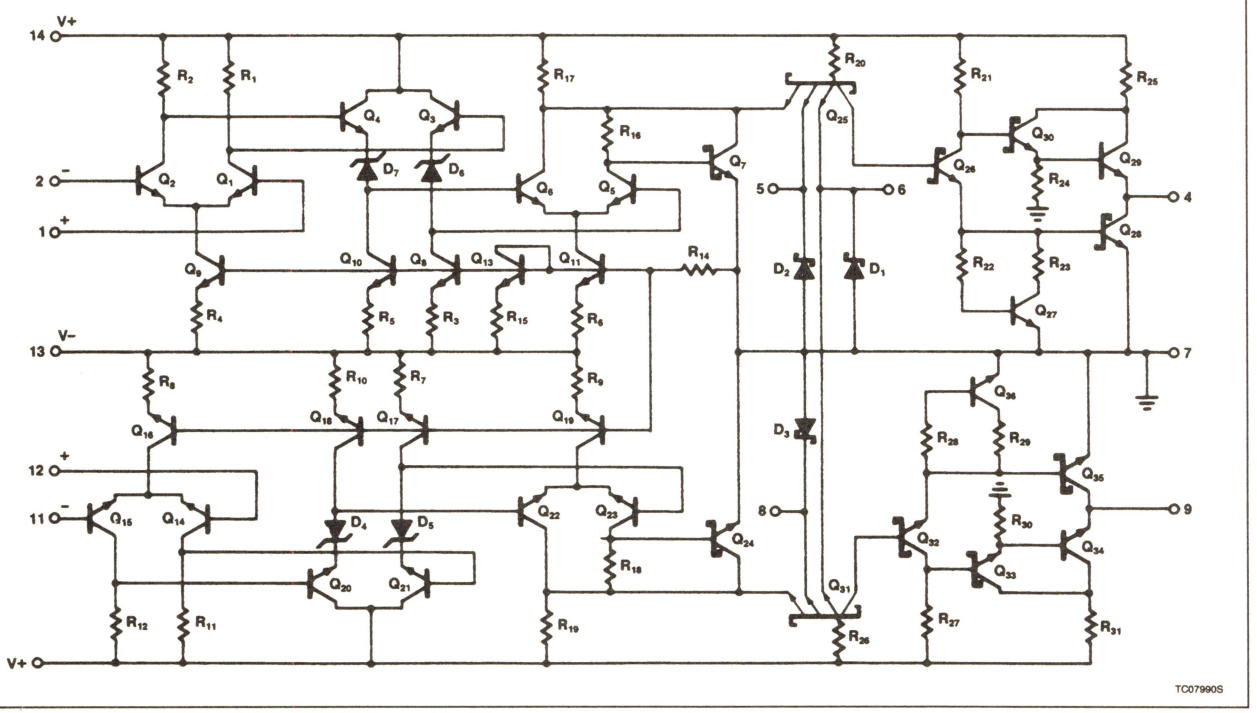
## EQUIVALENT SCHEMATIC



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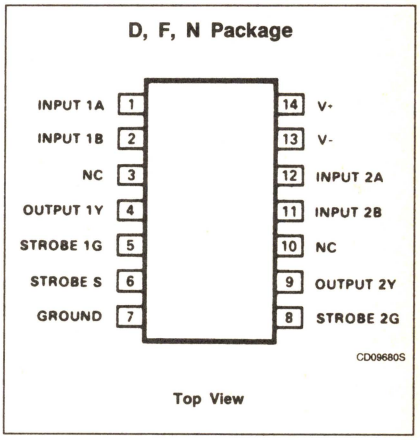
# SE/NE522
## High-Speed Dual Differential Comparator/Sense Amp

Linear Products

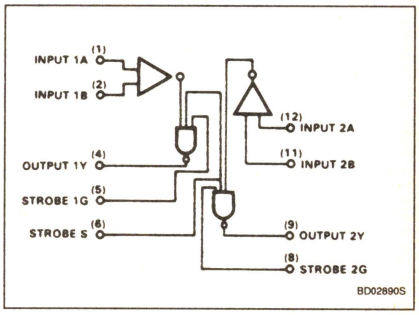
### FEATURES
- 15ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- Open collector output for wire-ORed applications
- Open collector output for wire-ORed applications
- Large common-mode input voltage range
- Operates from standard supply voltages

### APPLICATIONS
- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

### PIN CONFIGURATION




### BLOCK DIAGRAM




### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| | Supply voltage | | V |
| V+ | Positive | +7 | |
| V– | Negative | –7 | |
| $V_{IDR}$ | Differential input voltage | ±6 | V |
| $V_{IN}$ | Input voltage | | V |
| | Common-mode | ±5 | |
| | Strobe/gate | +5.25 | |
| $P_D$ | Power dissipation | 600 | mW |
| $T_A$ | Operating temperature range NE522 | 0 to 70 | °C |
| | SE522 | –55 to +125 | |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_{SOLD}$ | Lead temperature (solder, 60 sec) | +300 | °C |

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# SE/NE527
# Voltage Comparator

***Product Specification***

**Linear Products**

## DESCRIPTION

The SE/NE527 is a high-speed analog voltage comparator which, in the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates an "Emitter-Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

## FEATURES

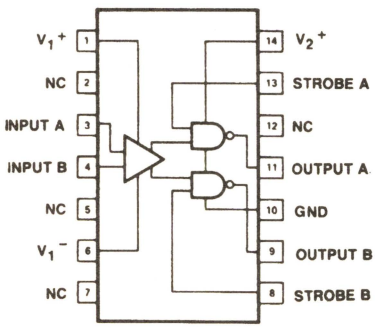
- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common-mode and differential voltage range**
- **MIL-STD 883A, B, C available**
- **Typical gain of 5000**

## APPLICATIONS

- **A/D conversion**
- **ECL-to-TTL interface**
- **TTL-to-ECL interface**
- **Memory sensing**
- **Optical data coupling**

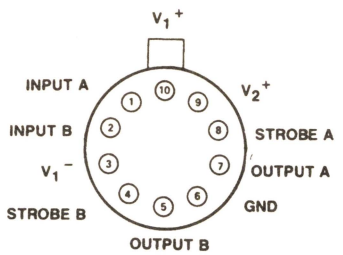
## PIN CONFIGURATIONS

**D, F, N Packages**




CD09721S

**H Package***



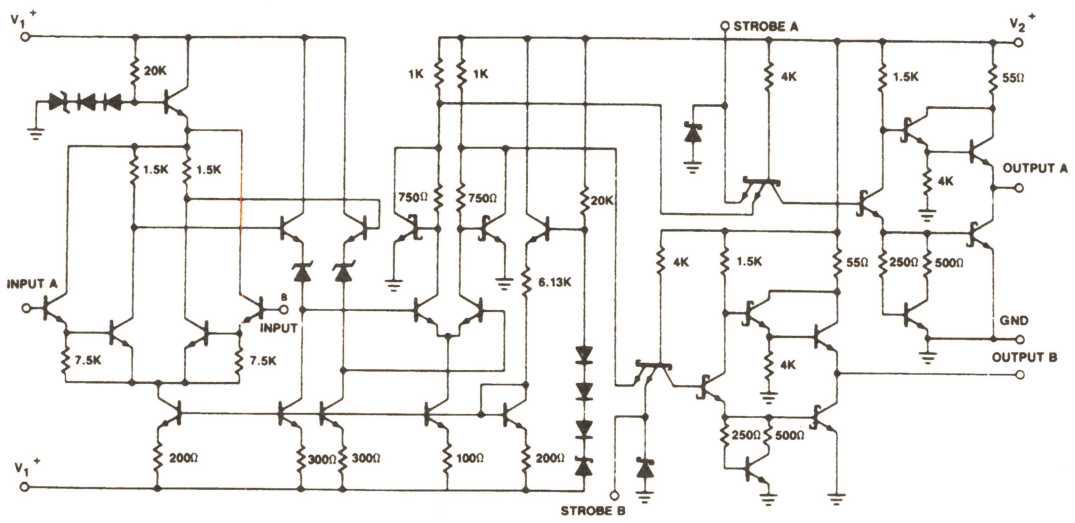

CD09730S

**NOTE:**
*Metal cans (H) not recommended for new designs.

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 14-pin Plastic DIP | | NE527N |
| 14-pin Cerdip | | NE527F |
| 14-pin SO DIP | | NE527D |
| 14-pin Cerdip | | SE527F |
| 10-lead metal can | | NE527H |
| 10-lead metal can | | SE527H |

## EQUIVALENT SCHEMATIC




TC08001S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# SE/NE529
# Voltage Comparator

***Product Specification***

**Linear Products**

## DESCRIPTION

The SE/NE529 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip.

## FEATURES

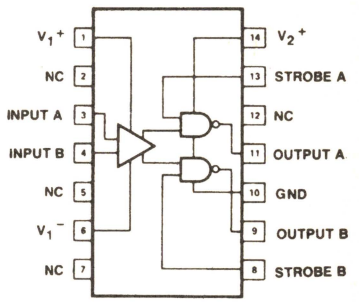
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common-mode and differential voltage range**
- **Typical gain 5000**

## APPLICATIONS

- **A/D conversion**
- **ECL-to-TTL interface**
- **TTL-to-ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **MIL-STD-883A, B, C available**

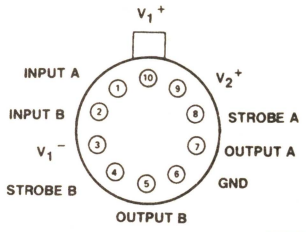
## PIN CONFIGURATIONS

**D, F, N Packages**




TOP VIEW

**H Package***

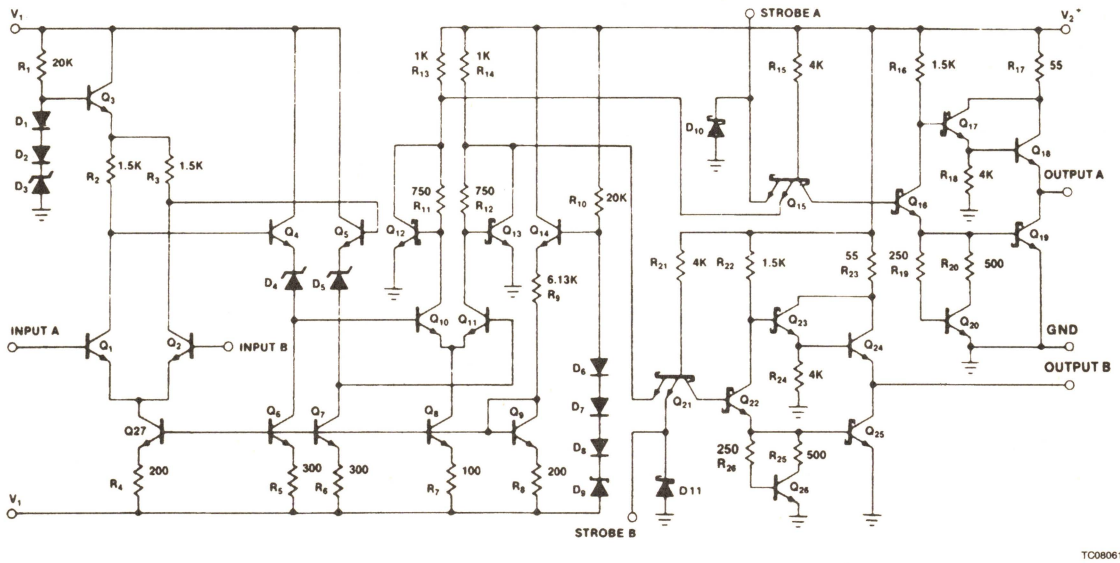



**NOTE:**
*Metal cans (H) not recommended for new designs.

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 14-pin plastic DIP | | NE529N |
| 14-pin Cerdip | | NE529F |
| 14-pin Cerdip | | SE529F |
| 14-pin SO DIP | | NE529D |
| 10-lead metal can | | NE529H |
| 10-lead metal can | | SE529H |

## EQUIVALENT SCHEMATIC

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# SE/NE5521 LVDT Signal Conditioner

*Advance Information*

**Linear Products**

## DESCRIPTION

The SE/NE5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LDVTs) and Rotary Variable Differential Transformers (RVDTs). The chip includes a low distortion, amplitude-stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output amplifier to provide amplification and filtering of the demodulated signal.

## FEATURES

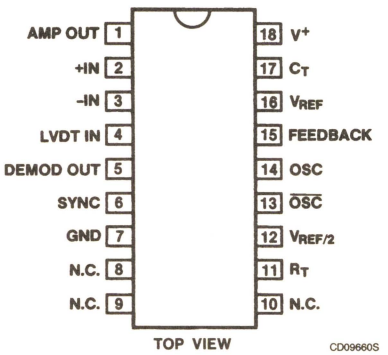
- **Low distortion**
- **Single supply 5V to 20V, or dual supply ±2.5V to ±10V**
- **Oscillator frequency 1kHz to 20kHz**
- **Capable of ratiometric operation**
- **Low power consumption (177mV typ)**

## APPLICATIONS

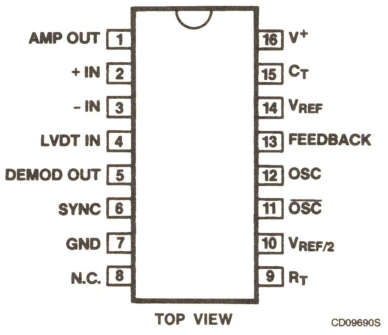
- **LVDT signal conditioning**
- **RVDT signal conditioning**
- **LPDT signal conditioning**
- **Bridge circuits**

## PIN CONFIGURATIONS

F, N Package



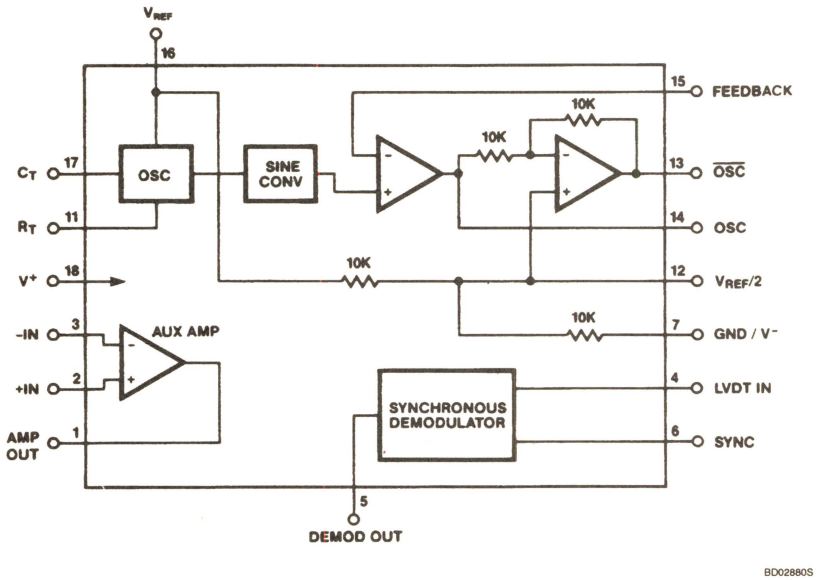

D Package




## ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 18-Pin Plastic DIP | | NE5521N |
| 18-Pin Cerdip | | NE5521F |
| 18-Pin SO DIP | | NE5521D |
| 18-Pin Plastic DIP | | SA5521N |
| 18-Pin Cerdip | | SE5521F |

## BLOCK DIAGRAM




NOTE:
Pin numbers are for F, N packages.



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# PCF8576
## Universal LCD Driver for Low Multiplex Rates

**Linear Products**

*Preliminary Specification*

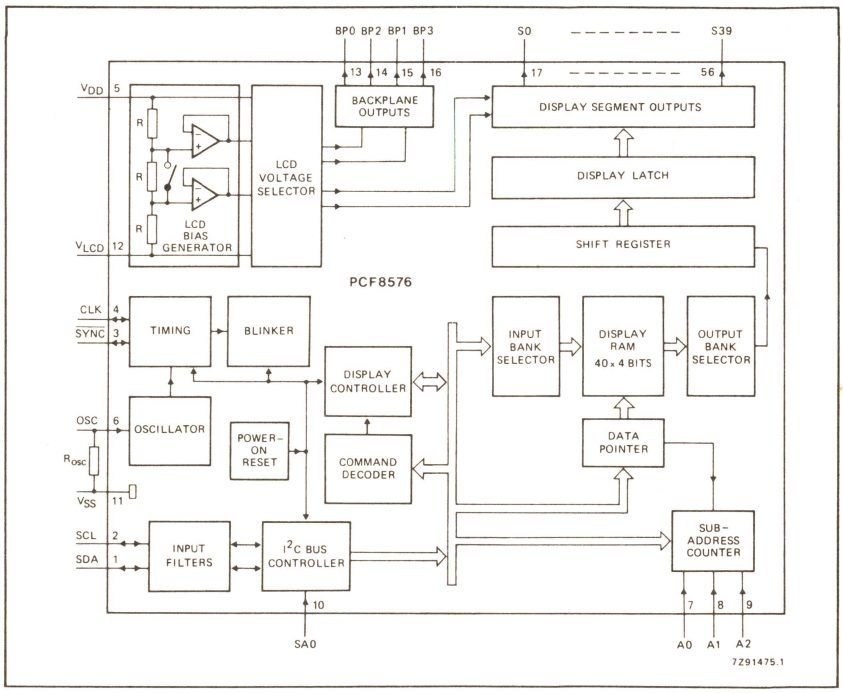
### DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors and communicates via a two-line bidirectional bus ($I^2C$). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

### FEATURES

- **Single-chip LCD controller/driver**
- **Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing**
- **Selectable display bias configuration: static, ½ or ⅓**
- **40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements**
- **40 x 4-bit RAM for display data storage**
- **Auto-incremented display data loading across device subaddress boundaries**
- **display memory bank switching in static and duplex drive modes**
- **Versatile blinking modes**
- **LCD and logic supplies may be separated**
- **Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs**
- **Low power consumption**
- **Power-saving mode for extremely low power consumption in battery-operated and telephone applications**
- **$I^2C$ bus interface**
- **TTL/CMOS compatible**
- **Compatible with any 4-bit, 8-bit or 16-bit microprocessors**
- **May be cascaded for large LCD applications (up to 2560 segments possible)**
- **Optimized pinning for single plane wiring in both single and multiple PCF8576 applications**
- **Space-saving 56-lead plastic mini-pack (VSO-56)**
- **Very low external component count (at most one resistor, even in multiple device applications)**
- **Compatible with Philips/Videlec chip-on-glass technology**
- **Manufactured in silicon gate CMOS process**

### BLOCK DIAGRAM

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# TEA1017
## 13-Bit Series – Parallel Converter

***Product Specification***

**Linear Products**

### DESCRIPTION

The TEA1017 is a bipolar integrated circuit intended to drive displays, triacs and relays and small stepper motors. The data is serially shifted into the device and is stored in 13 latches that drive the outputs.

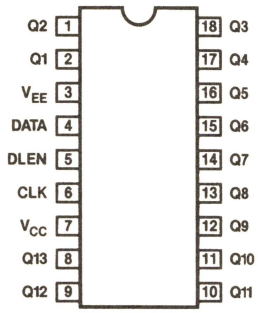
### FEATURES

- **TTL and CMOS compatible inputs**
- **Outputs drive load in both directions**
- **Power-on reset makes outputs floating**
- **Wide supply voltage range**

### APPLICATIONS

- **Driving Stepper Motors**
- **Driving Triacs**
- **Used as a Simple Switch**
- **Driving Mosaic Printhead**
- **Electronic Appliances; i.e. Washing Machines**
- **Electronic Equipment; i.e. Typewriters**
- **Relays**
- **Automotive Industry**

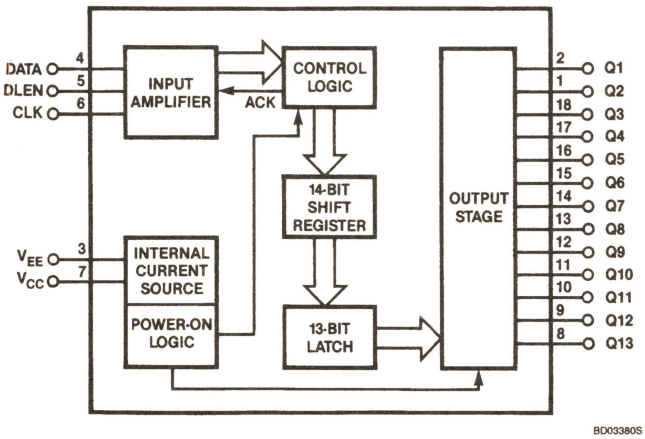
### PIN CONFIGURATION




### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 18-Pin Plastic DIP | −20°C to +80°C | TEA1017N |

### BLOCK DIAGRAM





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# SE/NE5560
## Switched-Mode Power Supply Control Circuit

*Product Specification*

**Linear Products**

### DESCRIPTION

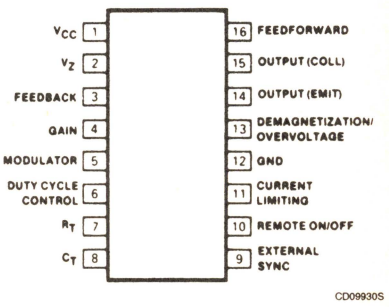
The SE/NE5560 is a control circuit for use in switched-mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched-mode power supplies, including an internal temperature-compensated reference source, internal Zener references, sawtooth generator, pulse-width modulator, output stage and various protection circuits.

### FEATURES

- **Stabilized power supply**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Pulse-width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle clamp**
- **Feed-forward control**
- **External synchronization**

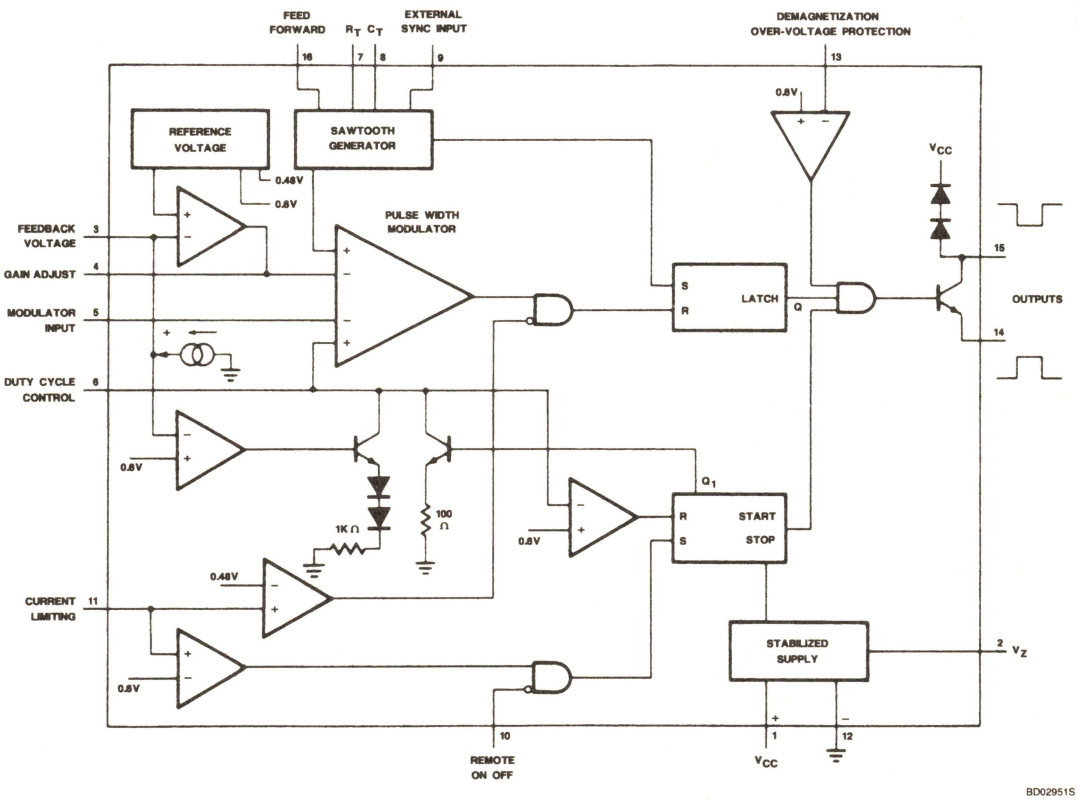
### PIN CONFIGURATION

**D, F, N Package**




**TOP VIEW**

### BLOCK DIAGRAM




**NOTE:**
1. See Voltage/Current fed supply characteristic curve.

Signetics

# SE/NE5561
## Switched-Mode Power Supply Control Circuit

*Product Specification*

**Linear Products**

### DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched-mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, overcurrent sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

### FEATURES

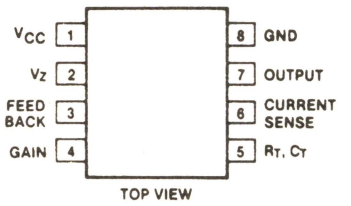
- **Micro-miniature (D) package**
- **Pulse-width modulator**
- **Current limiting (cycle-by-cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature-compensated reference**

### APPLICATIONS

- **Switched-mode power supplies**
- **D/C motor controller inverter**
- **DC/DC converter**

### PIN CONFIGURATION

**D, FE, N Packages**



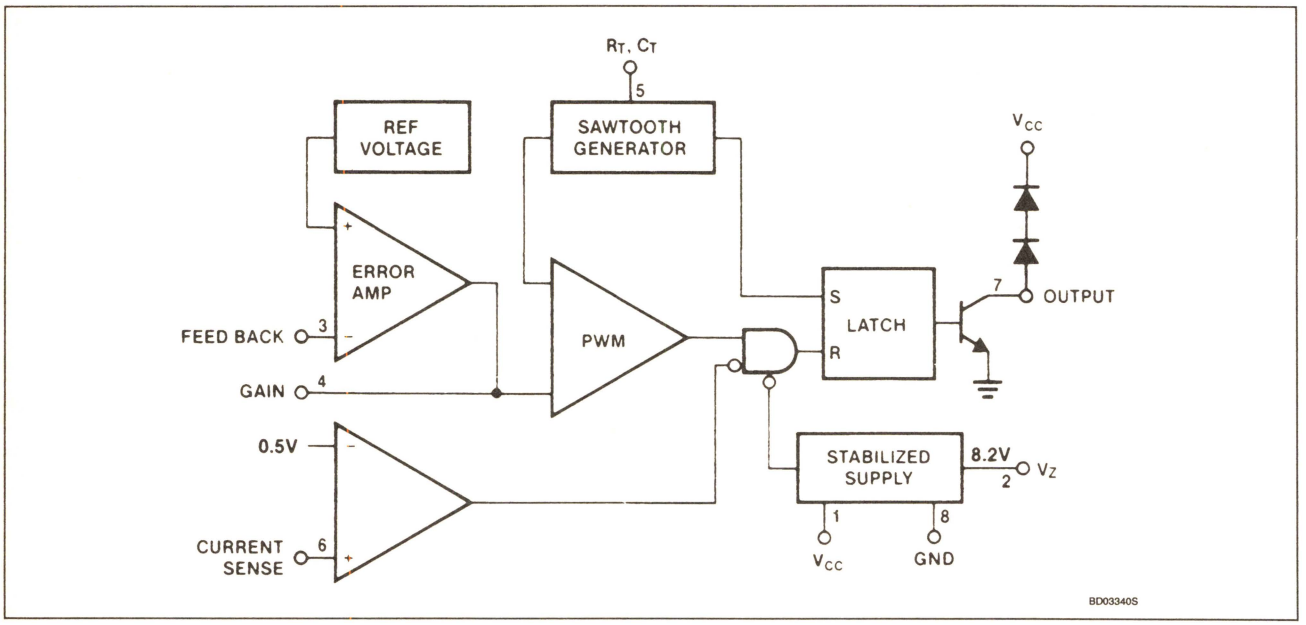

TOP VIEW

CD10190S

### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 8-pin Plastic DIP | | NE5561N |
| 8-pin Plastic DIP | | SE5561N |
| 8-pin Cerdip | | NE5561FE |
| 8-pin Cerdip | | SE5561FE |
| 8-pin SO DIP | | NE5561D |

### BLOCK DIAGRAM

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# SE/NE5562
# Switched-Mode Power Supply Control Circuit

*Preliminary Specification*

**Linear Products**

## DESCRIPTION

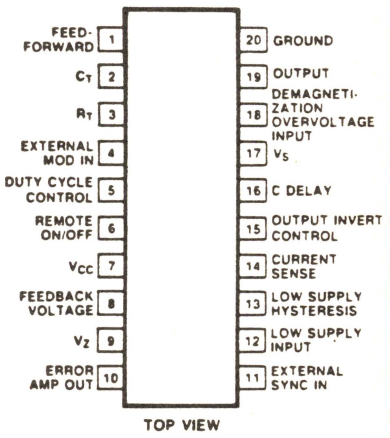
The SE/NE5562 is a single-output control circuit for Switched-Mode Power Supplies. This single monolithic IC contains all control and protection features needed for full-featured Switched-Mode Power Supplies.

## FEATURES

- **Stabilized power supply**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Pulse-width modulator**
- **Remote on/off switching**
- **Current limiting (2 levels)**
- **Low supply voltage, with adjustable hysteresis**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Duty cycle adjust and clamp**
- **Feed-forward control**
- **External synchronization**
- **Total shutdown after adjustable number of overcurrent faults**

## PIN CONFIGURATION

**D, F, N Packages**




TOP VIEW

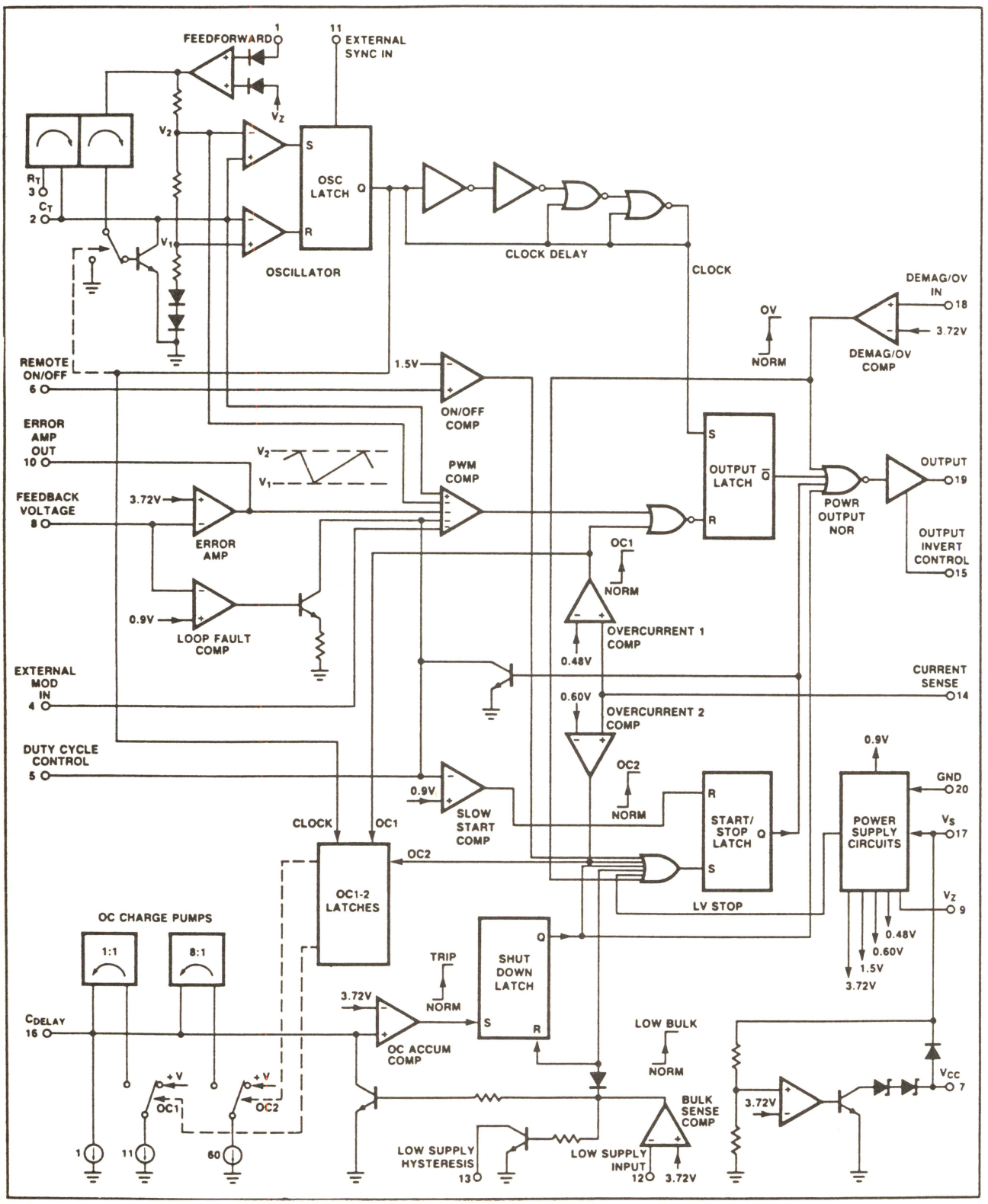
## ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 20-pin Plastic DIP | | NE5562N |
| 20-pin Plastic DIP | | SE5562N |
| 20-pin Cerdip | | NE5562F |
| 20-pin Cerdip | | SE5562F |
| 20-pin SOL DIP | | NE5562D |

# Switched-Mode Power Supply Control Circuit

# SE/NE5562

## BLOCK DIAGRAM



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# NE5568
## Switched-Mode Power Supply Controller

*Product Specification*

**Linear Products**

### DESCRIPTION

The NE5568 is a control circuit for use in switched mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low-cost SMPS applications where extensive housekeeping functions are not required. The NE5568 is a selected version of the NE5561.

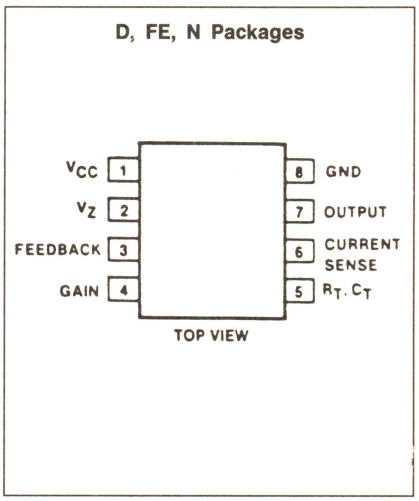
### FEATURES

- **Micro-miniature (D) package**
- **Pulse width modulator**
- **Current limiting (cycle by cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature-compensated reference**

### APPLICATIONS

- **Switch mode power supplies**
- **DC motor controller inverter**
- **DC/DC converter**

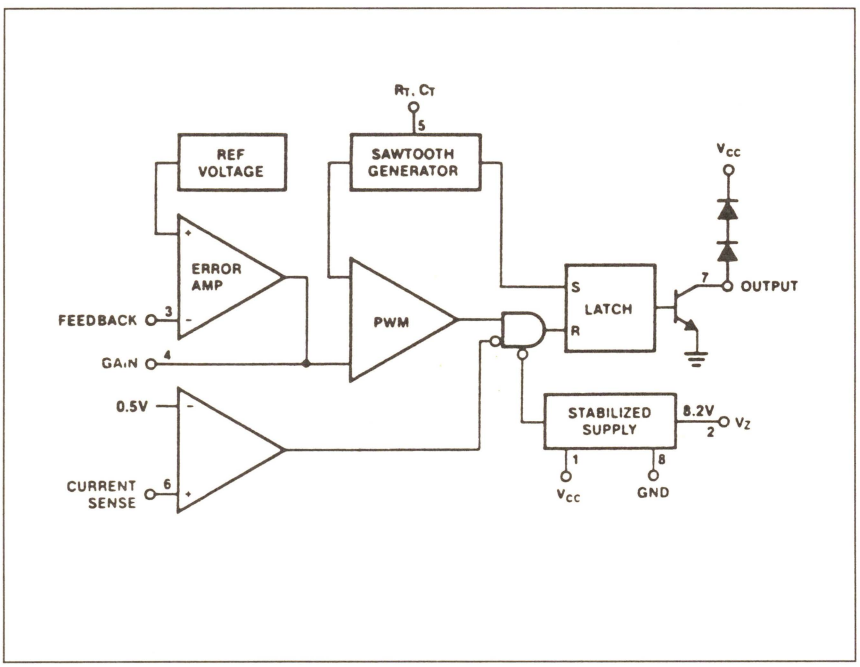
### PIN CONFIGURATION




### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 8-pin Plastic DIP | | NE5568N |
| 8-pin Cerdip | | NE5568FE |
| 8-pin SO DIP | | NE5568D |

### BLOCK DIAGRAM

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# TEA1039
# Control Circuit For Switched-Mode Power Supply

***Product Specification***

**Linear Products**

## DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g., a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

## FEATURES

- **Wide frequency range**
- **Adjustable input sensitivity**
- **Adjustable minimum frequency or maximum duty factor limit**
- **Adjustable overcurrent protection limit**
- **Supply voltage out-of-range protection**
- **Slow-start facility**

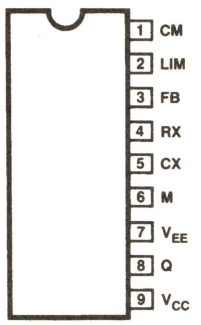
## APPLICATIONS

- **Home appliances**
- **Frequency regulation**
- **Flyback converters**
- **Forward converters**

## ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 9-pin Plastic SIP Power Package | −25°C to +125°C | TEA1039U |

## PIN CONFIGURATION




TOP VIEW

CD10370S

**PINNING**

| | | |
|---|---|---|
| 1 | CM | overcurrent protection input |
| 2 | LIM | limit setting input |
| 3 | FB | feedback input |
| 4 | RX | external resistor connection |
| 5 | CX | external capacitor connection |
| 6 | M | mode input |
| 7 | $V_{EE}$ | common |
| 8 | Q | output |
| 9 | $V_{CC}$ | positive supply connection |





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# TDA2595
## Horizontal Combination

Linear Products

### DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in color television receivers.

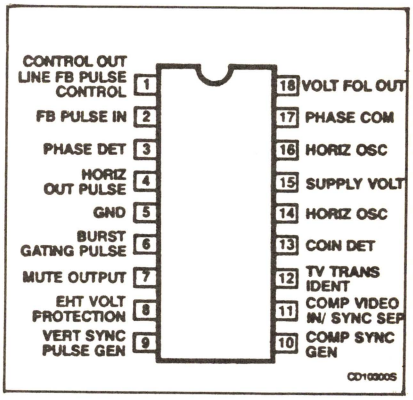
### FEATURES

- Positive video input; capacitively coupled (source impedance < 200Ω)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- $\varphi_1$ phase control between horizontal sync and oscillator
- Coincidence detector $\varphi_3$ for automatic time constant switching; overruled by the VCR switch
- Time constant switch between two external time constants for loop gain; both controlled by the coincidence detector $\varphi_3$
- $\varphi_1$ gating pulse controlled by coincidence detector $\varphi_3$
- Mute circuit depending on TV transmitter identification
- $\varphi_2$ phase control between line flyback and oscillator; the slicing levels for $\varphi_2$ control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4V or higher than 8V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot suppressor controlled by the line flyback control

### APPLICATIONS

- Television receivers
- Video receivers

### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 18-Pin Plastic DIP SOT102CS | −20 to +70°C | TDA2595N |

# TDA2653A
# Vertical Deflection

***Product Specification***

**Linear Products**

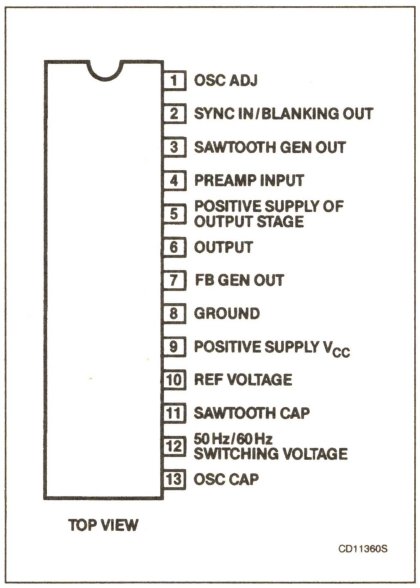
## DESCRIPTION

The TDA2653A is a monolithic integrated circuit for vertical deflection in video monitors and large screen color television receivers, e.g. 30AX and PIL-S4 systems.

## FEATURES

- **Oscillator; switch capability for 50Hz/60Hz operation**
- **Synchronization circuit**
- **Blanking pulse generator with guard circuit**
- **Sawtooth generator with buffer stage**
- **Preamplifier with fed-out inputs**
- **Output stage with thermal and short-circuit protection**
- **Flyback generator**
- **Voltage stabilizer**

## PIN CONFIGURATION




1, 13 Oscillator

The oscillator frequency is determined by a potentiometer at Pin 1 and a capacitor at Pin 13.

2 Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1V and 12V. The integrated frequency detector delivers a switching level at Pin 12.

The blanking pulse amplitude is 20V with a load of 1mA.

3 Sawtooth generator output

The sawtooth signal is fed via a buffer stage to Pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to Pin 11 (linearity) and via a resistor to Pin 4 (preamplifier).

4 Preamplifier input

The DC voltage is proportional to the output voltage (DC feedback). The AC voltage is proportional to the sum of the buffered sawtooth voltage at Pin 3 and the voltage, with opposite polarity, at the feedback resistor (AC feedback).

5 Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between Pins 7 and 5, and a diode between Pins 5 and 9 have to be connected for proper operation of the flyback generator.

6 Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7 Flyback generator output

An electrolytic capacitor has to be connected between Pins 7 and 5 to complete the flyback generator.

8 Negative supply (ground)

Negative supply of output stage and small signal part.

9 Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

10 Reference voltage of preamplifier

External adjustment and decoupling of reference voltage of the preamplifier.

11 Sawtooth capacitor

This sawtooth capacitor has been split to realize linearity control.

12 50Hz/60Hz switching level

This pin delivers a LOW voltage level for 50Hz and a HIGH voltage level for 60Hz. The amplitudes of the sawtooth signals can be made equal for 50Hz and 60Hz with these levels.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# TDA2579
## Synchronization Circuit

*Product Specification*

**Linear Products**

### DESCRIPTION

The TDA2579 generates and synchronizes horizontal and vertical signals. The device has a 3-level sandcastle output, a transmitter identification signal and also 50/60Hz identification.

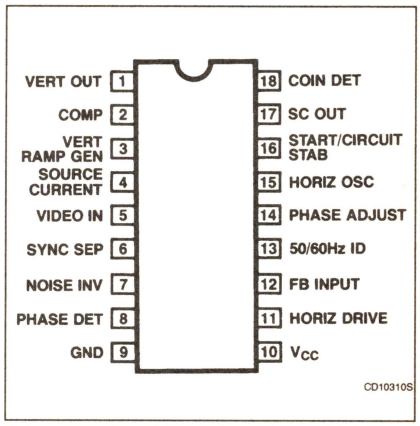
### FEATURES

- **Horizontal phase detector, (sync to osc), sync separator and noise inverter**
- **Triple current source in the phase detector with automatic selection**
- **Inhibit of horizontal phase detector and video transmitter identification**
- **Second phase detector for storage compensation of the horizontal output stage**
- **Stabilized direct starting of the horizontal oscillator and output stage**
- **Horizontal output pulse with constant duty cycle value of 29$\mu$s**
- **Duty factor of the horizontal output pulse is 50% when horizontal flyback pulse is absent**
- **Internal vertical sync separator and two integration selection times**
- **Divider system with three different reset enable windows**
- **Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified**
- **Vertical comparator with a low DC feedback signal**
- **50/60Hz identification output combined with mute function**
- **Automatic amplitude adjustment for 50 and 60Hz and blanking pulse duration**

### APPLICATIONS

- **Video Terminals**
- **Television**
- **Video Tape Recorder**

### PIN CONFIGURATION




### ORDERING CODE

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-pin Plastic DIP | 0°C to +70°C | TDA2579N |

Signetics

# TDA3651A/AQ/3653
## Vertical Deflection

***Product Specification***

**Linear Products**

### DESCRIPTION

The TDA3651A/AQ is a vertical deflection output circuit for drive of various deflection systems with deflector currents up to 2A peak-to-peak.

### FEATURES

- **Driver**
- **Output stage**
- **Thermal protection and output stage protection**
- **Flyback generator**
- **Voltage stabilizer**

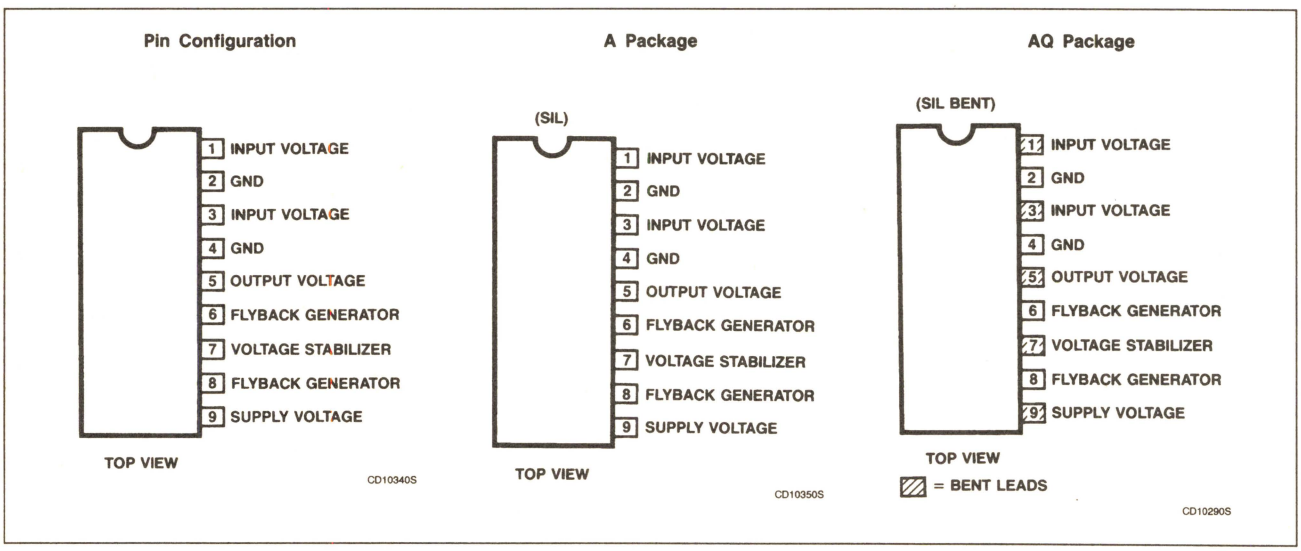
### APPLICATIONS

- **Video terminals**
- **Television**

### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 9-Pin Plastic SIP | 0 to 70°C | TDA3651A<br>TDA3653A |
| 9-Pin Plastic SIP BENT to DIP | 0 to 70°C | TDA3651AQ<br>TDA3653AQ |

### PIN CONFIGURATION



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# PCF8573
## Clock/Calendar With Serial I/O

***Product Specification***

**Linear Products**

### DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real-time clock/calendar in the Inter IC ($I^2C$) bus-oriented microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two-line bidirectional bus ($I^2C$). Back-up for the clock during supply interruptions is provided by a 1.2V nickel cadmium battery. The time base is generated from a 32.768kHz crystal-controlled oscillator.

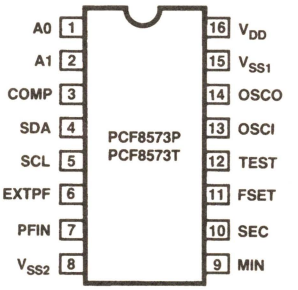
### FEATURES

- **Serial input/output has ($I^2C$) interface for minutes, hours, days and months**
- **Additional pulse outputs for seconds and minutes**
- **Alarm register for presetting a time for alarm or remote switching functions**
- **Battery back-up for clock function during supply interruption**
- **Crystal oscillator control (32.768kHz)**

### APPLICATIONS

- **Automotive**
- **Telephony**

### PIN CONFIGURATION




TOP VIEW

CD10280S

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | A0 | Address input |
| 2 | A1 | Address input |
| 3 | COMP | Comparator output |
| 4 | SDA | Serial data line ($I^2C$ bus) |
| 5 | SCL | Serial clock line ($I^2C$ bus) |
| 6 | EXTPF | Enable power fail flag input |
| 7 | PFIN | Power fail flag input |
| 8 | $V_{SS2}$ | Negative supply 2 ($I^2C$ interface) |
| 9 | MIN | One pulse per minute output |
| 10 | SEC | One pulse per second output |
| 11 | FSET | Oscillator tuning output |
| 12 | TEST | Test input; must be connected to $V_{SS2}$ when not in use |
| 13 | OSCI | Oscillator input |
| 14 | OSCO | Oscillator input/output |
| 15 | $V_{SS1}$ | Negative supply 1 (clock) |
| 16 | $V_{DD}$ | Common positive supply |

### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-pin Plastic DIP | −40°C to +85°C | PCF8573PN |
| 16-pin Plastic SO | −40°C to +85°C | PCF8573TD |

### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{DD}$ | Supply voltage range (clock) | −0.3 to 8 | V |
| $V_{SS2}$ | Supply voltage range ($I^2C$ interface) | −0.3 to 8 | V |
| $I_{IN}$ | Input current | 10 | mA |
| $I_{OUT}$ | Output current | 10 | mA |
| $P_D$ | Total Power Dissipation per package | 200 | mW |
| $T_A$ | Operating Ambient Temperature | −40 to 85 | °C |
| $T_{STG}$ | Storage Temperature | −55 to 125 | °C |

# Signetics

# SAF3019P
## Clock/Timer

***Product Specification***

**Linear Products**



## DESCRIPTION

The SAF3019 is a CMOS integrated circuit comprising a digital clock for minutes, hours, days and months, as well as an additional register for resetting. The time counter provides cycles of 28, 30 or 31 days automatically, depending on the length of the month.

The time reference is the 50 Hz mains frequency or a 32.768 Hz on-chip reference oscillator with an external crystal. If the 50 Hz mains frequency is interrupted, the circuit is automatically switched to crystal oscillator operation.

The circuit can be controlled by a microcomputer. The data transmission (e.g., TIME SET and TIME READ of the time counter and time register) is achieved via the CBUS. A microcomputer then controls the data processing and the display unit drive.

The circuit uses a 5V supply for data transmission. If the 5V supply is interrupted, the clock function is maintained by a 1.5V battery. The clock can then continue to function for an extended period, because the battery load current is only a few microamperes.

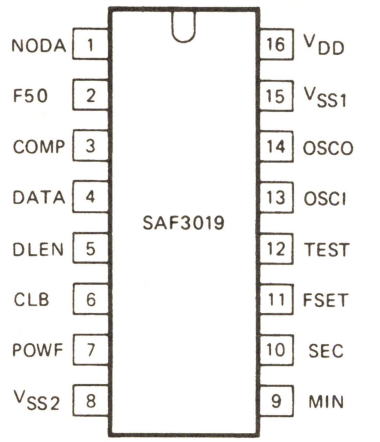
## FEATURES

- **Serial bidirectional CBUS interface for input/output of minutes, hours, day and month**
- **Additional pulse outputs for seconds and minutes**
- **Time register for presetting a time for alarm or remote switching functions**
- **Battery back-up for clock function during supply interruption**
- **Controlled either by the 50Hz mains frequency or a crystal oscillator (automatic switch)**

## APPLICATIONS

- **Clock displays**
- **Timers**
- **Appliances**
- **Control Systems**

## PIN CONFIGURATION




| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 16 | $V_{DD}$ | common positive supply (5V; $V_B$ = 1.5V) |
| 15 | $V_{SS1}$ | negative battery supply ($V_B$) |
| 8 | $V_{SS2}$ | ground ($V_{DD}$) |
| 4 | DATA | data input/output |
| 5 | DLEN | data line enable input CBUS (bidirectional) |
| 6 | CLB | clock burst input |
| 1 | NODA | comparator mode select input |
| 12 | TEST | test mode input (normally ground) |
| 2 | F50 | 50Hz mains frequency input |
| 13 | OSCI | input and output of the on-chip oscillator |
| 14 | OSCO | |
| 10 | SEC | 1 pulse per second output |
| 9 | MIN | 1 pulse per minute output |
| 3 | COMP | comparator output |
| 7 | POWF | power failure output |
| 11 | FSET | frequency setting signal output (128Hz) |

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-pin Plastic DIP | −40 to 85°C | SAF3019P |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# PIN-FOR-PIN FUNCTIONALLY-COMPATIBLE CROSS REFERENCE BY COMPETITOR

Linear Products

| COMPETITOR | COMPETITOR PART NUMBER | SIGNETICS PART NUMBER | TEMPERATURE (°C) | PACKAGE |
|---|---|---|---|---|
| AMD | AM6012DC | AM6012F | 0 to +70 | Ceramic |
| | DAC08AQ | DAC08AF | −55 to +125 | Ceramic |
| | DAC08CN | DAC08CN | 0 to +70 | Plastic |
| | DAC08CQ | DAC08CF | 0 to +70 | Ceramic |
| | DAC08EN | DAC08EN | 0 to +70 | Plastic |
| | DAC08EQ | DAC08EF | 0 to +70 | Ceramic |
| | DAC08HN | DAC08HN | 0 to +70 | Plastic |
| | DAC08HQ | DAC08HF | 0 to +70 | Ceramic |
| | DAC08Q | DAC08F | −55 to +125 | Ceramic |
| | LF198H | SE5537H | −55 to +125 | Metal can |
| | LF398H | NE5537H | 0 to +70 | Metal can |
| | LF398L | NE5537D | 0 to +70 | SO |
| | LF398N | NE5537N | 0 to +70 | Plastic |
| Datel | AM4532 | NE5534AF | 0 to +70 | Ceramic |
| | AM4532C | NE5534AF | 0 to +70 | Ceramic |
| | AM4532M | SE5534AF | −55 to +125 | Ceramic |
| | DACUP10BC | NE5020N | 0 to +70 | Plastic |
| | DACUP8BC | NE5018N | 0 to +70 | Plastic |
| | DACUP8BM | SE5019F | −55 to +125 | Ceramic |
| | DACUP8BQ | SE5018F | −55 to +125 | Ceramic |
| Exar | XR5532/A N | NE5532/AF | 0 to +70 | Ceramic |
| | XR5532/A P | NE5532/AN | 0 to +70 | Plastic |
| | XRL567CN | NE567F | 0 to +70 | Ceramic |
| | XRL567CP | NE567N | 0 to +70 | Plastic |
| | XR5534/A CN | NE5534/AF | 0 to +70 | Ceramic |
| | XR5534/A CP | NE5534/AN | 0 to +70 | Plastic |
| | XR5534/A M | SE5534/AF | −55 to +125 | Ceramic |
| | XR558CN | NE558F | 0 to +70 | Ceramic |
| | XR558CP | NE558N | 0 to +70 | Plastic |
| | XR558M | SE558F | −55 to +125 | Ceramic |
| | XR1524N | SG3524F | 0 to +70 | Ceramic |
| | XR1524P | SG3524N | 0 to +70 | Plastic |
| | XR2524P | SG3524N | 0 to +70 | Plastic |
| | XR3524N | SG3524F | 0 to +70 | Ceramic |
| | XR3524P | SG3524N | 0 to +70 | Plastic |
| Fairchild | μA080/DA | DAC08F | 0 to +70 | Ceramic |
| | μA0801CDC | MC1408F | 0 to +70 | Ceramic |
| | μA0801CPC | MC1408N | 0 to +70 | Plastic |
| | μA0801EDC | DAC08EF | 0 to +70 | Ceramic |
| | μA0801EPC | DAC08AF | 0 to +70 | Ceramic |
| | μA1458HC | MC1458H | 0 to +70 | Metal can |
| | μA1458TC | MC1458N | 0 to +70 | Plastic |
| | μA1488DC | MC1488F | 0 to +70 | Ceramic |
| | μA1488PC | MC1488N | 0 to +70 | Plastic |
| | μA1489/A DC | MC1489/AF | 0 to +70 | Ceramic |



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# Pin-for-Pin Functionally-Compatible Cross Reference by Competitor

| COMPETITOR | COMPETITOR PART NUMBER | SIGNETICS PART NUMBER | TEMPERATURE (°C) | PACKAGE |
|---|---|---|---|---|
| **Fairchild (Cont.)** | μA1489/A PC | MC1489/AN | 0 to +70 | Plastic |
| | μA198HM | NE5537H | 0 to +70 | Metal can |
| | μA198RM | NE5537N | 0 to +70 | Plastic |
| | μA2901DC | LM2901F | −40 to +85 | Ceramic |
| | μA2901PC | LM2901N | −40 to +85 | Plastic |
| | μA311RC | LM311F | 0 to +70 | Ceramic |
| | μA324DC | LM324F | 0 to +70 | Ceramic |
| | μA324PC | LM324N | 0 to +70 | Plastic |
| | μA3302DC | MC3302F | −40 to +85 | Ceramic |
| | μA3302PC | MC3302N | −40 to +85 | Plastic |
| | μA339/A DC | LM339/AF | 0 to +70 | Ceramic |
| | μA339/A PC | LM339/AN | 0 to +70 | Plastic |
| | μA3403DC | MC3403F | 0 to +70 | Ceramic |
| | μA3403PC | MC3403N | 0 to +70 | Plastic |
| | μA398HC | SE5537H | −55 to +125 | Metal Can |
| | μA398RC | SE5537N | −55 to +125 | Plastic |
| | μA555TC | NE555N | 0 to +70 | Plastic |
| | μA556PC | NE556-1N | 0 to +70 | Plastic |
| | | NE556N | 0 to +70 | Plastic |
| | μA723DC | μA723CF | 0 to +70 | Ceramic |
| | μA723DM | μA723F | −55 to +125 | Ceramic |
| | μA723HC | μA723CH | 0 to +70 | Metal Can |
| | μA723HM | μA723H | −55 to +125 | Metal Can |
| | μA723PC | μA723CN | 0 to +70 | Plastic |
| | μA733DC | μA733F | 0 to +70 | Ceramic |
| | μA733DM | μA733F | −55 to +125 | Ceramic |
| | μA733PC | μA733N | 0 to +70 | Plastic |
| | μA741HC | NE530H | 0 to +70 | Metal can |
| | μA741HM | SE530H | −55 to +125 | Metal can |
| | μA741NM | μA741N | −55 to +125 | Plastic |
| | μA741RC | μA741CF | 0 to +70 | Ceramic |
| | μA741TC | μA741CN | 0 to +70 | Plastic |
| | μA747DC | μA747CF | 0 to +70 | Ceramic |
| | μA747PC | μA747CN | 0 to +70 | Plastic |
| | μA9667DC | ULN2003F | 0 to +70 | Ceramic |
| | μA9667PC | ULN2003N | 0 to +70 | Plastic |
| | μA9668DC | ULN2004F | 0 to +70 | Ceramic |
| | μA9668PC | ULN2004N | 0 to +70 | Plastic |
| **Harris** | HA2539 | NE5539 | 0 to +70 | Plastic |
| | HA15102-2 | SE5532/AF | −55 to +125 | Ceramic |
| | HA15102-5 | NE5532/AF | 0 to +70 | Ceramic |
| | HA15135-2 | SE5534/AF | −55 to +125 | Ceramic |
| | HA15135-5 | NE5534/AF | 0 to +70 | Ceramic |
| | HA35102-5 | NE5532/AN | 0 to +70 | Plastic |
| **Intersil** | ADC0803LCD | ADC0803-1LCF | −40 to +85 | Ceramic |
| | ADC0804 | ADC0804-1C | 0 to +70 | Plastic |
| | ADC0805 | ADC0805-1LC | −40 to +85 | Plastic |
| **Motorola** | DAC08CD | DAC08CN | 0 to +70 | Plastic |
| | DAC08CQ | DAC08CF | 0 to +70 | Ceramic |
| | DAC08ED | DAC08EN | 0 to +70 | Plastic |
| | DAC08EF | DAC08EF | 0 to +70 | Ceramic |
| | DAC08HQ | DAC08HF | 0 to +70 | Ceramic |





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# Pin-for-Pin Functionally-Compatible Cross Reference by Competitor

| COMPETITOR | COMPETITOR PART NUMBER | SIGNETICS PART NUMBER | TEMPERATURE (°C) | PACKAGE |
|---|---|---|---|---|
| **Motorola (Cont.)** | DAC08Q | DAC08F | – 55 to +125 | Ceramic |
| | LM2901N | LM2901N | – 40 to +85 | Plastic |
| | LM311J-8 | LM311F | 0 to +70 | Ceramic |
| | LM311N | LM311N | 0 to +70 | Plastic |
| | LM324J | LM324F | 0 to +70 | Ceramic |
| | LM324N | LM324N | 0 to +70 | Plastic |
| | LM339/A J | LM339/AF | 0 to +70 | Ceramic |
| | LM339/A N | LM339/AN | 0 to +70 | Plastic |
| | LM358H | LM358H | 0 to +70 | Metal can |
| | LM358N | LM358N | 0 to +70 | Plastic |
| | LM393A/J | LM393/AF | 0 to +70 | Ceramic |
| | LM393A/N | LM393/AN | 0 to +70 | Plastic |
| | MC1408L | MC1408F | 0 to +70 | Ceramic |
| | MC1408P | MC1408N | 0 to +70 | Plastic |
| | MC1488L | MC1488F | 0 to +70 | Ceramic |
| | MC1488P | MC1488N | 0 to +70 | Plastic |
| | MC1489/A L | MC1489/AF | 0 to +70 | Ceramic |
| | MC1489/A P | MC1489/AN | 0 to +70 | Plastic |
| | MC1496L | MC1496F | 0 to +70 | Ceramic |
| | MC1496P | MC1496N | 0 to +70 | Plastic |
| | MC3302L | MC3302F | – 40 to +85 | Ceramic |
| | MC3302P | MC3302N | – 40 to +85 | Plastic |
| | MC3403L | MC3403F | 0 to +70 | Ceramic |
| | MC3403P | MC3403N | 0 to +70 | Plastic |
| | MC3410CL | MC3410CN | 0 to +70 | Ceramic |
| | MC3410L | MC3410N or NE5410N | 0 to +70 | Ceramic |
| | MC3510L | SE5410F | – 55 to +125 | Ceramic |
| | NE592F | NE592F | 0 to +70 | Ceramic |
| | NE592N | NE592N | 0 to +70 | Plastic |
| | NE565N | NE565N | 0 to +70 | Plastic |
| | SE592F | SE592F | – 55 to +125 | Ceramic |
| | SE592H | SE592H | – 55 to +125 | Metal can |
| **National** | ADC0803F | ADC0803-1LCF | – 40 to +85 | Ceramic |
| | ADC0803N | ADC0803-1LCN | – 40 to +85 | Plastic |
| | ADC0805 | ADC0805-1LC | – 40 to +85 | Plastic |
| | DAC08AQ | DAC08AF | – 55 to +125 | Ceramic |
| | DAC08CD | DAC08CN | 0 to +70 | Plastic |
| | DAC08CQ | DAC08CF | 0 to +70 | Ceramic |
| | DAC08ED | DAC08EN | 0 to +70 | Plastic |
| | DAC08HQ | DAC08HF | 0 to +70 | Ceramic |
| | DAC08Q | DAC08F | – 55 to +125 | Ceramic |
| | DAC0808LCJ | MC1408F | 0 to +70 | Ceramic |
| | DAC0808LCN | MC1408N | 0 to +70 | Plastic |
| | DAC0808LD | MC1408F | 0 to +70 | Ceramic |
| | LF198/A H | SE5537H | – 55 to +125 | Metal can |
| | LF398/A H | NE5537H | 0 to +70 | Metal can |
| | LF398/A N | NE5537N | 0 to +70 | Plastic |
| | LM13600AN | NE5517N | 0 to +70 | Plastic |
| | LM13600N | NE5517N | 0 to +70 | Plastic |
| | LM1458H | MC1458H | 0 to +70 | Metal can |

# Pin-for-Pin Functionally-Compatible Cross Reference by Competitor

| COMPETITOR | COMPETITOR PART NUMBER | SIGNETICS PART NUMBER | TEMPERATURE (°C) | PACKAGE |
|---|---|---|---|---|
| **National (Cont.)** | LM1458N | MC1458N | 0 to +70 | Plastic |
| | LM161H | SE529H | −55 to +125 | Metal can |
| | LM161J | SE529F | −55 to +125 | Ceramic |
| | LM2524J | SG3524F | 0 to +70 | Ceramic |
| | LM2524N | SG3524N | 0 to +70 | Plastic |
| | LM2901N | LM2901N | −40 to +85 | Plastic |
| | LM2903N | LM2903N | −40 to +85 | Plastic |
| | LM3089 | CA3089N | −55 to +125 | Plastic |
| | LM319H | LM119H | 0 to +70 | Metal can |
| | LM319J | LM319F | 0 to +70 | Ceramic |
| | LM319N | LM319N | 0 to +70 | Plastic |
| | LM324J | LM324F | 0 to +70 | Ceramic |
| | LM324N | LM324N | 0 to +70 | Plastic |
| | LM339/AJ | LM339/AF | 0 to +70 | Ceramic |
| | LM339/AN | LM339/AN | 0 to +70 | Plastic |
| | LM3524J | SG3524F | 0 to +70 | Ceramic |
| | LM3524N | SG3524N | 0 to +70 | Plastic |
| | LM358H | LM358H | 0 to +70 | Metal can |
| | LM358N | LM358N | 0 to +70 | Plastic |
| | LM361H | NE529H | 0 to +70 | Metal can |
| | LM361J | NE529D | 0 to +70 | SO |
| | LM361N | NE529N | 0 to +70 | Plastic |
| | LM393/A N | LM393/AN | 0 to +70 | Plastic |
| | LM555J | NE555F | 0 to +70 | Ceramic |
| | LM555N | NE555N | 0 to +70 | Plastic |
| | LM556J | SE556-1F | −55 to +125 | Ceramic |
| | LM556N | SE556-1N | −55 to +125 | Plastic |
| | LM556CJ | NE556-1F | 0 to +70 | Ceramic |
| | LM556CN | NE556-1N | 0 to +70 | Plastic |
| | LM565CN | NE565N | 0 to +70 | Plastic |
| | LM566N | SE566N | −55 to +125 | Plastic |
| | LM566CN | NE566N | 0 to +70 | Plastic |
| | LM567CN | NE567N | 0 to +70 | Plastic |
| | LM592 | NE592N | 0 to +70 | Plastic |
| | LM733CN | μA733CN | 0 to +70 | Plastic |
| | LM741CJ | μA741CF | 0 to +70 | Ceramic |
| | LM741CN | μA741CN | 0 to +70 | Plastic |
| | LM741J | μA741F | −55 to +125 | Ceramic |
| | LM741N | μA741N | −55 to +125 | Plastic |
| | LM747CJ | μA747CF | 0 to +70 | Ceramic |
| | LM747CN | μA747CN | 0 to +70 | Plastic |
| | LM747J | μA747F | −55 to +125 | Ceramic |
| | LM747N | μA747N | −55 to +125 | Plastic |
| **PMI** | DAC1408-8P | MC1408N | 0 to +70 | Plastic |
| | DAC1408-8Q | MC1408F | 0 to +70 | Ceramic |
| | PM747Y | μA747N | −55 to +125 | Plastic |
| **Raytheon** | RC5532/A DE | NE5532/AF | 0 to +70 | Ceramic |
| | RC5532/A NB | NE5532/AN | 0 to +70 | Plastic |
| | RC5534/A DE | NE5534/AF | 0 to +70 | Ceramic |
| | RC5534/A NB | NE5534/AN | 0 to +70 | Plastic |
| | RM5532/A DE | SE5532/AF | −55 to +125 | Ceramic |
| | RM5534/A DE | SE5534/AF | −55 to +125 | Ceramic |





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# Pin-for-Pin Functionally-Compatible Cross Reference by Competitor

| COMPETITOR | COMPETITOR PART NUMBER | SIGNETICS PART NUMBER | TEMPERATURE (°C) | PACKAGE |
|---|---|---|---|---|
| **Silicon General** | SG3524J | SG3524F | 0 to +70 | Ceramic |
| **Sprague** | UDN6118A | SA594N | −40 to +85 | Plastic |
| | UDN6118R | SA594F | −40 to +85 | Ceramic |
| | ULN8160A | NE5560N | 0 to +70 | Plastic |
| | ULN8160R | NE5560F | 0 to +70 | Ceramic |
| | ULN8161M | NE5561N | 0 to +70 | Plastic |
| **TI** | ADC0803 | ADC0803-1LCN | −40 to +85 | Plastic |
| | ADC0804CN | ADC0804-1C | 0 to +70 | Plastic |
| | ADC0805 | ADC0805-1LC | −40 to +85 | Plastic |
| | LM324D | LM324N | 0 to +70 | Plastic |
| | LM324J | LM324F | 0 to +70 | Ceramic |
| | LM339/AJ | LM339/AF | 0 to +70 | Ceramic |
| | LM339/AN | LM339/AN | 0 to +70 | Plastic |
| | LM358P | LM358N | 0 to +70 | Plastic |
| | LM358U | LM358H | 0 to +70 | Metal can |
| | LM393/A P | LM393/AN | 0 to +70 | Plastic |
| | MC1458P | MC1458N | 0 to +70 | Plastic |
| | MC1458U | MC1458H | 0 to +70 | Metal can |
| | NE5532/A JG | NE5532/AF | 0 to +70 | Ceramic |
| | NE5532/A P | NE5532/AN | 0 to +70 | Plastic |
| | NE5534/A JG | NE5534/AF | 0 to +70 | Ceramic |
| | NE5534/A P | NE5534/AN | 0 to +70 | Plastic |
| | NE555JG | NE555N | 0 to +70 | Plastic |
| | NE555P | NE555N | 0 to +70 | Plastic |
| | NE556D | NE556N | 0 to +70 | Plastic |
| | NE556J | NE556-1F | 0 to +70 | Ceramic |
| | NE556N | NE556-1N | 0 to +70 | Plastic |
| | NE592 | NE592N14 | 0 to +70 | Plastic |
| | NE592A | NE592F14 | 0 to +70 | Ceramic |
| | NE592J | NE592F | 0 to +70 | Ceramic |
| | NE592N | NE592N | 0 to +70 | Plastic |
| | SA556D | SA556N | −40 to +85 | Plastic |
| | SE5534/A JG | SE5534/AF | −55 to +125 | Ceramic |
| | SE555JG | SE555N | −55 to +125 | Plastic |
| | SE556J | SE556-1F | −55 to +125 | Ceramic |
| | SE556N | SE556-1N | −55 to +125 | Plastic |
| | SE592 | SE592N14 | −55 to +125 | Plastic |
| | SE592J | SE592F | −55 to +125 | Ceramic |
| | SE592N | SE592N | −55 to +125 | Plastic |
| | TL592A | NE592F14 | 0 to +70 | Ceramic |
| | TL592P | NE592N8 | 0 to +70 | Plastic |
| | μA723CJ | μA723CF | 0 to +70 | Ceramic |
| | μA723CN | μA723CN | 0 to +70 | Plastic |
| | μA723MJ | μA723F | −55 to +125 | Ceramic |
| | μA723MU | μA723D | −55 to +125 | SO |
| **Unitrode** | UC3524J | SG3524F | 0 to +70 | Ceramic |
| | UC3524N | SG3524N | 0 to +70 | Plastic |



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# Interface / Data Conversion Products

| Part Number | Description | Available in SO |
|---|---|---|
| **Analog-to-Digital Converters** | | |
| ADC0801/2/3/4/5 | 8-bit CMOS A/D converter | |
| SE/NE5030 | 10-bit high-speed microprocessor-compatible A/D converter | |
| NE5034 | 8-bit high-speed A/D converter | |
| NE5036 | 6-bit A/D converter, serial output | x |
| NE5037 | 6-bit A/D converter, parallel output | x |
| PCF8591 | 8-bit A/D and D/A converter | |
| PNA7507 | 7-bit A/D converter, 15MHz (Flash) | |
| TDA1534A | 14-bit A/D converter, serial output | |
| **Digital-to-Analog Converters** | | |
| AM6012 | 12-bit high-speed multiplying D/A converter | |
| DAC-08 Series | 8-bit high-speed multiplying D/A converter | x |
| DAC800 | 12-bit D/A converter | |
| MC1508-8/1408-8/1408-7 | 8-bit multiplying D/A converter | x |
| MC3410/3510/3410C | 10-bit high-speed multiplying D/A converter | |
| NE5020 | 10-bit microprocessor-compatible D/A converter | |
| NE5150/5151 | RGB video D/A converter | |
| PCF8591 | 8-bit A/D and D/A converter | |
| PNA7518 | 8-bit D/A converter, 30MHz | |
| SAB3013 | Six-function analog memory (6-bit D/A converter) | |
| SE/NE5018 | 8-bit microprocessor-compatible D/A converter | x |
| SE/NE5019 | 8-bit microprocessor-compatible D/A converter | x |
| SE/NE5118 | 8-bit microprocessor-compatible D/A converter, current output | |
| SE/NE5119 | 8-bit microprocessor-compatible D/A converter, current output | |
| SE/NE5410 | 10-bit high-speed multiplying D/A converter | |
| TDA1540P,D | 14-bit D/A converter, serial output | |
| **Comparators** | | |
| LM111/211/311 | Voltage comparator | x |
| LM119/219/319 | Dual voltage comparator | x |
| LM139/A/239/A/339/A | Quad voltage comparator | x |
| LM193/A/239/A/393/A | Low power dual voltage comparator | x |
| LM2901 | Quad voltage comparator | x |
| LM2903 | Low power dual voltage comparator | x |
| MC3302 | Quad voltage comparator | x |
| SE/NE521 | High-speed dual differential comparator/sense amplifier | x |
| SE/NE522 | High-speed dual differential comparator/sense amplifier | x |
| SE/NE527 | Voltage comparator | x |
| SE/NE529 | Voltage comparator | x |
| PCF1251T | Micropower voltage detector | x |
| **Position Measurement** | | |
| NE5520 | LVDT signal conditioner | x |
| SE/NE5521 | LVDT signal conditioner | |
| **Sample and Hold** | | |
| LF198/298/398 | Monolithic sample and hold circuit | x |
| SE/NE5537 | Sample and hold amplifier | x |
| TDA1535 | High performance sample and hold amplifier with resolution to 16 bits | |

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# Interface/Data Conversion Products

| Part Number | Description | Available in SO |
|---|---|---|
| **Drivers** | | |
| MC1488 | Quad line driver | x |
| MC1489/A | Quad line receiver | x |
| NE5090 | Addressable relay driver | x |
| NE5170 | Octal line driver | |
| NE5180/81 | Octal line receiver | |
| NE587 | LED decoder/driver | x |
| NE589 | LED decoder/driver | x |
| NE590 | Addressable peripheral driver | |
| NE591 | Addressable peripheral driver | |
| SA/NE594 | Vacuum fluorescent display driver | x |
| PCF2100 | 40-segment LCD duplex driver | x |
| PCF2110 | 60-segment LCD duplex driver | x |
| PCF2111 | 64-segment LCD duplex driver | x |
| PCF1303 | 18-segment LCD bar graph driver | |
| PCF2112 | 32-segment LCD static driver | x |
| PCF8576 | Universal LCD driver for low multiplex rates | x |
| PCF8577 | 32/64-segment LCD driver | x |
| SAA1060 | 32-segment LED driver | |
| SAA1061 | 16-segment LED driver | |
| SAA1062A | 20-segment LCD driver | x |
| SAA1063 | Vacuum fluorescent display driver (17-bit) | |
| ULN2003 | High voltage/current Darlington transistor array | x |
| ULN2004 | High voltage/current Darlington transistor array | x |



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# Communications Products

| Part Number | Description | Available in SO |
|---|---|---|
| **Analog and Audio Processing** | | |
| NE570 | Compandor | |
| SA/NE571 | Compandor | x |
| SA/NE572 | Programmable analog compandor | x |
| SAA7000 | Compact disc circuit | |
| SAA7010 | Demodulator for compact disc | |
| SAA7020 | Error corrector for compact disc | |
| SAA7030 | Filter circuit for compact disc | |
| **Audio/Stereo** | | |
| LM1870 | Stereo demodulator with blend | x |
| NE5240 | Dolby digital audio decoder | |
| NE542 | Dual low-noise preamplifier | |
| NE645/646 | Dolby B-type noise reduction circuit | |
| NE648/649 | Low voltage Dolby B-type noise reduction circuit | |
| NE650 | Dolby B-type noise reduction circuit | |
| NE660 | Dolby B-type noise reduction circuit | |
| NE670 | Low voltage Dolby B/C-type noise reduction circuit | |
| TDA1029 | Stereo audio switch | |
| TDA1074A | DC-controlled dual potentiometers | |
| TDA1522 | Stereo cassette preamplifier (dual) | |
| TDA1524A | Stereo, DC-controlled audio control | |
| TDA1578A | PLL stereo decoder | |
| TDA3810 | Spatial, stereo, pseudo-stereo processor | |
| TDA3806 | TV-stereo sound decoder (Zenith format) | |
| TDA3807 | Second audio program (SAP) FM decoder | |
| TEA5580 | PLL stereo decoder | |
| μA758 | FM stereo multiplex decoder phase locked loop | |
| **AM Radio** | | |
| SAA1057 | PLL radio tuning circuit | |
| TDA1072 | AM radio circuit | |
| TDD1742T | CMOS frequency synthesizer | x |
| TEA5550 | AM radio circuit | |
| TEA5570 | AM/FM radio receiver circuit | |
| **FM Radio** | | |
| CA3089 | FM I.F. system | |
| MC1496 | Balanced modulator/demodulator | |
| SA/NE602 | Double-balanced mixer and oscillator | x |
| SA/NE612 | Double-balanced mixer and oscillator | x |
| SA/NE604 | Low power narrow-band FM I.F. | x |
| SA/NE614 | Low power narrow-band FM I.F. | x |
| SAA1057 | PLL radio tuning circuit | |
| TDA0820T | Balanced modulator/demodulator | x |
| TDA1001B,T | FM noise suppression circuit | x |
| TDA1571 | FM mixer stage | |
| TDA1574 | FM front end IC | |
| TDA1576 | FM/I.F. (quadrature detector) | |
| TDA1596 | FM/I.F. amplifier | |
| TDA7000 | Single-chip FM radio | |
| TDA7010T | Single-chip FM radio, SO package | x |
| TDA7020T | FM radio (stereo receiver) | x |
| TDD1742T | CMOS frequency synthesizer | x |
| TEA5560 | FM radio circuit | |
| TEA5570 | AM/FM radio receiver circuit | |
| TEA6000 | FM/I.F. system and computer interface circuit | |

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# Communications Products

| Part Number | Description | Available in SO |
|---|---|---|
| **FSK Modems** | | |
| NE5050 | Power line modem | x |
| NE5080 | 2-Megabaud FSK transmitter, IEEE 802.4 | |
| NE5081 | FSK receiver, IEEE 802.4 | |
| **IR Remote Control Transmitters and Receivers** | | |
| SAA3004 | I/R transmitter (448 commands) | x |
| SAA3006 | I/R transmitter (2K commands, low voltage) | |
| SAA3028 | I/R receiver | |
| SAF1032P | Remote control receiver | |
| SAF1039P | Remote control transmitter | |
| TDA3047 | I/R preamplifier | |
| TDA3048 | I/R preamplifier | |
| **Phase Locked Loops** | | |
| SE/NE564 | High frequency phase locked loop | x |
| SE/NE565 | Phase locked loop | x |
| SE/NE566 | Function generator | x |
| SE/NE567 | Tone decoder/phase locked loop | x |
| SE/NE568 | 150MHz phase locked loop | |
| **Speech/Music Synthesis** | | |
| MEA8000 | Speech synthesizer | |
| OM8000 | Speech evaluation P.C. board | |
| OM8001 | Speech demonstrator | |
| OM8010/8011 | Speech encoding system | |
| PCD3311/3312 | DTMF/MODEM/Musical tone generator | x |
| PCF8200 | Single-chip CMOS male/female speech synthesizer | |
| SAA1099 | Stereo sound generator for sound effects and music synthesis | |
| UAA2183 | Sound generator IC for organs | |
| **Telephony** | | |
| NE5900 | Call progress decoder | |
| PCD3310 | Pulse and DTMF dialer with redial | |
| PCD3311/3312 | DTMF/MODEM/Musical tone generator | x |
| PCD3315 | CMOS redial and repertory dialer | x |
| PCD3343 | CMOS microcontroller for telephone sets | x |
| PCD3360/61 | Programmable multi-tone telephone ringer | x |
| PM4300/4337 | Low-cost, stand-alone microcomputer development system for MAB84xx family of microcomputers | |
| SA/NE602 | Double-balanced mixer and oscillator (cellular/portable for telephone) | x |
| SA/NE612 | Double-balanced mixer and oscillator (cellular/portable for telephone) | x |
| SA/NE604 | Low power narrow-band FM I.F. (cellular/portable for telephone) | x |
| SA/NE614 | Low power narrow-band FM I.F. (cellular/portable for telephone) | x |
| TDA7000 | Single-chip FM radio (for cordless telephone) | |
| TDA7050T | Low voltage mono/stereo power amplifier (for cordless telephone) | x |
| TEA1042 | Transmission interface with loudspeaking ability | |
| TEA1046/A | Transmission interface with DTMF | |
| TEA1060/61 | Telephone transmission circuit | |
| TEA1067 | Low voltage transmission IC with dialer interface | |
| TEA1075 | DTMF generator for telephone dialing | |
| TEA1080 | Supply IC for telephone peripherals | |
| **Timers** | | |
| PCF8573 | Clock/Timer with $I^2C$ interface | x |
| SA/SE/NE556/-1/SE556-1C | Dual timer | x |
| SA/SE/NE558 | Quad timer | x |
| SAF3019P | Clock/Timer | |
| SE/NE555/SE555C | Timer | x |

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# Amplifier Products

| Part Number | Description | Available in SO |
|---|---|---|
| **Companding** | | |
| NE570 | Compandor | |
| SA/NE571 | Compandor | |
| SA/NE572 | Programmable analog compandor | x |
| **Operational** | | |
| LM124/224/324/SA534 | Low power quad operational amplifier | x |
| LM158/258/358 | Low power dual operational amplifier | x |
| MC/SA1458/MC1558 | General purpose operational amplifier | x |
| MC3303/3403/3503 | Quad low power operational amplifier | x |
| NE1012 | Low noise operational amplifier | |
| NE1037 | Low noise, high-speed precision operational amplifier | |
| SE/NE4558 | Dual general purpose operational amplifier | x |
| NE5230 | Low voltage operational amplifier | x |
| SE/NE530 | High slew rate operational amplifier | |
| SE/NE531 | High slew rate operational amplifier | |
| SA/SE/NE532 | Low power dual operational amplifier | x |
| SE/NE538 | High slew rate operational amplifier | |
| SE/NE5512 | Dual high performance operational amplifier | x |
| SE/NE5514 | Quad high performance operational amplifier | x |
| SE/NE5532/A | Internally compensated dual low noise operational amplifier | x |
| NE5533/A/SA/SE/NE5534A | Single and dual low noise operational amplifier | x |
| SE/NE5535 | Dual high slew rate operational amplifier | x |
| μA741/741C/SA741C | General purpose operational amplifier | x |
| μA747/747C/SA747C | Dual operational amplifier | x |
| **Power** | | |
| OM200/S2 | Hearing aid amplifier | |
| TDA1010A | 6W audio amplifier | |
| TDA1013A | 4W audio amplifier with DC volume control | |
| TDA1015 | 1 to 4W audio amplifier | |
| TDA1020 | 12W audio amplifier | |
| TDA1510 | 2 × 12W audio amplifier | |
| TDA1512 | 12 to 20W audio amplifier | |
| TDA1515 | 24W BTL audio amplifier | |
| TDA1520A | 20W Hi-Fi audio amplifier | |
| TDA2611A | 5W audio output for TV | |
| TDA7050T | Low voltage mono/stereo power amplifier | x |
| **Transconductance** | | |
| NE5517/A | Dual operational transconductance amplifier | x |
| **Video** | | |
| NE5205 | Wideband high frequency amplifier | x |
| SE/NE5539 | Ultra high frequency operational amplifier | x |
| SE/NE5592 | Video amplifier | x |
| SE/NE592 | Video amplifier | x |
| μA733/C | Differential video amplifier | |

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# Video Products

| Part Number | Description | Available in SO |
|---|---|---|
| **Tuning** | | |
| MAB84xx | Single-chip 8-bit microcontroller family | |
| PCD8571 | 1K serial RAM | x |
| PCF8570 | 256×8 static RAM | x |
| PCF8573 | Clock/timer with $I^2C$ Interface | x |
| PCF8574 | 8-bit remote I/O expander | |
| SAA1300 | Video switch (5-output switch) | |
| SAB1164 | 1GHz divide by 64 (prescaler) | |
| SAB1165 | 1GHz divide by 64 (prescaler) | |
| SAB1256 | 1GHz divide by 256 (prescaler) | |
| SAB3013 | Six-function analog memory (6-bit D/A converter) | |
| SAB3035 | FLL tuning circuit (eight D/A converters) | |
| SAB3036 | FLL tuning circuit | |
| SAB3037 | FLL tuning circuit (four D/A converters) | |
| TDA0820T | Balanced modulator/demodulator | x |
| TDA5030 | VHF mixer-oscillator | |
| TDD1742T | CMOS frequency synthesizer | x |
| **Video I.F.** | | |
| TDA2540 | Video I.F. amplifier demodulator, AFT, NPN tuners | |
| TDA2541 | Video I.F. amplifier demodulator, AFT, PNP tuners | |
| TDA3540/41 | Video I.F./AFT | |
| TDA3806 | TV-stereo sound decoder (Zenith format) | |
| TDA3807 | Second audio program (SAP) FM detector | |
| TDA4501 | Complete video and sound I.F. IC with vertical and horizontal outputs | |
| TDA4502 | Complete video I.F. IC with vertical and horizontal sync | |
| TDA4503 | Small signal combination for B/W TV without castle generator | |
| **Sound I.F. and Special Audio Decoding** | | |
| TBA120U | I.F. amplifier and demodulator | |
| TDA2545A | Quasi-split sound I.F. | |
| TDA2546A | Quasi-split sound I.F. and sound demodulator | |
| TDA2555 | Dual TV sound demodulator | |
| **Sync Processing and Generation** | | |
| TDA2577A | Sync circuit with vertical oscillator and driver (with negative horizontal output) | |
| TDA2578A | Sync circuit with vertical oscillator and driver (with negative horizontal output) | |
| TDA2579 | Sync circuit with vertical oscillator and driver (with horizonta output) | |
| TDA2593 | Horizontal combination | |
| TDA2594 | Horizontal combination | |
| TDA2595 | Horizontal combination | |
| SAA1043 | Universal sync generator | |
| SAA1044 | Subcarrier coupler (used with SAA1043) | |
| **Color Decoding and Encoding** | | |
| NE5150/5151 | RGB video D/A converter | |
| TDA2501 | PAL or NTSC encoder | |
| TDA3505 | Chroma control circuit | |
| TDA3562A | PAL/NTSC decoder | |
| TDA3563 | NTSC decoder with RGB inputs | |
| TDA3564 | NTSC decoder | |
| TDA3568 | Monolithic integrated delay line and filter combination for NTSC television receivers | |
| TDA4555/4556 | Multistandard color decoder | |
| TDA4560 | Color transient improvement circuit (CTI) | |
| TDA4580 | Video control with two RGB and color difference inputs | |
| TEA2000 | RGB to NTSC/PAL encoder | |

***New product. Information available upon request.**

# Video Products

| Part Number | Description | Available in SO |
|---|---|---|
| **Vertical Deflection** | | |
| TDA2653A | Vertical deflection | |
| TDA3651A/AQ | Vertical deflection | |
| TDA3651A/AQ/3653 | Vertical deflection | |
| TDA3652 | Vertical deflection | |
| TDA3654 | Vertical deflection | |
| **Videotex/Teletext** | | |
| SAA5025D | 525-line teletext timing chain | |
| SAA5030 | Teletext video input processor | |
| SAA5040 | Teletext acquisition and control circuit | |
| SAA5045 | Gearing and address logic array (GALA) | |
| SAA5050/55 | Teletext character generator | |
| SAA5230 | Advanced video processor | |
| SAA5240 | Microprocessor controlled teletext circuit | |
| SAA5350 | Advanced display controller (625-line system) | |



Signetics Linear Products offers integrated circuits for: • Interface and Data Conversion • Communication Equipment • Amplifiers • Video Equipment • Power Conversion and Control



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# Small Area Networks ($I^2C$) Products

| Part Number | Description | Available in SO |
|---|---|---|
| MAB84xx | Single-chip 8-bit microcontroller family | |
| NE5036 | 6-bit A/D converter-serial output | x |
| PCB8573 | Clock/timer with $I^2C$ interface | |
| PCD8571 | 1K serial RAM | |
| PCD8572 | 1024-bit EEROM | |
| PCF2100 | 4-segment LCD duplex driver | x |
| PCF2110 | 60-segment LCD duplex driver | x |
| PCF2111 | 64-segment LCD duplex driver | x |
| PCF2112 | 32-segment LCD static driver | x |
| PCF8200 | Single-chip CMOS high performance speech synthesizer | |
| PCF8570 | 256×8 static RAM | x |
| PCF8574 | 8-bit remote I/O expandor | x |
| PCF8576 | Universal LCD driver for low multiplex rates | x |
| PCF8577 | 32/64-segment LCD driver for automotive | x |
| PCF8591 | 8-bit A/D and D/A converter | |
| SAA1057 | PLL radio tuning circuit | |
| SAA1060 | 32-segment LED driver | |
| SAA1061 | 16-segment LED driver | |
| SAA1063 | Vacuum fluorescent display driver (17-bit) | |
| SAA1300 | Video switch (5-output switch) | |
| SAA3028 | I/R receiver | |
| SAA5240 | Microprocessor controlled teletext circuit | |
| SAB3013 | 6-function analog memory (6-bit D/A converter) | |
| SAB3035 | FLL TV tuning circuit (eight D/A converters) | |
| SAB3036 | FLL TV tuning circuit | |
| SAB3037 | FLL TV tuning circuit (four D/A converters) | |
| SAF3019P | Clock/timer with $I^2C$ interface | |
| SCC84Cxx | CMOS 8-bit microcontroller family | |
| SCC83C351 | CMOS serial bus microcontroller | |
| SCC80C351 | CMOS serial bus microcontroller | |
| TDA1534A | 14-bit A/D converter-serial output | |
| TDA1540P,D | 14-bit D/A converter-serial output | |
| TDA8400 | Frequency synthesizer (Cypress) | |
| TDA8440 | Audio/video switch | |
| TDA8442 | I/O expandor | |
| TDA8443 | RGB/YUV matrix switch | |
| TDD1742T | CMOS frequency synthesizer | x |
| TEA6000 | FM I.F. system and computer interface circuit | |

***New product. Information available upon request.**

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# Signetics Programmable Logic Device Selection Guide

| Signetics P/N | Architecture | Package | Total Inputs (#Dedicated) | Product Terms | Internal State Registers | Outputs C, I/O, R, R I/O | $T_{PD}$† (Typical Values) | $I_{CC}$ (Typical Values) |
|---|---|---|---|---|---|---|---|---|
| **FPGA** | | | | | | | | |
| PLS103 | 16 × 9 × 9 | 28-Pin | 16 | 9 | 0 | 9 C | 20 ns | 120 mA |
| PLS151 | 18 × 15 × 12 | 20-Pin | 18 (6) | 15 | 0 | 12 I/O | 15 ns | 130 mA |
| **FPAD** | | | | | | | | |
| PLS162 | 16 × 5 | 24-Pin | 16 | 5 | 0 | 5 C | 20 ns | 120 mA |
| PLS163 | 12 × 9 | 24-Pin | 12 | 9 | 0 | 9 C | 20 ns | 120 mA |
| **FPLA** | | | | | | | | |
| PLS100 | 16 × 48 × 8 | 28-Pin | 16 | 48 | 0 | 8 C | 35 ns | 120 mA |
| PLS153 | 18 × 42 × 10 | 20-Pin | 18 (8) | 42 | 0 | 10 I/O | 30 ns | 130 mA |
| PLS153A | 18 × 42 × 10 | 20-Pin | 18 (8) | 42 | 0 | 10 I/O | 20 ns | 130 mA |
| PLUS153** | 18 × 42 × 10 | 20-Pin | 18 (8) | 42 | 0 | 10 I/O | 10 ns | 150 mA |
| PLC153** | 18 × 42 × 10 | 20-Pin | 18 (8) | 42 | 0 | 10 I/O | TBD | TBD |
| PLS161 | 12 × 48 × 8 | 24-Pin | 12 | 48 | 0 | 8 C | 35 ns | 120 mA |
| PLS173 | 22 × 42 × 10 | 24-Pin | 22 (12) | 42 | 0 | 10 I/O | 20 ns | 150 mA |
| PLC173** | 22 × 42 × 10 | 24-Pin | 22 (12) | 42 | 0 | 10 I/O | TBD | TBD |
| PLUS173** | 22 × 42 × 10 | 24-Pin | 22 (12) | 42 | 0 | 10 I/O | 10 ns | 150 mA |
| PLHS473** | 20 × 24 × 11 | 24-Pin | 20 (11) | 24 | 0 | 2 C & 9 I/O | 15 ns | 140 mA |
| PLC473** | 20 × 24 × 11 | 24-Pin | 20 (11) | 24 | 0 | 2 C & 9 I/O | 35 ns | 40 mA |
| PLHS18P8A** | 18 × 72 × 8 | 20-Pin | 18 (10) | 72 | 0 | 8 I/O | 14 ns | 120 mA |
| **FPLS** | | | | | | | | |
| PLS105 | 16 × 48 × 8 | 28-Pin | 16 | 48 | 6 | 8 R | 60 ns | 120 mA |
| PLS105A | 16 × 48 × 8 | 28-Pin | 16 | 48 | 6 | 8 R | 45 ns | 120 mA |
| PLC105** | 16 × 48 × 8 | 28-Pin | 16 | 48 | 6 | 8 R | 45 ns | 40 mA |
| PLUS405** | 16 × 64 × 8 | 28-Pin | 16 | 64 | 8 | 8 R | 20 ns | 190 mA |
| PLS155 | 16 × 45 × 12 | 20-Pin | 16 (4) | 45 | 4* | 8 I/O & 4 R I/O | 55 ns | 150 mA |
| PLS157 | 16 × 45 × 12 | 20-Pin | 16 (4) | 45 | 6* | 6 I/O & 6 R I/O | 55 ns | 150 mA |
| PLS159 | 16 × 45 × 12 | 20-Pin | 16 (4) | 45 | 8* | 4 I/O & 8 R I/O | 55 ns | 150 mA |
| PLS167 | 14 × 48 × 6 | 24-Pin | 14 | 48 | 6 plus 2* | 6 R | 60 ns | 120 mA |
| PLS167A | 14 × 48 × 6 | 24-Pin | 14 | 48 | 6 plus 2* | 6 R | 45 ns | 120 mA |
| PLS168 | 12 × 48 × 8 | 24-Pin | 12 | 48 | 6 plus 4* | 8 R | 60 ns | 120 mA |
| PLS168A | 12 × 48 × 8 | 24-Pin | 12 | 48 | 6 plus 4* | 8 R | 45 ns | 120 mA |
| PLS179 | 20 × 45 × 12 | 24-Pin | 20 (8) | 45 | 8* | 4 I/O & 8 R I/O | 45 ns | 145 mA |

**Outputs:**
C = Combinatorial output
I/O = Combinatorial I/O
R = Registered output
R I/O = Registered I/O

**Notes:**
*State registers shared with output registers
**Under development
†$T_{PD} = T_{IS} + T_{CKO}$ for registered devices



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Signetics

# PLS105
# Field Programmable Logic Sequencer (16 × 48 × 8)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 28**

## DESCRIPTION

The PLS105 is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 $Q_P$, and 8 $Q_F$ edge-triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs $I_{0-15}$ with six internal inputs $P_{0-5}$ fed back from the State Register to form up to 48 transition terms (AND terms). All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the LOW-to-HIGH transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal input variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output}}$ $\overline{\text{Enable}}$ function, as an additional user-programmable option.

Order codes are contained on the pages following.

## FEATURES

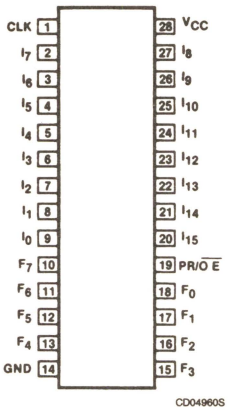
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **48 transition terms**
- **6-bit State Register**
- **8-bit Output Register**
- **Transition Complement Array**
- **Positive edge trigger clock**
- **Programmable asynchronous preset or Output Enable**
- **Power-on preset to all "1" of internal registers**
- **$f_{MAX}$ = 13.9MHz**
- **650mW power dissipation (typical)**
- **TTL compatible**
- **Single +5V supply**
- **Tri-state outputs**

## APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

## PIN CONFIGURATION

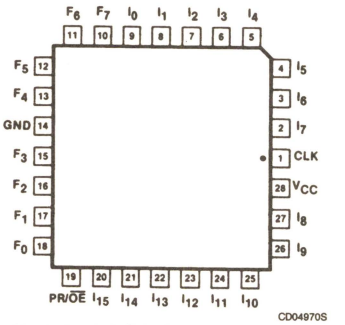
**N PACKAGE**




CD04960S

N = Plastic

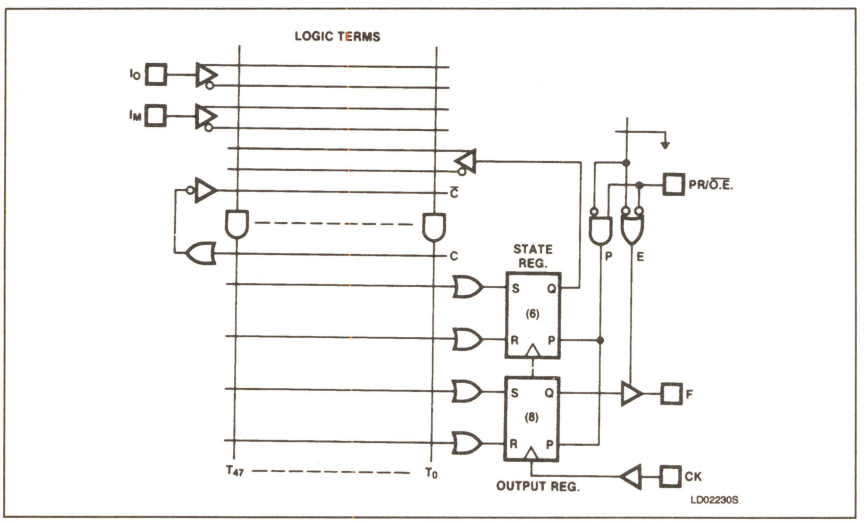
**A PACKAGE**




CD04970S

A = Plastic Leaded Chip Carrier

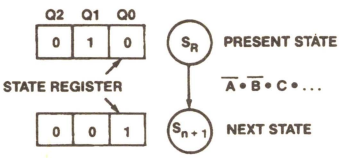
## FUNCTIONAL DIAGRAM




LD02230S

## LOGIC FUNCTION

**Typical State Transition:**




SET $Q_0$: $S_0 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$R_0 = 0$

RESET $Q_1$: $S_1 = 0$
$R_1 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD $Q_2$: $S_2 = 0$
$R_2 = 0$

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# PLS105A
# Field Programmable Logic Array (16 × 48 × 8)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 28**

## DESCRIPTION

The PLS105A is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 $Q_p$, and 8 $Q_F$ edge-triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs $I_{0-15}$ with 6 internal inputs $P_{0-5}$ fed back from the State Register to form up to 48 Transition terms (AND terms). All Transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse. Both True and Complement Transition terms can be generated by optional use of the internal input variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output-Enable}}$ function, as an additional user programmable option.

Order codes are contained on the pages following.

## FEATURES

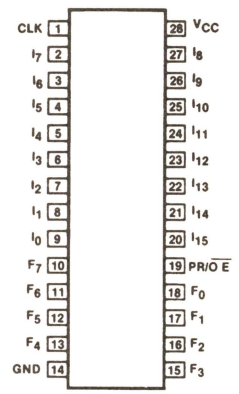
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **48 transition terms**
- **6-bit State Register**
- **8-bit Output Register**
- **Transition complement array**
- **Positive edge trigger clock**
- **Programmable asynchronous preset or output enable**
- **Power-on preset to all "1" of internal registers**
- **$f_{(MAX)}$ = 20MHz**
- **650mW power dissipation (typical)**
- **TTL compatible**
- **Single +5V supply**
- **Tri-state outputs**

## APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

## PIN CONFIGURATION

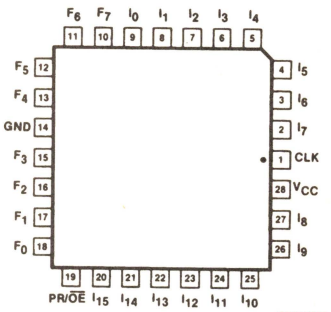
**N PACKAGE**



CD04960S

N = Plastic

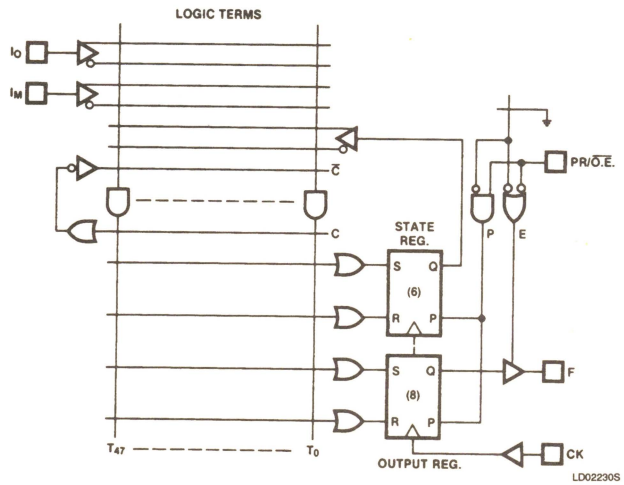
**A PACKAGE**



CD04970S

A = Plastic Leaded Chip Carrier

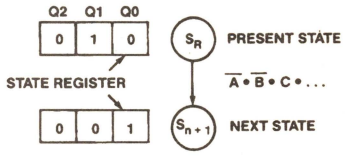
## FUNCTIONAL DIAGRAM



LD02230S

## LOGIC FUNCTION

**Typical State Transition:**




SET $Q_0$: $S_0 = (\overline{Q_2} \cdot Q_1 \cdot \overline{Q_0}) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

$R_0 = 0$

RESET $Q_1$: $S_1 = 0$

$R_1 = (\overline{Q_2} \cdot Q_1 \cdot \overline{Q_0}) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD $Q_2$: $S_2 = 0$

$R_2 = 0$

TB00900S

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# PLS155
# Field-Programmable Logic Sequencer (16 × 45 × 12)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 20**

## DESCRIPTION

The PLS155 is a Tre-state output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate $F_C$. It features 4 registered I/O outputs (F) in conjunction with 8 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

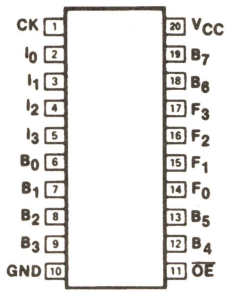
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

## FEATURES

- **Field-programmable (Ni-Cr link)**
- **4 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **8 bidirectional I/O lines**
- **4 bidirectional registers**
- **J-K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active HIGH or LOW outputs**
- **Programmable $\overline{OE}$ control**
- **Positive edge-triggered clock**
- **Clock frequency: 15MHz (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **TTL compatible**
- **Tri-state outputs**

## PIN CONFIGURATION

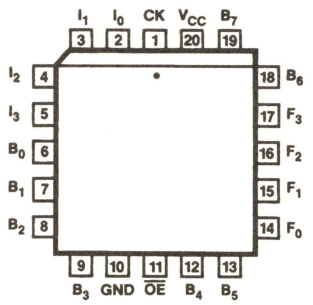
**N Package**




CD03310S

N = Plastic

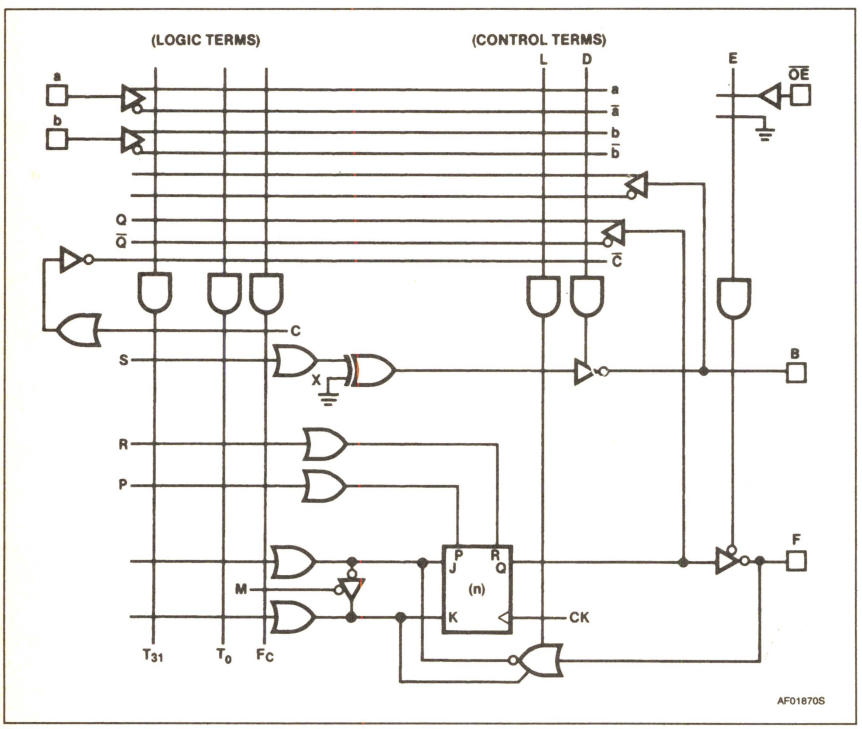
**A Package**




CD03320S

A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




## APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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# PLS157
# Field Programmable Logic Sequencer (16 × 45 × 12)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 20**

## DESCRIPTION

The PLS157 is a Three-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate $F_C$. It features 6 registered I/O outputs (F) in conjunction with 6 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

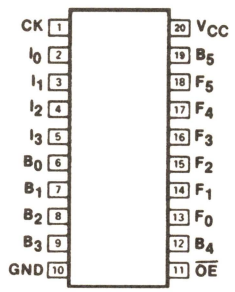
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

## FEATURES

- **Field programmable (Ni-Cr link)**
- **4 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **6 bidirectional I/O lines**
- **6 bidirectional registers**
- **J-K, T, or D-type flip-flops**
- **Three-State Outputs**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active HIGH or LOW outputs**
- **Programmable $\overline{OE}$ control**
- **Positive edge-triggered clock**
- **Clock frequency: 15MHz (max)**
- **Input loading: −100μA (max)**
- **Power dissipation: 750mW (typ)**
- **TTL compatible**

## PIN CONFIGURATION

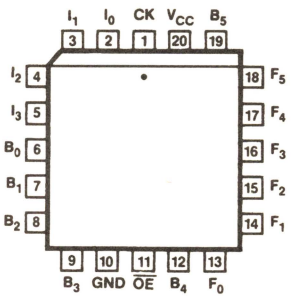
**N PACKAGE**




CD03370S

N = Plastic

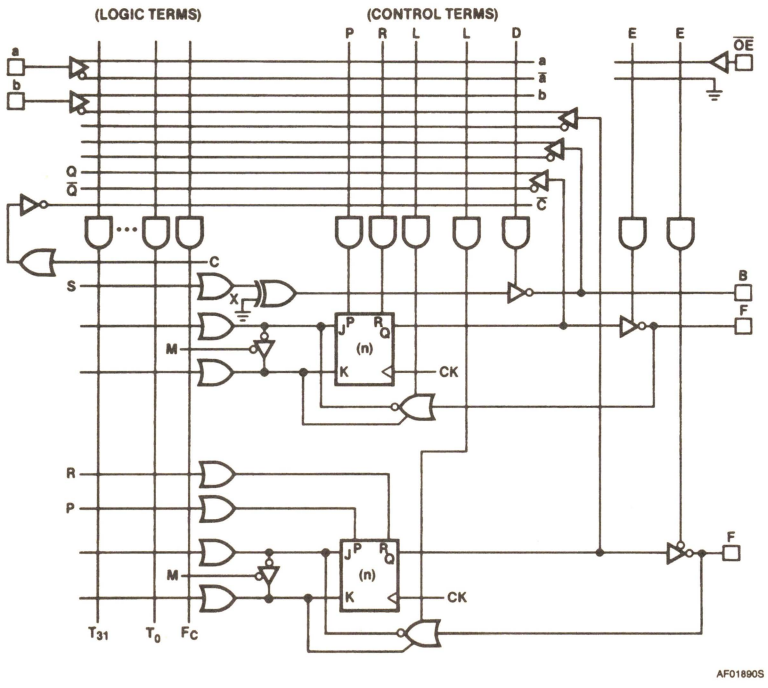
**A PACKAGE**




CD03380S

A = Plastic Leaded Chip Carrier

## FUNCTION DIAGRAM




## APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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# PLS159
# Field Programmable Logic Sequencer (16 × 45 × 12)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 20**

## DESCRIPTION

The PLS159 is a Three-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate $F_C$. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

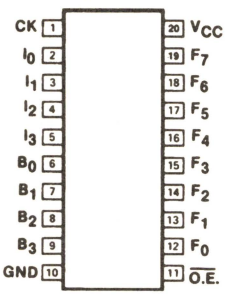
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

## FEATURES

- **Field programmable (Ni-Cr link)**
- **4 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **4 bidirectional I/O lines**
- **8 bidirectional registers**
- **J/K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active high or low outputs**
- **Programmable $\overline{O.E.}$ control**
- **Positive edge trigger clock**
- **Clock frequency: 15MHz (max)**
- **Input loading: −100μA (max)**
- **Power dissipation: 750mW (typ)**
- **TTL compatible**
- **Three-State Outputs**

## PIN CONFIGURATION

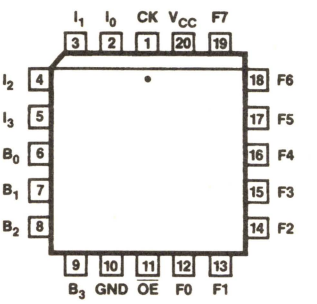
**N PACKAGE**




CD03350S

N = Plastic

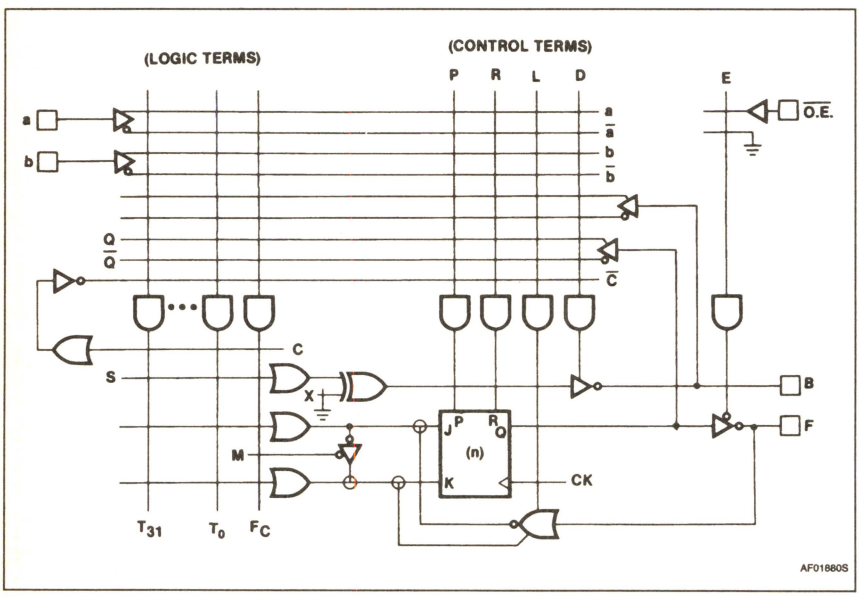
**A PACKAGE**




CD03360S

A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




AF01880S

## APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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# PLS159A
# Field Programmable Logic Sequencer (16 × 45 × 12)

**Signetics Programmable Logic**
***Objective Specification***

**Application Specific Products**
- **Series 20**

## DESCRIPTION

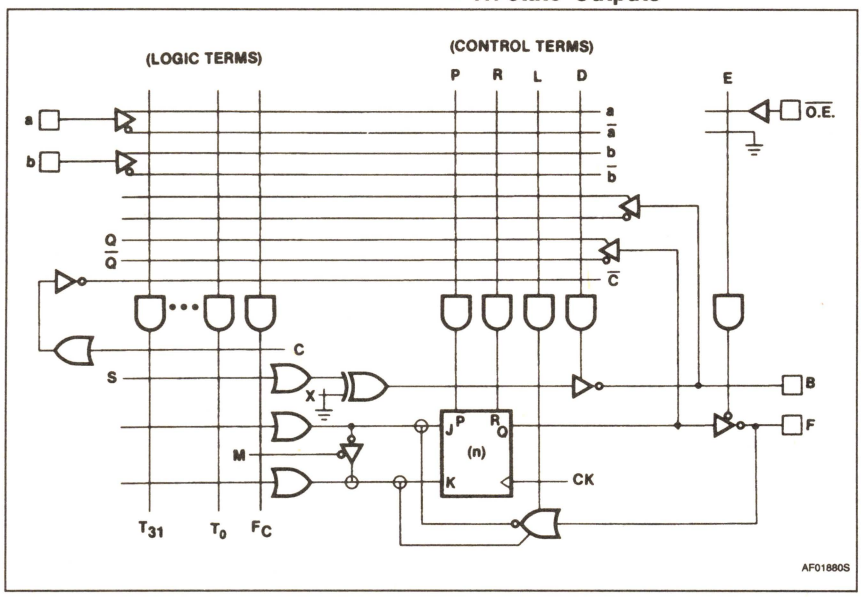
The PLS159A is a Tri-state output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate $F_C$. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

## FEATURES

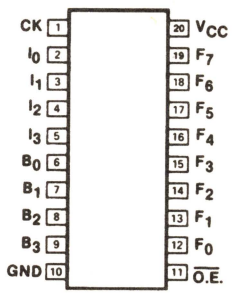
- **Field programmable (Ni-Cr link)**
- **4 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **4 bidirectional I/O lines**
- **8 bidirectional registers**
- **J/K, T, or D-type flip-flops**
- **Power on reset feature on all flip-flops ($F_n$ = 1)**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active high or low outputs**
- **Programmable $\overline{O.E.}$ control**
- **Positive edge-trigger clock**
- **Clock frequency: 18MHz (max)**
- **Input loading: −100μA (max)**
- **Power dissipation: 725mW (typ)**
- **TTL compatible**
- **Tri-state Outputs**

## FUNCTIONAL DIAGRAM



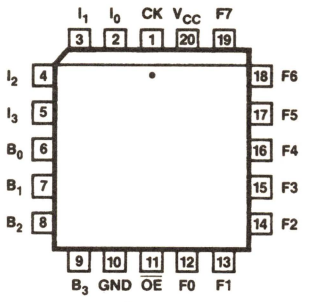

## PIN CONFIGURATION

**N PACKAGE**




N = Plastic

**A PACKAGE**




A = Plastic Leaded Chip Carrier

## APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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# PLS167
# Field Programmable Logic Sequencer (14 × 48 × 6)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLS167 is a bipolar, programmable state machine of the Mealy type. The Field Programmable Logic Sequencer (FPLS) contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 8 $Q_p$, and 4 $Q_f$ edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND Array combines 14 external inputs, $I_{0\text{-}13}$, with 8 internal inputs, $P_{0\text{-}7}$, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, $P_0$ and $P_1$ of the internal state register are brought off-chip to allow extending the Output Register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR Array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

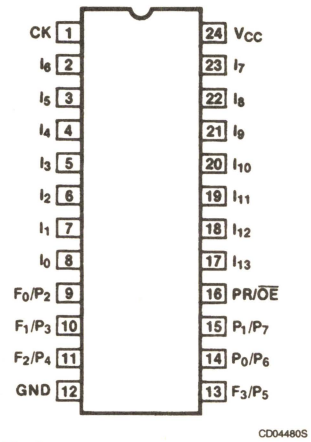
Order codes are contained on the pages following.

## FEATURES

- **Field programmable (Ni-Cr link)**
- **14 True/Complement buffered inputs**
- **48 programmable AND gates**
- **25 programmable OR gates**
- **8-bit State Register**
- **2-bit shared State/Output Register**
- **4-bit Output Register**
- **Transition Complement Array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On-chip Test Array**
- **$f_{(max)}$: 13.9MHz**
- **Power: 650mW (typ)**
- **TTL compatible**
- **Tri-state outputs**
- **Single +5V supply**
- **300 mil wide 24-pin DIP**

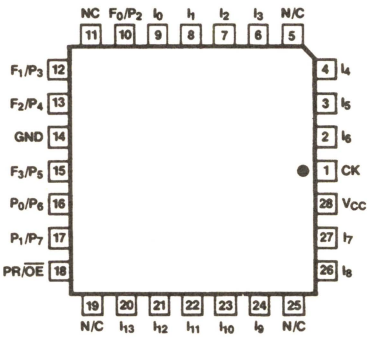
## PIN CONFIGURATION

**N PACKAGE**



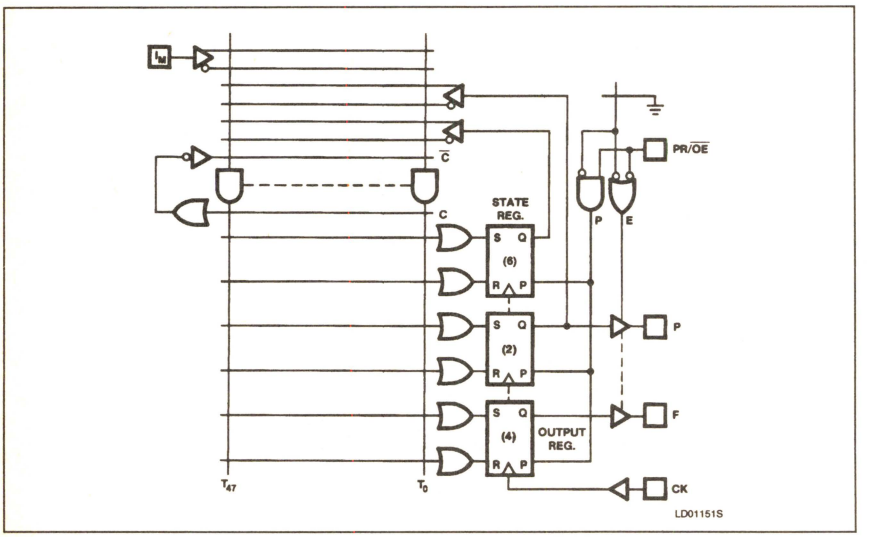

N = Plastic

**A PACKAGE**




A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




## APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Security locking systems**

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# PLS167A
# Field Programmable Logic Sequencer (14 × 48 × 6)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLS167A is a bipolar, programmable state machine of the Mealy type.The Field Programmable Logic Sequencer (FPLS) contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 8 $Q_p$, and 4 $Q_f$ edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 14 external inputs, $I_{0\text{-}13}$, with 8 internal inputs, $P_{0\text{-}7}$, fed back from the State register to form up to 48 transition terms (AND terms). In addition, $P_0$ and $P_1$ of the internal state register are brought off-chip to allow extending the output register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the low to high transition of the Clock pulse.

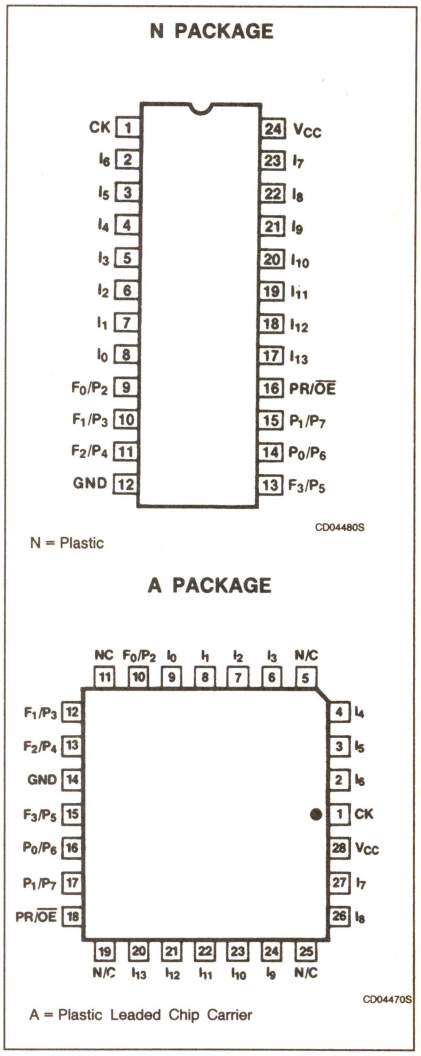
Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes are contained on the pages following.

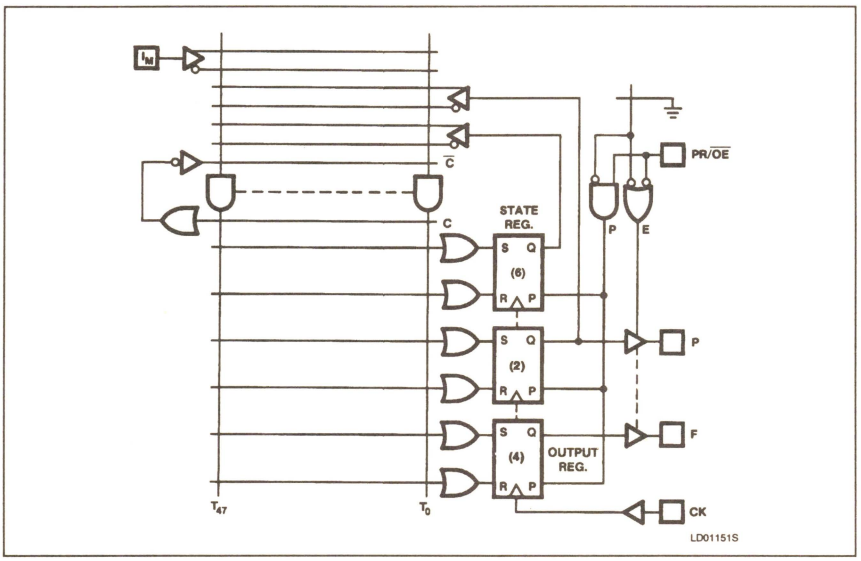
## FEATURES

- **Field programmable (Ni-Cr link)**
- **14 True/Complement buffered inputs**
- **48 programmable AND gates**
- **25 programmable OR gates**
- **8-bit state register**
- **2-bit shared state/output register**
- **4-bit output register**
- **Transition complement array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On/chip test array**
- **$f_{(max)}$: 20MHz**
- **Power: 650mW (typ)**
- **TTL compatible**
- **Tri-state outputs**
- **Single +5V supply**
- **300 mil wide 24-pin DIP**

## PIN CONFIGURATION




## FUNCTIONAL DIAGRAM




## APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Security locking systems**

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# PLS168
# Field Programmable Logic Sequencer (12 × 48 × 8)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLS168 is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 10 $Q_p$, and 4 $Q_f$ edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, $I_{0\text{-}11}$, with 10 internal inputs, $P_{0\text{-}9}$, fed back from the State register to form up to 48 transition terms (AND terms). In addition, $P_0$-$P_3$ of the internal state register are brought off-chip to allow extending the output register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the low to high transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

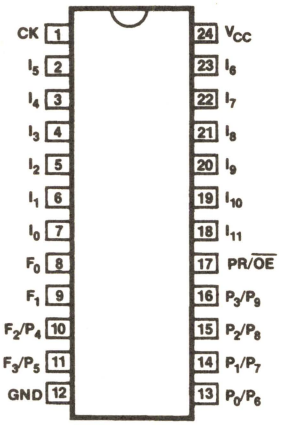
Order codes for this device are contained on the pages following.

## FEATURES

- **Field programmable (Ni-Cr link)**
- **12 True/Complement buffered inputs**
- **48 programmable AND gates**
- **29 programmable OR gates**
- **10-bit state register**
- **4-bit shared state/output register**
- **4-bit output register**
- **Transition complement array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On/chip test array**
- **$f_{(max)}$: 13.9MHz**
- **Power: 600mW**
- **TTL compatible**
- **Three-state outputs**
- **Single +5V supply**
- **300 mil wide 24-pin DIP**

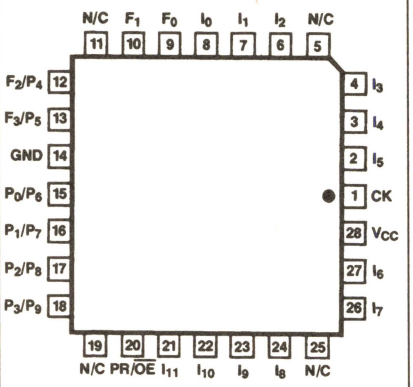
## PIN CONFIGURATION

**N PACKAGE**



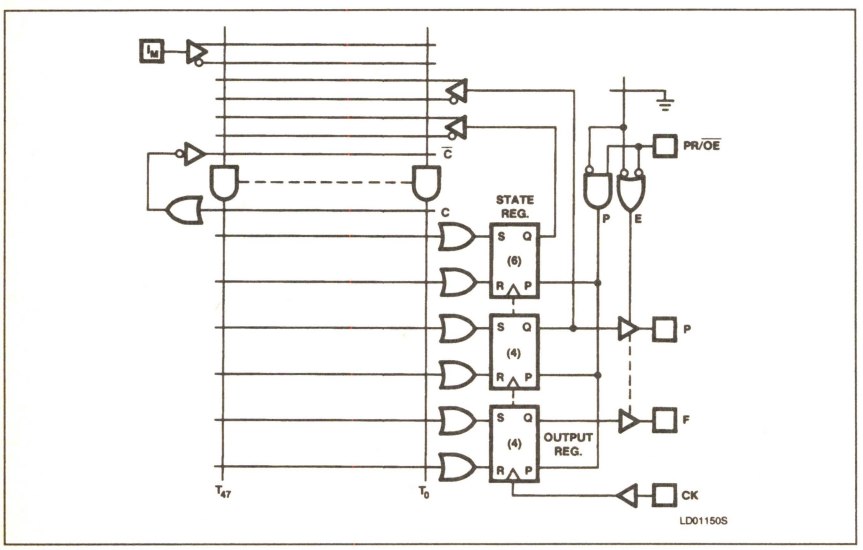

N = Plastic

**A PACKAGE**




A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




## APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

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# PLS168A
# Field Programmable Logic Sequencer (12 × 48 × 8)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLS168A is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 10 $Q_p$, and 4 $Q_f$ edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, $I_{0\text{-}11}$, with 10 internal inputs, $P_{0\text{-}9}$, fed back from the State register to form up to 48 transition terms (AND terms). In addition, $P_0$-$P_3$ of the internal state register are brought off-chip to allow extending the output register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the low to high transition of the Clock pulse.

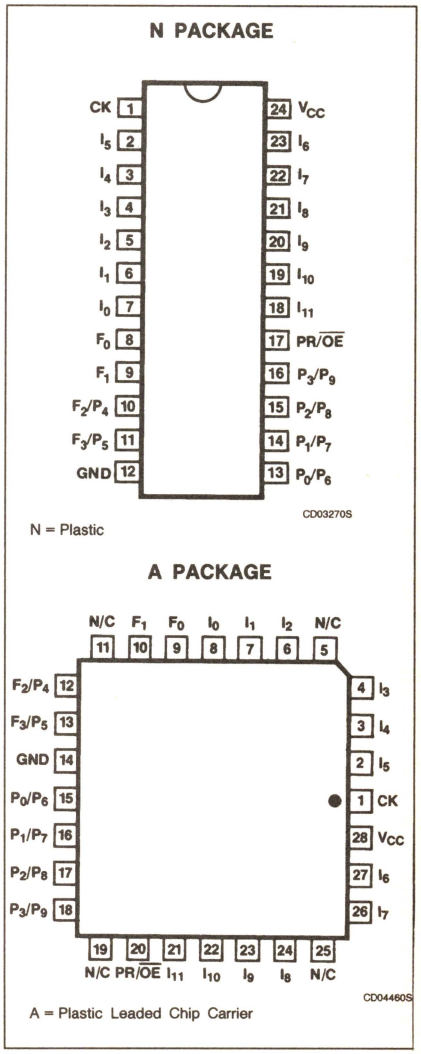
Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes for this device are contained on the pages following.

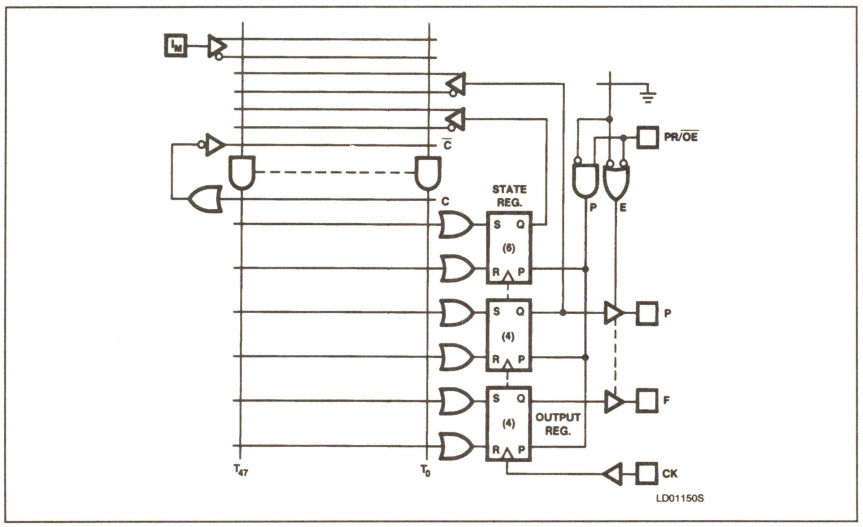
## FEATURES

- **Field programmable (Ni-Cr link)**
- **12 True/Complement buffered inputs**
- **48 programmable AND gates**
- **29 programmable OR gates**
- **10-bit state register**
- **4-bit shared state/output register**
- **4-bit output register**
- **Transition complement array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On/chip test array**
- **$f_{(max)}$: 20MHz**
- **Power: 600mW typ**
- **TTL compatible**
- **Three-state outputs**
- **Single +5V supply**
- **300 mil wide 24-pin DIP**

## PIN CONFIGURATION




## FUNCTIONAL DIAGRAM




## APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

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# PLS179
# Field Programmable Logic Sequencer (20 × 45 × 12)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLS179 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate $F_C$. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 20 inputs to 12 outputs.

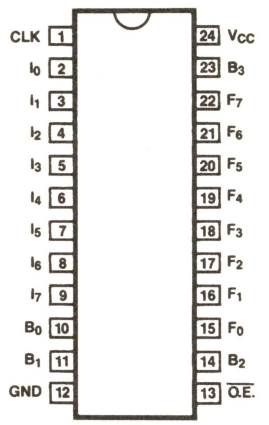
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 8 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

## FEATURES

- **Field programmable (Ni-Cr link)**
- **8 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **4 bidirectional I/O lines**
- **8 bidirectional registers**
- **J/K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active high or low outputs**
- **Programmable $\overline{O.E.}$ control**
- **Positive edge trigger clock**
- **Power-on reset on flip-flop (Fn = "1")**
- **Clock frequency: PLS179: 18MHz (max)**
- **Input loading: PLS179: – 100μA (max)**
- **Power dissipation: 725mW (typ)**
- **TTL Compatible**

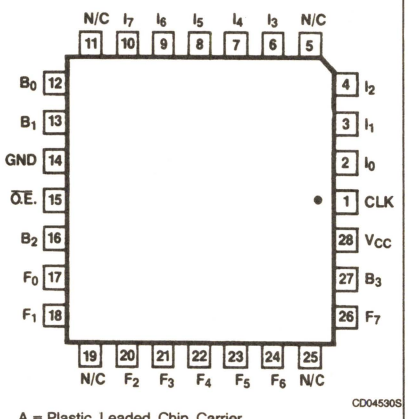
## PIN CONFIGURATION

**N PACKAGE**



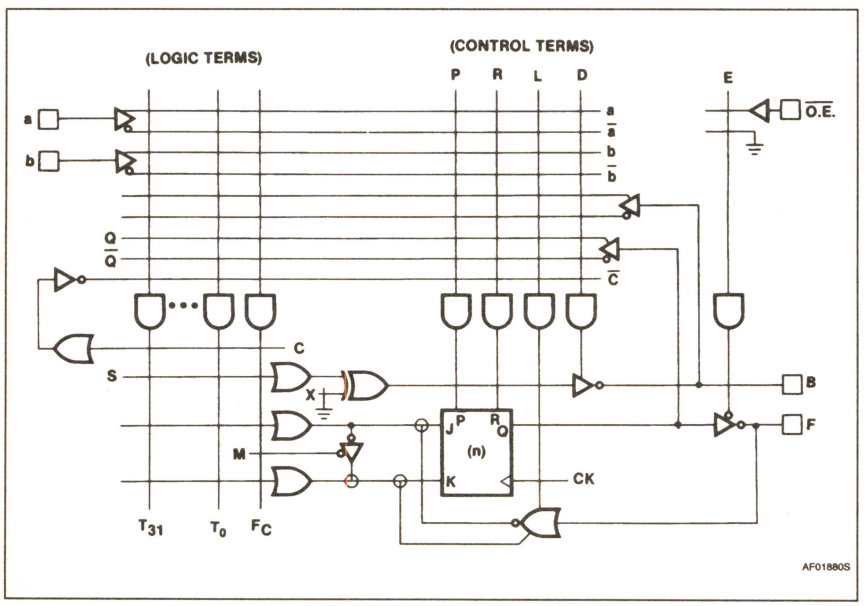

N = Plastic

**A PACKAGE***




A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




## APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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# PLS100/PLS101
## Field Programmable Array (16 × 48 × 8)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 28**

## DESCRIPTION

The PLS100 (Three-State) and PLS101 (Open Collector) are bipolar, fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The true, complement, or don't care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are selectively ORed to each output. The user must then only select which P-terms will activate an output by disconnecting terms which do not affect the output. In addition, each output can be fused as active HIGH (H) or active-LOW (L).

The PLS100 and PLS101 are fully TTL compatible, and include chip enable control for expansion of input variables and output inhibit. They feature either Open Collector or Three-State outputs for ease of expansion of product terms and application in bus-organized systems.

Order codes are contained on the pages following.

## FEATURES

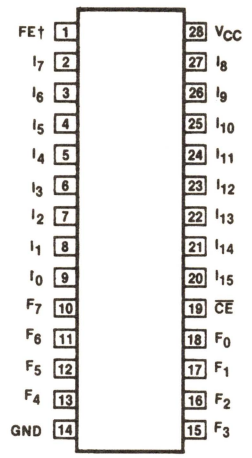
- **Field programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **I/O propagation delay: 50ns max**
- **Power dissipation: 600mW typ**
- **Input loading: −100μA max**
- **Chip enable input**
- **Output option:**
  - **PLS100: Three-state**
  - **PLS101: Open Collector**
- **Output disable function:**
  - **Three-state: Hi-Z**
  - **Open Collector: Hi**
- **Separate I/O architecture**

## APPLICATIONS

- **CRT display systems**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**
- **16-bit to 8-bit bus interface**
- **Random logic replacement**

## PIN CONFIGURATION

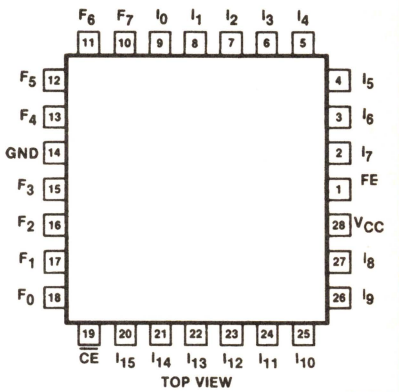
**N PACKAGE**




CD04281S

N = Plastic
†Open or grounded during normal operation.

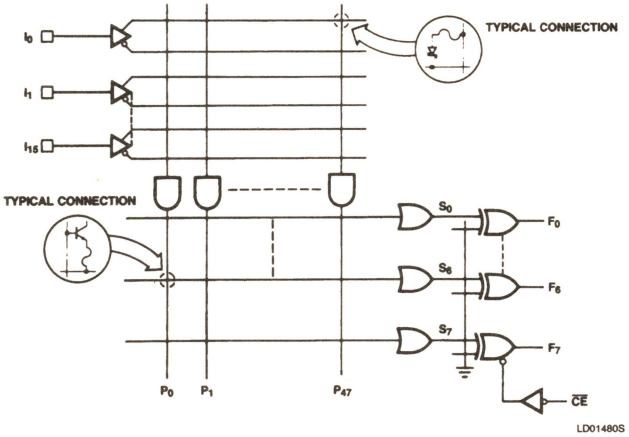
**A PACKAGE**




CD04271S

A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




LD01480S

Fusible Ni-Cr links are initially intact at all array cross-points.

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# PLS151
# Field-Programmable Gate Array (18 × 15 × 12)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 20**

## DESCRIPTION

The PLS151 is a single level logic element, consisting of 15 AND gates with fusible link connections for programming I/O polarity, I/O direction and output enable control.

All gates are linked to 6 inputs (I) and 12 bidirectional I/O lines (B). These yield variable I/O gate configurations via 3 direction control gates (D), ranging from 18 inputs to 12 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to each AND gate. The polarity of all gate outputs is individually programmable through a set of EX-OR gates for implementing AND/NAND logic functions. Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its inputs and outputs (DeMorgan's Theorem).

The PLS151 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are contained on the pages following.

## FEATURES

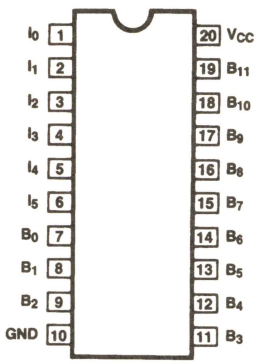
- **Field-Programmable (Ni-Cr link)**
- **6 inputs**
- **15 product terms:**
  - **12 logic terms**
  - **3 control terms**
- **12 bidirectional I/O lines**
- **Active high or low outputs**
- **Programmable output enable**
- **Power dissipation: 575mW (typ.)**
- **I/O propagation delay: 25ns (max.)**
- **Input loading: −100μA (max.)**
- **TTL compatible**
- **Tri-state outputs**

## APPLICATIONS

- **Random gating functions**
- **Address decoding**
- **Code detectors**
- **Memory mapped I/O**
- **Fault monitors**
- **I/O port decoders**

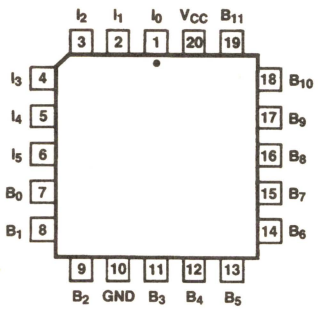
## PIN CONFIGURATION

**N Package**



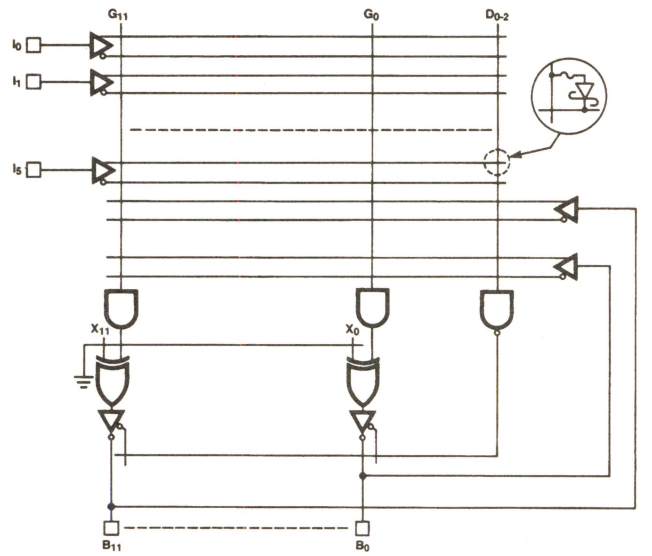

N = Plastic

**A Package**




A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




All Ni-Cr links are initially intact.

## LOGIC FUNCTION

**TYPICAL OUTPUT FUNCTIONS:**

**ACTIVE-HIGH**

$X = A \cdot \overline{B} \cdot C \cdot \ldots$

**ACTIVE-LOW**

$X = \overline{A \cdot \overline{B} \cdot C \cdot \ldots}$

$X = \overline{A} + B + \overline{C} + \ldots$

**NOTES:**
1. For each of the 12 outputs, either function X (Active-High) or $\overline{X}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

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# PLS153
# Field-Programmable Logic Array (18 × 42 × 10)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 20**

## DESCRIPTION

The PLS153 is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are contained on the pages following.

## FEATURES

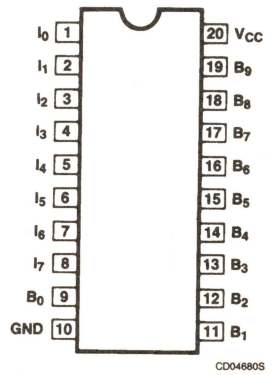
- **Field-Programmable (Ni-Cr links)**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active high or low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 40ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 650mW (typ.)**
- **Tri-state outputs**
- **TTL compatible**

## APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

## PIN CONFIGURATION

**N Package**




N = Plastic

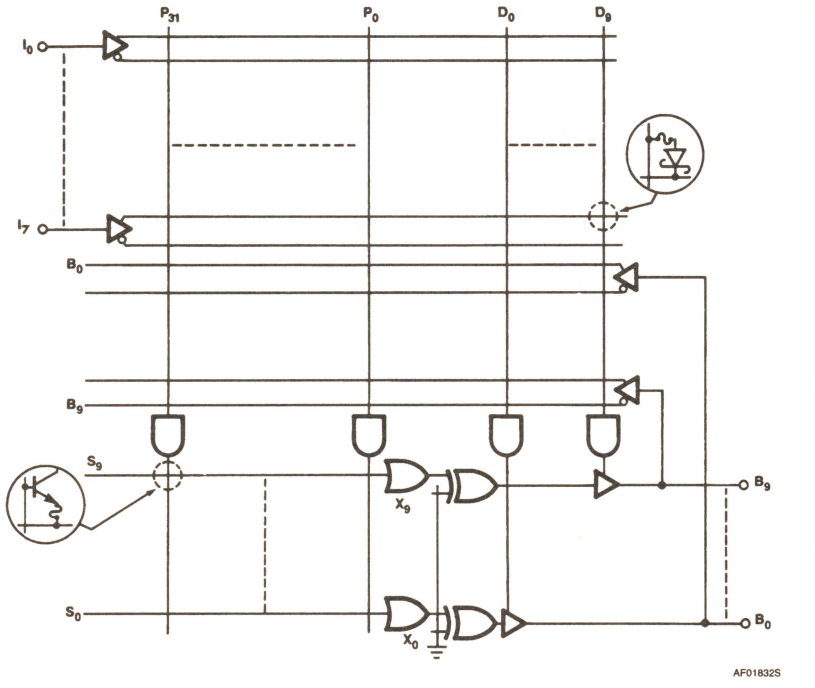
## LOGIC FUNCTION

**TYPICAL PRODUCT TERM:**
$Pn = A \cdot B \cdot C \cdot D \cdot \ldots$
**TYPICAL LOGIC FUNCTION:**
**AT OUTPUT POLARITY = H**
$Z = P0 + P1 + P2 \ldots$

**AT OUTPUT POLARITY = L**
$Z = \overline{P0 + P1 + P2 +} \ldots$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

**NOTES:**
1. For each of the 10 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

## FUNCTIONAL DIAGRAM

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# PLS162
# Field Programmable Address Decoder (16 × 5)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLS162 is a bipolar, Field Programmable Address Decoder. The device consists of five AND/NAND gates which share 16 common inputs. The type of gate is selected by programming the output as active-HIGH (H) or active-LOW (L). Each of the 16 inputs $I_0 - I_{15}$ can be programmed to provide the True (H), Complement (L), or Don't Care ( — ) state to each of the five AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS162 includes chip-enable control for output strobing and inhibit. It features Tri-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are contained on the following pages.

## FEATURES

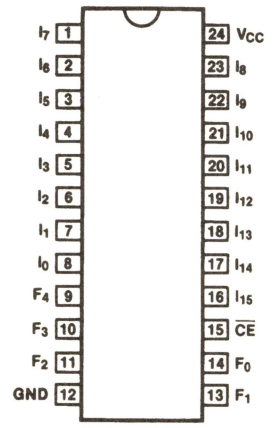
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **5 output functions**
- **Chip enable input**
- **I/O propagation delay: 30ns max**
- **Power dissipation: 500mW typ**
- **Input loading: −100μA max**
- **Output: Tri-State**
- **Output disable function: Hi-Z**
- **Fully TTL compatible**

## APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

## PIN CONFIGURATION

**N PACKAGE***




*N = Plastic

## LOGIC FUNCTION

**TYPICAL OUTPUT FUNCTIONS:**

**ACTIVE-HIGH**

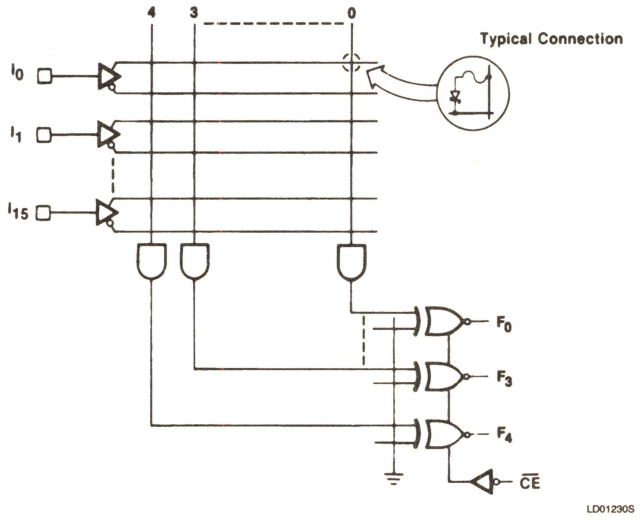
$$X = A \cdot \overline{B} \cdot C \cdot \ldots$$

**ACTIVE-LOW**

$$\overline{X} = \overline{A \cdot \overline{B} \cdot C \cdot \ldots}$$
$$X = \overline{A} + B + \overline{C} + \ldots$$

**NOTES:**
1. For each of the 5 outputs, either function X (active-high) or $\overline{X}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (F).

## FUNCTIONAL DIAGRAM




Fusible Ni-Cr links are initially intact at all array cross-points.

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# PLS163
# Field Programmable Address Decoder (12 × 9)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLS163 is a bipolar, Field Programmable Address Decoder. The device consists of nine AND/NAND gates which share 12 common inputs. The type of gate is selected by programming the output as active-HIGH (H) or active-LOW (L). Each of the 12 inputs $I_0 - I_{11}$ can be programmed to provide the True (H), Complement (L), or Don't Care ( — ) state to each of the nine AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS163 includes chip-enable control for output strobing and inhibit. It features Tri-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are contained on the following pages.

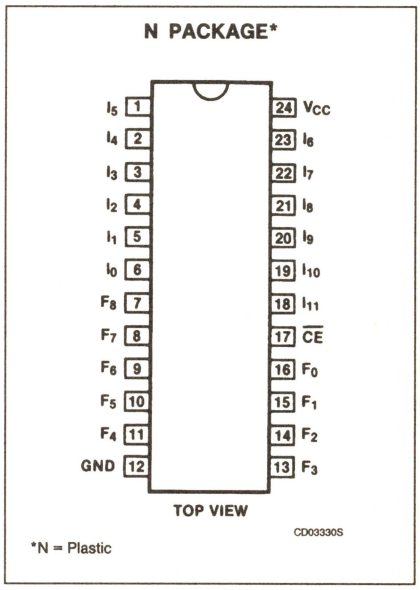
## FEATURES

- **Field programmable (Ni-Cr link)**
- **12 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay: 30ns max**
- **Power dissipation: 600mW typ**
- **Input loading: −100μA max**
- **Output: Tri-State**
- **Output disable function: Hi-Z**
- **Fully TTL compatible**

## APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

## PIN CONFIGURATION




*N = Plastic

## LOGIC FUNCTION

**TYPICAL OUTPUT FUNCTIONS:**

**ACTIVE-HIGH**

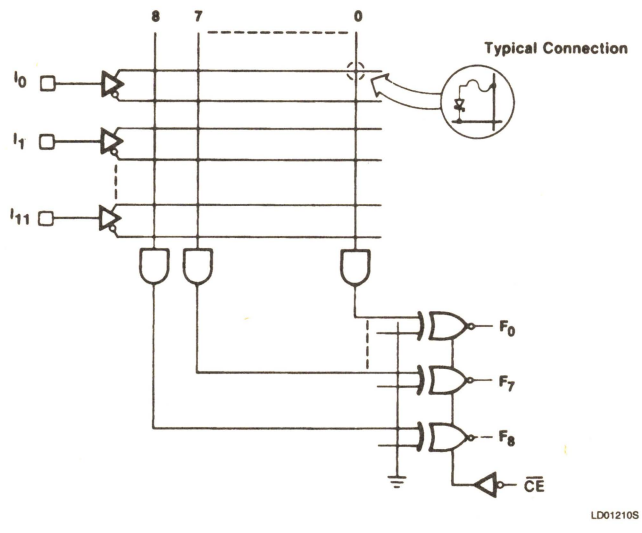
$$X = A \cdot \overline{B} \cdot C \cdot \ldots$$

**ACTIVE-LOW**

$$\overline{X = A \cdot \overline{B} \cdot C \cdot \ldots}$$
$$X = \overline{A} + B + \overline{C} + \ldots$$

**NOTES:**
1. For each of the 9 outputs, either function X (active-high) or $\overline{X}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (F).

## FUNCTIONAL DIAGRAM




Fusible Ni-Cr links are initially intact at all array cross-points.

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# PLS173
# Field Programmable Logic Array (22 × 42 × 10)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes for this device are contained in the pages following.

## FEATURES

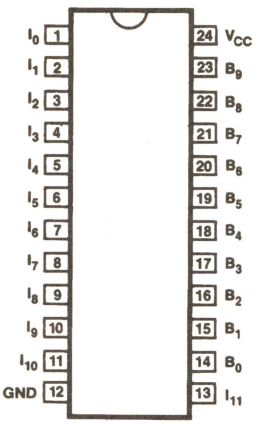
- **Field Programmable (Ni-Cr links)**
- **12 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active high or low outputs**
- **42 Product Terms:**
  - **32 Logic Terms**
  - **10 Control Terms**
- **I/O propagation delay: 30 nSec (max)**
- **Input loading: −100μA max**
- **Power dissipation: 750mW typ**
- **Output: three-state**
- **TTL compatible**

## APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

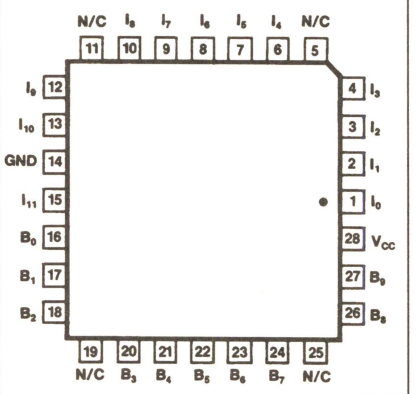
## PIN CONFIGURATION

**N PACKAGE**



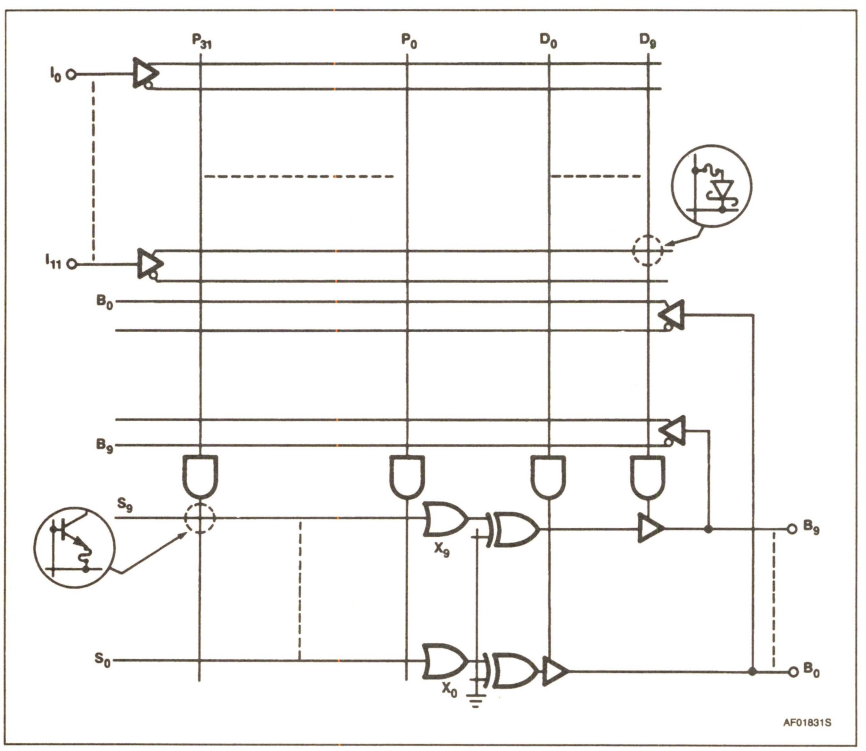

N = Plastic

**A PACKAGE**




A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




## LOGIC FUNCTION

**TYPICAL PRODUCT TERM:**
$Pn = A \cdot \bar{B} \cdot C \cdot D \cdot \ldots$

**TYPICAL LOGIC FUNCTION:**
**AT OUTPUT POLARITY = H**
$Z = P0 + P1 + P2 \ldots$

**AT OUTPUT POLARITY = L**
$Z = \overline{P0 + P1 + P2 + \ldots}$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

**NOTES:**
1. For each of the 10 outputs, either function Z (active-high) or Z (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

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# PLHS18P8
# Programmable AND Array Logic (18 × 72 × 8)

**Signetics Programmable Logic**
***Product Specification***

**Application Specific Products**
- **Series 20**

## DESCRIPTION

The PLHS18P8 is a two-level logic element consisting of 72 AND gates and 8 OR gates with fusible connections for programming I/O polarity and direction.

All AND gates are linked to 10 inputs (I) and 8 bidirectional I/O lines (B). These yield variable I/O gate configurations via 8 direction control gates, ranging from 18 inputs to 8 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates. The 72 AND gates are separated into 8 groups of 9 each. Each group of 9 is associated with one bidirectional pin. In each group, eight of the AND terms are ORed together, while the ninth is used to establish I/O direction. All outputs are individually programmable via an EX-OR gate to allow implementation of AND/OR or NAND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

The PLHS18P8 is field-programmable, allowing the user to quickly generate custom pattern using standard programming equipment.

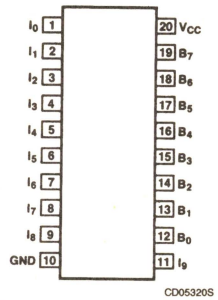
Order codes are contained in the pages following.

## FEATURES

- **100% functionally compatible with AmPAL18P8**
- **Field-programmable**
- **10 inputs**
- **8 bidirectional I/O lines**
- **72 AND gates/product terms**
  - **configured into eight groups of nine**
- **Programmable output polarity (Tri-state output)**
- **I/O propagation delay: 15ns (max)**
- **Power dissipation: 750mW (nominal)**
- **TTL compatible**
- **Verify Lock Fuse**
- **On-chip test features for extensive AC and DC parametric testing**

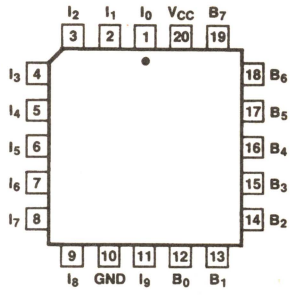
## PIN CONFIGURATION

**N PACKAGE**



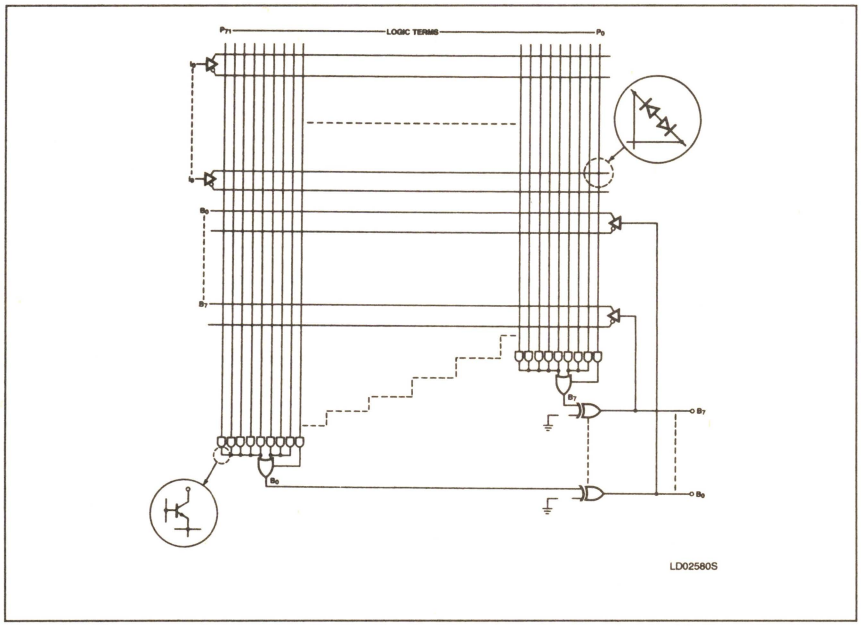

N = Plastic

**A PACKAGE**




A = Plastic Leader Chip Carrier

## FUNCTIONAL DIAGRAM




## LOGIC FUNCTION

**TYPICAL PRODUCT TERM:**
$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

**TYPICAL LOGIC FUNCTION:**

**AT OUTPUT POLARITY = H**
$Z = P0 + P1 + P2 \ldots$

**AT OUTPUT POLARITY = L**
$Z = \overline{P0 + P1 + P2 + \ldots}$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

**NOTES:**
1. For each of the 8 outputs, either function Z (active-high) or $\overline{Z}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

## APPLICATIONS

- **100% functional replacement for all 20-pin combinatorial PALs***
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**

*PAL is a registered trademark of Monolithic Memories, Inc.

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Signetics

# PLUS405A
# Field Programmable Logic Sequencer (16 × 64 × 8)

**Signetics Programmable Logic**
***Preliminary Specification***

**Application Specific Products**
- **Series 28**

## DESCRIPTION

The PLUS405A is a bipolar, programmable state machine of the Mealy type. Both the AND and the OR array are user programmable. All 64 AND gates are connected to the 16 external dedicated inputs ($I_0 - I_{15}$) and to the feedback paths of the 8 on-chip state registers ($Q_{P0} - Q_{P7}$). Both true and complement transition terms can be generated via optional use of the two internal Complement Arrays (input variables $C_0$, $C_1$).

All transition terms can include True, False and Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective registers. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the state and output registers.

All state ($Q_{P0} - P7$) and output ($Q_{F0} - F7$) registers are edge triggered, clocked J-K/S-R flip-flops, with asynchronous preset and reset options. The PLUS405A architecture provides the added flexibility of the J-K toggle function which is not allowed in the S-R mode. All 16 flip-flops may be individually programmed for operation in either the J-K or S-R configuration. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "I". (Note: Upon power-up, all registers are unconditionally preset to "I"). If desired, the initialization input pin (INIT) can be converted to an Output Enable ($\overline{OE}$) function as an additional user programmable feature.

Availability of two user programmable clocks allows the user to design an independently clocked, buried state machine.

Order codes are contained on the pages following.

## FEATURES

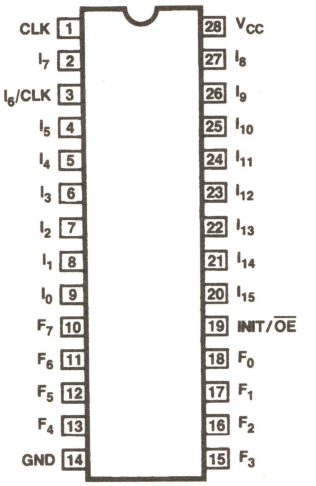
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **64 transition terms**
- **8-bit State Register**
- **8-bit Output Register**
- **2 Transition complement array term**
- **Multiple clocks**
- **Programmable asynchronous Preset/Reset or Output Enable**
- **Power-on preset to "1" of registers**
- **$f_{MAX}$ = 40MHz**
- **1000mW power dissipation (typical)**
- **TTL compatible**
- **J-K or S-R flip-flop functions**
- **Tri-state outputs**
- **Functional superset of PLS105/105A**

## APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

## PIN CONFIGURATION

**N Package**

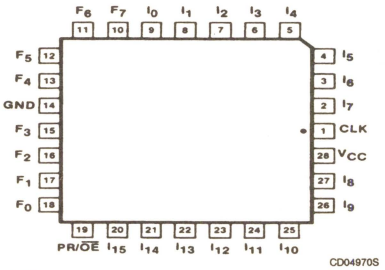



TOP VIEW

CD11461S

**NOTE:**
N = Plastic

**A Package**

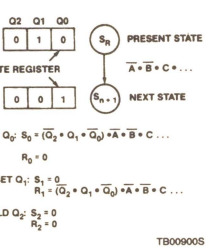



CD04970S

**NOTE:**
A = Plastic Leaded Chip Carrier

## LOGIC FUNCTION

**Typical State Transition:**




TB00900S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Signetics

# PLHS473
# Field Programmable Logic Array (20 × 24 × 11)

**Signetics Programmable Logic**
***Preliminary Specification***

**Application Specific Products**
- **Series 24**

## DESCRIPTION

The PLHS473 is a two level logic device consisting of 24 AND gates and 22 OR gates with fusible link connections for programming I/O polarity and direction. The Signetics state of the art Oxide Isolated Bipolar process is used to produce performance not yet achieved in devices of this complexity.

All AND gates are linked to 11 input pins, 9 bidirectional I/O pins, and 2 dedicated output pins. The bidirectional pins are controlled via the OR array. Using these features, the PLHS473 can be configured with up to 20 inputs and as many as 11 outputs.

On chip True/Complement buffers couple either the true or complement of all inputs ($I_0 - I_{10}$)) and bidirectional pins ($B_0 - B_8$) to all AND gates. All 24 AND gates may be optionally linked to any OR gate feeding a bidirectional pin or output pin ($O_A - O_B$). The output polarity is controlled by using the fuse option on the EX-OR gates found on all bidirectional and output pins. This makes the implementation of AND/OR and AND/NOR functions possible.

The PLHS473 contains two new features of significance. A code verification lock has been incorporated to improve user security. The addition of three test columns and one test row enables the user to test the device in an unprogrammed state.

The PLHS473 is field programmable using Vertical Avalanche Migration Programmed (VAMP)™ fuses to program the cells. This enables the generation of custom logic patterns using standard programming equipment.

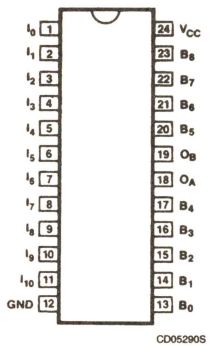
Order codes for this device are contained in the pages following.

## FEATURES

- **Field programmable**
- **11 dedicated inputs**
- **2 dedicated outputs**
- **9 bi-directional I/O lines**
- **24 Product Terms**
- **22 OR gates**
- **I/O direction decoded in OR array**
- **Output enable decoded in OR array**
- **I/O propagation delay: 20nSec (max)**
- **Input loading: −100μA (max)**
- **Power dissipation: 700mW (typ)**
- **Security fuse**
- **Testable in unprogrammed state**
- **Output: Programmable as Tri-State or Open Collector.**
- **TTL compatible**

## PIN CONFIGURATION

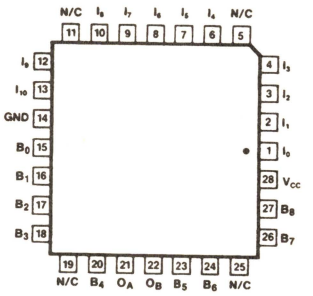
**N PACKAGE**




CD05290S

N = Plastic

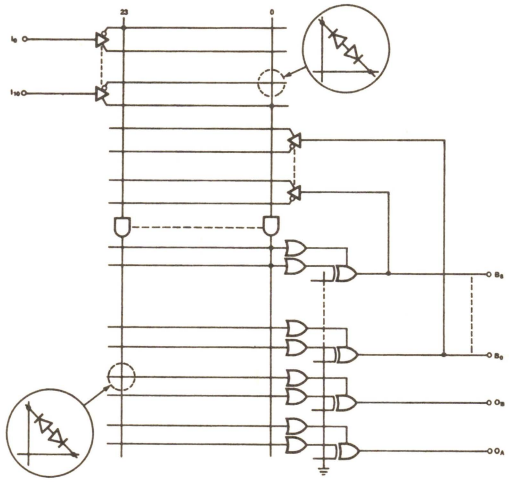
**A PACKAGE**




CD05300S

A = Plastic Leaded Chip Carrier

## FUNCTIONAL DIAGRAM




LD02640S

## LOGIC FUNCTION

**TYPICAL PRODUCT TERM:**
$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

**TYPICAL LOGIC FUNCTION:**
**AT OUTPUT POLARITY = H**
$Z = P0 + P1 + P2 \ldots$

**AT OUTPUT POLARITY = L**
$Z = \overline{P0 + P1 + P2 +} \ldots$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

**NOTES:**
1. For each of the 11 outputs, either function Z (active-high) or $\overline{Z}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I), fixed output pins (0) and bidirectional pins (B).

## APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**

Signetics

# Signetics

# Selection Guide

## Bipolar Memory Products

| DEVICE[5] | ORGANIZATION | OUTPUT CIRCUIT[1] | OUTPUT LOGIC[2] | ACCESS TIME[3] | PACKAGE[4] | PINS | MAX $I_{CC}$ |
|---|---|---|---|---|---|---|---|
| **RAMs** | | | | | | | |
| 82S25 | 16 × 4 | OC | B | 50 | N | 16 | 105 |
| 3101A | 16 × 4 | OC | B | 35 | N | 16 | 105 |
| 74S189 | 16 × 4 | TS | B | 35 | N | 16 | 110 |
| 74F189A | 16 × 4 | TS | — | 20 | N, A | 16, 20 | 55 |
| 82S16 | 256 × 1 | TS | T | 50 | N | 16 | 115 |
| 74S301 | 256 × 1 | OC | B | 50 | N | 16 | 130 |
| 82LS16 | 256 × 1 | TS | T | 40 | N | 16 | 70 |
| 74LS301 | 256 × 1 | OC | B | 40 | N | 16 | 70 |
| 82S09 | 64 × 9 | OC | T | 45 | A, N | 28 | 190 |
| 82S09A | 64 × 9 | OC | T | 35 | A, N | 28 | 190 |
| 82S19 | 64 × 9 | OC | B | 35 | N | 28 | 190 |
| 82S212 | 256 × 9 | TS | B | 45 | N | 22 | 185 |
| 82S212A | 256 × 9 | TS | B | 35 | N | 22 | 185 |
| 8X350 | 256 × 8 | TS | B | N/A | N | 22 | 185 |
| **PROMs** | | | | | | | |
| 82S23 | 32 × 8 | OC | — | 50 | N, A | 16, 20 | 96 |
| 82S23A | 32 × 8 | OC | — | 25 | N, A | 16, 20 | 96 |
| 82US23[6] | 32 × 8 | OC | — | 10 | N, A | 16, 20 | 115 |
| 82S123 | 32 × 8 | TS | — | 50 | N, A | 16, 20 | 96 |
| 82S123A | 32 × 8 | TS | — | 25 | N, A | 16, 20 | 96 |
| 82US123[6] | 32 × 8 | TS | — | 10 | N, A | 16, 20 | 115 |
| 82S126 | 256 × 4 | OC | — | 50 | N, A | 16, 20 | 120 |
| 82S126A | 256 × 4 | OC | — | 30 | N, A | 16, 20 | 120 |
| 82S129 | 256 × 4 | TS | — | 50 | N, A | 16, 20 | 120 |
| 82S129A | 256 × 4 | TS | — | 27 | N, A | 16, 20 | 120 |
| 10149 | 256 × 4 | OE | — | 20 | F | 16 | 150 |
| 10149A | 256 × 4 | OE | — | 10 | F | 16 | 160 |
| 100149 | 256 × 4 | OE | — | 20 | F | 16 | 150 |
| 100149A | 256 × 4 | OE | — | 10 | F | 16 | 160 |
| 82S130 | 512 × 4 | OC | — | 50 | N, A | 16, 20 | 140 |
| 82S130A | 512 × 4 | OC | — | 33 | N, A | 16, 20 | 140 |
| 82S131 | 512 × 4 | TS | — | 50 | N, A | 16, 20 | 140 |
| 82S131A | 512 × 4 | TS | — | 30 | N, A | 16, 20 | 140 |
| 82LS135 | 256 × 8 | TS | — | 100 | A, N | 20 | 100 |
| 82S135 | 256 × 8 | TS | — | 45 | A, N | 20 | 150 |
| 82S115 | 512 × 8 | TS | — | 60 | N | 24 | 175 |
| 82S137 | 1024 × 4 | TS | — | 60 | N, A | 18, 20 | 140 |
| 82S137A | 1024 × 4 | TS | — | 45 | N, A | 18, 20 | 140 |
| 82S137B | 1024 × 4 | TS | — | 35 | N, A | 18, 20 | 140 |
| 82S137C[6] | 1024 × 4 | TS | — | 25 | N, A | 18, 20 | 140 |
| 82S147 | 512 × 8 | TS | — | 60 | A, N | 20 | 155 |
| 82S147A | 512 × 8 | TS | — | 45 | A, N | 20 | 155 |
| 82S147B[6] | 512 × 8 | TS | — | 25 | N, A | 20 | 155 |
| 82LS181 | 1024 × 8 | TS | — | 120 | A, N | 24 | 80 |
| 82S181 | 1024 × 8 | TS | — | 70 | N | 24 | 175 |
| 82S181A | 1024 × 8 | TS | — | 55 | N, A | 24, 28 | 175 |
| 82S181C | 1024 × 8 | TS | — | 35 | N, N3, A | 24, 28 | 175 |
| 82S183 | 1024 × 8 | TS | — | 60 | N, A | 24, 28 | 175 |
| 82S185 | 2048 × 4 | TS | — | 100 | N | 18 | 120 |





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# Selection Guide

| DEVICE[5] | ORGANIZATION | OUTPUT CIRCUIT[1] | OUTPUT LOGIC[2] | ACCESS TIME[3] | PACKAGE[4] | PINS | MAX $I_{CC}$ |
|---|---|---|---|---|---|---|---|
| **PROMs** | | | | | | | |
| 82S185A | 2048 × 4 | TS | — | 50 | N | 18 | 155 |
| 82S185C[6] | 2048 × 4 | TS | — | 25 | N, A | 18, 20 | 155 |
| 82HS187 | 1024 × 8 | TS | R | 55 | N, A | 24, 28 | 175 |
| 82HS187A | 1024 × 8 | TS | R | 45 | N, A | 24, 28 | 175 |
| 82HS189 | 1024 × 8 | TS | R | 55 | N, A | 24, 28 | 175 |
| 82HS189A | 1024 × 8 | TS | R | 45 | N, A | 24, 28 | 175 |
| 82HS191 | 2048 × 8 | TS | — | 20 | N, N3, A | 24, 28 | 175 |
| 82S191 | 2048 × 8 | TS | — | 80 | N, A | 24, 28 | 175 |
| 82S191A | 2048 × 8 | TS | — | 55 | N, A | 24, 28 | 175 |
| 82S191C | 2048 × 8 | TS | — | 35 | A, N, N3 | 24 | 175 |
| 82HS195 | 4096 × 4 | TS | — | 45 | N | 20 | 145 |
| 82HS195A | 4096 × 4 | TS | — | 35 | N | 20 | 145 |
| 82HS195B | 4096 × 4 | TS | — | 25 | N | 20 | 145 |
| 82HS197[6] | 2048 × 8 | TS | R | 65 | N | 24 | 175 |
| 82HS199[6] | 2048 × 8 | TS | R | 65 | N | 24 | 175 |
| 82HS321 | 4096 × 8 | TS | — | 45 | N, A | 24, 28 | 175 |
| 82HS321A | 4096 × 8 | TS | — | 35 | N, A | 24, 28 | 175 |
| 82HS321B | 4096 × 8 | TS | — | 30 | N, A | 24, 28 | 175 |
| 82HS641 | 8192 × 8 | TS | — | 55 | N | 24, 28 | 175 |
| 82HS641A | 8192 × 8 | TS | — | 45 | N | 24, 28 | 175 |
| 82HS641B | 8192 × 8 | TS | — | 35 | N | 24, 28 | 175 |
| 82HS1281[6] | 16384 × 8 | TS | — | 45 | N | 24 | 185 |

**NOTES:**

1. Output circuit
   OE = Open Emitter
   OC = Open Collector
   TS = 3-State
2. Output logic
   T = Transparent — input data appears on output during Write
   B = Blanked — output is blanked during Write
   R = Registers
   I/O = Programmable input/output option
3. Commercial (0°C to +75°C)
4. Packages:
   N = Plastic Dual In Line (N3 = 300mil-wide)*
   A = Plastic Square Leaded Chip Carrier
   D = Small Outline Large (SO-L)
   *Whenever a single device is offered in both 300mil-wide and 600mil-wide packages, designate either N3 (300mil) or N (600mil) to assure proper order entry and shipment.
5. Part numbers:
   82Sxxx Junction-Isolated
   82HSxxx Oxide-Isolated
   82USxxx Oxide-Isolated TiW fuse
6. Objective specification (under product development)



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Signetics

# 82HS187
# 82HS187A
# 8K-Bit TTL Bipolar PROM

***Product Specification***

**Bipolar Memory Products**

## DESCRIPTION

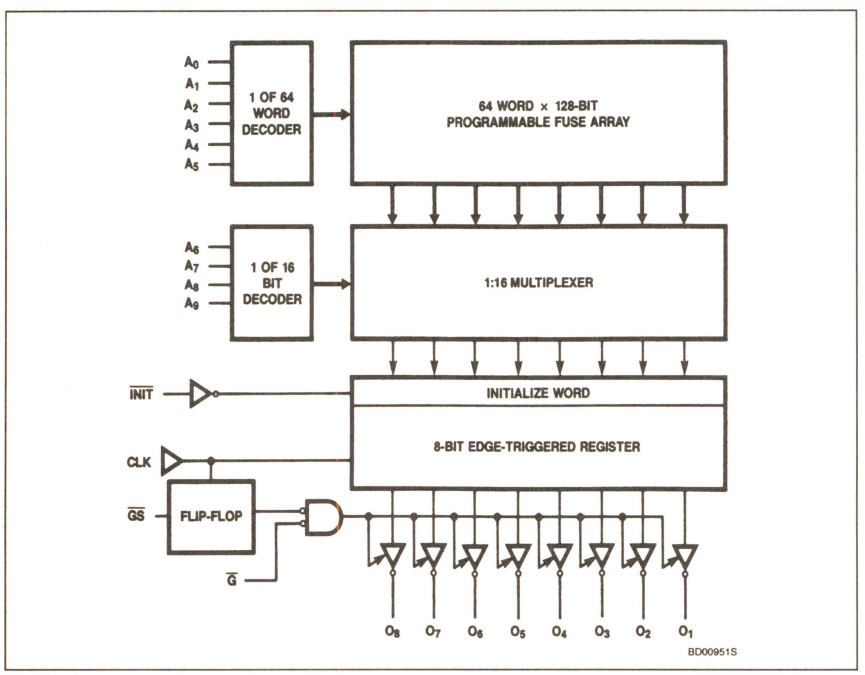
The 82HS187 is a programmable read only memory containing D-type, master-slave data registers. The 82HS187 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is Three-state for ease in connection to bus-organized systems. The combination of on-chip registers and Three-state outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition whenever the asynchronous chip enable ($\overline{G}$) is High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of $V_{CC}$.

The 82HS187 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register and will appear at the outputs upon an application of a Low on $\overline{INIT}$ if the outputs are enabled, and will control the state of the data registers independent of all other inputs. The unprogrammed state of $\overline{INIT}$ is all ones.

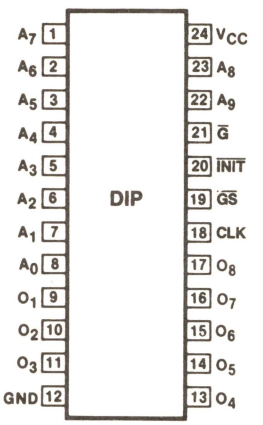
Data is read from the PROM by first applying an address to inputs $A_0$ to $A_9$. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the addresses and synchronous chip enable can be removed and the output data will remain stable.

## BLOCK DIAGRAM




## PIN CONFIGURATION

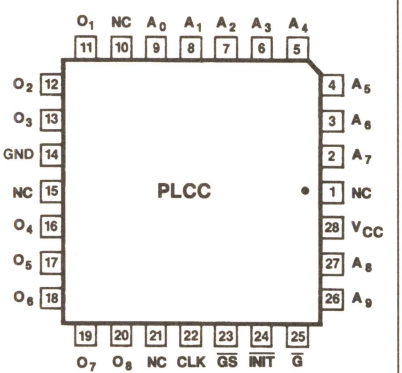
**N PACKAGE**




TOP VIEW

CD01200S

**A PACKAGE**




CD04531S

## FEATURES

- **On-chip edge-triggered registers**
- **Programmable register with asynchronous Initialize function**
- **24-pin 300mil-wide DIP package**
- **Read cycle "Address setup plus clock to output delay"**
  - **N82HS187: 55ns max**
  - **N82HS187A: 45ns max**
- **Outputs: Three-state**
- **Unprogrammed outputs are High level**
- **Synchronous and asynchronous enables for word expansion**

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# 82HS189
# 82HS189A
# 8K-Bit TTL Bipolar PROM

***Product Specification***

**Bipolar Memory Products**

## DESCRIPTION

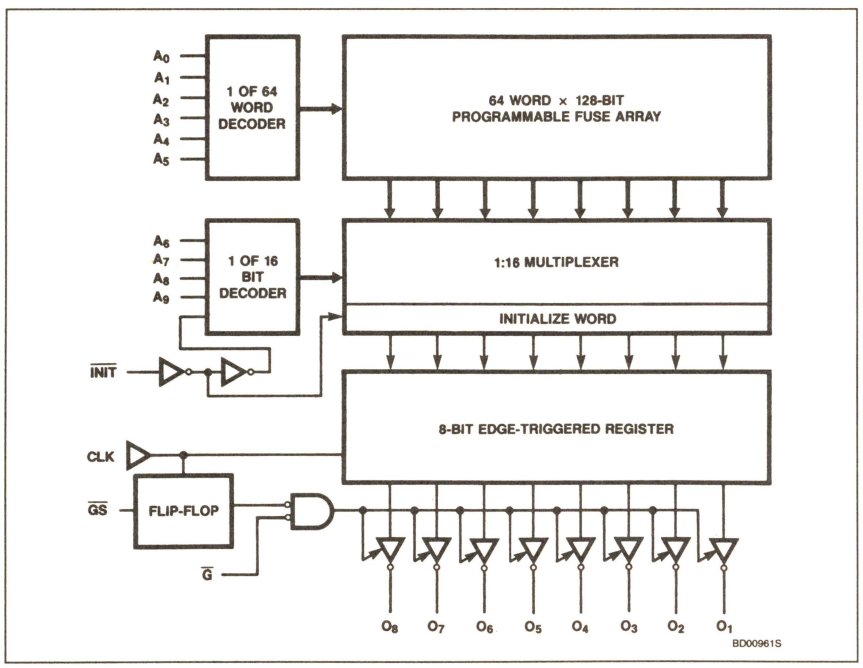
The 82HS189 is a programmable read only memory containing D-type, master-slave data registers. The 82HS189 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is Three-state for ease in connection to bus-organized systems. The combination of on-chip registers and Three-state outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition if the asynchronous chip enable ($\overline{G}$) is held High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of $V_{CC}$.

The 82HS189 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of $\overline{INIT}$ is all ones.

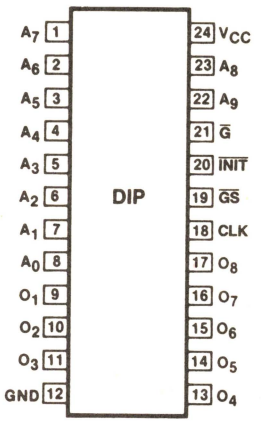
Data is read from the PROM by first applying an address to inputs $A_0$ to $A_9$. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the addresses and synchronous chip enable can be removed and the output data will remain stable.

## BLOCK DIAGRAM




## PIN CONFIGURATION

**N PACKAGE**

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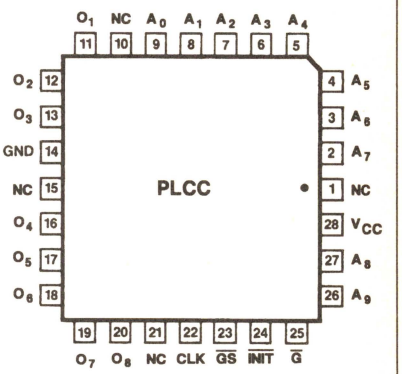


## FEATURES

- **On-chip edge-triggered registers**
- **Asynchronous and synchronous enables for word expansion**
- **Programmable register with synchronous initialize function**
- **24-pin 300mil package**
- **Read cycle "Address Setup plus Clock to Output Delay"**
  - **N82HS189: 55ns max**
  - **N82HS189A: 45ns max**
- **Unprogrammed outputs are High level**
- **Outputs: Three-state**

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# 82HS321
# 82HS321A
# 82HS321B
## 32K-Bit TTL Bipolar PROM

**Bipolar Memory Products**

*Product Specification*

## DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

## FEATURES

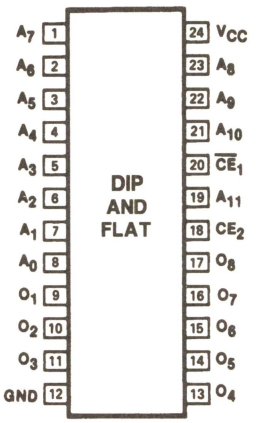
- **Address access time:**
  **N82HS321: 45ns max**
  **N82HS321A: 35ns max**
  **N82HS321B 30ns max**
- **Power dissipation: 20μW/bit typ**
- **Input loading: −100μA max**
- **2 chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: Three-state**

## APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

## PIN CONFIGURATION

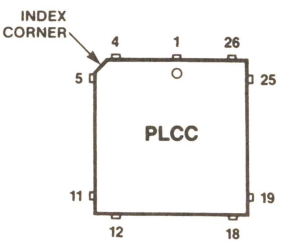
**N PACKAGE**




TOP VIEW

CD00951S

**A PACKAGE**

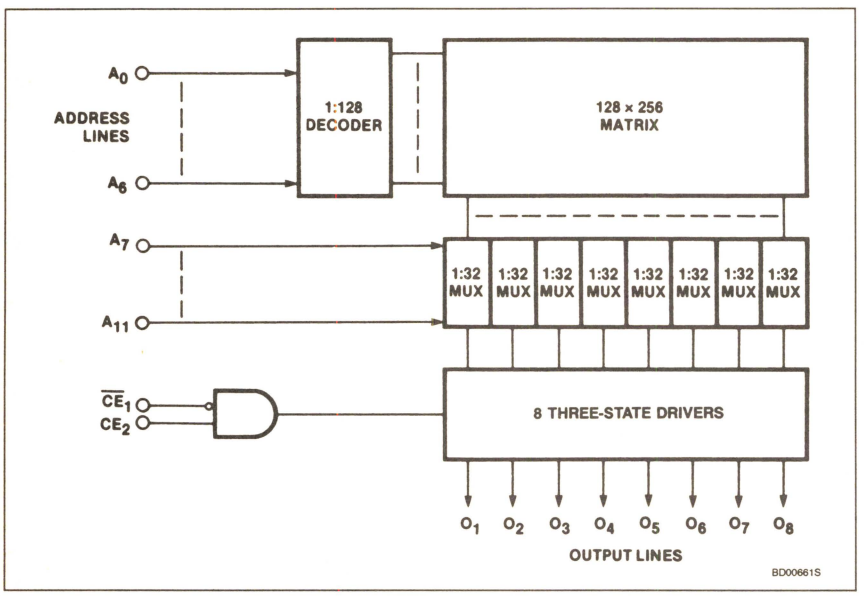



TOP VIEW

CD0028PS

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 15 | NC |
| 2 | $A_7$ | 16 | $O_4$ |
| 3 | $A_6$ | 17 | $O_5$ |
| 4 | $A_5$ | 18 | $O_6$ |
| 5 | $A_4$ | 19 | $O_7$ |
| 6 | $A_3$ | 20 | $O_8$ |
| 7 | $A_2$ | 21 | NC |
| 8 | $A_1$ | 22 | $\overline{CE}_2$ |
| 9 | $A_0$ | 23 | $A_{11}$ |
| 10 | NC | 24 | $\overline{CE}_1$ |
| 11 | $O_1$ | 25 | $A_{10}$ |
| 12 | $O_2$ | 26 | $A_9$ |
| 13 | $O_3$ | 27 | $A_8$ |
| 14 | GND | 28 | $V_{CC}$ |

## BLOCK DIAGRAM

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# 32K-Bit TTL Bipolar PROM (4096 × 8) 82HS321, 82HS321A, 82HS321B

## ORDERING CODE

| PACKAGE DESCRIPTION | ORDER CODES |
|---|---|
| Plastic Dual Inline 600mil wide 24-pin | N82HS321 N • N82HS321A N • N82HS321B N |
| Ceramic Dual Inline 600mil wide 24-pin | N82HS321 F • N82HS321A F • N82HS321B F |
| Plastic Leaded Chip Carrier 450mil sq 28-pin | N82HS321 A • N82HS321A A • N82HS321B A |

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +7 | $V_{dc}$ |
| $V_{IN}$ | Input voltage | +5.5 | $V_{dc}$ |
| $V_O$ | Output voltage<br>Off-state | +5.5 | $V_{dc}$ |
| $T_A$<br>$T_{STG}$ | Temperature range<br>Operating<br>Storage | 0 to +75<br>−65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

| PARAMETER | | TEST CONDITIONS[1,2] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[5] | Max | |
| **Input voltage** | | | | | | |
| $V_{IL}$ | Low[3] | | | | 0.8 | V |
| $V_{IH}$ | High[3] | | 2.0 | | | |
| $V_{IC}$ | Clamp | $I_{IN} = -12mA$ | | −0.8 | −1.2 | |
| **Output voltage** | | $\overline{CE}_1$ = Low, $CE_2$ = High | | | | |
| $V_{OL}$ | Low | $I_{OUT} = 9.6mA$ | | | 0.45 | V |
| $V_{OH}$ | High | $I_{OUT} = -2mA$ | 2.4 | | | |
| **Input current** | | | | | | |
| $I_{IL}$ | Low | $V_{IN} = 0.45V$ | | | −100 | μA |
| $I_{IH}$ | High | $V_{IN} = 5.5V$ | | | 40 | |
| **Output current** | | | | | | |
| $I_{OZ}$ | Hi-Z state | $\overline{CE}_1$ = High, $CE_2$ = Low, $V_{OUT} = 0.5$ | | | −40 | μA |
| | | $\overline{CE}_1$ = High, $CE_2$ = Low, $V_{OUT} = 5.5$ | | | 40 | |
| $I_{OS}$ | Short circuit[4] | $\overline{CE}_1$ = Low, $CE_2$ = High, $V_{OUT} = 0V$ | −15 | | −70 | mA |
| **Supply current** | | | | | | |
| $I_{CC}$ | | $V_{CC} = 5.25V$ | | 130 | 175 | mA |
| **Capacitance** | | | | | | |
| | | $\overline{CE}_1$ = High, $CE_2$ = Low, $V_{CC} = 5.0V$ | | | | |
| $C_{IN}$ | Input | $V_{IN} = 2.0V$ | | 5 | | pF |
| $C_{OUT}$ | Output | $V_{OUT} = 2.0V$ | | 8 | | |

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# 82HS641
# 82HS641A
# 82HS641B
## 64K-Bit TTL Bipolar PROM

*Product Specification*

**Bipolar Memory Products**

The 82HS641 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing Procedure. The 82HS641 is supplied with all outputs at a logical High. Outputs are programmed to a logic low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip address decoding with 1 chip enable input for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused applications.

Ordering information can be found on the following page.

This device is also processed to military requirements for operating over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

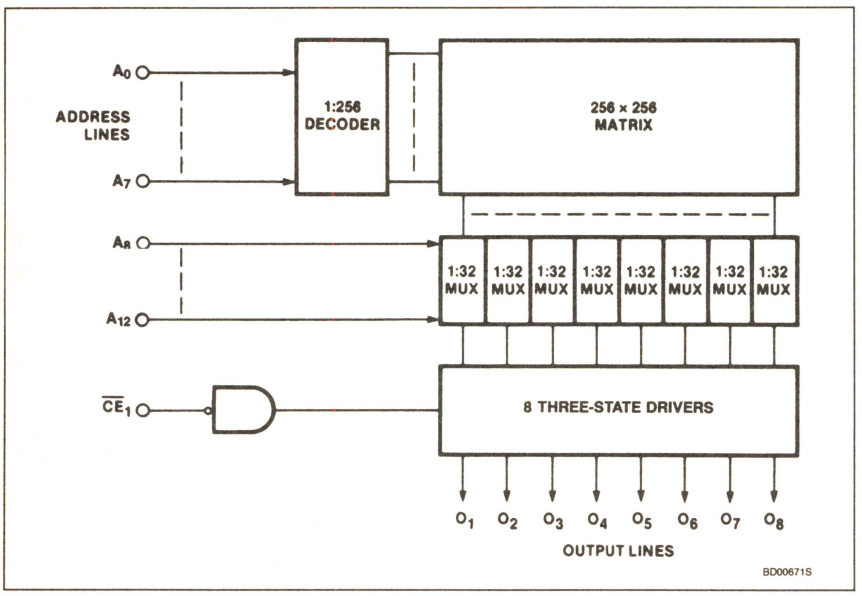
### FEATURES

- **Address access time:**
  - **N82HS641 55ns max**
  - **N82HS641A 45ns max**
  - **N82HS641B 35ns max**
- **Power dissipation: 10$\mu$W/bit typ**
- **Input loading: −100$\mu$A max**
- **One chip enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: Three-state**

### APPLICATIONS

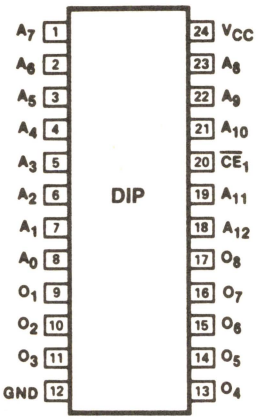
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

### BLOCK DIAGRAM




### PIN CONFIGURATION

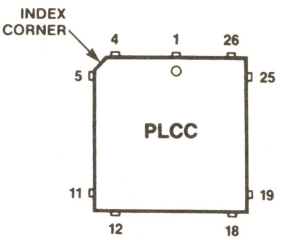
**N PACKAGE**




TOP VIEW

CD00960S

**A PACKAGE**




TOP VIEW

CD0028PS

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 15 | NC |
| 2 | $A_7$ | 16 | $O_4$ |
| 3 | $A_6$ | 17 | $O_5$ |
| 4 | $A_5$ | 18 | $O_6$ |
| 5 | $A_4$ | 19 | $O_7$ |
| 6 | $A_3$ | 20 | $O_8$ |
| 7 | $A_2$ | 21 | NC |
| 8 | $A_1$ | 22 | $A_{12}$ |
| 9 | $A_0$ | 23 | $A_{11}$ |
| 10 | NC | 24 | $\overline{CE}_1$ |
| 11 | $O_1$ | 25 | $A_{10}$ |
| 12 | $O_2$ | 26 | $A_9$ |
| 13 | $O_3$ | 27 | $A_8$ |
| 14 | GND | 28 | $V_{CC}$ |

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# 64K-Bit TTL Bipolar PROM (8192 × 8) — 82HS641, 82HS641A, 82HS641B

## ORDERING CODE

| PACKAGE DESCRIPTION | ORDER CODES |
|---|---|
| Plastic Dual Inline<br>600mil wide 24-pin | N82HS641 N • N82HS641A N • N82HS641B N |
| Ceramic Dual Inline<br>600mil wide 24-pin | N82HS641 F • N82HS641A F • N82HS641B F |
| Plastic Leaded Chip Carrier<br>450mil sq 28-pin | N82HS641 A • N82HS641A A • N82HS641B A |

## ABSOLUTE MAXIMUM RATINGS

| | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +7 | $V_{dc}$ |
| $V_{IN}$ | Input voltage | +5.5 | $V_{dc}$ |
| $V_O$ | Output voltage<br>Off-state | +5.5 | $V_{dc}$ |
| $T_A$<br>$T_{STG}$ | Temperature range<br>Operating<br>Storage | 0 to +75<br>−65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

| PARAMETER | | TEST CONDITIONS[1,2] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[5] | Max | |
| **Input voltage** | | | | | | |
| $V_{IL}$ | Low[3] | | | | 0.8 | V |
| $V_{IH}$ | High[3] | | 2.0 | | | |
| $V_{IC}$ | Clamp | $I_{IN} = -12mA$ | | −0.8 | −1.2 | |
| **Output voltage** | | $\overline{CE}_1$ = Low | | | | |
| $V_{OL}$ | Low | $I_{OUT} = 9.6mA$ | | | 0.45 | V |
| $V_{OH}$ | High | $I_{OUT} = -2mA$ | 2.4 | | | |
| **Input current** | | | | | | |
| $I_{IL}$ | Low | $V_{IN} = 0.45V$ | | | −100 | μA |
| $I_{IH}$ | High | $V_{IN} = 5.5V$ | | | 40 | |
| **Output current** | | | | | | |
| $I_{OZ}$ | Hi-Z State | $\overline{CE}_1$ = High, $V_{OUT} = 0.5V$ | | | −40 | μA |
| | | $\overline{CE}_1$ = High, $V_{OUT} = 5.5V$ | | | 40 | |
| $I_{OS}$ | Short circuit[4] | $\overline{CE}_1$ = Low, $V_{OUT} = 0V$ | −15 | | −70 | mA |
| **Supply current** | | | | | | |
| $I_{CC}$ | | $V_{CC} = 5.25V$ | | 130 | 175 | mA |
| **Capacitance** | | $\overline{CE}_1$ = High<br>$V_{CC} = 5.0V$ | | | | |
| $C_{IN}$ | Input | $V_{IN} = 2.0V$ | | 5 | | pF |
| $C_{OUT}$ | Output | $V_{OUT} = 2.0V$ | | 8 | | |

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# 82S191C
# 16K-Bit TTL Bipolar PROM

***Product Specification***

**Bipolar Memory Products**

## DESCRIPTION

The 82S191C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191C is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S191C devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

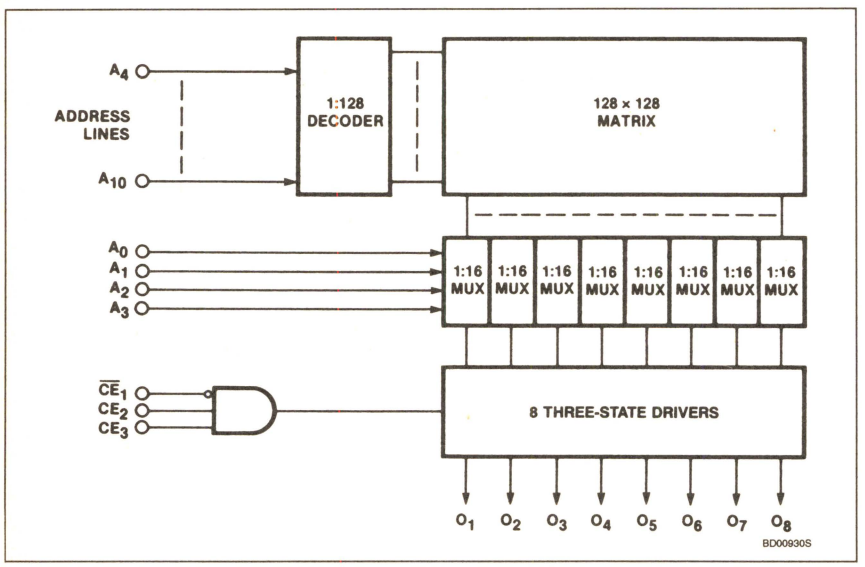
## FEATURES

- **Address access time: 35ns max**
- **Power dissipation: 40$\mu$W/bit typ**
- **Input loading: −100$\mu$A max**
- **Three chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Outputs: Three-state**

## APPLICATIONS

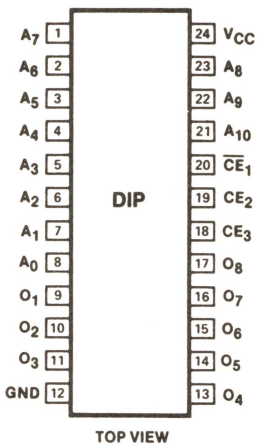
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

## BLOCK DIAGRAM

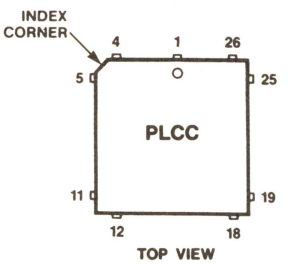



## PIN CONFIGURATION

**N PACKAGE**




**A PACKAGE**




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 15 | NC |
| 2 | $A_7$ | 16 | $O_4$ |
| 3 | $A_6$ | 17 | $O_5$ |
| 4 | $A_5$ | 18 | $O_6$ |
| 5 | $A_4$ | 19 | $O_7$ |
| 6 | $A_3$ | 20 | $O_8$ |
| 7 | $A_2$ | 21 | NC |
| 8 | $A_1$ | 22 | $\overline{CE}_3$ |
| 9 | $A_0$ | 23 | $\overline{CE}_2$ |
| 10 | NC | 24 | $\overline{CE}_1$ |
| 11 | $O_1$ | 25 | $A_{10}$ |
| 12 | $O_2$ | 26 | $A_9$ |
| 13 | $O_3$ | 27 | $A_8$ |
| 14 | GND | 28 | $V_{CC}$ |

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# 10149
# 1K-Bit ECL Bipolar PROM

***Product Specification***

**Bipolar Memory Products**

## DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149 is suitable for use in high performance ECL systems. The outputs are capable of driving 50Ω loads.

A chip enable input is provided for ease of memory expansion.

Ordering information can be found on the folowing page.

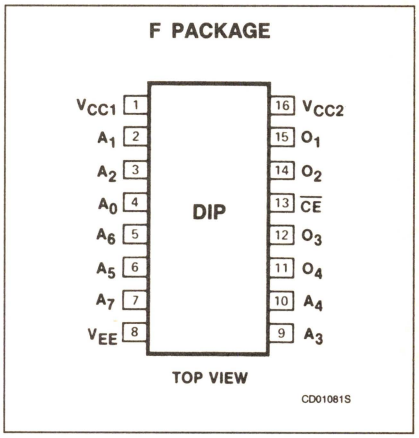
## FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

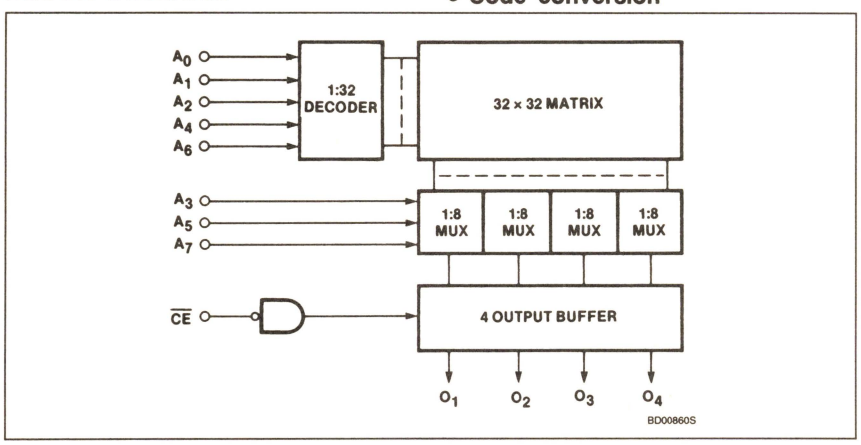
## APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

## PIN CONFIGURATION




## BLOCK DIAGRAM

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# Signetics

# 74F764/765
## DRAM Dual-Ported Controllers

**Logic Products**

***Preliminary Specification***

### FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Replaces 25 discrete devices**
- **Performs arbitration, signal timing, address multiplexing, and refresh**
- **9 address output pins allow direct control of up to 256K dynamic RAMS**
- **External address multiplexing enables control of 1 Mbit (or more) dynamic RAMS**
- **Separate refresh clock allows adjustable refresh timing**
- **F764 has on-chip 18-bit address input latch**
- **100 MHz Maximum clock rate**
- **Allows control of dynamic RAMs with row access times down to 40 ns**

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F764/765 | 150 MHz | 150 mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74F764N, N74F765N |
| PLCC-44 | N74F764A, N74F765A |

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $\overline{REQ1}$, $\overline{REQ2}$ | Request inputs (Active LOW) | 1.0/1.0 | 20 μA/0.6 mA |
| CP | Clock input | 1.0/1.0 | 20 μA/0.6 mA |
| RCP | Refresh clock input | 1.0/1.0 | 20 μA/0.6 mA |
| A1–A18 | Address inputs | 1.0/1.0 | 20 μA/0.6 mA |
| GNT | Grant output | 1750/100 | 35 mA/60 mA |
| $\overline{SEL1}$, $\overline{SEL2}$ | Select outputs (Active LOW) | 1750/100 | 35 mA/60 mA |
| DTACK | Data Transfer Acknowledge output | 1750/100 | 35 mA/60 mA |
| $\overline{RAS}$ | Row Address Strobe (output active LOW) | 1750/100 | 35 mA/60 mA |
| WG | Write Gate output | 1750/100 | 35 mA/60 mA |
| $\overline{CASEN}$ | Column Address Strobe Enable output (Active LOW) | 1750/100 | 35 mA/60 mA |
| MA0–MA8 | Address outputs | 1750/100 | 35 mA/60 mA |

NOTE: One (1.0) FAST Unit Load is defined as; 20 μA in the HIGH state and 0.6 mA in the LOW state.

### DESCRIPTION

The 74F764/765 DRAM Dual-Ported Controller is a high speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

The 74F764 contains an on-chip address input latch which latches the address inputs at the start of a memory access cycle.

The 74F765 is an unlatched option of the 74F764, designed for use in systems that provide latched address lines i.e. processors with non-multiplexed address and data bus.

Both devices are available in 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.





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# 74LS765
# DRAM Controller

**DRAM Dual-Ported Controller**
***Preliminary Specification***

**Products**

## FEATURES

- **Allows two microprocessors to access the same bank of DRAM**
- **Replaces 25 TTL devices to perform arbitration, signal timing, multiplexing, and refresh generation**
- **9 address output pins allow control of up to 256K DRAMS**
- **Separate refresh clock allows adjustable refresh timing**
- **Same as LS764 but without input latch**
- **30MHz Maximum Clock rate**

## DESCRIPTION

The 74LS765 DRAM Dual-Ported Controller is a high speed, clocked dual port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of memory. The device performs arbitration, signal timing, address multiplexing and refresh, replacing up to 25 discrete TTL devices.

The 'LS765 unlatched option eliminates the address input latch to facilitate use with latched address outputs.

The device is available in a 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS765 | 45ns | 215mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS765N* |
| PLCC-44 | N74LS765A** |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| $\overline{REQ}_1$, $\overline{REQ}_2$ | Request inputs (active LOW) | 1LSUL |
| CP | Clock input | 1LSUL |
| RCP | Refresh clock input | 1LSUL |
| A1 – A18 | Address inputs | 1LSUL |
| GNT | Grant output | 60LSUL |
| $\overline{SEL}_1$, $\overline{SEL}_2$ | Select outputs (active LOW) | 60LSUL |
| DTACK | Data transfer acknowledge output | 60LSUL |
| $\overline{RAS}$ | Row address strobe (output active LOW) | 60LSUL |
| WG | Write gate output | 60LSUL |
| $\overline{CASEN}$ | Column address strobe enable output (active LOW) | |
| MA0 – MA8 | Address outputs | 60LSUL |

**NOTE:**
One 74LS Unit Load (LSUL) is defined as: 20$\mu$A in the HIGH state and 0.4mA in the LOW state.



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# 8X60
# FIFO RAM Controller (FRC)

***Product Specification***

**Products**

## FEATURES

- **12-Bit FIFO Address Generator**
- **Data Rate Exceeding 8MHz**
- **Asynchronous Read/Write Operations**
- **Three-State Address Outputs**
- **User-Defined Word Width**
- **Specifically Designed for Use with High-Speed Bipolar RAMs (Adaptable for Use with MOS RAMs)**
- **TTL Input and Output**
- **16mA Address-Drive Capability**

## USE AND APPLICATION

- **Interface Between Independently-Clocked Systems**
- **Buffer Memories for Disk and/or Tape**
- **Data Communication Concentrators**
- **CPU/Terminal Buffering**
- **DMA Applications**
- **CRT Terminals**

## PRODUCT DESCRIPTION

The Signetics 8 × 60 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed/high-capacity First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs — see **Applications** on the last page of this data sheet. The FRC can control up to 4096 words of buffer memory; intermediate buffer sizes can be selected — refer to the memory length table on the next page. Built-in arbitration logic handles read/write operations on a first-come/first-served basis.

As shown in Figure 1, the FRC consists of:

- A 12-Bit Write Address Generation Counter (Counter #1) and a 12-Bit Read Address Generation Counter (Counter #2).
- A 12-Bit Up/Down Status Counter (Counter #3).
- Twelve Three-State Address Drivers.
- Control Logic.

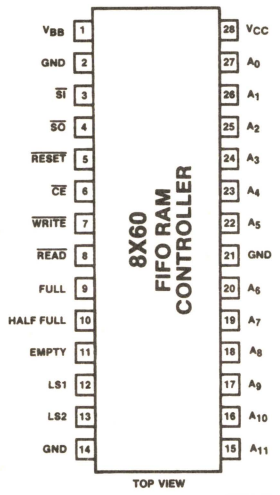
The two address counters, #1 and #2, respectively, are used to generate write and read addresses; the outputs of these counters are multiplexed to the three-state address drivers. Counter #3 generates **full, empty,** and **half full** status.

## FUNCTIONAL OPERATION

The FRC operates in either of two basic modes — **write** into the FIFO buffer memory or **read** from the FIFO buffer memory. These two operations are described in subsequent paragraphs and the complete sequence is summarized in Table 1. Typical Write/Read timing relationships, arbitration logic, and chip-enable control are shown in the Timing Diagrams.

## PIN CONFIGURATION

**N, F PACKAGE**




CD07430S

| PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|
| 1 | $V_{BB}$ | Supply voltage for internal circuits. |
| 2, 14, 21 | GND | Circuit ground. |
| 3 | $\overline{SI}$ | Shift-In request for write cycle; active-low input. |
| 4 | $\overline{SO}$ | Shift-Out request for read cycle; active-low input. |
| 5 | $\overline{RESET}$ | Active-low master reset input. |
| 6 | $\overline{CE}$ | Active-low chip enable input. |
| 7 | $\overline{WRITE}$ | Write cycle address valid; active-low output. |
| 8 | $\overline{READ}$ | Read cycle address valid; active-low output. |
| 9 | FULL | Memory full status output; also, override input capability. Active when **high.** |
| 10 | HALF FULL | Memory half-full status output; active-high. |
| 11 | EMPTY | Memory empty status output; also, override input capability. Active when **high.** |
| 12 | LS1 | Least significant bit (LSB) of the memory length select input. |
| 13 | LS2 | Most significant bit (MSB) of the memory length select input. |
| 15 – 20<br>22 – 27 | $A_{11} - A_0$ | Three-state address outputs: $A_0$ = LSB. |
| 28 | $V_{CC}$ | Supply voltage. |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGES $V_{CC}$ = 5V ± 10%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N8X60N |
| Hermetic CERDIP | N8X60F |

853-0298 81495



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# Signetics SMD Products

## Standard Products

Signetics Corporation, and it's parent N. V. Philips are the world leaders in SMD Technology. Philips developed both the SOT for Transistors in the 1960s, and the SO for ICs in the early 1970s. Signetics, through it's Philips connection, has offered SMD components longer than any other IC manufacturer in the US and has the most experience and broadest line of products and packages available. In addition to SMD IC's, Philips offers a broad line of other components in SMD format, including capacitors, resistors, transistors, and diodes. Philips offers an excellent line of automatic pick-and-place equipment. Through it's own assembly factories worldwide, Philips also has the broadest experience in SMD Manufacturing Technology. Signetics' and Philips' SMD leadership is a result of being able to help customers use this technology through a more thorough understanding of the relationships between devices, placement equipment, and manufacturing technology, as well as having the broadest range of SMD components, equipment, and services available in the world.

The purpose of this pocket guide is to provide users with details of the SMD IC packages offered through Signetics, including mechanical outlines, standardization, footprint information, and a complete list of available parts and their appropriate packages, as well as a tentative list of parts to be released in the near future.

Since the part list grows almost daily, this pocket guide is updated and published quarterly. DO NOT USE OUTDATED POCKET GUIDES. ASK YOUR LOCAL SALES OFFICE FOR A CURRENT ONE.

Further, if you need a component not listed in this guide, please CHECK WITH YOUR LOCAL SIGNETICS SALES REPRESENTATIVE.



**Table 1**

| No. of Pins | SO (0.150″ Wide) | SOL (0.300″ Wide) | PLCC |
|---|---|---|---|
| 8 | X | | |
| 14 | X | | |
| 16 | X | X | |
| 20 | | X | X |
| 24 | | X | |
| 28 | | X | X |
| 32 | | | X |
| 44 | | | X |
| 52 | | | X |
| 68 | | | X |
| 84 | | | X |


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# SMD Products

## SMD PACKAGES

Commercial SMD packages fall into two general categories: Small Outline (both the 0.150 inch wide SO and the 0.300 inch wide SOL) and the PLCC (Plastic Leaded Chip Carrier, also referred to as a PCC). Both of these packages use the same materials and assembly technology as used for the standard plastic DIL. Both have 0.050 inch lead spacing. The SO/SOL is dual-in-line with a Gull-Wing lead bend, while the PLCC is square or rectangular with a J-Bend lead bend. Both lead bends are designed for mounting directly to the surface of a printed circuit board. The SO/SOL packages are for the smaller pin count devices, i.e., those up to 28 pins, while the PLCC is for those parts with up to 84 pins. There is, however, some overlap due to the need to accomodate larger die in smaller pin counts (see Table 1).

## MILITARY PACKAGES

To support the implementation of defense and aerospace systems in surface mount technology Signetics Military Division offers products processed to MIL-M-38510, DESC selected item drawings, and MIL-STD-883 Revision C in the following packages:

Ceramic leadless chip carriers; triple laminated with metal lid and gold plated terminals in 20 to 68 leads.

Ceramic flat packages; frit glass sealed alumina CERPAC in 14 to 28 leads, and brazed leaded ceramic in 52 leads.

All military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

For more information on Signetics military SMD ICs please refer to the military products data manual or contact the Signetics Military Division, Sacramento, California, 916-924-6010.

## SEMICUSTOM

The full complement of SMD packaging including both SO's and PLCC's is available for designing with Signetics Semicustom products.

## STANDARDIZATION

All Signetics small outline packages (SO-8, SO-14, SO-16, SOL-16, SOL-20, SOL-24, SOL-28) meet the specifications detailed in the *JEDEC STANDARD* #MS-012AA-AC and #MS-013AA-AE. All Signetics PLCC packages (20, 28, 44, 52, 68, and 84 pins) meet the specifications covered in the *JEDEC Registered Outline* #MS-047AA-AH. The PLCC-32 meets the specifications covered in *JEDEC Registered Outline* #MO-052-AE.

## SPECIFICATIONS

Below are the specific dimensions of each of our packages.

Pinouts for devices in SO packages are the same as all standard DIPs except for a few linear devices identified with an asterisk(*). Pin configurations for each of the PLCC formats are indicated in the drawings below. **THESE ARE THE MOST CURRENT DRAWINGS. DISCARD PREVIOUS POCKET GUIDE.**

# SMD Products

## THERMAL CHARACTERISTICS

For complete thermal resistance data including both $\Theta_{JA}$ and $\Theta_{JC}$ of SO, SOL and PLCC packages see "SMD Thermal Considerations."

ASSUMPTIONS

- Junction temperature ($T_J$) is the temperature of a powered IC measured at the substrate diode. When the device is powered, the heat generated causes the $T_J$ to rise above the ambient temperature ($T_A$).
- Prior to 1985, SO packages were assembled with Alloy-42 leadframes. Currently, all SMD packages use Copper lead frames with the exception of the very low power devices (CMOS and High Speed CMOS) and the analog parts in SO-8. Although the power is low enough in these exceptions that $\Theta_{JA}$ is adequate with Alloy-42, they will gradually be shifted into copper leadframes.
- The ability of the package to conduct heat from the chip to the environment is expressed in terms of thermal resistance, normally called Theta JA ($\Theta_{JA}$). $\Theta_{JA}$is the total resistance from the junction to ambient and is often separated into two components: $\Theta_{JC}$ (junction to case) and $\Theta_{CA}$ (case to ambient) $\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$.
- $\Theta_{JA}$ values for SMD packages with copper leadframes are listed in Table #2. Test conditions for these values follow:
  Test Ambient — Still air
  Test Fixture — Glass epoxy test board
  Test Board Size
  — SO — 1.12″ × 0.75″ × 0.059″
  — SOL — 1.58″ × 0.75″ × 0.059″
  — PLCC — 2.24″ × 2.24″ × 0.062″
- Calculate power (P) by multiplying $V_{CC}$ nominal × $I_{CC}$ at $T_A$.
  $P = IE$
- Calculate rise in ($T_J$) by multiplying Power by $\Theta_{JA}$

$$\Delta T_J = (P \times \Theta_{JA})$$

Signetics

**Table 2 Typical $\Theta_{JA}$ Values for SMD Packages***

| No. of Pins | Die Size (sq mils) | Average $\Theta_{JA}$ (°C/W) | | |
|---|---|---|---|---|
| | | SO | SOL | PLCC |
| 8 | 3k | 159 | — | — |
| 14 | 5k | 118 | — | — |
| 16 | 5k | 110 | — | — |
| 16 | 12k | — | 97 | — |
| 20 | 12k | — | 87 | 73 |
| 24 | 12k | — | 75 | — |
| 28 | 12k | — | 71 | — |
| 32 | 30k | — | — | 60 |
| 44 | 30k | — | — | 47 |
| 52 | 50k | — | — | 42 |
| 68 | 50k | — | — | 44 |
| 84 | 50k | — | — | 34 |

*(Values express in °C/W)



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# SMD Products

## SHIPPING

SO/SOL and PLCC packages can be shipped in either Tubes or in Tape & Reel.

PLCC Tubes are 19.33″ long and the number of components/tube are listed below. The SO tubes are being modified to use an improved turn-lock end-stop developed by Philips and will be shortened from the present 20.12″ to 19.5″. Both the current and the new quantities are indicated in Table 3 below.

Signetics' Tape & Reel meets the requirements specified in proposed specification #EIA-481-A using 13 inch reels. Tape sizes and quantity/reel are indicated in Table 3. Note: As more customers move into high volume production, the quantities/reel will be increased to fill the reels. This will be in the second half of 1986 and exact quantities will be provided at that time.

**Table 3**

| Package Description | Tube Specification | Qty Per Tube | Tape Specification | Tape Size (mm) Width x Pitch | Qty Per Reel |
|---|---|---|---|---|---|
| SO-8, 0.15 Body | D570-0004 | 96 | EIA-481-A | 12 x 8 | 2500 |
| SO-14, 0.15 Body | D570-0004 | 55 | EIA-481-A | 16 x 8 | 2500 |
| SO-16, 0.15 Body | D570-0004 | 48 | EIA-481-A | 16 x 12 | 1000 |
| SO-16, 0.30 Body | D570-0002 | 46 | EIA-481-A | 24 x 12 | 1000 |
| SO-20, 0.30 Body | D570-0002 | 37 | EIA-481-A | 24 x 12 | 1000 |
| SO-24, 0.30 Body | D570-0002 | 31 | EIA-481-A | 24 x 12 | 1000 |
| SO-28, 0.30 Body | D570-0002 | 26 | EIA-481-A | 24 x 12 | 1000 |
| PLCC-20, Square | D570-0020 | 45 | EIA-481-A | 16 x 12 | 1000 |
| PLCC-28, Square | D570-0020 | 36 | EIA-481-A | 24 x 16 | 750 |
| PLCC-44, Square | D570-0020 | 26 | EIA-481-A | 32 x 24 | 500 |
| PLCC-52, Square | D570-0020 | 22 | EIA-481-A | 32 x 24 | 500 |
| PLCC-68, Square | D570-0020 | 18 | EIA-481-A | 44 x 32 | 250 |
| PLCC-84, Square | D570-0020 | 15 | EIA-481-A | 44 x 36 | 250 |
| PLCC-32, Rect | D570-0020 | 36 | EIA-481-A | 24 x 16 | 750 |

NOTES: EIA-481-A (taping of surface mount components for automatic placement) is the electronic industry standard.



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# SMD Products

## FOOTPRINTS

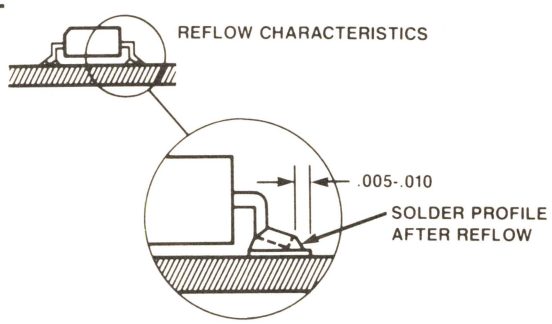
The suggested footprints should work in most manufacturing environments for Signetics and Philips packages (as well as other manufacturers' packages that meet the JEDEC standard).

These pad widths allow 0.008-inch traces between footprints while still keeping an 0.008-inch gap between trace and footprint.

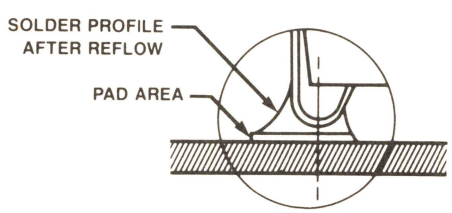
Experienced designers stress that pad length can be important for SO packages. They should be long enough to provide a solder fillet of 0.005- to 0.10-inch after reflow, but not long enough to allow the device to float off centerline during the reflow operation. For the PLCC, care must be taken not to run the footprint too far under the package, but rather, extend it out approximately 0.050-inch to the outside. This will help reduce solder bridges under the package where they cannot be seen during visual inspection.

## SOLDERING CRITERIA

### FOR SO/SOL




### FOR PLCC







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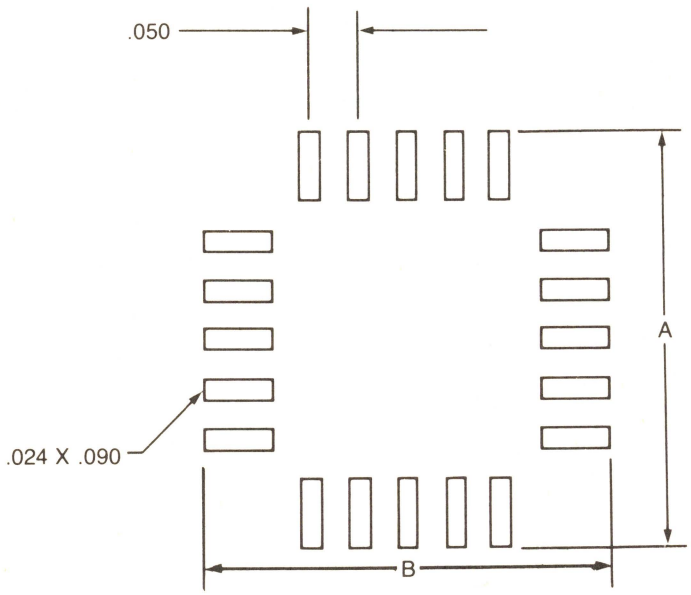
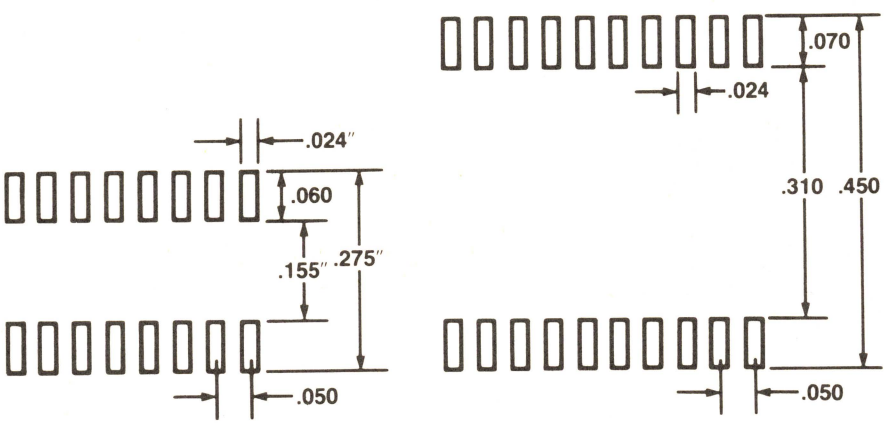
# SMD Products

## FOOTPRINTS FOR PLCC




| | A | B |
|---|---|---|
| 20 | .440 | .440 |
| 28 | .540 | .540 |
| 32 | .540 | .460 |
| 44 | .740 | .740 |
| 52 | .840 | .840 |
| 68 | 1.040 | 1.040 |
| 84 | 1.240 | 1.240 |

## FOOTPRINTS FOR SO/SOL




Dimensions in inches.

# SMD Products

## SMD LITERATURE

| | |
|---|---|
| SMD Pocket Guide | Published Quarterly |
| SMD Reliability Data | Available |
| SMD Thermal Considerations | Available |
| SMD Substrate Design Guidelines | Available |
| SMD Fluxing & Cleaning | Available |
| SMD Adhesive Application & Curing | Available |
| SMD Test and Repair | Available |
| SMD Soldering Techniques | Q4 '86 |
| SMD Solder Joint Criteria | Q4 '86 |
| SMD Component & Substrate Solderability | Q4 '86 |
| SMD Tape & Reel | 2H '86 |

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# Silicon Systems Microperipheral IC Selector Guide

| SSI Device Numbers | | Head Type | # of Channels | Max Input Noise nV/√Hz | Max Input Capacitance (pf) | Read Gain (typ) | Write Current Range (mA) | Power Supplies | Read/Write Data Port(s) |
|---|---|---|---|---|---|---|---|---|---|
| New | Old | | | | | | | | |
| **HDD READ/WRITE AMPLIFIERS** | | | | | | | | | |
| 32R104B | 104 | Ferrite | 4 | 2.4 | 23 | 35 | 15 to 45 | +6V,−4V | Differential, Bi-directional |
| 32R104BLN | 104L | Ferrite | 4 | 1.7 | 23 | 35 | 15 to 45 | +6V,−4V | Differential, Bi-directional |
| 32R114 | 114 | Thin Film | 4 | 1.1 | 65 | 123 | 55 to 110 | ±5V | Differential/Differential |
| 32R115 | 115 | Ferrite | 2, 4, 5 | 1.8 | 20 | 40 | 30 to 50 | ±5V | Differential, Bi-directional |
| 32R117 | 117 | Ferrite | 2, 4, 6 | 2.1 | 23 | 100 | 10 to 50 | +5V,+12V | Differential/TTL |
| 32R117A | 117A | Ferrite | 2, 4, 6 | 1.7 | 20 | 100 | 10 to 50 | +5V,+12V | Differential/TTL |
| 32R188 | 188 | Ferrite | 4 | 2.4 | 18 | 43 | 35 to 70 | +6V,−5V | Differential, Bi-directional |
| 32R501 | 501 | Ferrite | 4, 6, 8 | 1.5 | 23 | 100 | 10 to 50 | +5V,+12V | Differential/TTL |
| *32R510A | 510A | Ferrite | 2, 4, 6 | 1.5 | 20 | 100 | 10 to 40 | +5V,+12V | Differential/TTL |
| *32R511 | 511 | Ferrite | 4, 6, 8 | 1.5 | 20 | 100 | 10 to 40 | +5V,+12V | Differential/TTL |
| *32R512 | 512 | Thin Film | 8 | 0.9 | 32 | 150 | 10 to 40 | +5V,+12V | Differential/TTL |
| *32R514 | 514 | Ferrite | 2, 4, 6 | 1.5 | 20 | 150 | 10 to 40 | +5V,+12V | Differential/TTL |
| 32R520 | 520 | Thin Film | 4 | 0.9 | 65 | 123 | 30 to 75 | ±5V | Differential/Differential |
| 32R521 | 521 | Thin Film | 6 | 0.9 | 65 | 100 | 20 to 70 | +5V,+12V | Differential/TTL |
| *32R522 | 522 | Thin Film | 4, 6 | 1.0 | 32 | 100 | 6 to 35 | +5V,+12V | Differential/TTL |

| SSI Device Numbers | | Circuit Function | Features |
|---|---|---|---|
| New | Old | | |
| **HDD PULSE DETECTION** | | | |
| 32P540 | 540 | Read Data Processor | Time Domain Filter |
| 32P541 | 541 | Read Data Processor | AGC, Amplitude & Time Pulse Qualification, RLL Compatible |
| **HDD DATA RECOVERY** | | | |
| 32D531 | 531 | Data Synchronizer | Data Synchronizer/Write Precompensation |
| * 32D532 | 532 | Data Separator | Data Synchronizer/2, 7 RLL ENDEC |
| * 32D533 | 533 | Data Synchronizer | Data Synchronizer/Write Precompensation |
| * 32D534 | 534 | Data Separator | Data Synchronizer/MFM ENDEC/Write Precompensation |
| * 32D535 | 535 | Data Separator | Data Synchronizer/2, 7 RLL ENDEC/Write Precompensation |
| **HDD HEAD POSITIONING** | | | |
| 32H101A | 101A | Preamplifier-Ferrite Head | AV = 93, BW = 10MHz, $e_n$ = 7.0nV/√Hz |
| 32H116 | 116 | Preamplifier-Thin Film Head | AV = 250, BW = 20MHz, $e_n$ = .94nV/√Hz |
| * 32H567 | 567 | Servo Demodulator | Di-bit Quadrature Servo Pattern: PLL Synchronization |
| * 32H568 | 568 | Servo Controller | Track & Seek Mode Operation; Microprocessor Interface |
| * 32H569 | 569 | Servo Motor Driver | Head Parking, Spindle Motor Braking |
| **HDD SPINDLE MOTOR CONTROL** | | | |
| 32M590 | 590 | 2-Phase Motor Speed Control | ±0.035% Speed Accuracy; Unipolar Operation |
| 32M591 | 591 | 3-Phase Motor Speed Control | ±0.05% Speed Accuracy; Unipolar Operation |
| *32M593 | 593 | 3-Phase Motor Speed Control | ±0.037% Speed Accuracy; Bipolar Operation |
| **HDD CONTROLLER/INTERFACE** | | | |
| * 32B450A | 450A | SCSI Controller | Async transfer to 2MBPS; Initiate/Target Modes; Internal Drivers; CMOS |
| * 32C452 | 452 | Storage Controller | 20Mbits/sec; CMOS; Programmable; AIC-010 Compatible |
| * 32C453 | 453 | Buffer Controller | Non-mux addressing to 16K; CMOS; AIC-300 Compatible |
| 32B545 | 545 | Support Logic | Includes ST506 Bus Drivers/Receivers |
| **FLOPPY DISK DRIVE CIRCUITS** | | | |
| * 34D441 | 441 | Data Separator | High Performance Analog Data Separator, NEC 765 Compatible |
| 34P570 | 570 | Read Data Path | 2 Channel Read/Write With Read Data Path |
| 34R575 | 575 | Read/Write | 2, 4 Channel Read/Write Circuit |
| 34B580 | 580 | Support Logic | Port Expander, Includes SA400 Interface Drivers/Receivers |
| **TAPE DRIVER CIRCUITS** | | | |
| 35P550 | 550 | Read Data Path | 4 Channel Read/Write With Read Data Path |

* New Note: New numbering system effective 10/1/87.


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| SSI Device Numbers | | Operating Modes | | | Features | Power Supplies | Available Packages |
|---|---|---|---|---|---|---|---|
| New | Old | 212A | V.22,V.21 | V.22 BIS | | | |
| **K-SERIES SINGLE CHIP MODEM FAMILY** | | | | | | | |
| 73K212 | K212 | x | | | 1200/300 BPS, Bell 212A/103 compatible | 12V | 28, 22 DIP, 28 PLCC |
| 73K212L | K212L | x | | | Low power K212, 40mW, +5V single supply | 5V | 28, 22 DIP, 28 PLCC |
| 73K221 | K221 | | x | | 1200/600 BPS, CCITT V.22/V.21 compatible | 12V | 28, 22 DIP, 28 PLCC |
| 73K221L | K221L | | x | | Low power K221, 40 mW, +5V single supply | 5V | 28, 22 DIP, 28 PLCC |
| 73K222 | K222 | x | x | | 1200/600/300 BPS Bell 212/103, CCITT V.22/V.21 | 12V | 28, 22 DIP, 28 PLCC |
| 73K222L | K222L | x | x | | Low power K222, 40mW, +5V single supply | 5V | 28, 22 DIP, 28 PLCC |
| 73K222U | K222U | x | x | | K222 with integral 16C450 UART | 5V | 40 DIP, 44 PLCC |
| 73K322 | | | x | | K221 with V.23 mode for European applications | 12V | 28, 22 DIP, 28 PLCC |
| 73K322L | | | x | | Low power K223, 40mW, +5V single supply | 5V | 28, 22 DIP, 28 PLCC |
| 73K224 | K224 | x | x | x | 2400/1200/300 BPS, V.22 bis, V.22/V.21, Bell 212/103 | 12V | 28, 22 DIP, 28 PLCC |
| 73K224L | K224L | x | x | x | Low power K224, 75mW, +5V single supply | 5V | 28, 22 DIP, 28 PLCC |
| 73K324 | – | | x | x | K224 with V.23 mode for European applications | 12V | 28, 22 DIP, 28 PLCC |
| 73K324L | – | | x | x | Low power K224, 100mW, +5V single supply | 5V | 28, 22 DIP, 28 PLCC |
| **MODEM/MODEM SUPPORT** | | | | | | | |
| 73M214 | 214 | x | x | x | 2400 BPS modem analog processor | ±5V | 28 DIP |
| 73M223 | 223 | | | | 1200 BPS half-duplex V.23 FSK modem | 5V | 16 DIP |
| 73M3522 | 3522 | x | x | | Hi-performance filter for 1200 BPS modems | ±5V | 16 DIP |

| SSI Device Numbers | | Circuit Function | Features | Power Supplies | Packages |
|---|---|---|---|---|---|
| New | Old | | | | |
| **TONE SIGNALING PRODUCTS** | | | | | |
| 75T201 | 201 | Integrated DTMF Receiver | Binary of 2-of-8 output | 12V | 22 DIP |
| 75T202 | 202 | Integrated DTMF Receiver | Low-power, binary output | 5V | 18 DIP |
| 75T203 | 203 | Integrated DTMF Receiver | Binary output, early detect | 5V | 18 DIP |
| 75T204 | 204 | Integrated DTMF Receiver | Low-power, binary output | 5V | 14 DIP, 16 SO |
| 75T2089 | 20C89 | Integrated DTMF Transceiver | Generator and Receiver, µP interface | 5V | 22 DIP |
| 75T2090 | 20C90 | Integrated DTMF Transceiver | Generator and Receiver, µP interface, Call Progress | 5V | 22 DIP |
| 75T957 | 957 | Integrated DTMF Receiver | Early Detect, Dial Tone reject | 5V | 22 DIP, 24 SO |
| 75T980 | 980 | Imprecise Call Progress Detector | Energy detect in 305-640 Hz band, Teltone | 5V | 8 DIP |
| 75T981 | 981 | Precise Call Progress Detector | Detects 350, 400, 440, 480 Hz, Teltone second-source | 5V | 22 DIP |
| 75T982 | 982 | Precise Call Progress Detector | Detects 350, 440, 480, 620 Hz, Teltone second-source | 5V | 22 DIP |
| **TELEPHONY/DIGITAL TELECOM** | | | | | |
| 78P233 | 233 | DS-1 Line Interface | T1 Clock Recovery and Data Extraction | 5V | 24 DIP |
| 78P8050 | 80C50 | T1 Transmitter | Bell D2, D3, D4, serial format and mux low power | 5V | 28 DIP, PLCC |
| 78P8060 | 80C60 | T1 Receiver | Bell D2, D3, serial synch and demux, low power | 5V | 28 DIP, PLCC |
| 78P243 | – | 2048 Kbps PCM Interface | Clock and data recovery of HDB3–encoded signals | 5V | 20, 24 DIP |
| 78A093 | 78093 | 12x8x1 Crosspoint Switch | Low ON resistance, two versions | 5-12V | 40 DIP |
| 78A207 | 207 | Integrated MF Receiver | Detects central office tone signals | 5V | 20 DIP |
| 78A217F/B | – | MFRZ Forward & Backward Receivers | Separate foward and backward receivers; compatible with SSI 75M207 | 5V | 20 DIP |
| 78A400 | – | 4-Wire Loopback | 2713 Hz detector, failsafe timeouts | ±5V | 16 DIP, 18 SO |
| 78A420 | – | 4-Wire Loopback with Gain | 78M400 with gain block | ±5V | 22 DIP |

Note: New numbering system effective 10/1/87.



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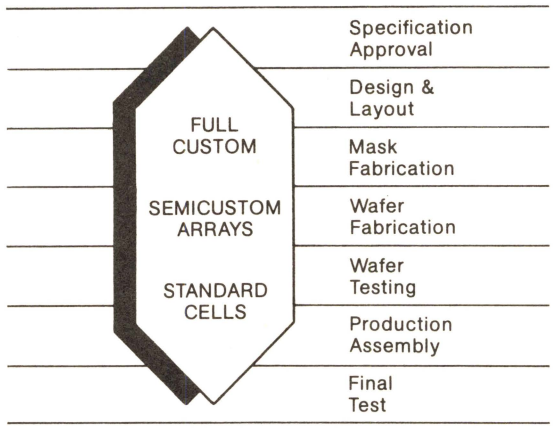
In both engineering and technology, we offer versatility: with design capabilities for digital, analog, and combined digital/analog IC's along with a wafer fabrication capability that includes both Bipolar and CMOS technologies.




# Quality Assurance

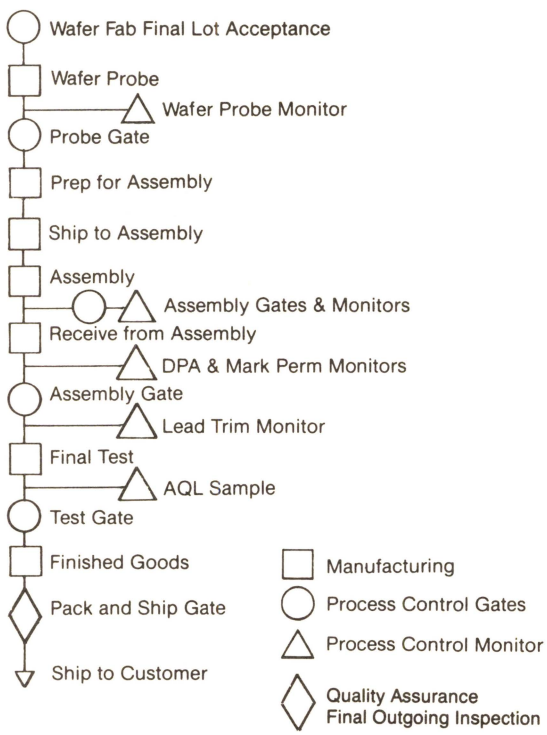
### A MESSAGE FROM SILICON SYSTEMS' PRESIDENT AND CEO

Quality is the secret to long term success. It literally overshadows the short term emphasis on price, delivery, or any other measure of performance.
At Silicon Systems, we have based our quality philosophy on the development of a "state of mind" in each employee, related to job performance and to its reflection in the overall level of quality and reliability of our product.
We have programs that are dedicated to process control, overall product reliability and outstanding outgoing quality. Rapid analysis of failures and returns, proving responsive service to our customers, also generates quick solutions to our own problems. We believe that the high levels which we achieve in quality, reliability and service are directly attributable to belief in the basic tenets of quality within our corporate culture.

### Q.A. CAPABILITIES—In-Process Inspections

Every major manufacturing step is followed by an appropriate in-process quality control inspection gate. Silicon Systems has established inspection gates in areas such as Wafer Fabrication, Wafer Probe, Assembly, and Final Test areas.
In addition to these established gates, Silicon Systems also has established monitors during various stages in the manufacturing process. It is this built-in quality that ensures failure-free shipment of Silicon Systems' products.
Quality control monitors have been placed throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediate manufacturing steps. This data is used to determine quality trends or long term changes in the quality of specific operations. A general description of the product flow and QC inspection points are shown.

### PROCESS CONTROL GATES AND MONITORS




Silicon Systems

For more information, contact **Silicon Systems**

silicon systems™

14351 Myford Road, Tustin, California 92680 (714) 731-7110, TWX 910-595-2809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# S-MOS SYSTEMS, INC.
# MEMORY PRODUCTS

## Static RAMs

Our static RAMs are fabricated using advanced CMOS technology. In addition to our advanced 32K x 8, S-MOS also offers 1K x 4, 2K x 8 and 8K x 8 static RAMs with industry standard pinouts. In addition to standard dual in-line types, our 2K x 8, 8K x 8 and 32K x 8 SRAMs are available in space-saving small outline packages. Selected versions are also offered in industrial temperature range.

## Static RAMs

| Organization | Part Number | Access Time (ns Max.) | Average Operating Current (mA Typ.) | Standby Supply Current (μA Typ.) | Package |
|---|---|---|---|---|---|
| 1024 x 4 | SRM 6514 | 250/3000 | 6/0.03 (max.) | 40/3 (max.) | 18[1] |
| 1024 x 4 | SRM 2114 | 250 | 14 | 0.1 | 18[1] |
| 2048 x 8 | SRM 2016 | 100/120 | 30/25 | 1 | 24[1,2,4] |
| 2048 x 8 | SRM 2017 | 100/120 | 30/25 | 1 | 24[1,2,4] |
| 2048 x 8 | SRM 2018 | 100/120 | 30/25 | 1 | 24[1,2,4] |
| 16,384 x 1 | SRM 2367 | 35/45 | 40 | 20 | 20[1] |
| 4096 x 4 | SRM 2268 | 45/55/70 | 40 | 20 | 20[1] |
| 8192 x 8 | SRM 2064* | 150 | 3 | 2 | 28[1,2] |
| 8192 x 8 | SRM 2264 | 90/100/120 | 50/50/45 | 2 | 28[1,2] |
| 32,768 x 8 | SRM 20256* | 100/120 | 40 | 2 | 28[1,2,5] |
| 65,556 x 4 | SRM 20258 | 45/55 | TBD | TBD | 24[1,3] |

(1) Plastic DIP (2) Small Outline (3) Ceramic DIP (4) 300 mil Skinny DIP (5) Shrink DIP

*Industrial temperature range available (−45°C to +85°C)

## Mask ROMs

S-MOS offers a wide variety of CMOS masked ROMs from 64K to 1Mbit. Prototype turnaround is typically accomplished in 7–8 weeks. The code should be included in EPROMs, accompanied by a truth table, and the S-MOS ROM confirmation sheet.

| | Organization | Part Number | Access Time (ns Max.) | Average Operating Current (mA Typ.) | Standby Supply Current (μA Typ.) | Package |
|---|---|---|---|---|---|---|
| MASK ROMS | 8192 x 8 | SMM 2364 | 450 | 15/12 | 0.1 | C, 24 |
| | 8192 x 8 | SMM 2365 | 350/450 | 15/12 | 0.1 | C, 28 |
| | 16,384 x 8 | SMM 6313 | 250 | 16 | 0.1 | C, 28 |
| | 32,768 x 8 | SMM 2325 | 450/850 | 4/3 | 0.1 | C, 28 |
| | 32,768 x 8 | SMM 2326 | 450/850 | 4/3 | 0.1 | C, 28 |
| | 32,768 x 8 | SMM 6325 | 250 | 16 | 0.1 | C, 28 |
| | 32,768 x 8 | SMM 6326 | 250 | 16 | 0.1 | C, 28 |
| | 131,072 x 8 | SMM 4310 | 100 | 30 | 0.1 | C, 28 |



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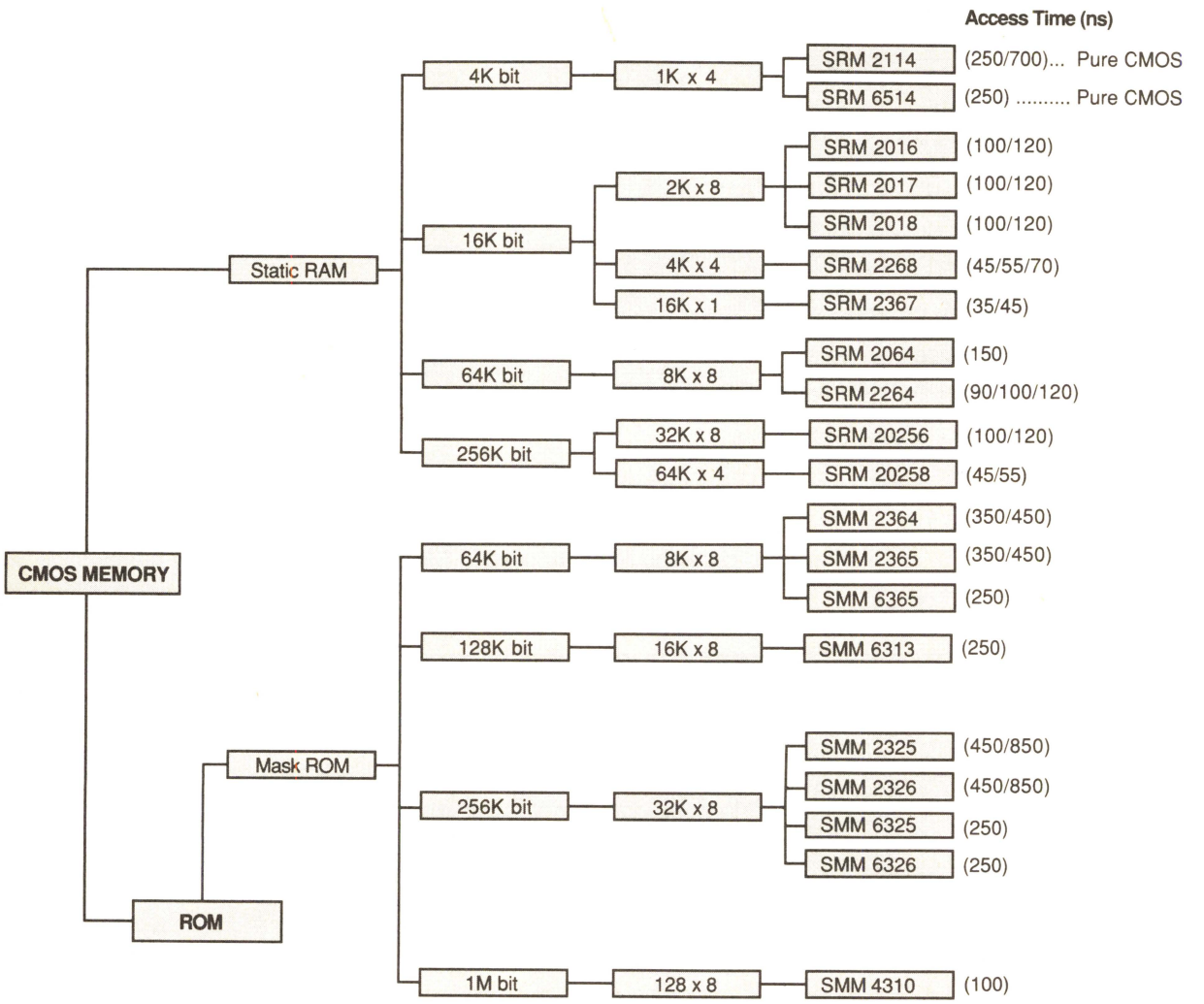
# S-MOS SYSTEMS, INC.
# MEMORY PRODUCTS

## Memory Products

S-MOS is a leader in CMOS design and manufacturing of memory products. Over the past three years we have moved quickly to expand our product offerings to OEMs. Our affiliate, Seiko Epson, has a world-class automated 6″, 1.2μm fabrication line. Our state-of-the-art SRM 20256, 32K x 8 SRAM is one of the many new products presently being produced on the six-inch fab line. We also offer mask ROMs in a variety of speeds and package types.

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# SPRAGUE PERIPHERAL POWER & DISPLAY DRIVERS

in order of (1) output current, (2) output voltage, and (3) number of drivers

| OUTPUTS* | | | FEATURES | | | | | PART NUMBER | HERM. AVAIL. | SMD AVAIL. |
|---|---|---|---|---|---|---|---|---|---|---|
| mA | V | # | SERIAL INPUT | LATCHED DRIVERS | DIODE CLAMP | SAT. OUT. | INTERNAL PROTECT. | | | |
| **SINK DRIVERS** | | | | | | | | | | |
| 10 | 20 | 8 | — | ✓ | ✓ | ✓ | — | UCN5881EP | — | ✓ |
| **100** | **30** | **32** | ✓ | ✓ | — | — | — | **UCN5833A** | — | ✓ |
| | **40** | **8** | ✓ | ✓ | — | ✓ | — | **UDN2595A†** | — | ✓ |
| | **40** | **32** | ✓ | ✓ | — | ✓ | — | **UCN5832A** | — | ✓ |
| | **225** | **32** | ✓ | — | **TFEL DISPLAY ROW DRIVER** | | | **UCN5851/52A** | ✓ | ✓ |
| 200 | 200 | 8 | — | — | — | — | — | UDN6540B | — | — |
| **250** | **70** | **4** | — | — | ✓ | ✓ | — | **SERIES UHP400†** | ✓ | — |
| | **150** | **7** | — | — | ✓ | — | — | **SERIES ULN7000A** | — | — |
| 300 | 50 | 8 | — | — | ✓ | ✓ | — | UDN2596/98A | — | — |
| | 80 | 2 | — | — | — | ✓ | — | SERIES UDN3610M | ✓ | — |
| | 80 | 2 | — | — | ✓ | ✓ | — | SERIES UDN5710M | ✓ | — |
| | 80 | 4 | — | — | ✓ | ✓ | — | SERIES UDN5700A | ✓ | ✓ |
| **350** | **50** | **4** | — | ✓ | ✓ | — | — | **UCN5800A** | ✓ | ✓ |
| | **50** | **7** | — | — | ✓ | — | — | **SERIES ULN2000A** | ✓ | ✓ |
| | **50** | **8** | — | — | ✓ | — | — | **SERIES ULN2800A** | ✓ | ✓ |
| | **50** | **8** | — | ✓ | ✓ | — | — | **UCN5801A** | ✓ | ✓ |
| | **60** | **16** | **4 TO 16-LINE LATCHED DECODE/DRIVER** | | | | | **UCN5816A** | ✓ | ✓ |
| | **95** | **7** | — | — | ✓ | — | — | **SERIES ULN2020A** | ✓ | ✓ |
| | **95** | **8** | — | — | ✓ | — | — | **SERIES ULN2820A** | ✓ | ✓ |
| | **100** | **8** | ✓ | — | ✓ | — | — | **SERIES UCN5820A** | ✓ | ✓ |
| | **100** | **8** | ✓ | ✓ | ✓ | — | — | **SERIES UCN5840A** | ✓ | ✓ |
| | **150** | **4** | — | ✓ | ✓ | — | — | **UCN5900A** | ✓ | ✓ |
| | **150** | **8** | — | ✓ | ✓ | — | — | **UCN5901A** | ✓ | ✓ |
| 500 | 50 | 7 | — | — | ✓ | — | — | SERIES ULN2010A | ✓ | — |
| | 50 | 8 | — | — | ✓ | — | — | SERIES ULN2810A | ✓ | — |
| **600** | **70** | **2** | — | — | ✓ | ✓ | — | **SERIES UDN5740/50M** | — | — |
| 700 | 60 | 4 | — | — | ✓ | ✓ | ✓ | UDN2543B | — | — |
| **750** | **50** | **8** | — | — | ✓ | ✓ | — | **UDN2597/99A** | — | — |
| 1000 | 70 | 2 | — | — | ✓ | ✓ | — | UDN5725M | — | ✓ |
| **1250** | **20** | **4** | **STEPPER MOTOR TRANSLATOR/DRIVER** | | | | | **UCN4204B** | — | — |
| | **50** | **4** | **STEPPER MOTOR TRANSLATOR/DRIVER** | | | | | **UCN5804B** | — | — |
| | **60** | **4** | — | — | ✓ | ✓ | — | **UDN2540B** | — | — |
| | **80** | **4** | — | ✓ | ✓ | — | — | **UCN5813/14B†** | — | — |
| 1500 | 80 | 2 | — | — | ✓ | — | — | ULN2061/62M | — | ✓ |
| | 80 | 4 | — | — | ✓ | — | — | SERIES ULN2064/65B | ✓ | ✓ |
| **1750** | **80** | **4** | ✓ | ✓ | ✓ | — | ✓ | **UCN5825/26B** | — | — |
| 2000 | 80 | 4 | — | — | ✓ | — | ✓ | UDN2545B | — | — |
| **3000** | **90** | **4** | — | — | ✓ | — | — | **UDN7078W** | — | — |
| 4000 | 50 | 3 | — | — | ✓ | — | ✓ | UDN2938W/39B | — | — |
| | 80 | 4 | — | — | ✓ | — | — | UDN2878/79W | — | — |
| **SOURCE DRIVERS** | | | | | | | | | | |
| **−10** | **20** | **16** | — | ✓ | ✓ | ✓ | — | **UCN5882EP** | — | ✓ |
| −25 | 80 | 8 | — | ✓ | — | — | — | UCN5815A† | ✓ | ✓ |
| | 80 | 10 | ✓ | ✓ | — | — | — | UCN5810AF† | ✓ | ✓ |
| | 80 | 12 | ✓ | ✓ | — | — | — | UCN5811A† | — | — |
| | 80 | 20 | ✓ | ✓ | — | — | — | UCN5812AF† | ✓ | ✓ |
| | 80 | 32 | ✓ | ✓ | — | — | — | UCN5818AF† | ✓ | ✓ |
| | 115 | 6 | — | — | — | — | — | UDN6116A† | — | — |
| | 115 | 8 | — | — | — | — | — | UDN6118/28A† | — | ✓ |
| | 200 | 8 | — | — | — | — | — | UDN6510/14A | — | — |
| **−120** | **±25** | **8** | — | — | ✓ | ✓ | — | **UDN2585A** | — | ✓ |
| | **30** | **8** | — | — | ✓ | ✓ | — | **UDN2985/86A** | — | ✓ |
| | **50** | **8** | ✓ | ✓ | ✓ | ✓ | — | **UCN5895A** | — | ✓ |
| −350 | 35 | 8 | — | — | ✓ | — | ✓ | UDN2987A | — | — |
| | −80 | 8 | — | — | ✓ | — | — | UDN2580/88A† | ✓ | ✓ |
| | 80 | 8 | — | — | ✓ | — | — | UDN2981-84A | ✓ | ✓ |
| | 80 | 8 | ✓ | ✓ | ✓ | — | — | UCN5890/91A | — | — |
| **−1500** | **35** | **4** | — | — | ✓ | ✓ | — | **UDN2941B** | — | — |
| −4000 | 60 | 4 | — | — | ✓ | — | — | UDN2944W | — | — |
| **−6000** | **60** | **4** | — | — | ✓ | — | — | **UDN2948W** | — | — |
| **SOURCE/SINK DRIVERS** | | | | | | | | | | |
| ±15 | 100 | 32 | ✓ | AC PLASMA DISPLAY DRIVERS | | | | UCN5857-60A | ✓ | ✓ |
| **±20** | **80** | **32** | ✓ | **TFEL DISPLAY COLUMN DRIVER** | | | | **UCN5853/54A†** | — | ✓ |
| ±40 | 150 | 10 | ✓ | ✓ | — | — | — | UCN5910A | ✓ | — |
| **±500** | **40** | **2** | **FULL-BRIDGE** | ✓ | — | — | | **UDN2993B** | — | ✓ |
| ±800 | 30 | 3 | HALF-BRIDGE | ✓ | ✓ | — | | UDN2933/34B | ✓ | ✓ |
| **±1000** | **26** | **1** | **HALF-BRIDGE** | ✓ | ✓ | ✓ | | **UDN2943Z** | — | — |
| | **34** | **1** | **POWER OP AMP** | ✓ | — | — | | **ULN3751B/Z†** | — | — |
| | **40** | **2** | **POWER OP AMP** | ✓ | — | — | | **ULN3755B/W** | — | — |
| | **45** | **4** | **STEPPER MOTOR TRANSLATOR/DRIVER** | | | | | **UCN5871B** | — | ✓ |
| ±2000 | 15 | 3 | HALF-BRIDGE | ✓ | ✓ | ✓ | | UDN2931B/W | — | — |
| | 30 | 1 | HALF-BRIDGE | ✓ | — | — | | UDN2935/50Z | — | — |
| | 50 | 1 | PWM FULL-BRIDGE | ✓ | — | ✓ | | UDN2953B/54W | — | — |
| | 50 | 2 | FULL-BRIDGE | ✓ | — | ✓ | | UDN2998W | — | — |
| | 50 | 3 | 3-PHASE BRUSHLESS CONTROL/DRIVER | | | ✓ | | UDN2936/37W | — | — |
| **±3000** | **45** | **2** | **PWM CONTROL** | ✓ | — | ✓ | | **UDN2962B/W** | — | — |
| ±4000 | 50 | 2 | PWM CONTROL | ✓ | — | ✓ | | UDN2965W-2 | — | — |
| **±8000** | **50** | **1** | **HALF-BRIDGE** | ✓ | — | ✓ | | **UDN2951Z/55W** | — | — |

*Current is maximum tested condition, voltage is absolute maximum rating.
†Output ratings shown are for selected units (suffix −1).

***For application engineering assistance, write or call Semiconductor Group, Sprague Electric Company, 115 Northeast Cutoff, Box 2036, Worcester, MA 01613. Tel. 800-247-2077 (In Mass. 800-247-2076).***

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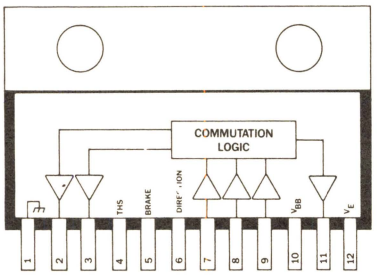
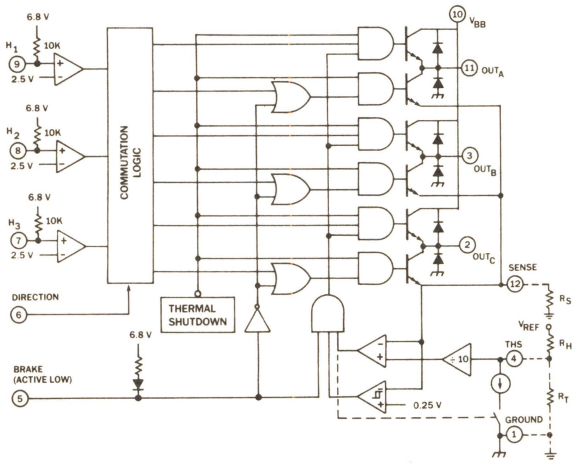
# SMART POWER ICs

## For Motor Driver Applications

### UDN2936W 3-Phase Brushless DC Motor Controller/Driver

*Features:* ±3 A peak output current
50 V sustaining
Internal commutation logic
Internal clamp diodes
Internal PWM control
Internal thermal shutdown

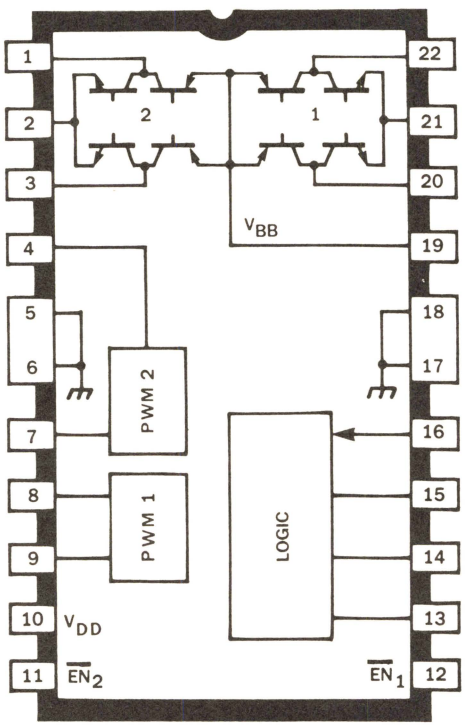



The UDN2936W combines low-level amplification, commutation logic, and power drivers to control and drive 3-phase brushless dc motors to ±2 A and 50 V. Current control is performed with an external sense resistor and pulse-width modulating the source drivers. Internal protection circuitry prevents crossover current when braking or changing direction.

### UCN5871B BiMOS II Stepper-Motor Translator/Driver

*Features:* To ±1 A per phase
45 V sustaining
Wave drive, two-phase, & half-step
Internal PWM Current Control
Internal clamp diodes
Power-ON reset
Internal thermal shutdown




The UCN5871B provides complete control and drive for a two-phase bipolar stepper-motor with continuous output current ratings to ±1 A per phase (1.5 A startup) and will sustain 45 V. The low-power CMOS logic section provides the sequencing logic, direction and output enable control, and the power-ON reset function. Three stepper-motor drive formats are externally selectable. Internal PWM current is user-controllable.

SMART POWER integrated circuits from Sprague Electric combine low-power CMOS, $I^2L$, or bipolar logic with bipolar or DMOS power drivers. Many devices are specifically intended for driving various types of motors (and other inductive loads) with ratings to ±8 A or 90 V (sustaining) and include current sensing, thermal shutdown, and PWM current control. All motor drivers from Sprague Electric Co. include internal high-current clamp diodes.

**For complete technical information, write Sprague Electric Company, P.O. Box 9102, Mansfield, MA 02048. For the name of your nearest Sprague Semiconductor Distributor, call Sprague Electric Company, Distribution Division at 617/339-3701.**

**For application engineering assistance, write or call Semiconductor Group, Sprague Electric Company, 115 Northeast Cutoff, Box 2036, Worcester, MA 01613. Tel. 800/247-2077 (In Mass., 800/247-2076).**

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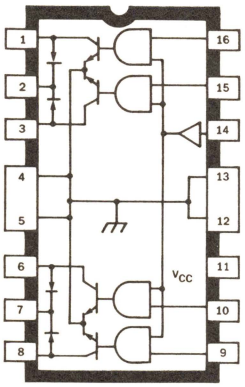
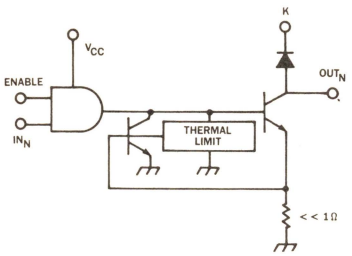
# POWER INTERFACE ICs

## UDN2543B Quad Nand-Gate Power Driver for Incandescent or Inductive Loads

***Features:*** **To 1 A and 60 V per output**
**Over-current limited**
**Internal clamp diodes**
**Individual thermal limiting**

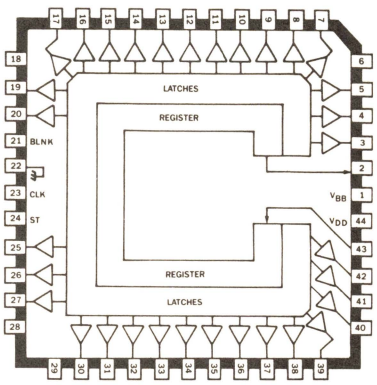


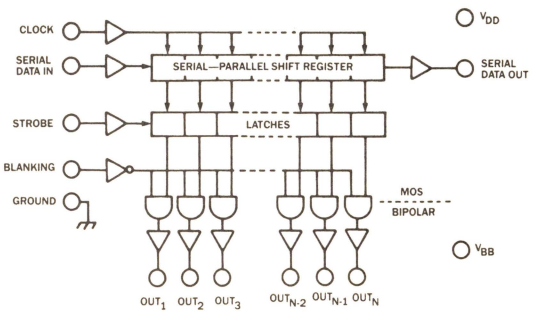




The UDN2543B is a 4-channel driver for use with incandescent lamps, relays, motors, or solenoids, Each channel is independently current and temperature limited to protect the load and driver against turn-on/ in-rush current, a stalled motor or shorted filament. Internal high-current clamp diodes and a 35 V sustaining rating provide protection against inductive load transients. In the OFF state, the outputs will withstand up to 60 V.

## BiMOS II High-Speed Serial-Input Latched Drivers with Active DMOS Pulldowns

***Features:*** **10-Bit UCN5810AF/LWF (DIP/SOIC)**
**12-Bit UCN5811A (DIP)**
**20-Bit UCN5812AF/EPF (DIP/PLCC)**
**32-Bit UCN5818AF/EPF (DIP/PLCC)**
**−25 mA/80 V source outputs**
**15 mA active DMOS pulldowns**




"Smart power" BiMOS II drivers combine low-power, high-speed CMOS logic and control circuitry with bipolar power drivers for load ratings from 25 mA (64 channels) to 2 A (4 channels) or 150 V, or DMOS drivers for operation to 225 V. Typical applications include VF, TFEL, or LED displays; thermal, ink-jet, or impact print heads; stepper motors, and reed relays. Drivers intended for use with inductive loads include internal clamp diodes. Active DMOS pulldowns provide high-speed turn-off and reduced power requirements in display applications.

Sprague power interface ICs provide economical monolithic solutions to interfacing between low-power logic levels and peripheral power loads to 225 V or ±8 A. Many devices include internal clamp diodes for use with inductive loads such as motors, relays, or solenoids; internal logic for serial-to-parallel conversion, decoders, latches, input or output enabling, and commutation or stepping logic for motors; and protection features such as thermal shutdown and current sensing/limiting.

**For completed technical information, write Sprague Electric Company, P.O. Box 9102 Mansfield, MA 02040. For the name of your nearest Sprague Semiconductor Distributor, call Sprague Electric Company, Distribution Division at 617/338-3701.**

**For application engineering assistance, write or call Semiconductor Group, Sprague Electric Company, 115 Northeast Cutoff, Box 2036, Worcester, MA 01613. Tel. 800/247-2077 (In Mass., 800/247-2076).**

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# STANFORD TELECOMMUNICATIONS, INC.

## CUSTOM PRODUCTS FOR COMMUNICATIONS

| | | | |
|---|---|---|---|
| **STEL-1023** | C/A CODER | **STEL-2012** | CONVOLUTIONAL ENCODER |
| **ST-1172A** | CMOS NCO | **STEL-2015/6/7** | VITERBI DECODERS |
| **STEL-2172** | ECL NCO | **STI-5268** | ENCODER / VITERBI DECODER |
| **STEL-9172** | NCO EVALUATION BOARD | **STEL-2110** | BIT SYNCHRONIZER/DEMODULATOR |
| **STEL-9272** | VHF FREQUENCY SYNTHESIZER | **STEL-2210** | PHASE ESTIMATOR |
| **STI-2003** | COMPLEX MAC | **STEL-9268** | SERIAL VITERBI DECODER |
| **STI-2010** | VITERBI DECODER | **STEL-68020** | MULTIBUS SBC |

## BURST VITERBI DECODERS STEL-2015/6/7

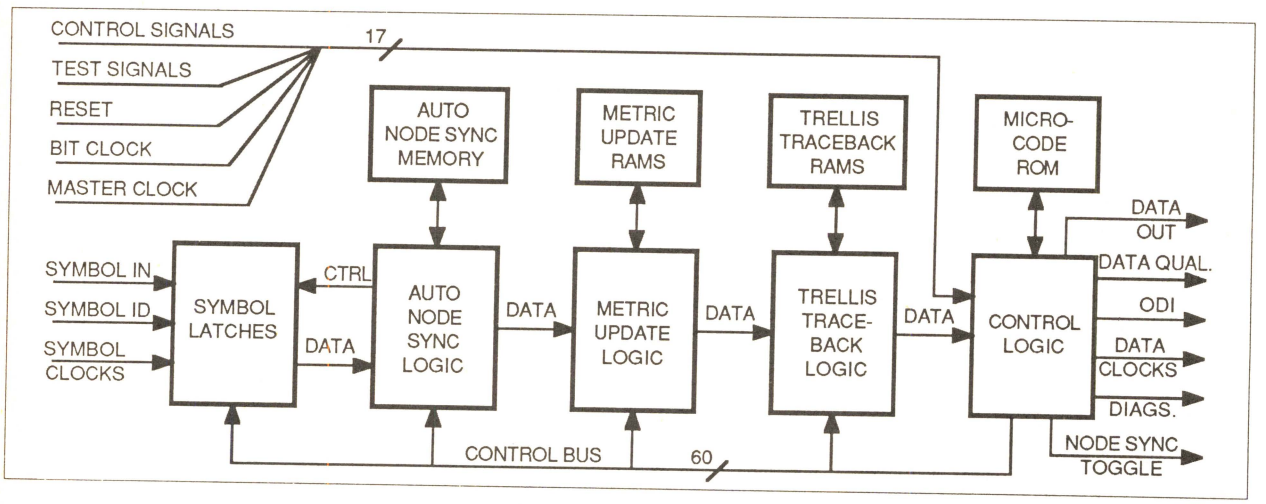
Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. FEC techniques can reduce the required transmission power at the expense of the bandwidth required. This is an invaluable factor in satellite communication systems where transmitter power is severely limited. The STEL-2015/6/7 are designed to allow these features to be applied in burst carrier (TDMA) systems since they incorporate special start and end of burst circuitry to perform internal node sync and to correctly decode the data at the end of the burst in such systems. The STEL-2017 is a constraint length 7 decoder which operates at data rates up to 1024 Kbits per second. The STEL-2016 and STEL-2015 are similar devices designed to operate with constraint lengths of 6 and 5, respectively. The STEL-2016 operates at data rates of up to 2048 Kbps and the STEL-2015 operates at up to 4096 Kbps. These higher rates are possible with the lower constraint lengths because of the reduced amount of processing required. These devices will be available early in 1988.

### FEATURES (STEL-2017)

- **UP TO 1024K BITS/SEC DATA RATE**
- **CONSTRAINT LENGTH SEVEN**
- **RATES 1/3, AND 1/2 IN DIRECT MODE**
- **RATES 2/3, 3/4, 4/5, 5/6, 6/7, AND 7/8 IN PUNCTURED MODE**
- **FIVE BIT SOFT DECISION INPUT IN SIGN + MAGNITUDE FORMAT**
- **CODING GAIN OF 5.3 dB (@ BER OF $10^{-5}$), RATE 1/2 (K=7)**
- **CODING GAIN OF 6.1 dB (@ BER OF $10^{-5}$), RATE 1/3 (K=7)**
- **INTERNAL OR EXTERNAL NODE SYNC CAPABILITY**
- **ALL MEMORY INCLUDED ON CHIP**
- **EIGHT SELECTABLE SETS OF POLYNOMIALS**
- **LOW POWER CONSUMPTION**

**The STEL2015/6/7 are packaged in a 48-pin DIP, and are available in both ceramic and plastic.**

### BLOCK DIAGRAM




*STANFORD TELECOMMUNICATIONS, INC. 2421 Mission College Blvd. Santa Clara, CA 95054*

Stanford Telecommunications Inc.



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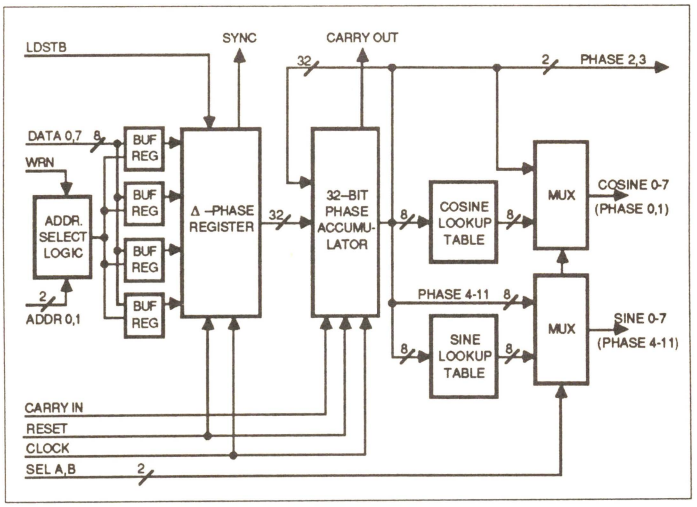
# 25 MHz CMOS 32-BIT RESOLUTION NUMERICALLY CONTROLLED OSCILLATOR ST-1172A

The ST-1172A has a wide range of applications in digital communication and signal processing systems. The NCO provides a simple solution to many common signal processing problems and makes possible new digital signal processing techniques which were previously impractical.

## BLOCK DIAGRAM




## FEATURES

- **32-BIT FREQUENCY RESOLUTION**
- **25 MHz CLOCK FREQUENCY**
- **8-BIT SINE AND COSINE OUTPUTS OR 12-BIT PHASE OUTPUT AVAILABLE**
- **MICROPROCESSOR BUS INTERFACE**
- **LOW POWER CONSUMPTION - 300 mW**
- **PIN COMPATIBLE WITH ST-1172**
- **MIL AND COMMERCIAL AVAILABILITY**

## APPLICATIONS

- **FREQUENCY SYNTHESIZERS**
- **HIGH-SPEED HOPPED FREQUENCY SOURCES**
- **SINGLE SIDEBAND CONVERTERS**
- **BASEBAND RECEIVERS**
- **DIGITAL SIGNAL PROCESSORS**

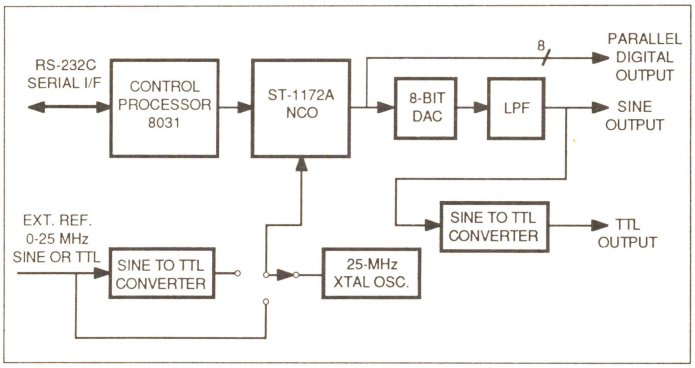
**The ST-1172A is packaged in a 40-pin DIP. It is available in both plastic and ceramic packages, and is also available screened to MIL-883C standards.**
**US Price: $240 (100 up, in plastic)**

# CMOS NCO EVALUATION BOARD STEL-9172

## FEATURES

- **SINE AND TTL OUTPUTS**
- **1 Hz TO 10 MHz OPERATION**
- **FIXED FREQUENCY MODE.**
  GENERATES A FIXED FREQUENCY FROM 1 Hz TO 10 MHz
- **SWEPT FREQUENCY MODE.**
  SWEEPS BETWEEN A START AND A STOP FREQUENCY AT UP TO 10K STEPS/SEC.
- **STEPPED FREQUENCY MODE.**
  STEPS THROUGH A USER SELECTED SEQUENCE OF UP TO 8 FREQUENCIES AT UP TO 10K STEPS/SEC.

## BLOCK DIAGRAM




## DESCRIPTION

The STEL-9172 is an evaluation board for the ST-1172A Numerically Controlled Oscillator (NCO) chip. It allows the NCO to be set up in three modes, Fixed Frequency, Swept Frequency, and Stepped Frequency, from a device such as a terminal via the on-board microcomputer using menu driven software. Frequencies from 1 Hz to 10 MHz can be generated with a resolution of 1 Hz. The interface is RS-232C compatible. The board requires a 5 volt power supply, and both sinusoidal and TTL compatible outputs are available. The system can be operated from either the on-board 25-MHz crystal controlled oscillator or an external reference clock. The ST-1172A NCO chip generates digital sine waves with a frequency resolution of 32-bits. The phase and amplitude resolutions are both 8-bits, which means that the spurious components below the Nyquist frequency are generally more than 40 dB below the primary output component. For more information on the ST-1172A chip itself please refer to the ST-1172A data sheet.

**The STEL-9172 requires an external 5 volt power supply.**
**US Price: $2975 (1-9)**
**Availabilty: 2-4 weeks**

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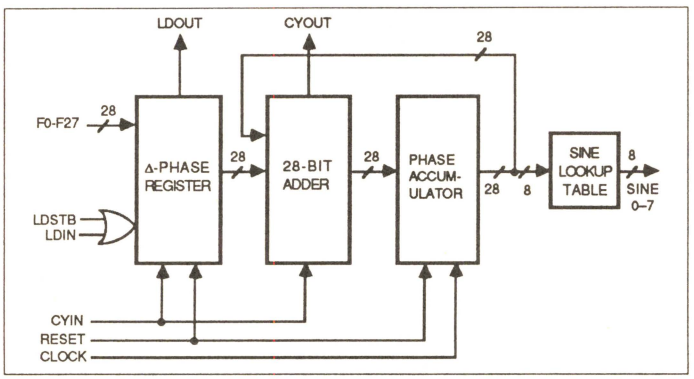
# 300-MHz ECL 100K 28-BIT RESOLUTION NUMERICALLY CONTROLLED OSCILLATOR STEL-2172

The STEL-2172 is an ECL Numerically Controlled Oscillator which operates at up to 300 MHz. This monolithic device is ideal for use in frequency synthesizers, frequency hoppers, and other precision frequency sources. It has a 28 bit frequency resolution (1 part in 268,435,456) making it possible to generate frequencies from 1 Hz up to more than 120 MHz with a resolution of almost 1 Hz. The device provides an 8-bit digitized sine wave output allowing it to generate sine waves with more than 45 dB of purity when used with a suitable high speed D-to-A converter. The STEL-2172 is similar to the ST-1172A CMOS NCO which operates at up to 25 MHz.

## BLOCK DIAGRAM




## FEATURES

- 300-MHz CLOCK FREQUENCY
- 28-BIT FREQUENCY RESOLUTION
- 8-BIT PARALLEL SINE OUTPUT
- CASCADABLE FOR ULTRA-HIGH RESOLUTION
- TTL INPUTS FOR CONVENIENT INTERFACING TO CONTROL LOGIC

## APPLICATIONS

- VHF FREQUENCY SYNTHESIZERS
- VERY HIGH SPEED HOPPED FREQUENCY SOURCES
- DIGITAL SIGNAL PROCESSING

**The STEL-2172 is packaged in a 156-pin ceramic PGA with heat sink mounting studs. A heat sink is required.**
**US Price - $625 (100's)**

# 130 MHz DIGITAL DIRECT FREQUENCY SYNTHESIZER STEL-9272

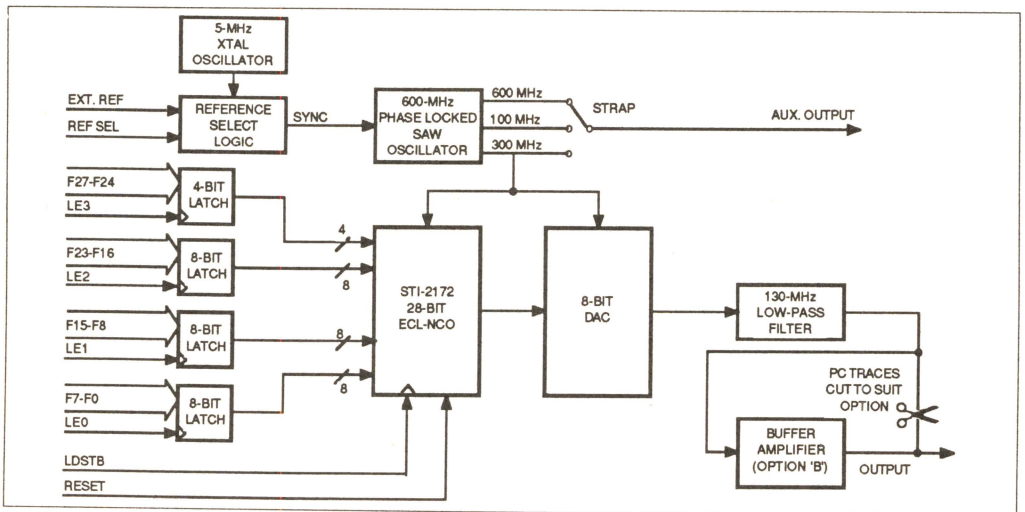
The STEL-9272 is a digital frequency synthesizer based on the STEL-2172 ECL-NCO chip. It includes a 300-MHz clock generator which may be slaved to an external 5-MHz signal. The system also includes a parallel control interface and an anti-aliasing filter at the output of the digital to analog converter. It provides a signal in the 2 KHz to 130 MHz band with a resolution of just over 1 Hz. All spurious components are more than 37 dB below the carrier at all frequencies up to 130 MHz. The frequency control input data may be loaded as a parallel 28-bit word or as 4 bytes, and frequency changes may be made as rapidly as every 125 nsecs.

## FEATURES

- 2 KHz TO 130 MHz DIGITAL DIRECT SYNTHESIZER
- 1.1-Hz RESOLUTION
- 37 dB SIGNAL PURITY AT ALL FREQUENCIES
- 300-MHz INTERNAL CLOCK CAN FREE-RUN OR BE SLAVED TO EXTERNAL 5-MHz SOURCE

**US PRICE:** $9,750 (1-9)

## BLOCK DIAGRAM

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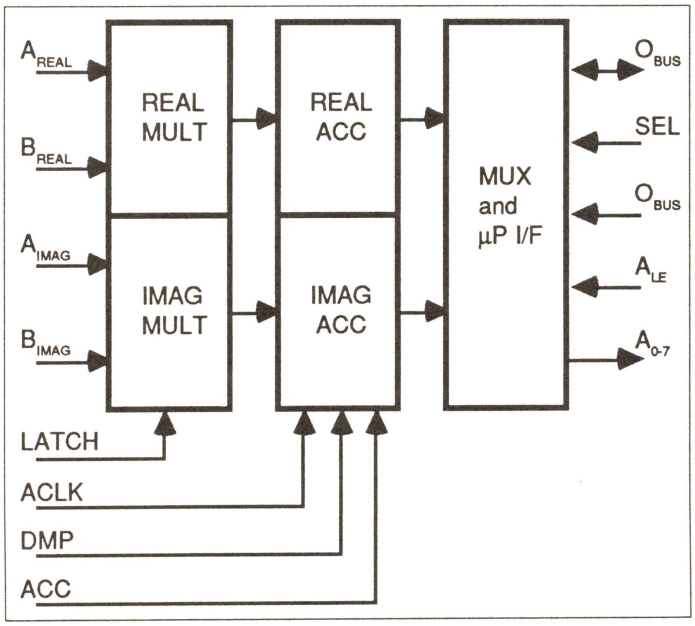
# COMPLEX MULTIPLIER / ACCUMULATOR STI-2003

The STI-2003 Complex Multiplier/ Accumulator is well suited for demodulation of digital data in satellite communication links. The complex MAC function on one chip offers single chip solutions to special signal processing tasks such as frequency translation or baseband conversion.

## BLOCK DIAGRAM




## FEATURES

- **4-BIT MULTIPLIER WITH 22-BIT ACCUMULATOR**
- **LATCHED OVERFLOW AND UNDERFLOW BITS.**
- **MAXIMUM MAC RATE OF 6 MHz**
  **No dump overhead**
- **8-BIT BUS INTERFACE.**
- **ON-CHIP ADDRESS LATCH**
  **for demultiplexing data/address bus**
- **3µ CMOS TECHNOLOGY**
- **PACKAGING: 84-pin Ceramic PGA**
- **TTL COMPATIBLE**
  **Outputs drive 2 standard TTL loads**
- **LOW POWER CONSUMPTION**
  **Less than 200 mW at 6MHz operation**

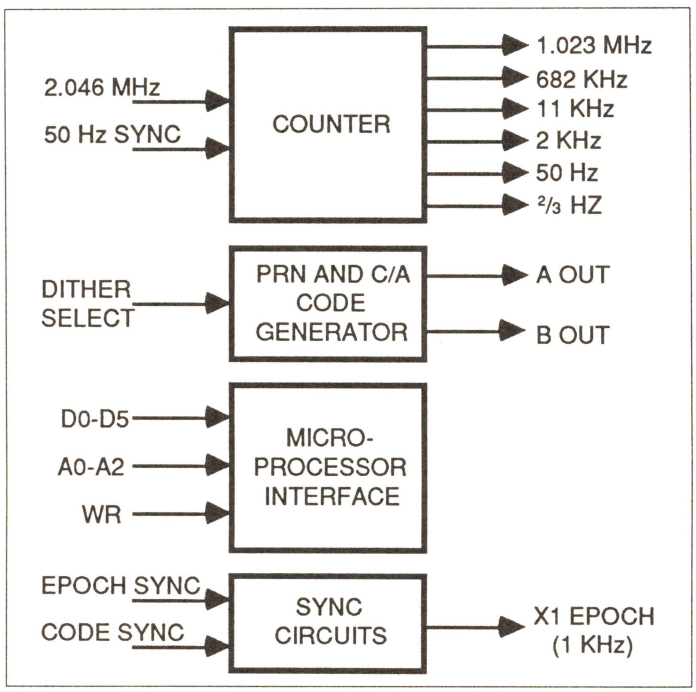
## APPLICATIONS

- **DIGITAL DEMODULATORS**
- **DIGITAL IMAGE REJECTION MIXERS**
- **ADAPTIVE EQUALIZERS**
- **DIGITAL MATCHED FILTERS**

**US Price: $350 (100 +)**

# C/A CODER STEL-1023

## BLOCK DIAGRAM




## FEATURES

- **GENERATES C/A AND PRN CODES**
- **GENERATES ALL TIMING**
- **LOW POWER CMOS, 100 mW**

The STEL-1023 C/A Coder generates the C/A (Clear/Aquisition) codes and other timing information required in GPS (Global Positioning System) receivers. It is designed to operate in micro-processor based sytems; all control functions are stored in on-chip registers. The C/A code may be dithered, and two outputs are available, one of which can be dithered independently of the other. Timing outputs are available at 1.023 MHz, 682 KHz, 11 KHz, 2 KHz, 1 KHz, 50 Hz and 2/3 Hz. The 1 KHz and 50 Hz output phasing may be synchronized to external inputs. This chip allows the parts count in a GPS receiver to be considerably reduced.

**The STEL-1023 is packaged in a 28-pin DIP**

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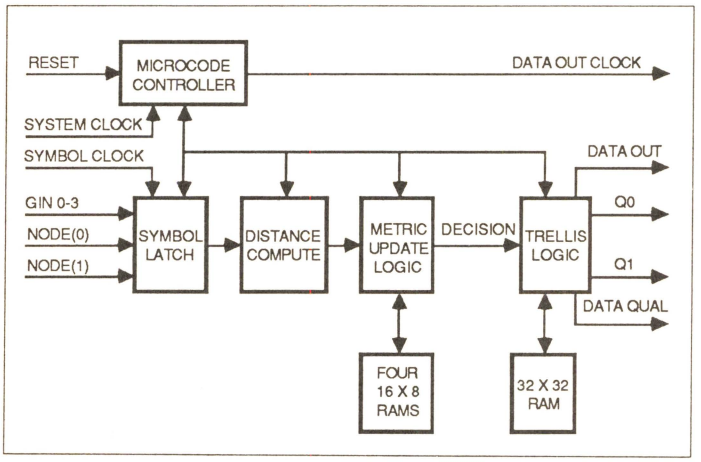
# VITERBI DECODER STI - 2010

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STI-2010 is the first commercially available monolithic Viterbi Decoder which requires no external components. The decoder works at data rates up to 256K bits per second. In addition, the decoder has the capability to perform internal node sync.

## BLOCK DIAGRAM




## FEATURES

- UP TO 256K BITS/SEC DATA RATE
- CONSTRAINT LENGTH SIX
- TWO SELECTABLE SETS OF RATE 1/2 POLYNOMIALS: G1=101001, G2=110111 AND G1=111011, G2=110001
- RATE 1/3 POLYNOMIALS: G1=101001, G2=110111, G3=111101
- FOUR BIT SOFT DECISION IN SIGN + MAGNITUDE FORMAT
- CODING GAIN 5.0 dB, RATE 1/2 (@ BER OF $10^{-5}$),
- CODING GAIN 5.3 dB, RATE 1/3 (@ BER OF $10^{-5}$)
- ALL MEMORY ON CHIP
- LOW POWER CONSUMPTION: 250 mw TYPICAL
- SINGLE 5V SUPPLY
- INTERNAL OR EXTERNAL NODE SYNC CAPABILITY

**The STI-2010 is packaged in a 40-pin plastic DIP.**
**US Price: $300 (100 +)**

# CONVOLUTIONAL ENCODER STEL-2012

## APPLICATIONS

Convolutional Encoding and Viterbi Decoding are used to provide Forward Error Correction (FEC), which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited and bandwidth is available, FEC techniques can reduce the transmission power required to achieve a given Bit Error Rate (BER). The STEL-2012 is designed to work with the STI-2010 Viterbi Decoder chip, which is capable of handling data rates up to 256 Kb/s. Separately, the STEL-2012 will work at up to 1 Mb/s.

## CIRCUIT DESCRIPTION

The STEL-2012 Convolutional Encoder is shown in the Block Diagram below. Incoming data is loaded into a shift register on the rising edges of the clock. Each of the blocks G1, G2, and G3 generates the even parity (i.e. the LSB of the sum) of its inputs, and the output symbol is selected from the 3 $G_i$ by the multiplexer. In order to generate the output code, the select inputs S0 and S1 must be switched through the correct cycle once during each clock cycle, generating 2 or 3 output symbols for each input data bit. Thus the rate desired is automatically selected according to how the S0 and S1 inputs are cycled.

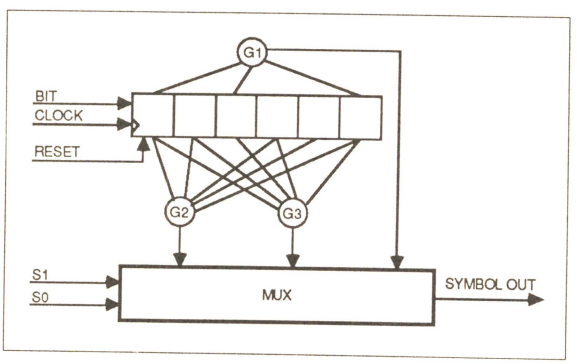
Note that the output information rate is two (rate 1/2) or three (rate 1/3) times the input data rate.

## FEATURES

- DATA RATES UP TO 1Mb/s
- CONSTRAINT LENGTH K=6
- RATE 1/2 AND RATE 1/3 ENCODING
- 24 PIN SKINNY-DIP PACKAGE
- LOW POWER - 750 mW

**US Price: $75 (100's)**

## BLOCK DIAGRAM

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# CONVOLUTIONAL ENCODER VITERBI DECODER STI-5268

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, Forward Error Correction techniques can reduce the required transmission power at the expense of the bandwidth required. The **STI-5268** is designed to perform this specific communications related function.

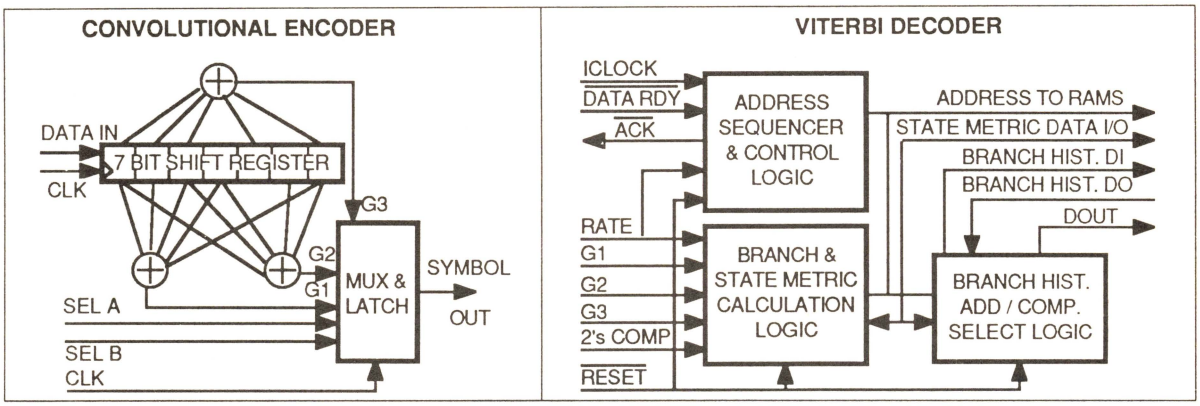
The encoder creates a stream of symbol bits which occur at a rate of 2 or 3 times the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of information despite a high symbol error rate resulting from a noisy link. The Viterbi decoder is used at the receiver to retrieve the original data from the corrupted received signal.

## FEATURES

- **CONSTRAINT LENGTH SEVEN**
- **RATE 1/2 OR 1/3**
- **THREE BIT SOFT DECISION IN SIGN + MAGNITUDE OR 2'S COMPLEMENT**
- **UP TO 9600 BITS/SEC DATA RATE**
- **CODING GAIN OF 5.2 dB AT $10^{-5}$ BER, RATE 1/2**
- **CODING GAIN OF 6 dB AT $10^{-5}$ BER, RATE 1/3**
- **EXTREMELY LOW POWER CONSUMPTION, 40 mW TYPICAL**

**The STI-5268 is packaged in a 68-pin ceramic PGA and is also available with MIL-STD 883C screening.**
**US Price: $425 (100 +)**

## BLOCK DIAGRAM




# SERIAL VITERBI DECODER STEL-9268

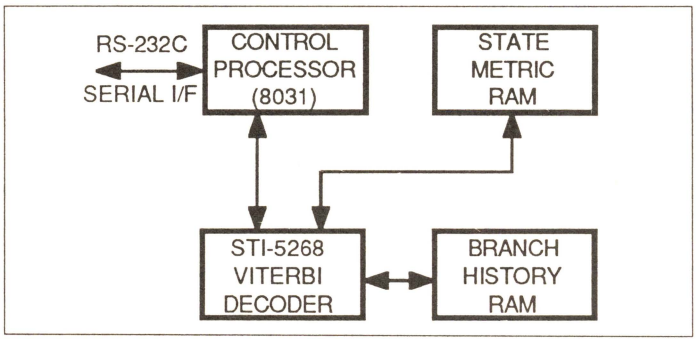
The Viterbi algorithm for decoding convolutionally encoded data is complex and extremely time consuming to compute using software. The **STEL-9268** is designed to perform this specific communications related function. It allows any computer with an RS-232C port to offload the burden of decoding Viterbi coded data with a constraint length K=7, at rates 1/2 and 1/3. It is especially suited to applications involving computer simulations of data transmission systems, where it can be used to significantly speed up the simulation. It can also be used in real systems when a soft decision is available from the demodulator.

## FEATURES

- **CONSTRAINT LENGTH K=7**
- **RATE 1/2 OR 1/3**
- **THREE BIT SOFT DECISION IN SIGN + MAGNITUDE OR 2'S COMPLEMENT**
- **CODING GAIN OF 5.2 dB AT $10^{-5}$ BER, RATE 1/2**
- **CODING GAIN OF 6 dB AT $10^{-5}$ BER, RATE 1/3**
- **PACKED SYMBOL INPUT FORMAT**
- **RS-232C INTERFACE OPERATES AT 9600 BPS**
- **120 VOLT POWER SUPPLY**

**US Price: $4,900 (1-9)**
**Availability: 4-6 weeks**

## BLOCK DIAGRAM

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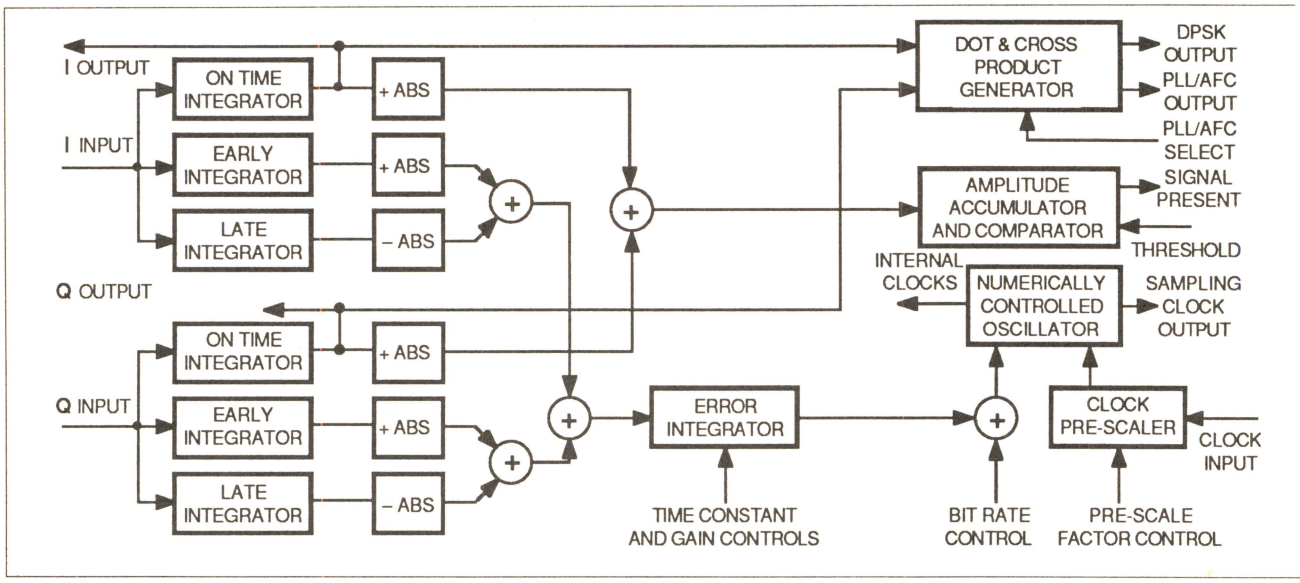
# BIT SYNCHRONIZER/ PSK DEMODULATOR STEL-2110

The STEL-2110 Bit Synchronizer/PSK Demodulator provides bit timing to control the sampling of the signal in a receiver as well as a feedback signal to control the frequency of the local oscillator. It can be used in high speed coherent PSK, QPSK and DPSK modems in either continuous carrier or burst carrier environments. Soft decision output data is provided to facilitate the inclusion of Forward Error Correction (FEC) using convolutional coding and Viterbi decoding into the system.

## FEATURES

- **UP TO 6 MBPS OPERATION IN BPSK MODE AND 12 MBPS IN QPSK MODE**
- **CARRIER TRACKING FEEDBACK WITH PLL OR AFC OUTPUTS**
- **BIT TIMING DRIVEN BY NCO**
- **PROGRAMMABLE 2nd ORDER LOOP**
- **PROGRAMMABLE DATA RATES**
- **DPSK OUTPUT AVAILABLE**

## BLOCK DIAGRAM



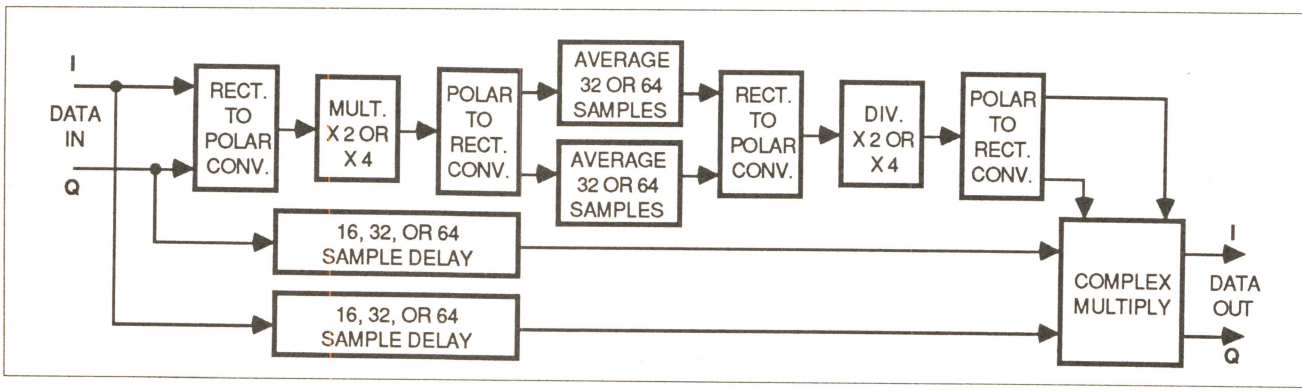

# BLOCK PHASE ESTIMATOR STEL-2210

The STEL-2210 Phase Estimator provides a phase reference for demodulating BPSK (binary PSK) or QPSK (quadrature PSK) data in the presence of phase roll (frequency offset). The device generates an averaged phase reference without using a phase-locked loop, so that the phase acquisition time is very short. This makes the device ideal for use in burst-mode systems. The device operates on 6-bit soft decision data and is suitable for use with Forward Error Correction (FEC) systems using convolutional coding and Viterbi decoding.

## FEATURES

- **UP TO 6 MBPS OPERATION IN BPSK MODE AND 12 MBPS IN QPSK MODE**
- **COMPENSATES FOR FREQUENCY OFFSET OF UP TO 0.6% OF SYMBOL RATE AT $E_b/N_o$ OF UP TO 4 dB**

## BLOCK DIAGRAM

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## MULTIBUS I SINGLE BOARD COMPUTER STEL-68020

### DESCRIPTION

The STEL-68020 is a single board computer based on an MC68020 processor running at 12.5 MHz, with a 68881 or 68882 co-processor. The board is Multibus I compatible both electrically and physically, and has 1.064 Mbytes of dual ported RAM, 64 Kbytes of which is non-volatile (backed-up with a lithium battery). A useful feature of the system is that it has sockets for up to 512 Kbytes of ROM or EPROM on board, making it self contained in many applications. The board also has 5 serial ports and four 8 bit timers. Flexible interrupt options are available, with 7 levels of interrupt, and the board supports the many features of the versatile Multibus I / IEEE796 Bus interface, including the Multimaster and Master/Slave bus arbitration operating modes. A reset switch and 2 status lights are accessible from the front of the card. The popular VRTX® real-time operating system has been ported to this SBC, and can be implemented in just 4Kbytes of memory.

® VRTX is the Trademark of Ready Systems, Inc., Palo Alto, CA.

**US Price: $3450 (1-9)**
**Availability: 2-4 weeks**

### FEATURES

- **12.5-MHz, 32 bit microprocessor**
- **Floating point co-processor**
- **1 Mbyte dual-port dynamic RAM**
- **64 Kbytes dual-port non-volatile RAM**
- **Sockets for 8 ROM/EPROM chips, supporting up to 256 or 512 Kbytes**
- **One async RS-232C port with hardware programmable baud rate**
- **Three sync/async RS-232C ports with software programmable baud rates**
- **One sync/async RS-423 port with software programmable baud rate**
- **Sync ports support Bisync, HDLC, SDLC, NRZ, NRZI, and FM protocols, with CRC-16 or CCITT error checking**
- **Four individually programmable 8-bit timers with separate pre-scalers**
- **7 prioritized interrupt levels, all maskable except the highest**

# STANFORD TELECOMMUNICATIONS

## Company Profile

Stanford Telecommunications, Inc. is a technology leader in advanced signal processing and satellite communications network control software. The Company develops, manufactures, and supports earth terminal electronic systems that provide the vital information links between satellites and their users. The systems also provide the control of complex networks of spacecraft and earth terminals. Most of the company's business is for agencies of the U.S. Government.

The Company's technologies include:

- advanced digital signal processing, often implemented using our own proprietary custom and semi-custom integrated circuits;
- information processing software - all of the Company's products contain microprocessors or minicomputers;
- microwave frequency electronics.

The markets addressed by these technologies include electronic systems for all three categories of spacecraft; communications, surveillance, and the revolutionary new navigation satellites. In addition, the Company performs important engineering functions in design for the next-generation U.S. Air Traffic Control and the Space Station.

You may be able to take advantage of STI's systems and integrated circuit design expertise in the design of your next custom or semi-custom integrated circuits. STI can help you with all phases of the design of integrated circuits, from concept through system design and chip design to turnkey procurement. For further information, please write or call Gwyn Edwards at Stanford Telecommunications, Inc., (408) 980-5666.

**For further information on the products listed in this section, please write or call Patricia Laakso at Stanford Telecommunications, Inc., 2421 Mission College Blvd., Santa Clara, CA 95054-1298. (408) 980-5684.**

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# Overview

Texas Instruments Military program offers high reliability integrated circuits covering a complete product spectrum. The program is designed to meet and support Military processing requirements. Standard device offerings include JM38510, DESC Standard Military Drawing (SMD), Class B Processing, and the Military Temperature Range.

| Product Line | Processing Flows | Types |
|---|---|---|
| Logic | SN, SNJ, JM38510 | 54TTL<br>54S<br>54LS<br>54AC<br>54ACT<br>54ALS<br>54AS<br>54BCT<br>54F<br>54HC<br>54HCT |
| | B | PAL® |
| Linear | SN, SNJ, JM38510 | Interface, Control, Display Drivers |
| MOS Memory | SM, SMJ | EPROM, DRAM, SRAM |
| Bipolar Memory | JBP, SNJ | PROM, RAM |
| Microprocessor | SM, SMJ | 320 DSP Family<br>340 GSP Family |
| | SN, SNJ | 8 Bit Slice Family |
| | Class B | SBP9989, SBR9000 |

® PAL is a registered trademark of Monolithic Memories, Inc.

# Military Product Flows

| Process Level | Order As | Description |
|---|---|---|
| JM38510 Class S | JM38510/XXXXXSXA | Qualified per MIL-M-38510 Class S. Produced in DESC certified production facilities. |
| JM38510 Class B | JM38510/XXXXXBXA | Qualified per MIL-M-38510 Class B. Produced in DESC certified production facilities. |
| DESC SMD | Drawing Number | Certified and symbolized to the DESC Standard Military Drawing where TI is an approved source. |
| Class B | SNJ, JBP, SMJ, B | Screened per requirements of MIL-Std-883 Class B Method 5004 & 5005.<br>Conforms to the requirements of JEDEC Publication 101. (For detailed screening information, see Military Products Designers' Reference Guide.) |
| Military Extended Temperature Range | SN54, SN55, SM | Standard Commercial Processing |

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# Packages Available

| Package Description | Package Type | Logic | Linear | Bipolar Memory | MOS Memory | μP |
|---|---|---|---|---|---|---|
| Ceramic DIP | J | ALL | X | X | X | |
| | JG | | X | | | |
| | JT | All except TTL, 54S | | X | | |
| Side Braze Ceramic DIP | JD | | X | | X | X |
| Ceramic Flatpack | W | ALL | X | | | |
| | WC | | X | | | |
| | U | | X | | | |
| Ceramic Chip Carrier (Square) | FK | All except TTL | X | X | | |
| | FD | | X | | | X |
| Ceramic Chip Carrier (Rect) | FG, FV | | | | X | |
| Pin Grid Array | GB | | | | | X |
| Ceramic Chip Carrier (Leaded) | FJ | | X | | | X |

# DESC Standard Military Drawings

The DESC Standard Military Drawing (SMD) program provides industry standard specifications in compliance with MIL-Std-883, Class B requirements for devices that are not JAN qualified. Texas Instruments fully supports the DESC SMD program. Contact the factory for 1988 DESC approval plans. The DESC SMD nomenclature is described below.

82005 or 5962-85155 — 01 — X — X

DRAWING NUMBER

DEVICE TYPE

PACKAGE TYPE

C = 14 Pin DIP
D = 14 Pin Flatpack
E = 16 Pin DIP
F = 16 Pin Flatpack
L = 24 Pin DIP (300 MIL)
P = 8 Pin DIP
R = 20 Pin DIP
S = 20 Pin Flatpack
2 = 20 Pad LCCC
3 = 28 Pad LCCC
Z = 44 Pad LCCC

LEAD FINISH

A = Solder DIP (Standard)
B = Tin Plate
C = Gold Plate

# Logic

Digital Logic Nomenclature

EXAMPLE: SNJ — 54 — LS00 — J

PREFIX

Blank, SN = Standard Prefix
SNJ = Class B Processing

MIL TEMPERATURE (−55°C/125°C)

CIRCUIT DESIGNATOR

Blank = Standard TTL
LS = Low Power Schottky
S = Schottky
ALS = Advanced Low Power Schottky
F, AS = Advanced Schottky
HC = High-speed CMOS
HCT = TTL compatible HC
AC = Advanced CMOS
ACT = TTL compatible Advanced CMOS
BCT = BiCMOS

PACKAGE

J = CDIP
JT = 24 pin, 300 mil CDIP
W = Flatpack
FK = LCCC

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# Advanced CMOS Logic (ACL)

ACL Nomenclature EXAMPLE: SNJ 54 AC 11 000 J

- PREFIX
  - Blank = Standard Process
  - SNJ = Class B Process Option
- MILITARY TEMP RANGE
- PRODUCT FAMILY
  - AC = Advanced CMOS
  - ACT = TTL Compatible AC
- CENTER PIN VCC AND GND
- EQUIVALENT TTL FUNCTION
- PACKAGE TYPE
  - J = CDIP
  - FD/FK = LCCC

## Advanced Logic

### EPIC Advanced CMOS Logic

TI's 1-micron EPIC Advanced CMOS Logic (ACL) family offers a 3X speed improvement over the High-Speed CMOS logic devices currently available and provides 24 mA of output drive. These products have a typical propagation delay of < 3 ns. Typical maximum operating frequency is 150 MHz. The advanced features of this family are made possible by a 1-micron, twin-well CMOS process which TI calls EPIC (Enhanced Performance Inplanted CMOS).

The ACL family provides superior latchup protection and electrostatic discharge protection on the inputs or outputs. At the same time, ACL offers all the traditional advantages of CMOS technology, such as low power consumption, high noise immunity and flexible power-supply requirements.

This advanced CMOS logic family is a joint development of Texas Instruments and Signetics/Philips. Each company has the responsibility to design specific functions in the 1-micron logic family product spectrum. The agreement involved the exchange of design data bases that allowed TI and Signetics/Philips to introduce a new alternately-sourced, identically specified product line into the marketplace.

Features:
PROP DELAY: < 3 NS
IOL, IOH: 24 mA
Vcc: 3V to 5.5V for AC
4.5V to 5.5V for ACT
- ZERO STANDBY POWER • ESD PROTECTION
- LATCH-UP PROTECTION • I μGATE LENGTH
- Center Pin Vcc and Ground

Packages: CERAMIC DIP: J, JT CHIP CARRIER: FK

### 54F Devices

Texas Instruments offers military versions of general-purpose SSI and MSI digital-logic functions in the 54F series of bipolar TTL integrated circuits.

TI currently supplies bipolar logic products from five families—TTL, Schottky (S), low-power Schottky (LS), advanced low-power Schottky (ALS), and advanced Schottky (AS). The addition of the 54F devices complements TI's existing family of standard products offered in military temperature range.

54F devices are offered in ceramic dual-in-line (DIP) packages as well as leadless chip carriers (LCCC) and ceramic flat packs.

Contact Texas Instruments Field Sales Offices for up to date 54F device product spectrum.

Advanced Logic Family Comparison

| | 54ALS | 54AS | 54F | 54HC | 54AC |
|---|---|---|---|---|---|
| Power/Gate-Static | 1.2 mW | 8 mW | 4 mW | 2.5 nW | 2.5 nW |
| 100 KHz | 1.2 mW | 8 mW | 4 mW | 0.17 mW | 0.2 mW |
| Typical Prop Delay | 4 nS | 1.7 nS | 3 nS | 8 nS | 3 nS |
| Speed-Power Product | 4.8 pJ | 13.6 pJ | 12 pJ | 1.4 pJ | 0.6 pJ |
| FMAX-Typical | 80 MHz | 160 MHz | 140 MHz | 40 MHz | 150 MHz |
| Output Current | | | | | |
| Standard | —.4/4 mA | —2/20 mA | —1/20 mA | —4/4 mA | —24/24 mA |
| Buffer/Drivers | —12/12 mA | —12/48 mA | —12/48 mA | —6/6 mA | —24/24 mA |
| Transceivers | —12/12 mA | —12/48 mA | —3/48 mA | —6/6 mA | —24/24 mA |
| Registers/Latches | —1/12 mA | —12/32 mA | —3/20 mA | —6/6 mA | —24/24 mA |
| (82X, 84X) | — | —24/32 mA | —3/20 mA | — | — |
| (10XX) | —1/12 mA | —40/40 mA | | — | — |
| Product Features | | | | | |
| ESD Protection | Yes | Yes | Yes | Yes | Yes |
| Miller Killer CKTS | AC, DC | AC, DC | AC, DC | — | — |
| Inputs | PNP | PNP | PNP | PMOS/NMOS | PMOS/NMOS |
| DC & AC Guar Over Temp | Yes | Yes | Yes | Yes | Yes |
| Worst Case Limits | Yes | Yes | Yes | Yes | Yes |
| Functional Comparison-Defined Functions | 40% LS<br>60% New | 23% STTL<br>77% New<br>35% Fast, 65% New | 21% STTL<br>79% New | 72% TTL, 16% HCT<br>6% HC4000, 6% New | |
| Alternate Source | National | National | FSC, MOT, SIG | MOT, NSC, RCA | Philips/SIG |

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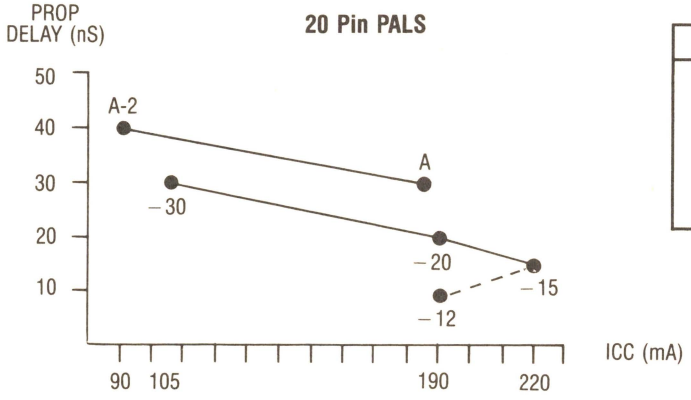
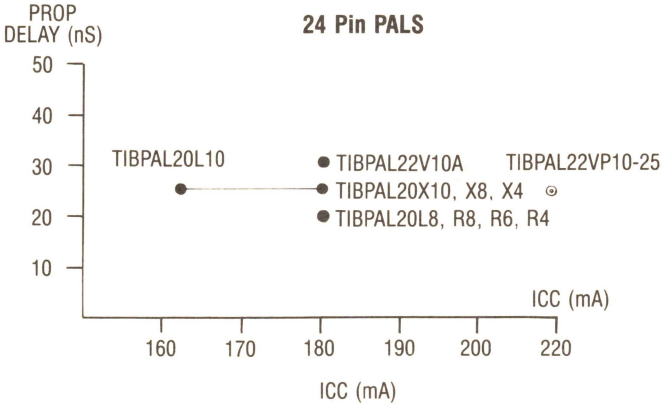
# Bipolar Impact Technology

## Fastest PALS

IMPACT™ (IMPlanted Advanced Composed Technology) is an advanced bipolar technology. IMPACT's 2 $\mu$M feature size and 1.05 mil$^2$ transistor area offers performance advantages in speed, power, and circuit density over preceding bipolar technologies, the IMPACT technology is in production today and is being applied PAL product families, and selected MSI/LSI ALS and AS devices.




| DEVICE | MAX ICC | MAX tpd |
|---|---|---|
| 16XXA | 180 mA | 30 nS |
| 16XXA-2 | 90 mA | 40 nS |
| 16XX-12* | 190 mA | 12 nS |
| 16XX-15 | 220 mA | 15 nS |
| 16XX-20 | 190 mA | 20 nS |
| 16XX-30 | 105 mA | 30 nS |




| DEVICE | MAX ICC | MAX tpd |
|---|---|---|
| TIBPAL22V10A | 180 mA | 30 nS |
| TIBPAL22VP10-25 | 220 mA | 25 nS |
| TIBPAL20L10-25 | 165 mA | 25 nS |
| TIBPAL20X10-25 | 180 mA | 25 nS |
| TIBPAL20X8-25 | 180 mA | 25 nS |
| TIBPAL20X4-25 | 180 mA | 25 nS |
| TIBPAL20L8-20 | 180 mA | 20 nS |
| TIBPAL20R8-20 | 180 mA | 20 nS |
| TIBPAL20R6-20 | 180 mA | 20 nS |
| TIBPAL20R4-20 | 180 mA | 20 nS |

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PAL is a registered trademark of Monolithic Memories, Inc.
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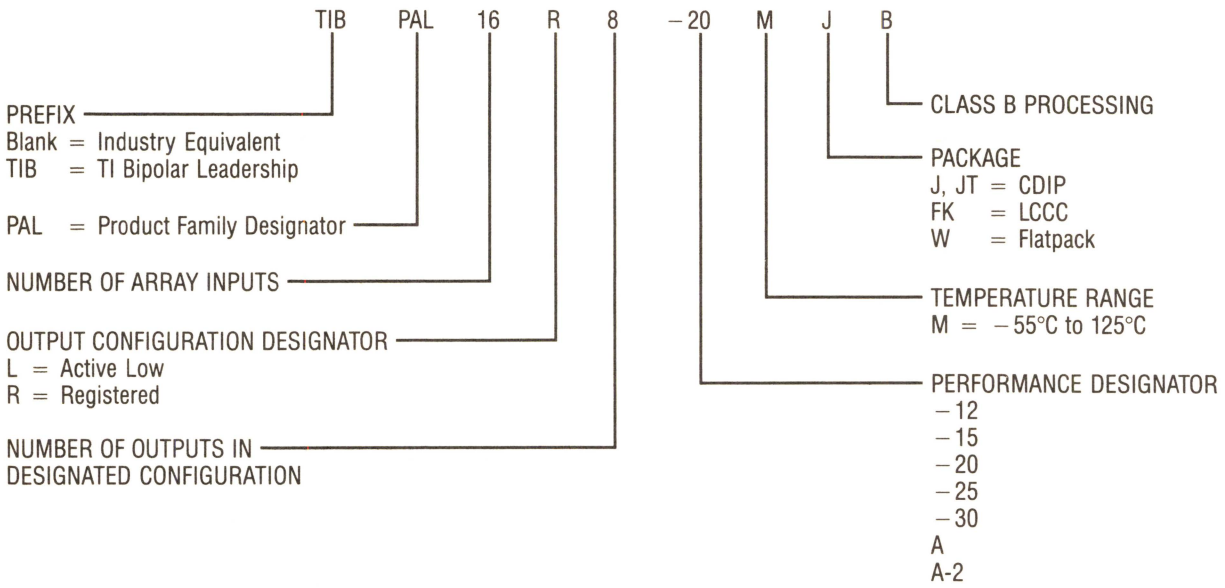
# Programmable Array Logic

PAL Nomenclature (Industry Leadership Part Types)







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# Linear

## Linear Nomenclature

Orders for linear functions as described in Selection Guide should include complete Device Type Number as noted:
EXAMPLE: LinCMOS Dual, Low Bias Operational Amplifier. Device Type Number—TLC27L2BMJGB.

TLC 27 L 2 A M JG B

**PREFIX**
Must contain two or three letters
TL = TI Linear Products
TLC = TI LinCMOS Products

**CIRCUIT DESIGNATION**
Must contain two or three numbers

**BIAS CURRENT**
L = Low, M = Med
No Letter = High

**DEVICE COMPLEXITY**
1 = Single
2 = Dual
4 = Quad

**INPUT OFFSET VOLTAGE**
A = 5.0 mV
No Letter = 10.0 mV

**OPERATING TEMPERATURE RANGE**
M = Military (−55°C to 125°C)

**PACKAGE**
FK = LCC
J = 14 Pin C-DIP
JG = 8 Pin C-DIP
L = T099/T0100
KJ = 4 Pin T03
LA = T039
LD = T046
K = 2 Pin T03

**Class B Processing**

**STANDARD SECOND SOURCE PREFIXES**

| | | |
|---|---|---|
| ADC = National | OP = PMI | SG = Silicon General |
| LM = National | RM = Raytheon | μA = Fairchild |
| MC = Motorola | SE = Signetics | LT, LTC = Linear Technology |

Interface functions as described in Selection Guide should include complete Device Type Number as noted:
EXAMPLE: Dual Line Driver with Class B Processing. Device Type Number—SNJ55109AJ

SNJ 55 109A J

**PREFIX**
SN = TI Interface Product
SNJ = TI Interface Product with Class B Processing

**MIL TEMP RANGE**
(−55°C to 125°C)

**CIRCUIT DESIGNATION**
May contain two, three or four numbers & letters

**PACKAGE**
FD, FK = Chip Carrier
J = 14/16/20Pin C-DIP
JD = Size Braze DIP
JG = 8 Pin C-DIP
W = Flat Pack

**STANDARD SECOND SOURCE PREFIXES**
AM = AMD
DS = National
μA = Fairchild

Texas Instruments



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# MOS Memory

## MOS Memory Nomenclature

EXAMPLE: SMJ 4164 –15 JD S

**PREFIX**
SM = Standard Prefix
SMJ = Class B Processing, JEDEC Publication 101

**CIRCUIT DESIGNATOR**
Must contain four characters

**ACCESS TIME**
Device types are available with various speeds

**TEMPERATURE RANGE**
Must contain one letter only
M = –55°C to 125°C
S = –55°C to 100°C (except 4164 & 4256 which are –55°C to 110°C)
E = 40°C to 85°C
L = 0°C to 70°C

**PACKAGE TYPE**
Must contain one or two letters

### Military Memories

Texas Instruments offers a wide selection of MOS Memories. Three basic types are offered: DRAMs, EPROMs and SRAMs. Most are offered in both through hole style Ceramic Dual-in-line packages and surface mountable Leadless Ceramic Chip Carrier (LCCC) or Ceramic Small Outline "J" formed (CSOJ) packages.

### DRAMs

There are an assortment of DRAM densities and organizations offered in the DRAM product line. Densities range from 64K through 1 Meg. Organizations offered include X1 and X4. A Specialized version of the DRAM is the Video RAM (VRAM) which includes an onboard shift register. The VRAM is also offered in a X1 and a X4 organization.

### EPROMs

Texas Instruments' EPROM family features High Voltage CMOS technology. While these CMOS EPROMS are pin compatible with existing NMOS EPROMs they feature low standby and active power without sacrificing speed. Densities range from 128K to 512K with a 1 Meg planned for late 1988.

### SRAMs

CMOS Static RAMs are new product offerings for TI. This product line features TI's exclusive EPIC™ technology and the six transistor (6T) memory cell design for improved speed, increased temperature stability and greater resistance to soft errors. Initial product offering will be a 16K X 1 part. 1988–89 plans include 64K and 72K density parts with long range plans to include 256K density devices. Access times range from 25 to 55 ns.

| Device | Type | Temp Range | Maximum Access Time (ns) | Organization | Package Type | |
|---|---|---|---|---|---|---|
| | | | | | Through Hole | Surface Mountable |
| 4161 | VRAM | S | 150, 200 | 64K × 1 | 20 Pin CDIP (JD) | |
| 4164 | DRAM | S,L | 120, 150, 200 | 64K × 1 | 16 Pin CDIP (JD) | 18 Pad LCCC (FG) |
| 4256 | DRAM | S | 120, 150, 200 | 256K × 1 | 16 Pin CDIP (JD) | 18 Pad LCCC (FV) |
| 4416 | DRAM | S,L | 150, 200 | 16K × 4 | 18 Pin CDIP (JD) | 18 Pad LCCC (FG) |
| 4461* | VRAM | S | 150, 200 | 64K × 4 | 20 Pin CDIP (JD) | 20/26 Pin CSOJ (HJ)* |
| 4464 | DRAM | S | 120, 150, 200 | 64K × 4 | 18 Pin CDIP (JD) | 18 Pad LCCC (FV)* |
| 44C256* | DRAM | M | 120, 150 | 256K × 4 | 20 Pin CDIP (JD) | 20/26 Pin CSOJ (HJ)* |
| 44C257* | DRAM | M | 120, 150 | 256K × 4** | 20 Pin CDIP (JD) | 20/26 Pin CSOJ (HJ)* |
| 4C1024* | DRAM | M | 120, 150 | 1 Meg × 1 | 18 Pin CDIP (JD) | 20/26 Pin CSOJ (HJ)* |
| 4C1027* | DRAM | M | 120, 150 | 1 Meg × 1** | 18 Pin CDIP (JD) | 20/26 Pin CSOJ (HJ)* |
| 27C256 | EPROM | M | 200, 250, 300 | 32K × 8 | 28 Pin CDIP (J) | 32 Pad LCCC (FG)* |
| 27C128 | EPROM | M | 200, 250, 300 | 16K × 8 | 28 Pin CDIP (J) | 32 Pad LCCC (FG)* |
| 27C512 | EPROM | M | 250, 300 | 64K × 8 | 28 Pin CDIP (J) | 32 Pad LCCC (FG)* |
| 27C010* | EPROM | M | 200, 250, 300 | 128K × 8 | 28 Pin CDIP (J) | 32 Pad LCCC (FG)* |
| 27C210* | EPROM | M | 200, 250, 300 | 64K × 16 | 28 Pin CDIP (J) | 32 Pad LCCC (FG)* |
| 61CD16 | SRAM | M | 25, 35, 45 | 16K × 1 | 20 Pin CDIP (JD) | 20 Pad LCCC (FG)* |
| 64C16* | SRAM | M | 25, 35, 45 | 4K × 4 | 20 Pin CDIP (JD) | 20 Pad LCCC (FG)* |
| 68CE16* | SRAM | M | 30, 40, 55 | 2K × 8 | 24 Pin CDIP (JD) | 32 Pad LCCC (FG)* |
| 68CE64* | SRAM | M | 30, 40, 55 | 8K × 8 | 28 Pin CDIP (JD) | 32 Pad LCCC (FG)* |
| 61C64* | SRAM | M | 30, 40, 55 | 64K × 1 | 22 Pin CDIP (JD) | 22 Pad LCCC (FG)* |
| 64C64* | SRAM | M | 30, 40, 55 | 16K × 4 | 22 Pin CDIP (JD) | 22 Pad LCCC (FG)* |
| 69CE72* | SRAM | M | 30, 40, 55 | 8K × 9 | 28 Pin CDIP (JD) | 32 Pad LCCC (FG)* |

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**Static Column Decode

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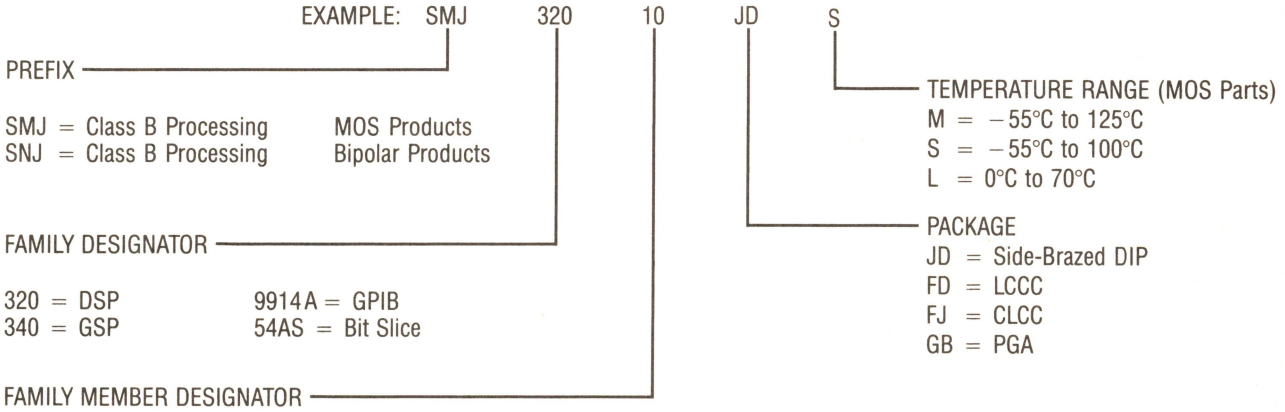
# Application Processors

Part Number Nomenclature




## Application Processors

Texas Instruments offers a variety of specialized processors that can be used in a number of military applications. Included are the 320 Digital Signal Processor (DSP) family, 340 Graphics System Processor (GSP) family, 8 Bit Slice family and the IEEE 488 General Purpose Interface Bus (GPIB) Controller. These state-of-the-art components can reduce component count up to 10X and improve system speed. System power can also be reduced by the component count reduction alone.

## Digital Signal Processors

The 320 DSP family circuits are finding their way into military applications such as missile guidance, smart munitions, control (servo, position and rate, reference), communications and signal processing (digital filtering, data encryption, data scrambling), FFTs, voice processing, radar/sonar, ECM, EC2M and many others. The 320 family includes the 32010, 320C10, 32020 and the 320C25. The 32010 and 32020 are both NMOS technology devices while the 320C10 and 320C25 are both CMOS technology devices. All 320 family devices feature the highly-pipelined modified Harvard Architecture and mostly single cycle instruction sets.

## Graphics System Processor

Texas Instruments has responded to the evolution within the Graphics industry with the development of a family of VLSI products to address their specific needs. Graphics system requirements have gone from static 2-dimensional (2D) wire frame and Sprite graphics to the present color filled 2D and 3D real-time systems with letter quality text. To meet those demands, a high-performance processor and controller are necessary to provide control of the VRAM and insure little overhead in managing the display memory. The SMJ34010 Graphics System Processor (GSP) and the SMJ34061 video system controller were developed by TI to address these needs.

The SMJ34010 combines the best features of general purpose processors and graphics controllers to create a powerful and flexible GSP. The on-chip processor executes both graphics instructions and general purpose instructions. The GSP is a true 32-bit processor with 32-bit internal data paths, a 32-bit ALU, a 128 megabyte address space, 32-bit general purpose registers, a 32-bit stack pointer and a 256 byte instruction cache to increase performance. Non-processor functions include CRT timing, screen refresh and DRAM refresh. Separate interfaces are provided for



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# Application Processors

communicating with a Host processor to provide the video timing signals necessary to control a CRT monitor and for connecting directly to DRAMs and VRAMs.

The SMJ34061 Video System Controller (VSC) is a high performance NMOS device that controls the video display and the dynamic memory of a bit-mapped graphics system. The principle role of the VSC is to provide an external processor with virtually unlimited access to video memory eliminating delays caused by conflicts with display update functions. Using the SMJ34061 relieves the system CPU of the burden of controlling system memory, refreshing video memory and reloading VRAM internal shift registers for bit-mapped displays.

## SMJ9914A GPIB Controller

The SMJ9914A provides an interface between a Microprocessor System and the General Purpose interface bus specified in the IEEE-488 1975/1978 standards and the IEEE-488a 1980 supplement. It relieves the processor of the task of maintaining the IEEE protocol. By utilizing the interrupt capabilities of the device, the bus does not have to be continually polled, and fast responses to changes in the interface configuration can be achieved. This device can be complimented using the SNJ95160B and SNJ95161B transceiver/drivers.

## Bit-Slice Family

Texas Instruments' Bit-Slice product family compliments the other processor products by offering maximum flexibility at the fastest possible speed. While Bit-Slice solutions require typically higher component counts and power than some of the more dedicated processors there are certain high performance applications that need the features of a Bit-Slice design. TI's bit-slice family utilizes TI's oxide isolated 2-um IMPACT-S™ process. The combination of IMPACT™ technology and a low voltage internal circuit configuration called Schottky Transistor Logic (STL) offers high performance with low power dissipation.

The SNJ54AS888 is a registered 8-bit ALU slice that is the main component in TI's 8-bit slice product family. It can be cascaded to word widths up to 64 bits. The 8-bit ALU can perform seven arithmetic and six logical instructions, besides arithmetic, logical or circular shifts. Other devices in the family include the SNJ54AS890 14-bit microsequencer and the SNJ54AS897 16-bit barrel shifter.

## Hardware/Software Support

All of TI's microprocessor products are well supported with both hardware and software development tools. Contact the factory for details.

320 Digital Signal Processor Family Features

| Characteristics | SMJ320C10 | SMJ32020 | SMJ320C25** |
|---|---|---|---|
| Technology | 2 μM CMOS | 2.4 μM NMOS | 1.8 μM CMOS |
| Bar Size (Sq Mils) | 41K | 115K | 110K |
| Clock Rate (Max) | 20 MHz | 20 MHz | 40 MHz |
| Cycle Time (Min) | 200 ns | 200 ns | 100 ns |
| Through-Put | 5 MIPs | 5 MIPs | 10 MIPs |
| Base Instructions | 60 | 109 | 133 |
| Max Power (W) | 0.4 | 2.2 | 1.0/0.4* |
| Temp Range (Degrees c) | −55 to 125 | −55 to 100 | −55 to 125 |
| On-Board Data RAM | 144 × 16 | 544 × 16 | 544 × 16 |
| Packages | 40/44 Pin JD/FD | 68 Pin GB/FJ | 68 PIN GB/FJ |

*Standby Power
**Planned Product

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## Semicustom

Texas Instruments has actively participated in the military semicustom market for over 8 years. With a complete family of high performance, low power CMOS gate arrays and military qualified standard cells, the Military Custom/Semicustom Department of Texas Instruments continues to provide its customers with the state of the art military system solution. This complete military semicustom product line is backed by a dedicated customer service network and by a comprehensive design and manufacturing support system that has placed TI at the forefront of the military semiconductor industry through the quality and reliability of its military products.

## Standard Cell Technology

The SN54/74SC Standard Cell products are custom design equivalents of standard products. Each cell layout is handcrafted by an IC designer, then thoroughly modeled and characterized. These logic building blocks are designed for interconnection on silicon, rather than on a printed circuit board, providing an efficient and economical path to the development of unique integrated circuits, customized for the user's application. Semicustom and custom circuits now incorporate major system functions such as processing, memory, and interface at the VLSI level.

Texas Instruments offers the SN54/74SC standard cell family based on 1- and 2-$\mu$M twin-well CMOS technology. The 2-$\mu$M standard cell family is fabricated using an advanced double-level metal process, and the 1-$\mu$M product family is a natural geometric progression of the 2-$\mu$M.

## CMOS Standard Cell Software Library

Texas Instrument's design staff has carefully constructed the CMOS standard cell library to offer both functional variety and design flexibility. The library contains over 300 cells, encompassing a wide variety of elements ranging from simple inverters to complex LSI structures. Each cell is fully characterized over the military temperature range and contains a circuit simulation model, a logic simulation model, and a detailed data sheet.

In an effort to continually expand the variety and complexity of cells as well as ensure their accuracy, quarterly updates are performed. For further information on the software library contact your local TI Field Sales Office.

## CMOS Gate Arrays

Texas Instruments also has available a high performance, low power CMOS gate array family. These arrays are designed utilizing the same proven 1.0 micron technology as previously noted for the standard cells. This family of arrays provides a high performance solution to random logic design needs with the benefit of fast turn around time and design cost effectiveness.

TI has participated in the gate array market for over eight years and this has provided the learning experience necessary for rapid availability of easily-routed low-risk arrays.

## Gate Array Library

The CMOS gate array library provides a one-for-one mapping of all logic cells found in the TI standard cell library. This approach allows for a flexible design scenario wherein logic designs may be captured on a workstation regardless of final standard cell or gate array implementation. This approach also allows TI to readily convert an array or standard cell to the other technology without adding the unnecessary risk of re-generating the data base already in place.

## Criteria for Semicustom Technology Implemented

Both the CMOS gate arrays and CMOS standard cells offer the customer unique benefits in many potential applications. Each design will have to be evaluated for its specific semicustom requirements and target technology decisions would be made accordingly.

In general, a gate array is best suited for logic-only applications wherein there is an equitable balance between the number of gates and number of I/O cells utilized. This design would then need to fit into a given gate array with a reasonable number of available gates and I/O's utilized.

A random logic design which is dominated by the amount of core logic or by the number of I/O buffers must be evaluated for standard cell implementation. The potential dramatic reduction in final chip area could warrant the rejection for an inefficiently used gate array.

All designs requiring specialized on-chip functions, complex high performance macro cells, or extraordinary buffer requirements would immediately be targeted for a standard cell implementation.

## Technology Roadmap

Texas Instruments remains committed to supporting the semiconductor requirements of military systems. This commitment holds true for semicustom products. While supporting existing design commitments, TI will continue to improve technology for all semicustom products to offer state-of-the-art, high performance, reliable products. Our technology roadmap will encompass sub-micron CMOS which has already been proven feasible on TI's 4 mega-bit DRAMs. Process development towards further feature size minimization and also the incorporation of additional metalization levels is also underway.

Texas Instruments is well aware of the need for long term support of military programs. It is the intention of TI to support all semicustom products in their designed geometrics. Where this support is threatened by the obsolescence of a given process or set of design rules, TI would be capable of upgrading existing designs to the mainstream. An example of this is TI's ability to utilize a 3 micron standard cell data set for equivalent logical definition in either 2 or 1 micron.



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# TEXAS INSTRUMENTS 32-BIT PROCESSOR FAMILY

A new generation of 32-bit VLSI logic devices from Texas Instruments reflects the high degree of system integration made possible by continuing improvements in bipolar and CMOS process technologies. TI will offer nine integrated circuits, including the:

74ACT8832 32-bit registered ALU
74AS8833 64-bit to 32-bit funnel shifter
74AS8834 64-bit by 40-bit register file
74ACT8818 16-bit microsequencer
74ACT8836 32-bit multiplier
74ACT8837 64-bit floating point processor
74AS8838 32-bit barrel shifter.
74AS8839 32-bit shuffle/exchange network
74AS8840 Digital crossbar switch

All the devices except the barrel shifter are designed to support parity checking and generation, as well as master/slave error checking. Pin grid array package sizes range from 84-to 208-pins.

## TECHNOLOGY

Fabricated in 1-$\mu$m EPIC™ CMOS or IMPACT™ Bipolar technology, this chip set offers a combination of maximum integration and superior performance to the designer. Logic functions fabricated in EPIC technology can operate at clock frequencies up to 150 MHz. EPIC devices combine the performance associated with advanced bipolar processes with the low power consumption typical of CMOS.

In the past, the use of bipolar technology to achieve the complexities required by today's superminicomputer manufacturers was limited by the power dissipation required for high-speed operation.

TI has solved this problem, for the most part, by using a proprietary internal circuitry known as Schottky Transistor Logic (STL) which requires a 2-volt internal $V_{CC}$. Using two types of contact metallization on the same substrate to achieve a 300 mV noise margin, STL technology has allowed TI to offer VLSI bipolar products that operate at very low power levels.

## CHIP SET DEFINITION

TI's new 32-bit family has been designed to meet the following design criteria:

- 50-75 ns worst case cycle time
- 4 watts maximum power dissipation per package
- scientific accuracy (double precision floating point)
- no elaborate heat sinking required
- no glue logic required
- support 32-bit bus widths (address and data).

## TYPICAL APPLICATIONS

These design criteria result in a chip set that is well-suited to the following applications:

- Superminicomputers
- High resolution graphics
- Digital signal processing
- Array processors
- High end engineering workstations
- Artifical intelligence
- Fault tolerant computers.




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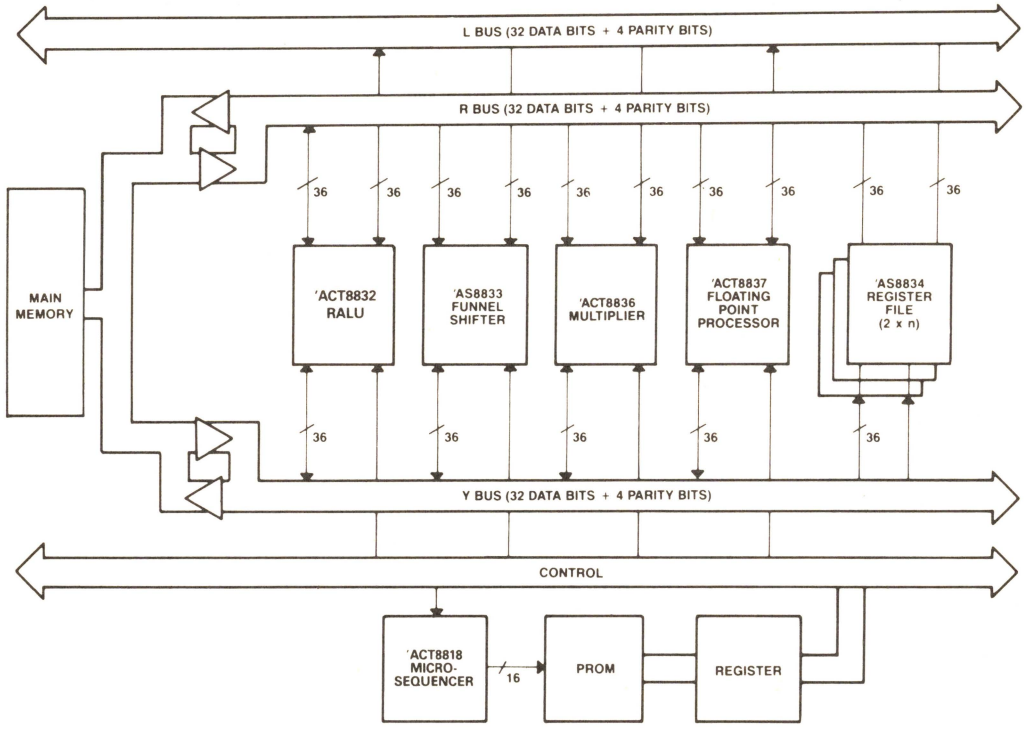
# TEXAS INSTRUMENTS 32-BIT PROCESSOR FAMILY




**VLSI 32-Bit Family**

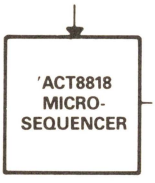
The 74ACT8832 is a 32-bit registered ALU that can be configured to operate as four 8-bit ALUs, two 16-bit ALUs, or a single 32-bit ALU. The device is 100% upwardly compatible with the 74AS888 bit-slice processor and includes a 64-word by 36-bit register file.

An 74AS8833 64-bit to 32-bit funnel shifter is provided separately from the RALU to increase overall system speed and offer the designer a high degree of flexibility and system parallelism.

The 74ACT8836, a 32-bit by 32-bit integer multiplier accumulator, can handle a wide variety of data types, including two's complement, signed and mixed. It can be configured for pipelined or flow-through operation.

The 74ACT8837 floating point processor is designed with 1-$\mu$m CMOS technology. It supports IEEE single and double precision floating point formats and can be configured for pipelined or flow-through operations.

An 74AS8834 64-word by 40-bit register file expands the internal register files of the 74AS8832. Four address ports operate independently to support most significant half and least significant half swap operations.




The 74ACT8818 16-bit microsequencer can address 64K of microcode memory. A 68-word by 20-bit push down stack permits address and status information to be stored during subroutine calls and interrupts.

# HIGH PERFORMANCE MICROPROGRAMMABLE BUILDING BLOCKS FROM TEXAS INSTRUMENTS

## 8 BIT-SLICE PROCESSOR FAMILY

| PINS/ PKG. | DEVICE TYPE | MAX POWER (W) | Tpd (ns) MAX | DESCRIPTION | AVAIL. |
|---|---|---|---|---|---|
| 68 | 74AS888 | 1.53 | 100 §¶ | 8-BIT REGISTERED ALU | NOW |
| 68 | 74AS888-1 | 1.53 | 87 §¶ | SPEED ENHANCED VERSION OF AS888 | NOW |
| 68 | 74AS887 | 1.53 | 75 § | NON-CASCADABLE 8-BIT REGISTERED ALU | NOW |
| 68 | 74AS890 | 1.82 | 76 § | 14-BIT MICROSEQUENCER | NOW |
| 68 | 74AS890-1 | 1.82 | 69 § | SPEED ENHANCED VERSION OF AS890 | NOW |
| 68 | 74AS895 | 1.53 | 87 § | 8-BIT MEMORY ADDRESS GENERATOR | NOW |
| 68 | 74AS897A | 0.85 | 33 | 16-BIT EXPANDABLE BARREL SHIFTER | NOW |
| 24/28 | 74AS870/871 | 1.05 | 15 | DUAL 16 X 4 REGISTER FILES | NOW |

## ECL 8 BIT-SLICE PROCESSOR FAMILY

| | | | | | |
|---|---|---|---|---|---|
| 84 | TIE10H888 | 5 | 20 § | AS888 10KH OUTPUTS | 3Q88 |
| 84 | TIE100888 | 5 | 20 § | AS888 100K OUTPUTS | 3Q88 |
| 84 | TIET888 # | 5 | 40 § | AS888 TTL OUTPUTS | 1Q88 |
| 84 | TIE10H890 | 5 | 16 § | AS890 10KH OUTPUTS | 2Q88 |
| 84 | TIE100890 | 5 | 16 § | AS890 100K OUTPUTS | 2Q88 |
| 84 | TIET890 # | 5 | 20 § | AS890 TTL OUTPUTS | 1Q88 |
| 84 | TIE10H897 | 2.5 | 8 | AS897 10KH OUTPUTS | 2Q88 |
| 84 | TIE100897 | 2.5 | 8 | AS897 100K OUTPUTS | 2Q88 |
| 84 | TIET897 # | 2.5 | 8 | AS897 TTL OUTPUTS | 1Q88 |

## 32 BIT PROCESSOR FAMILY

| | | | | | |
|---|---|---|---|---|---|
| 208 | 74ACT8832 # | 4 | 50 § | 32-BIT CMOS REGISTER ALU | 1Q88 |
| 156 | 74AS8833 | 4 | 50 § | 64-BIT TO 32-BIT FUNNEL SHIFTER | 2Q88 |
| 156 | 74AS8834 # | <4 | 20 | 64-WORD BY 40-BIT REGISTER FILE | 1Q88 |
| 156 | 74ACT8836 # | <1 | 35 ‡† | 32 X 32 BIT CMOS MULTIPLIER/ACCUMULATOR | 1Q88 |
| 208 | 74ACT8837 # | <1 | 50 | 64-BIT CMOS FLOATING POINT PROCESSOR | 1Q88 |
| 84 | 74AS8838 | <4 | 25 | 32-BIT BARREL SHIFTER | NOW |
| 85 | 74AS8839 | <4 | 25 | 32-BIT SHUFFEL EXCHANGE NETWORK | NOW |
| 156 | 74AS8840 | <4 | 25 | 16 PORT CROSSBAR SWITCH | NOW |

## 16-BIT CMOS PROCESSOR FAMILY

| | | | | | |
|---|---|---|---|---|---|
| 120 | ACT8816 | <1 | 45 | 16-BIT CMOS CASCADABLE 3-PORT REGISTERED ALU | 2Q88 |
| 84 | ACT8818 # | <1 | 45 | 1μm EPIC™ 16-BIT CMOS MICROSEQUENCER | 4Q87 |
| 52 | 74ACT29116-1 | 145mW | 85 § | 16-BIT MICROGRAMMABLE PROCESSOR | NOW |

## CMOS MULTIPLIERS

| | | | | | |
|---|---|---|---|---|---|
| 156 | ACT8836 | <1 | 35 †‡ | 32 X 32 BIT MULTIPLIER/ACCUMULATOR | 1Q88 |
| 208 | ACT8837 | <1 | 40 ‡ | 64-BIT FLOATING POINT PROCESSOR | 1Q88 |
| 64 | THCT1010-100 | 150mW | 100 † | 16 X 16 BIT MULTIPLIER/ACCUMULATOR | NOW |
| 64 | TACT1010-65 | 150mW | 65 † | 16 X 16 BIT MULTIPLIER/ACCUMULATOR | NOW |

† MULTIPLY/ACCUMULATE TIME
‡ INTERNAL PIPELINE MODE
§ MAXIMUM SYSTEM INSTRUCTION CYCLE TIME
¶ 16-BIT CONFIGURATION
# PROTOTYPE SAMPLES AVAILABLE

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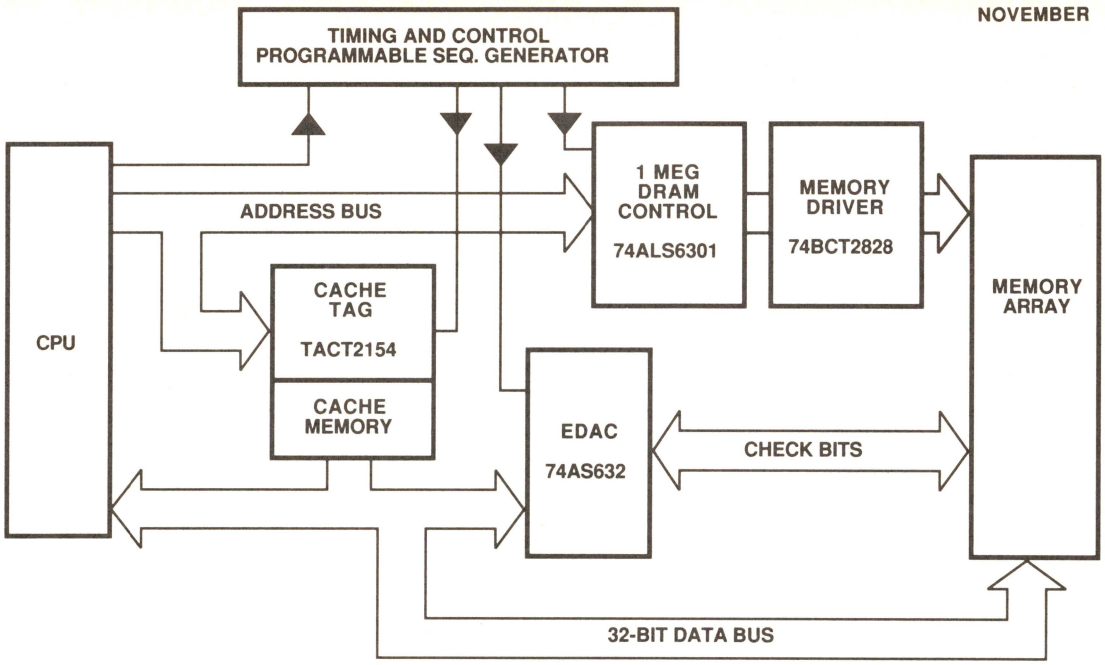
# MEMORY MANAGEMENT PRODUCTS FROM TEXAS INSTRUMENTS

NOVEMBER 1987




## DRAM CONTROLLERS
## PROVIDE ADDRESS MULTIPLEXING AND REFRESH CONTROL

| DIP PINS | DEVICE TYPE | Tpd (ns) MAX | FEATURES | AVAIL. |
|---|---|---|---|---|
| 40 | TMS4500A | 250 † | 64K DRAMS, ON-CHIP REFRESH TIMING CONTROL | NOW |
| 48 | THCT4502 | 125 † | 256K DRAMS, ON-CHIP REFRESH TIMING CONTROL | NOW |
| 48 | THCT4502B | 115 † | 256K DRAMS, ON-CHIP REFRESH TIMING CONTROL | NOW |
| 48 | 74ALS2967 | 35 † | 256K DRAMS, >200 TO 60 NS DRAMS, RASI, CASI | 4Q87 |
| 48 | 74ALS2968 | 35 † | 256K DRAMS, >200 TO 60 NS DRAMS, RASI, CASI | NOW |
| 52 | 74ALS6301 | 35 † | 1M-BIT DRAMS, >200 TO 60 NS DRAMS, RASI, CASI | NOW |
| 52 | 74ALS6302 | 35 † | 1M-BIT DRAMS, >200 TO 60 NS DRAMS, RASI, CASI | 4Q87 |

## CACHE ADDRESS COMPARATORS
## ON CHIP PARITY GENERATION AND CHECKING

| | | | | |
|---|---|---|---|---|
| 24 | TMS2150 | 35 ‡ | 512 X 8 CACHE TAG RAM | NOW |
| 24 | TACT2150 | 30/20 ‡ | 1 μm EPIC™, FASTEST AVAILABLE, 512 X 8 RAM | NOW |
| 28 | 74ACT2151¶ | 25/35 ‡ | 1K X 11 CACHE TAG RAM | 1Q88 |
| 28 | 74ACT2152 | 25/35 ‡ | 2K X 8 CACHE TAG RAM | NOW |
| 28 | 74ACT2153¶ | 25/35 ‡ | 1K X 11 RAM WITH OPEN DRAIN MATCH PIN | 1Q88 |
| 28 | 74ACT2154 | 25/35 ‡ | 2K X 8 RAM WITH OPEN DRAIN MATCH PIN | NOW |
| 48 | 74ACT2155 | 25/35 ‡ | 2K X 8 RAM 68030 CACHE TAG RAM | 1Q88 |
| 48 | 74ACT2158 | 25/35 ‡ | 8K X 9 CACHE TAG RAM | 1Q88 |
| 48 | 74ACT2159 | 25/35 ‡ | 8K X 9 RAM WITH OPEN DRAIN MATCH PIN | 1Q88 |

## ERROR DETECTION AND CORRECTION UNITS
## CORRECTS 1-BIT MEMORY ERRORS AND FLAGS 2-BIT ERRORS

| | | | | |
|---|---|---|---|---|
| 40 | 74ALS616 | 40 § | 16-BIT, 3-STATE | NOW |
| 40 | 74AS616 | 25 § | SPEED ENHANCED ALS616 | NOW |
| 28 | 74LS630 | 30 § | 16-BIT, NO BYTE-WRITE, 3-STATE | NOW |
| 28 | 74LS631 | 30 § | 16-BIT, NO BYTE-WRITE, OPEN COLLECTOR | NOW |
| 52 | 74ALS632A | 40 § | 32-BIT, 3-STATE | NOW |
| 52 | 74ALS632B | 30 § | SPEED ENHANCED ALS632A | NOW |
| 52 | 74AS632 | 25 § | FASTEST 32-BIT EDAC AVAILABLE | NOW |
| 48 | 74ALS634A | 40 § | 32-BIT, NO BYTE-WRITE, 3-STATE | NOW |
| 48 | 74AS634 | 25 § | SPEED ENHANCED ALS634 | NOW |

† MEMORY ACCESS TIME
‡ ADDRESS MATCH TIME
§ SINGLE BIT DETECTION TIME
¶ PROTOTYPE SAMPLES AVAILABLE

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## MEMORY MAPPERS
## PROVIDE PAGE MEMORY MAPPING

| DIP PINS | DEVICE TYPE | $T_{pd}$ (ns) MAX | FEATURES | AVAIL. |
|---|---|---|---|---|
| 40 | 74LS610 | 85 † | LATCHED, 3-STATE OUTPUTS | NOW |
| 40 | 74LS611 | 90 † | LATCHED, OPEN COLLECTOR OUTPUTS | NOW |
| 40 | 74LS612 | 85 † | 3-STATE OUTPUTS | NOW |
| 40 | 74LS613 | 90 † | OPEN COLLECTOR | NOW |

## MOS MEMORY DRIVERS WITH SERIES DAMPING RESISTORS

| | | | | |
|---|---|---|---|---|
| 20 | 74BCT2240 | 35 ‡ | BiCMOS OCTAL BUFFER/DRIVERS INVERTING 3-STATE | 4Q87 |
| 20 | 74BCT2241 | 35 ‡ | BiCMOS OCTAL LINE/MOS DRIVERS 3-STATE | 4Q87 |
| 20 | 74BCT2244 | 35 ‡ | BiCMOS OCTAL LINE/MOS DRIVERS 3-STATE | 4Q87 |
| 20 | 74BCT2540 | 35 ‡ | BiCMOS OCTAL BUFFER/DRIVERS INVERTING 3-STATE | 4Q87 |
| 20 | 74BCT2541 | 35 ‡ | BiCMOS OCTAL LINE/MOS DRIVERS 3-STATE | 4Q87 |
| 24 | 74BCT2827 | 12 ‡ | BiCMOS 10-BIT BUFFER/DRIVER 3-STATE | NOW |
| 24 | 74BCT2828 | 12 ‡ | BiCMOS 10-BIT BUFFER/DRIVER INVERTING 3-STATE | NOW |
| 20 | 74ALS2240 | 15 ‡ | OCTAL BUFFER/DRIVERS INVERTING 3-STATE | NOW |
| 14 | 74ALS2242 | 30 ‡ | QUAD BUS TRANSCEIVER/MOS DRIVER | NOW |
| 20 | 74ALS2244 | 30 ‡ | OCTAL BUFFER/DRIVERS INVERTING 3-STATE | 1Q88 |
| 20 | 74ALS2540 | 30 ‡ | OCTAL LINE/MOS DRIVERS 3-STATE | NOW |
| 20 | 74ALS2541 | 30 ‡ | OCTAL LINE/MOS DRIVERS 3-STATE | NOW |
| 20 | 74AS2620 | 30 ‡ | OCTAL BUS TRANSCEIVER/MOS DRIVER | NOW |
| 20 | 74AS2623 | 35 ‡ | OCTAL BUS TRANSCEIVER/MOS DRIVER | NOW |
| 20 | 74AS2640 | 35 ‡ | OCTAL BUS TRANSCEIVER/MOS DRIVER | NOW |
| 20 | 74AS2645 | 35 ‡ | OCTAL BUS TRANSCEIVER/MOS DRIVER | NOW |

† ADDRESS MATCH TIME
‡ Iol (mA)

## MEMORY MANAGEMENT DESIGN KIT

THIS KIT CONTAINS:
- SN74ACT2154 CACHE TAG, SN74AS632 EDAC, SN74ALS6301, DRAM CONTROLLER, SN74BCT2828, MEMORY DRIVER, TMS4464 256K MEMORY, 10ns PAL AND TIBPAL82S105B SEQUENCE GENERATOR SAMPLE DEVICES
- SUPPORTING DOCUMENTATION
- SCHEMATIC CAPTURE SOFTWARE FROM FUTURENET AND LOGIC AUTOMATION

ORDER PART NUMBER SN74MMDK01 $149.00 EACH

| SUPPORT DOCUMENTATION | LIT. ID # |
|---|---|
| MEMORY MANAGEMENT INFORMATION PACKET | SDVP039 |
| MEMORY MANAGEMENT APPLICATIONS BOOK | SDVA002A |
| • 4502 USER'S MANUAL | |
| • ALS2968/6301 APPLICATIONS NOTE | |
| • CACHE TAG ARTICLE REPRINTS | |
| • ALS632 APPLICATIONS REPORT | |
| • WHY USE AN EDAC? (APPLICATIONS BRIEF) | |
| LS630/631 APPLICATIONS REPORT | SDLA003 |
| LS610 THRU 613 APPLICATIONS NOTE | SDLA004 |
| LSI DATA BOOK | SDVD001 |
| ALS/AS DATA BOOK | SDAD001B |
| BIT SLICE FAMILY PRODUCTS APPLICATIONS NOTE | SDBA001 |
| BIT SLICE PRODUCT BULLETIN | SDBT001 |
| AS888/890 USER'S GUIDE | SDBU001A |
| AS897 USER'S GUIDE | SDBU003 |
| 32-BIT PROCESSOR FAMILY DESCRIPTION | SDBV001A |
| • 8832 PRODUCT DESCRIPTION | SDBV002 |
| • 8833 PRODUCT DESCRIPTION | SDBV003 |
| • 8834 & 8838 PRODUCT DESCRIPTION | SDBV004 |
| • 8835 PRODUCT DESCRIPTION | SDBV005 |
| • 8836 PRODUCT DESCRIPTION | SDBV006 |
| • 8837 PRODUCT DESCRIPTION | SDBV007 |
| • 8839 PRODUCT DESCRIPTION | SDBV009 |
| • 8840 PRODUCT DESCRIPTION | SDBV010 |
| 2 VOLT REGULATOR PRODUCT APPLICATIONS | SDBA002 |
| 74AS-EVM-8 BIT SLICE EVALUATION MODULE USER'S GUIDE | SDBU004 |

The following documents are in development. Contact the factory for availability.

- AS8840 Digital Crossbar Switch Application Brief
- High-performance Graphics Using the AS88XX Family, Application Brief
- FIR Implementation Using the 74ACT8836 32 x 32 MAC Application Note
- ACT8818 Data Manual
- ACT8832 Data Manual

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# FIFO MEMORY PRODUCTS FROM TEXAS INSTRUMENTS

## FIFO CROSS REFERENCE

| DIP PINS | DEVICE TYPE | DENSITY | fmax | DEPTH EXPANSION | AVAILABILITY | DEVICE TYPE | fmax | DEPTH EXPANSION |
|---|---|---|---|---|---|---|---|---|
| 20 | 74S225 | 16 X 5 | 10 | YES | NOW | MMI 74S225 † | 10 | YES |
| | | | | | | 74S225A † | 20 | YES |
| 20 | 74ALS229A | 16 X 5 | 30 | NO | NOW | ---- | ---- | ---- |
| 16 | 74ALS232A | 16 X 4 | 30 | NO | NOW | ---- | ---- | ---- |
| 20 | 74ALS233A | 16 X 5 | 30 | NO | NOW | ---- | ---- | ---- |
| 16 | 74ALS234 | 64 X 4 | 30 | YES | NOW | IDT IDT72403 | 25 | YES |
| | | | | | | CYPRESS CY7C403 | 25 | YES |
| 20 | 74ALS235 | 64 X 5 | 25 | YES | NOW | MMI 67413 | 25 | NO |
| | | | | | | 67413A | 30 | NO |
| 16 | 74ALS236 | 64 X 4 | 30 | YES | NOW | MMI 67401 | 10 | NO |
| | | | | | | 67401A | 15 | NO |
| | | | | | | 67401B | 16.7 | NO |
| | | | | | | C67401 † | 10 | YES |
| | | | | | | C67401A † | 15 | YES |
| | | | | | | C67401B † | 16.7 | YES |
| | | | | | | 67L401 † | 10 | YES |
| | | | | | | 67411 | 25 | NO |
| | | | | | | 67411A | 30 | NO |
| 24 | 74ALS2232 ‡ | 64 X 8 | 35 | NO | 1Q88 | MMI 67417 | 10 | NO |
| 28 | 74ALS2233 ‡ | 64 X 9 | 35 | NO | 1Q88 | ---- | ---- | ---- |
| 28 | 74ALS2234 ‡ | 64 X 9 | 35 | YES | 1Q88 | CYPRESS CYC409 | 35 | YES |
| 28 | 74ACT7202A ‡ | 1K X 9 | 25 | YES | 1Q88 | IDT IDT7202/A † | 20 | YES |

† PIN-FOR-PIN AND FUNCTIONALLY COMPATIBLE WITH TI DEVICE TYPE.
‡ PROTOTYPE SAMPLES AVAILABLE

## FIFOs OFFER DATA RATE MISMATCH SOLUTIONS

** In applications where data must be buffered between different speed peripherals or processors, the use of a FIFO queue will resolve the data rate mismatch problem.

** In buffering applications where the delay from input to output is not critical (i.e. CPU to printer) either a toggle or zero fall-through FIFO can be used. In this instance only the input and output clocking rates and the depth of the FIFO are critical.

** In buffering applications where the fall-through delays are important (i.e. bus interface), the zero fall-through architecture should be used.

Texas Instruments offers both zero and toggle fall-through FIFOs in various depths and widths. Capable of transfer rates from 10 to 40 MHz, both architectures can help you achieve your design goals. For example:

- The 24 ns typical fall-through time of TI's SN74ALS232A/233A/229A devices is a 50% improvement over other 16 x 4 and 16 x 5 FIFOs of this architecture and the Icc (max) for the 'ALS232A is 125 mA.
- TI's 'ALS234/5/6 and 'S225 Toggle Fall-through FIFOs offer the ability to be cascaded to create larger data buffers for continuous streams of data at rates of 10-30 MHz. Best of all, you pay no performance penalty when cascading the device.
- The SN74ALS2234 (64 x 9) Zero Fall-through FIFOs dual-port architecture allows high throughput (40 MHz) with no ripple delays.
- TI's EPIC™ CMOS SN74ACT7202 (1K x 9) Zero Fall-through FIFO, offers an access time of 35 ns at < 100 mA Icc at Fmax and 0 standby power.

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TEXAS INSTRUMENTS

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# 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2661, JANUARY 1986 – REVISED JUNE 1987

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability . . . 'AS632
- Dependable Texas Instruments Quality and Reliability

| DEVICE | PACKAGE | BYTE-WRITE | OUTPUT |
|---|---|---|---|
| 'AS632 | 52-pin | yes | 3-State |
| 'AS634 | 48-pin | no | 3-State |

## description

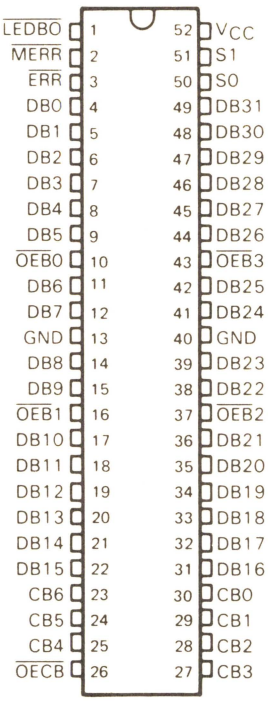
The 'AS632 and 'AS634 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('AS632) or 48-pin ('AS634) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

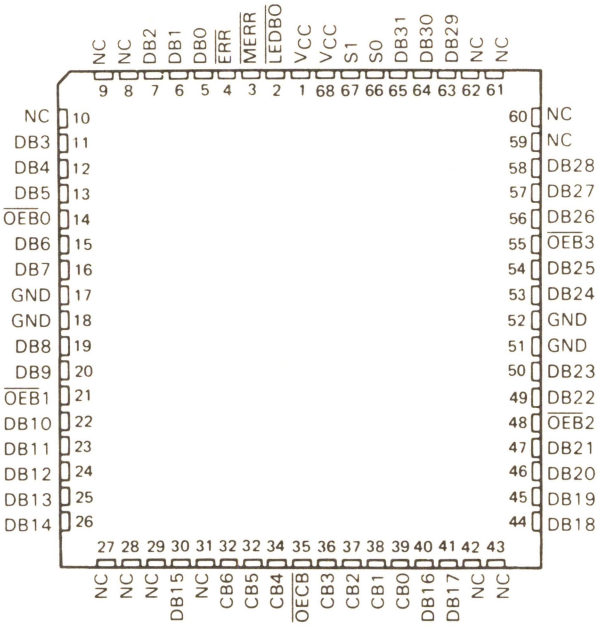
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

'AS632 . . . JD PACKAGE
(TOP VIEW)




'AS632 . . . FN PACKAGE
(TOP VIEW)




NC – No internal connection

For complete data sheet information call Texas Instruments at 1-800-232-3202.

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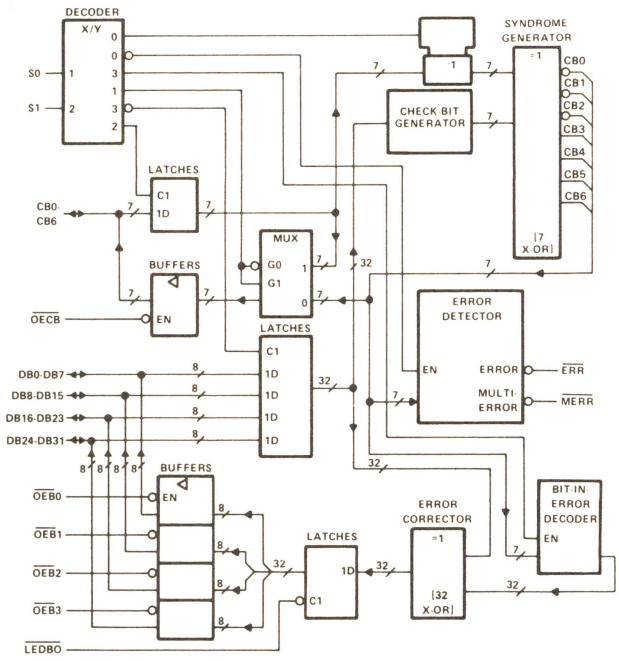
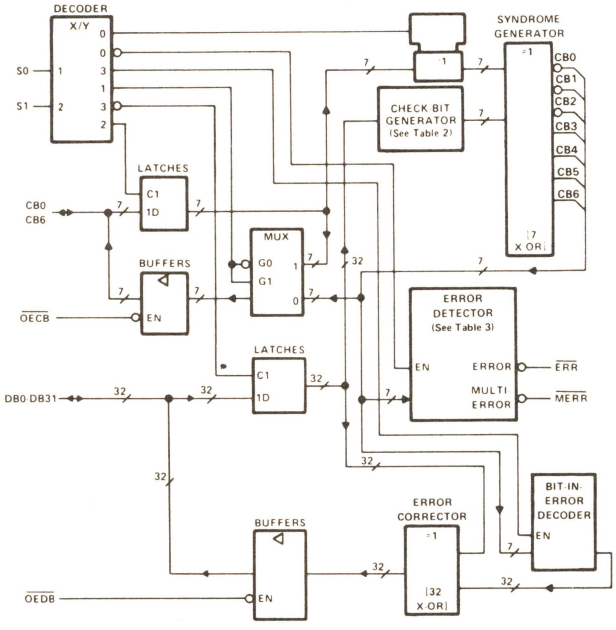
## 'AS632 logic diagram (positive logic)




## 'AS634 logic diagram (positive logic)

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D2900, JANUARY 1986—REVISED SEPTEMBER 1987

- **Provides Control for 16K, 64K, 256K, and 1M Dynamic RAMs**
- **Highest-Order Two-Address Bits Select One of Four Banks of RAMs**
- **Supports Scrubbing Operations and Nibble-Mode Access**
- **Separate Output Enable for Multi-Channel Access to Memory**
- **52-Pin Dual-In-Line Package**

## description

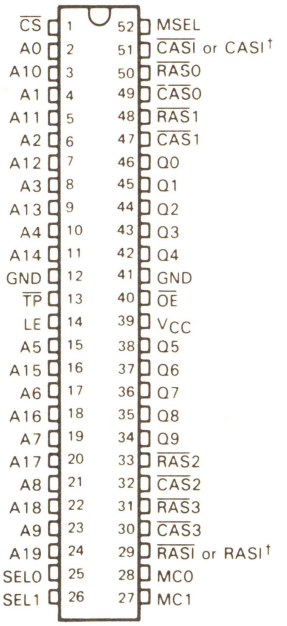
The 'ALS6301 and 'ALS6302 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS6301 offers active-low Row Address Strobe Input ($\overline{\text{RASI}}$) and Column Address Strobe Input ($\overline{\text{CASI}}$), while the 'ALS6302 offers active-high Row Address Strobe Input (RASI) and Column Address Strobe Input (CASI) inputs.

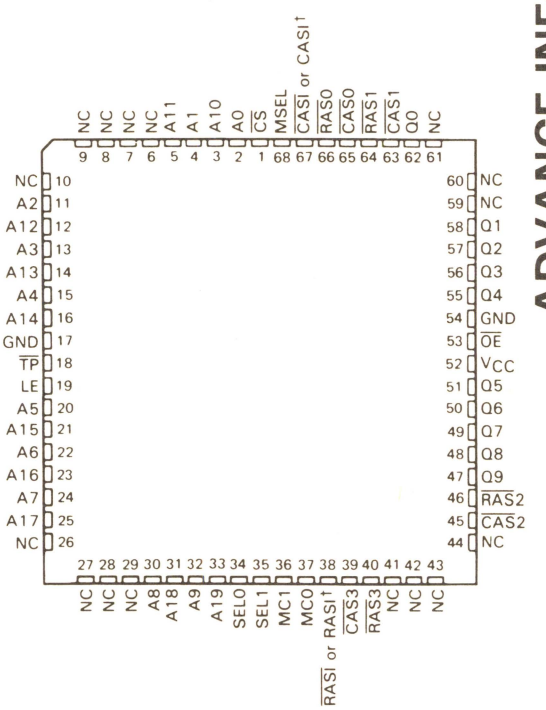
Using two 10-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 1M. These latches and the two row/column refresh address counters feed into a 10-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS6301 and 'ALS6302 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all $\overline{\text{RAS}}$ outputs will be active (low) while only one $\overline{\text{CAS}}$ output is active at a time.

**SN74ALS6301, SN74ALS6302 . . . JD OR N PACKAGE**
**(TOP VIEW)**




**SN74ALS6301, SN74ALS6302 . . . FN PACKAGE**
**(TOP VIEW)**




† 'ALS6301 has active-low inputs $\overline{\text{CASI}}$ and $\overline{\text{RASI}}$; 'ALS6302 has active-high inputs CASI and RASI.

The SN74ALS6301 and SN74ALS6302 are characterized for operation from 0°C to 70°C.

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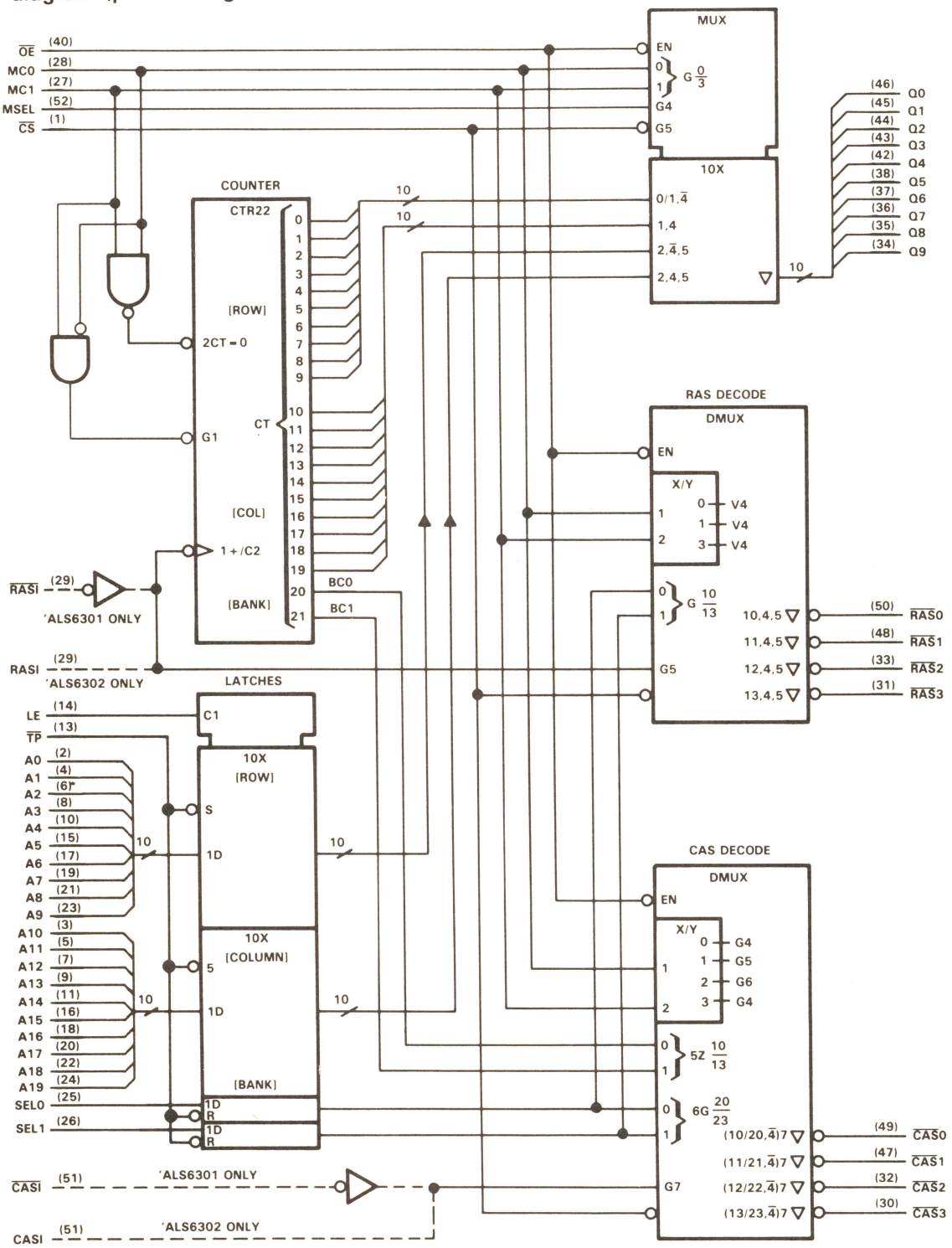
## logic diagram (positive logic)




Pin numbers shown are for JD and N packages.

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D2900, JANUARY 1986 – REVISED APRIL 1987

- **Provides Control for 16K, 64K, and 256K Dynamic RAMs**
- **Highest-Order Two-Address Bits Select One of Four Banks of RAMs**
- **Supports Scrubbing Operations and Nibble-Mode Access**
- **Separate Output Enable for Multi-Channel Access to Memory**
- **48-Pin Dual-In-Line Package**

## description

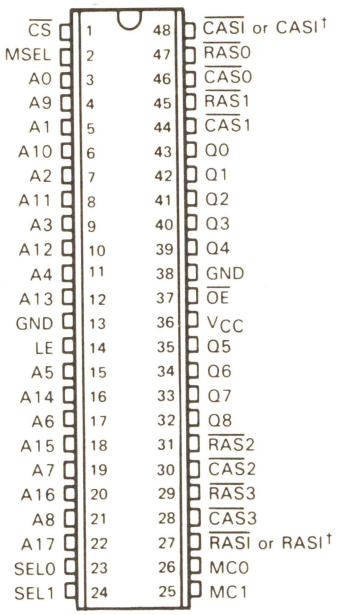
The 'ALS2967 and 'ALS2968 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS2967 offers active-low Row Address Strobe Input ($\overline{RASI}$) and Column Address Strobe Input ($\overline{CASI}$), while the 'ALS2968 offers active-high Row Address Strobe Input (RASI) and Column Address Strobe Input (CASI) inputs.

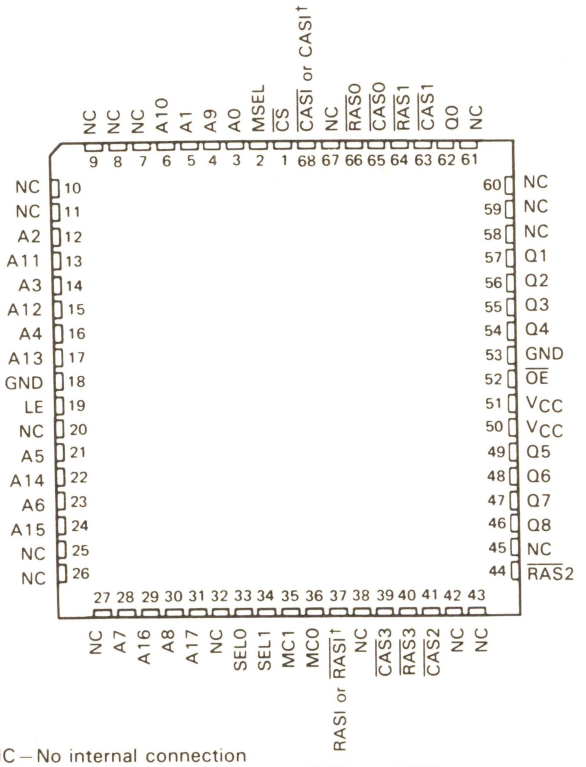
Using two 9-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 256K. These latches and the two row/column refresh address counters feed into a 9-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four $\overline{RAS}$ and $\overline{CAS}$ outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS2967 and 'ALS2968 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding $\overline{RAS}$ and $\overline{CAS}$ signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all $\overline{RAS}$ outputs will be active (low) while only one $\overline{CAS}$ output is active at a time.

**SN74ALS2967, SN74ALS2968 . . . JD OR N PACKAGE**
**(TOP VIEW)**




**SN74ALS2967, SN74ALS2968 . . . FN PACKAGE**
**(TOP VIEW)**




NC – No internal connection
† 'ALS2967 has active-low inputs $\overline{CASI}$ and $\overline{RASI}$; 'ALS2968 has active-high inputs CASI and RASI.

The SN74ALS2967 and SN74ALS2968 are characterized for operation from 0°C to 70°C.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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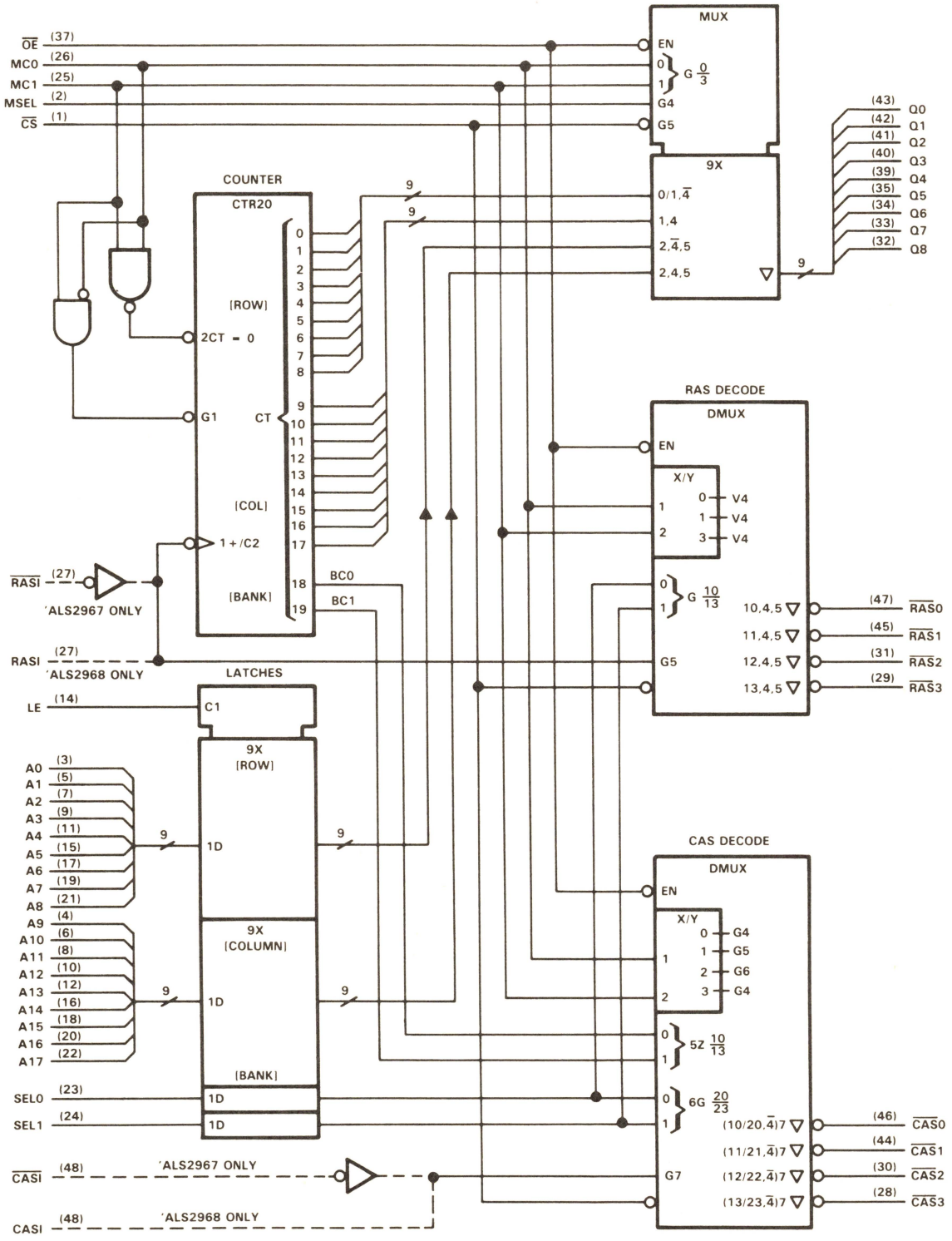
## logic diagram (positive logic)

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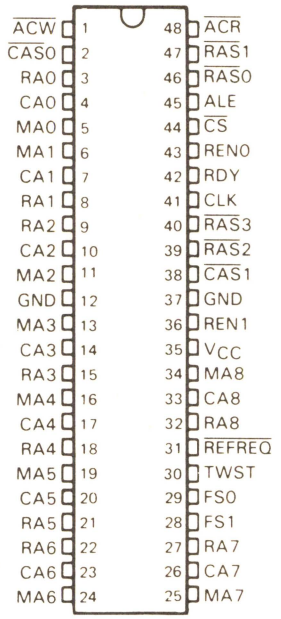
# THCT4502B
# DYNAMIC RAM CONTROLLER

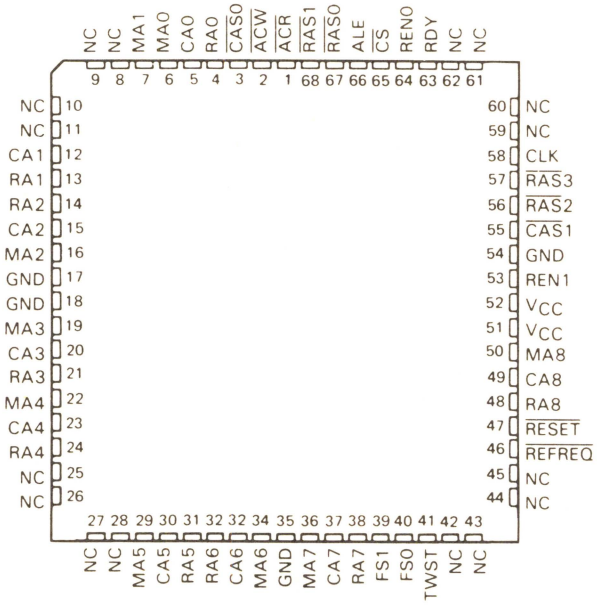
D2989, JUNE 1987

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K and 256K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 2 Megabytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
  - Asynchronous $\overline{\text{RESET}}$ Function Provided in FK and FN Packages
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range:
  115 ns ALE low to $\overline{\text{CAS}}$ low
- Functionally Equivalent to TMS4500A/B and to VTI VL4500A and VL4502
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

JD OR N PACKAGE
(TOP VIEW)




FK OR FN PACKAGE
(TOP VIEW)




NC – No internal connection

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# THCT4502B
# DYNAMIC RAM CONTROLLER

## description

The THCT4502B is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

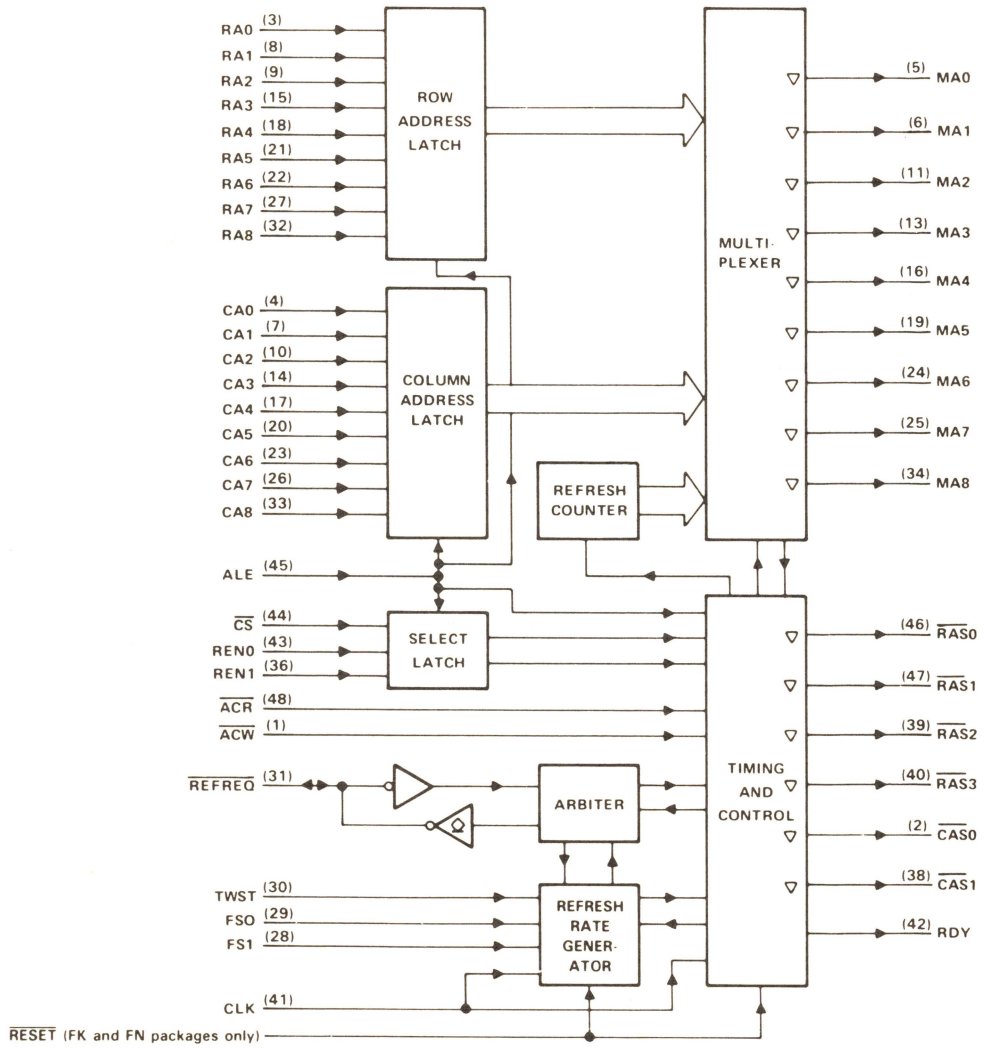
The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

A refresh timer is provided to generate the necessary timing to refresh the dynamic memories and ensure data retention.

The THCT4502B also contains refresh/access arbitration circuitry to resolve conflicts between access requests and memory-refresh cycles.

The THCT4502B is characterized for operation from 0°C to 70°C.

## functional block diagram

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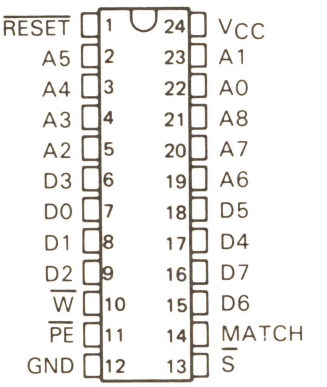
# TACT2150
# 512 × 8 CACHE ADDRESS COMPARATOR

D2993, JANUARY 1987—REVISED MAY 1987

- **Address to MATCH Valid Time**
  **TACT2150-20 . . . 20 ns max**
  **TACT2150-30 . . . 30 ns max**
- **300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages**
- **53 mA Typical Supply Current**
- **On-Chip Parity Generation and Checking**
- **Parity Error Output/Force Parity Error Input**
- **On-Chip Address/Data Comparator**
- **Asynchronous, Single-Cycle Reset**
- **Easily Expandable**
- **Fully Static**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

DW, JD, OR NT PACKAGE
(TOP VIEW)




## description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using Advanced CMOS technology for high-speed, low-power interface with bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be acheived with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 512 × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width.

The TACT2150 operates from a single 5 V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.



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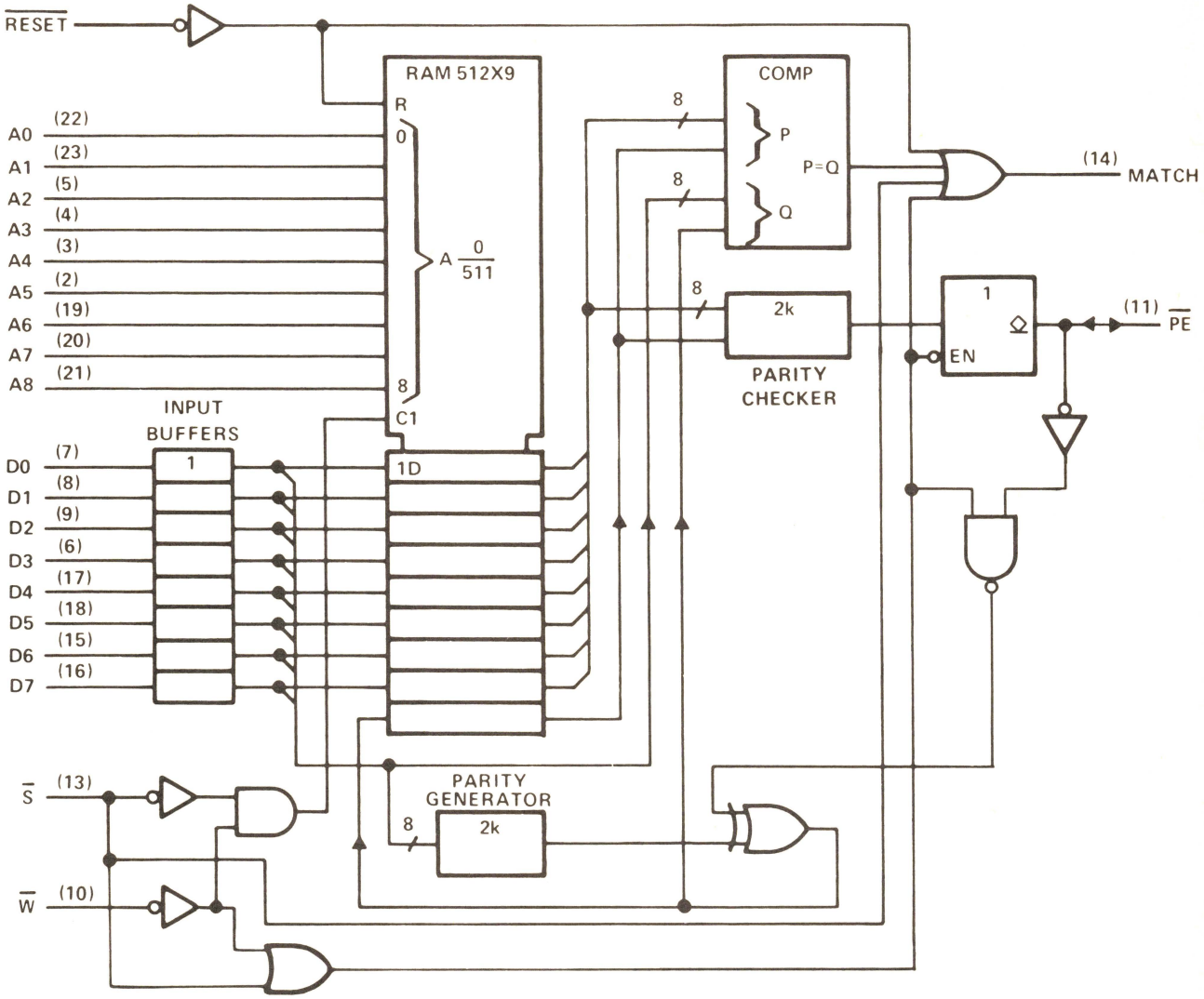
## functional block diagram (positive logic)




### MATCH OUTPUT DESCRIPTION

MATCH = $V_{OH}$ if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET} = V_{IL}$,
or: $\overline{S} = V_{IH}$,
or: $\overline{W} = V_{IL}$

MATCH = $V_{OL}$ if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET} = V_{IH}$,
$\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

### FUNCTION TABLE

| OUTPUT | | FUNCTION |
|---|---|---|
| MATCH | $\overline{PE}$ | DESCRIPTION |
| L | L | Parity Error |
| L | H | Not Equal |
| H | L | Undefined Error |
| H | H | Equal |

Where S = $V_{IL}$, W = $V_{IH}$, RESET = $V_{IH}$

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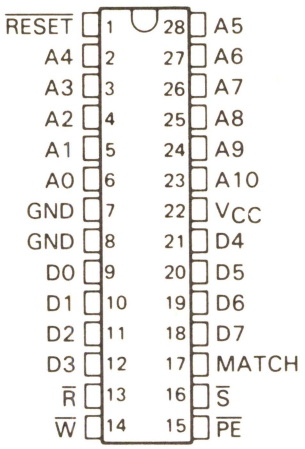
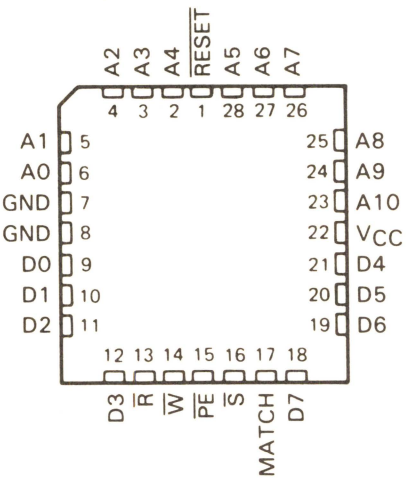
D3050, SEPTEMBER 1987

- Fast Address to Match Delay 25 or 35 ns Max
- Common I/O with Read Feature
- On-Chip Address/Data Comparator
- On-Chip Parity Generator and Checking
- Parity Error Output, Force Parity Error Input
- Easily Expandable
- Choice of Open-Drain or Totem-Pole MATCH Output
- EPIC™ (Enhanced Performance Implanted CMOS) 1-$\mu$m Process
- Fully TTL-Compatible

JD OR N PACKAGE
(TOP VIEW)




FN PACKAGE
(TOP VIEW)




## description

The 'ACT2152 and 'ACT2154 cache address comparators consist of a high-speed 2K × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2152 has a totem-pole MATCH output while the 'ACT2154 has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A10 with the data D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated odd parity are written in the 9-bit memory location addressed by A0-A10. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

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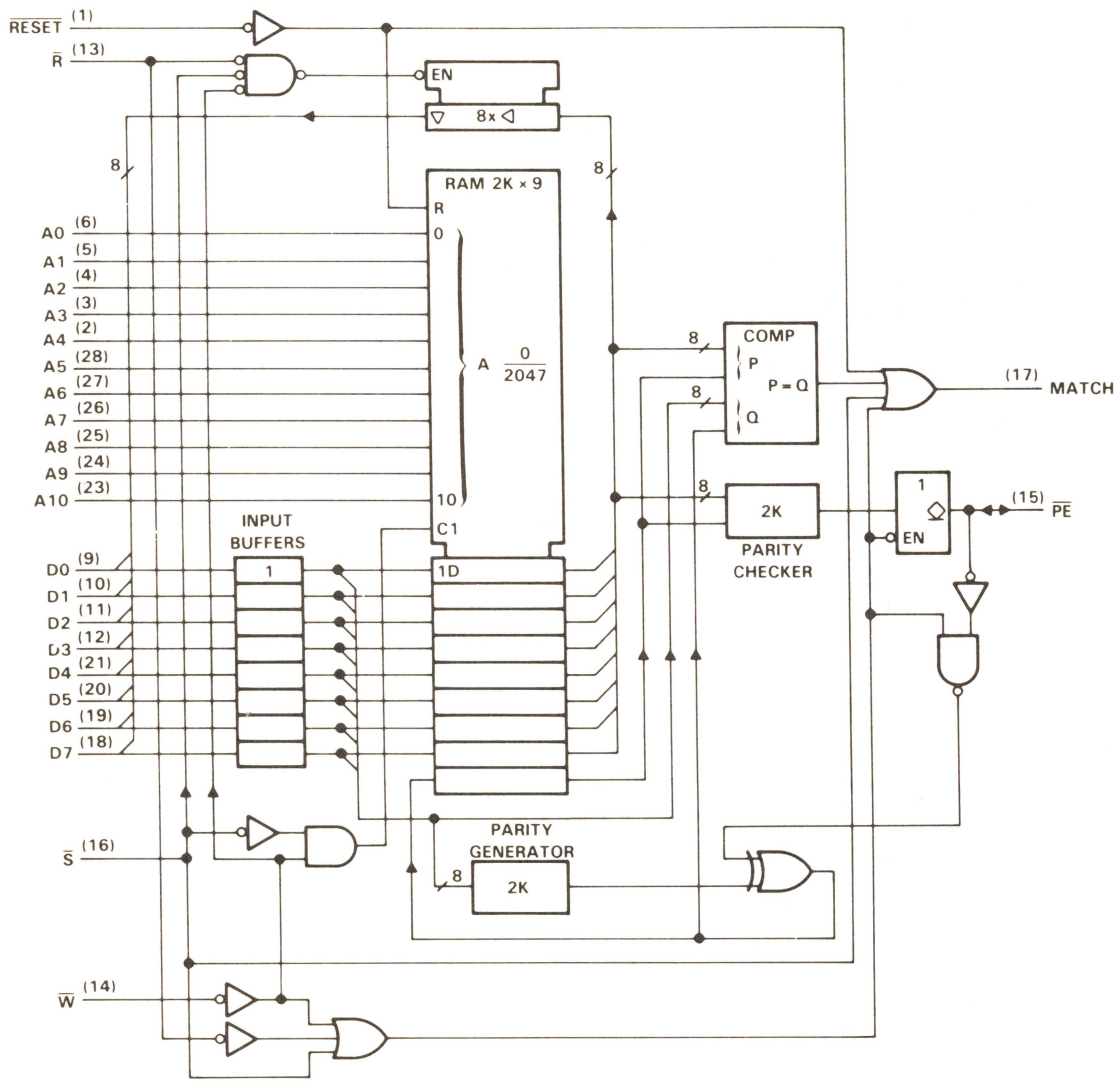
A read mode is provided with the 'ACT2152 and 'ACT2154, which allows the contents of RAM to be read at the D0-D7 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low, and $\overline{W}$ is high.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 2K × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

These cache address comparators operate from a single +5-V supply and are offered in 28-pin 600-mil ceramic side-brazed, plastic dual-in-line, or PLCC packages.

The 'ACT2152 and 'ACT2154 are characterized for operation from 0°C to 70°C.

**functional block diagram (positive logic)**

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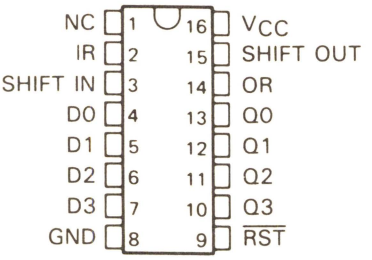
# SN54ALS236, SN74ALS236
# 64 × 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

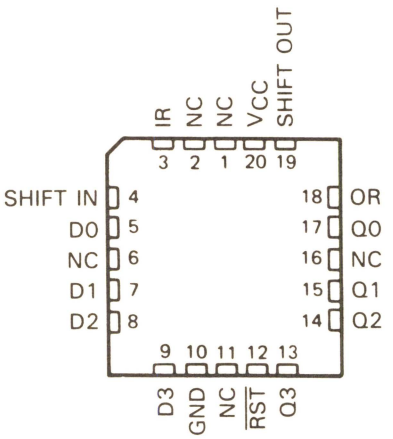
D2958, OCTOBER 1986

- **Asynchronous Operation**
- **Organized as 64 Words of 4 Bits**
- **Data Rates from 0 to 30 MHz**
- **Pin-Compatible with MMI67401B with Higher Speed**
- **Dependable Texas Instruments Quality and Reliability**

**SN54ALS236 . . . J PACKAGE**
**SN74ALS236 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54ALS236 . . . FK PACKAGE**
**SN74ALS236. . . FN PACKAGE**
**(TOP VIEW)**




NC – No internal connection.

## description

The SN54ALS236 and SN74ALS236 are 256-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS236 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low

Status of the 'ALS236 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

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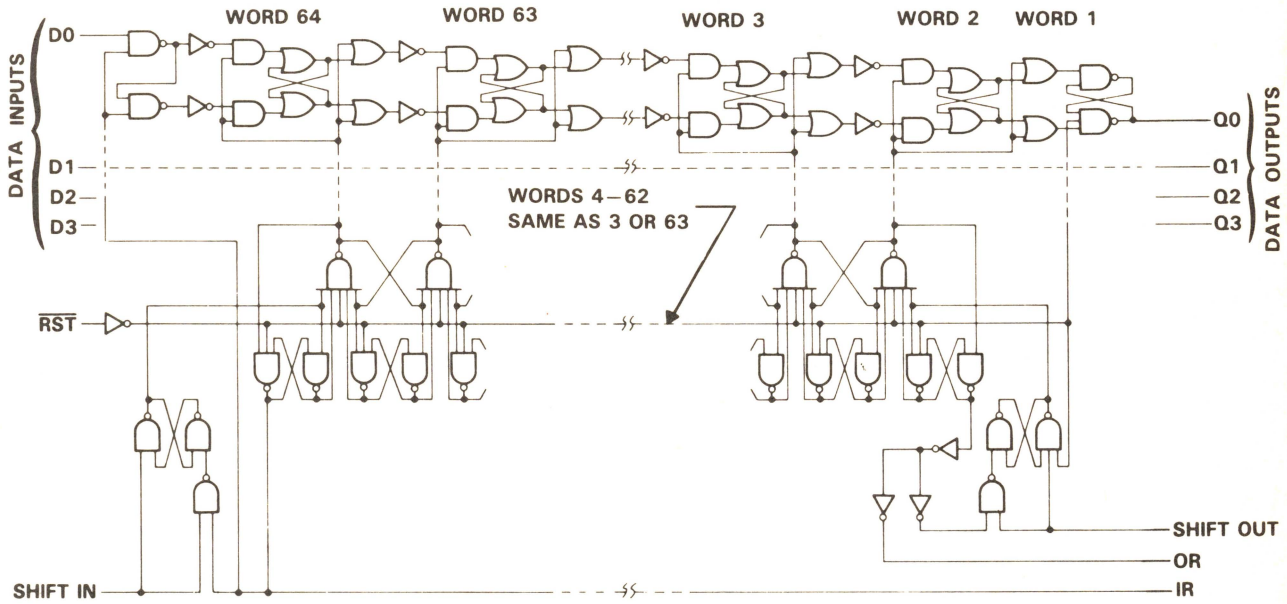
## description (continued)

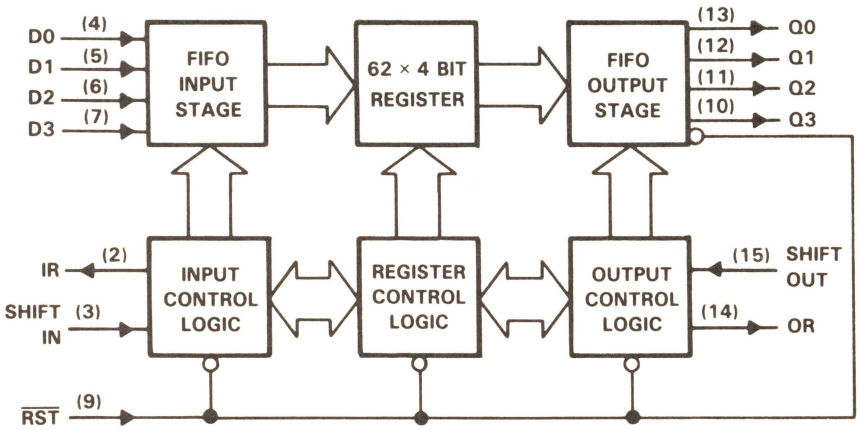
The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs.

The SN54ALS236 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS236 is characterized for operation from 0°C to 70°C.

## logic diagram (positive logic)




## functional block diagram




Pin numbers shown are for D, J, and N packages.

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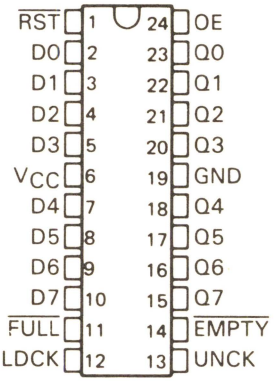
# SN54ALS2232, SN74ALS2232
# 64 × 8 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

OCTOBER 1987

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 8 Bits Each**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typ**
- **3-State Outputs**

**SN54ALS2232 . . . JD PACKAGE**
**SN74ALS2232 . . . DW OR NT PACKAGE**
**(TOP VIEW)**




For chip carrier information contact the factory

## description

These 512-bit memories use Advanced Low-Power Schottky IMPACT-X™ technology and feature high speed and fast fall through times. They are organized as 64 words by 8 bits each.

A FIFO memory is a storage device that allows data to be written into independent data rates. These FIFOs are designed to process data at rates from 0 to 40 megahertz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

A low level on the reset input ($\overline{RST}$) resets the internal stack control pointers and also sets $\overline{EMPTY}$ low and sets $\overline{FULL}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{RST}$ pulse or from an empty condition, will cause $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the $\overline{FULL}$ or $\overline{EMPTY}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

Status of the FIFO memory is monitored by the $\overline{FULL}$ and $\overline{EMPTY}$ output flags. The $\overline{FULL}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{EMPTY}$ output will be low when the memory is empty, and high when it is not empty.

The SN54ALS2232 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS2232 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

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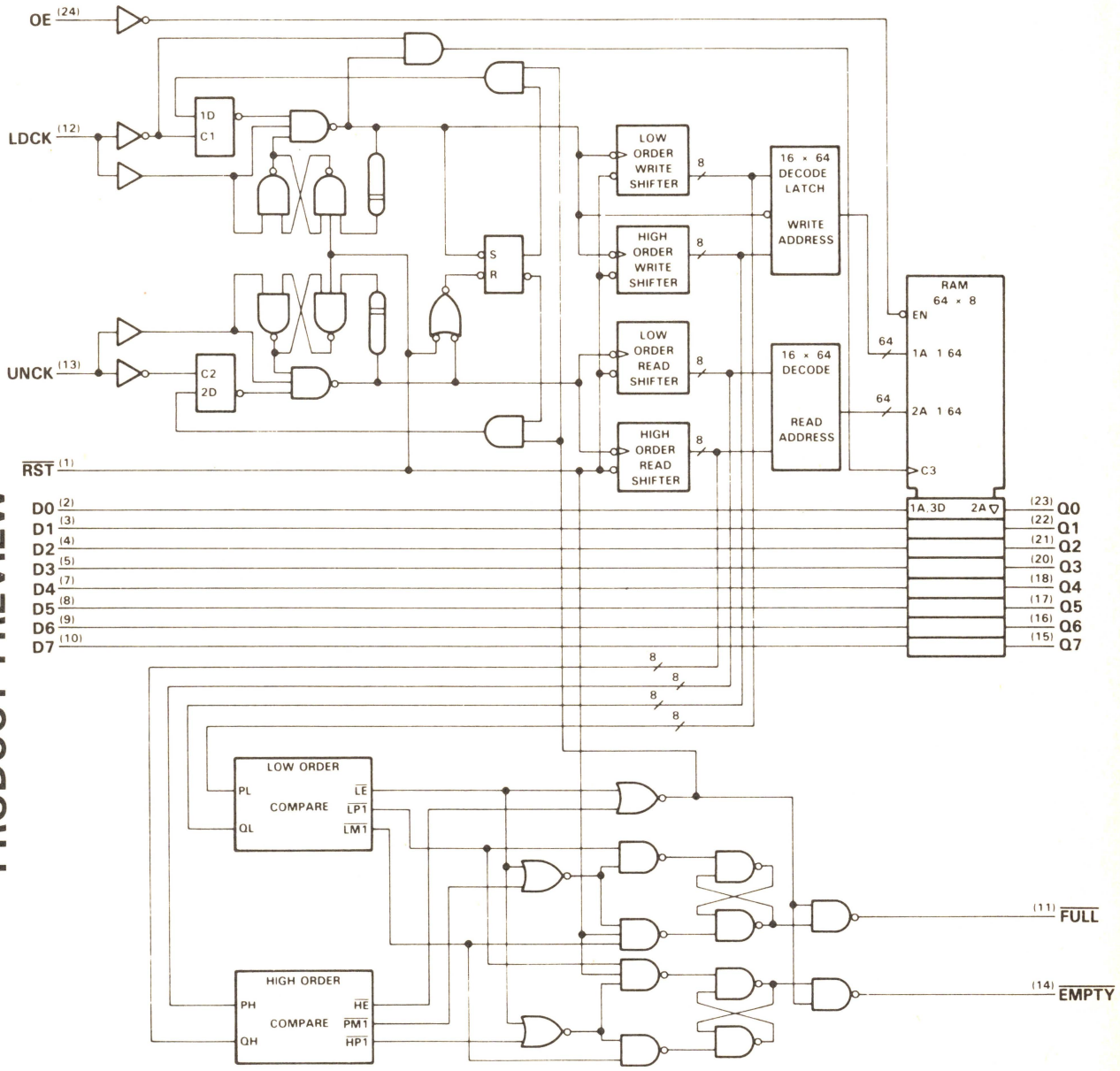
## logic diagram (positive logic)

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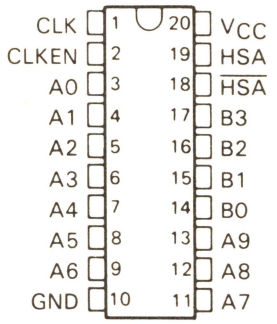
# SN54ALS6310, SN54ALS6311, SN74ALS6310, SN74ALS6311
# STATIC COLUMN AND PAGE-MODE ACCESS DETECTORS

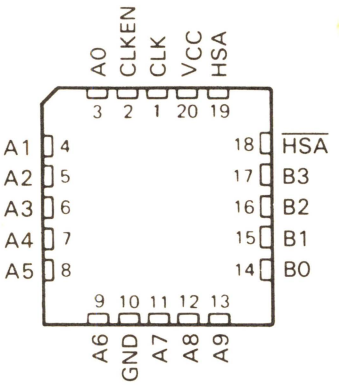
D3020, JUNE 1987

- **Detects Present Row Equal to Last Row Address**
- **High-Performance Compare:**
  **'ALS6310 CLK to HSA = XX ns**
  **'ALS6311 Address to HSA = XX ns**
- **Compatible with 16K to 1M DRAMs**
- **Easily Interfaced with Microprocessor and Memory Timing Controller**
- **Dependable Texas Instruments Quality and Reliability**

**SN54ALS' . . . J PACKAGE**
**SN74ALS' . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54ALS' . . . FK PACKAGE**
**SN74ALS' . . . FN PACKAGE**
**(TOP VIEW)**




## description

The 'ALS6310 and 'ALS6311 are high-performance address comparators designed for implementing static column and page-mode access cycles.

When interfaced with the memory timing controller, these devices will detect if the present row being accessed is the same as the last row accessed. This is the fundamental requirement for implementing static column decode or page-mode access cycles.

The 'ALS6310 features two 14-bit registers and a high-speed address comparator. The first register is used to save the present row address while the second register is used to save the previous row address. On the high-to-low transition of CLK, the first register loads the new row address present on A0-A9. At the same time, the second register loads the address previously saved in the first register. The two row addresses are then compared. The High-Speed Access outputs (HSA and $\overline{\text{HSA}}$) will signal if the two addresses are equal.

The B0-B1 inputs are provided to monitor access cycles to different banks of memory. When used in conjunction with the 'ALS2968 and 'ALS6302 series DRAM controllers, the 'ALS6310 and 'ALS6311 can monitor up to 16 banks of memory. The CLK input on the 'ALS6310 can typically be interfaced with the microprocessor's Address Latch Enable (ALE) or Address Strobe (AS) outputs. This configuration simplifies the memory timing controller interface. Refer to the typical application diagram for further information.

The 'ALS6311 features one 14-bit register feeding a high-speed address comparator. This architecture offers a faster address match time, but does require the memory timing controller to generate the CLK input. Typically, the 14-bit register would only be updated if there was a change in row or bank address. Refer to the application diagram for further information.

More information on static column DRAM access can be found in the Texas Instruments application report *System Solutions for Static Column Decode*.

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PRODUCT PREVIEW

For complete data sheet information call Texas Instruments at 1-800-232-3202.

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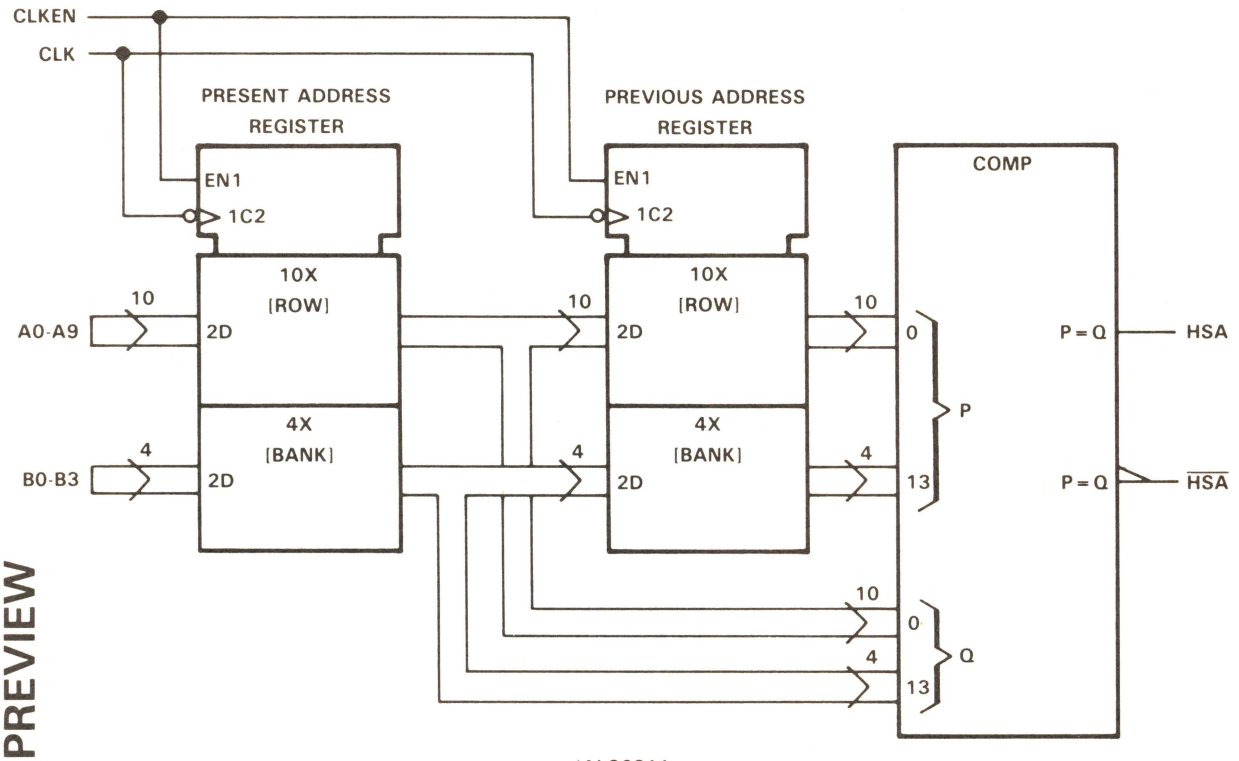
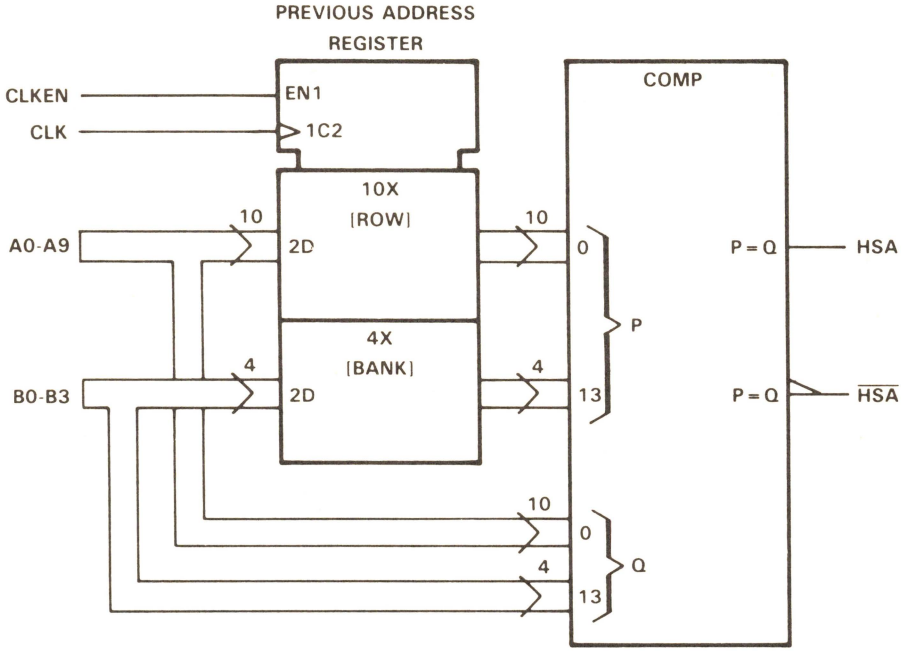
## logic diagrams (positive logic)

'ALS6310




'ALS6311

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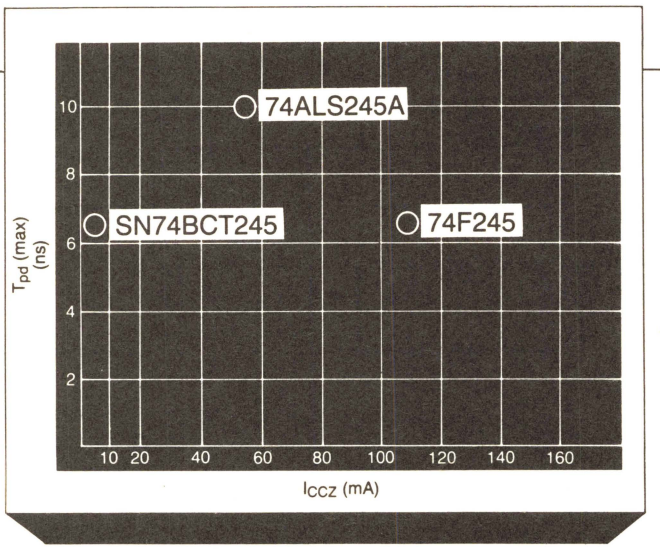
# TEXAS INSTRUMENTS BiCMOS BUS INTERFACE

## OVERVIEW

Texas Instruments new BiCMOS bus interface family is now available to reduce your system's power consumption up to 25% while maintaining advanced speed and output drive.

Fabricated in TI's BiCMOS process, which combines the best of bipolar and CMOS technologies, TI's new bus interface devices have switching speeds comparable to advanced bipolar products and provide the 48/64 mA drive current needed for high capacitive loads and backplanes. In addition, TI's BiCMOS devices can reduce disable supply currents by 95%, and typically reduce active currents by 50-80% over their bipolar equivalents. The comparison below of TI's new BiCMOS devices with existing technologies demonstrates the potential savings. The result can be a total system IC power savings of more than 25%.

Designated SN74BCT, TI's BiCMOS bus interface family comprises 44 popular bus interface functions, including 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers, allowing for easy plug-in upgrades. These devices give you a simple means to rid your system of power waste without compromising advanced performance.




*BiCMOS provides advanced bipolar speed with low CMOS power.*

## BiCMOS FEATURES AND BENEFITS

| FEATURE | BENEFIT |
|---|---|
| • Advanced bipolar performance | • Supports 25-30 MHz bus cycle times |
| • 48/64 mA output drive current | • Drives high capacitive loads and backplanes |
| • Low power consumption | • Up to 95% power savings over advanced bipolar devices |
| • Offered with popular industry-standard functions | • Easy to implement for plug-in upgrades |

**'863 9-bit Transceiver**

| | $I_{CC}$ max (mA) | |
|---|---|---|
| | Enabled | Disabled |
| SN74BCT29863 | 30 | 7 |
| AM29863* | 160 | 160 |
| 74F863† | 145 | 155 |
| Current Reduction | 71-81% | 95-96% |

**'827 10-bit Buffer/Driver**

| | $I_{CC}$ max (mA) | |
|---|---|---|
| | Enabled | Disabled |
| SN74BCT29827 | 40 | 5 |
| AM29827* | 80 | 80 |
| 74F827† | 90 | 90 |
| Current Reduction | 50-56% | 94% |

*1985 Advanced Micro Devices Bipolar Microprocessor Logic and Interface Databook
†1986 Signetics FAST Data Manual

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# BiCMOS™
# PRODUCT INDEX

| DEVICE | FUNCTION | TYPICAL | |
|---|---|---|---|
| | | $I_{CC}$ | $I_{CCZ}$ |
| 74BCT240 | Octal Bus Driver | 53 † | 4 † |
| 74BCT241 | Octal Bus Driver | 53 | 4 |
| 74BCT244 | Octal Bus Driver | 53 | 4 |
| 74BCT245 | Octal Bus Transceiver | 53 † | 4 † |
| 74BCT2240 | Octal Bus Driver with series damping resistor | 53 † | 4 † |
| 74BCT2241 | Octal Bus Driver with series damping resistor | 53 † | 4 † |
| 74BCT2244 | Octal Bus Driver with series damping resistor | 53 † | 4 † |
| 74BCT299 | 8-Bit Universal Shift/Storage Register | 50 † | 4 † |
| 74BCT323 | 8-Bit Universal Shift/Storage Register | 50 † | 4 † |
| 74BCT373 | Octal D-type Latch | 50 † | 4 † |
| 74BCT374 | Octal D-type Flip-Flop | 50 † | 4 † |
| 74BCT533 | Octal D-type Latch | 50 † | 4 † |
| 74BCT534 | Octal D-type Flip-Flop | 50 † | 4 † |
| 74BCT540 | Octal Bus Driver (flow through) | 50 † | 4 † |
| 74BCT541 | Octal Bus Driver (flow through) | 50 † | 4 † |
| 74BCT543 | Octal Registered Transceiver | 50 † | 4 † |
| 74BCT544 | Octal Registered Transceiver | 50 † | 4 † |
| 74BCT573 | Octal D-type Flip-Flop (flow through) | 53 † | 4 † |
| 74BCT574 | Octal D-type Flip-Flop (flow through) | 53 † | 4 † |
| 74BCT620 | Octal Bus Transceiver | 53 † | 4 † |
| 74BCT623 | Octal Bus Transceiver | 53 † | 4 † |
| 74BCT640 | Octal Bus Transceiver | 53 † | 4 † |
| 74BCT646 | Octal Registered Bus Transceiver | 50 † | 4 † |
| 74BCT648 | Octal Registered Bus Transceiver | 50 † | 4 † |
| 74BCT651 | Octal Registered Bus Transceiver | 50 † | 4 † |
| 74BCT652 | Octal Registered Bus Transceiver | 50 † | 4 † |
| 74BCT29818 | Pipeline Register | 40 † | 4 † |
| 74BCT819 | Pipeline Register | 40 † | 4 † |
| 74BCT29821 | 10-Bit D-type Flip-Flop | 30 † | 3 † |
| 74BCT29822 | 10-Bit D-type Flip-Flop | 30 † | 3 † |
| 74BCT29823 | 9-Bit Register | 30 † | 3 † |
| 74BCT29824 | 9-Bit Register | 30 † | 3 † |
| 74BCT29825 | 8-Bit Register | 30 † | 3 † |
| 74BCT29826 | 8-Bit Register | 30 † | 3 † |
| 74BCT29827 | 10-Bit Buffer | 28 | 2.2 |
| 74BCT29828 | 10-Bit Buffer | 28 | 2.2 |
| 74BCT2827 | 10-Bit Buffer with series damping resistor | 28 | 2.2 |
| 74BCT2828 | 10-Bit Buffer with series damping resistor | 28 | 2.2 |
| 74BCT29833 | Registered Transceiver | 55 | 30 |
| 74BCT29834 | Registered Transceiver | 55 | 30 |
| 74BCT29841 | 10-Bit D-type Latch | 30 † | 3 † |
| 74BCT29842 | 10-Bit D-type Latch | 30 † | 3 † |
| 74BCT29843 | 9-Bit Latch | 30 † | 3 † |
| 74BCT29844 | 9-Bit Latch | 30 † | 3 † |
| 74BCT29845 | 8-Bit Latch | 30 † | 3 † |
| 74BCT29846 | 8-Bit Latch | 30 † | 3 † |
| 74BCT29853 | Latched Transceiver | 55 | 30 |
| 74BCT29854 | Latched Transceiver | 55 | 30 |
| 74BCT29861 | 10-Bit Transceiver | 22 | 4.5 |

† Preliminary data

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| DEVICE | FUNCTION | TYPICAL | |
|---|---|---|---|
| | | $I_{CC}$ | $I_{CCZ}$ |
| 74BCT29862 | 10-Bit Transceiver | 22 † | 4.5 † |
| 74BCT29863 | 9-Bit Transceiver | 22 | 4.5 |
| 74BCT29864 | 9-Bit Transceiver | 22 † | 4.5 † |
| 74ABCT11240 | Octal Bus Driver | 53 † | 4 † |
| 74ABCT11241 | Octal Bus Driver | 53 † | 4 † |
| 74ABCT11244 | Octal Bus Driver | 53 † | 4 † |
| 74ABCT11245 | Octal Bus Transceiver | 53 † | 4 † |
| 74ABCT11299 | 8-Bit Universal Shift/Storage Register | 50 † | 4 † |
| 74ABCT11323 | 8-Bit Universal Shift/Storage Register | 50 † | 4 † |
| 74ABCT11373 | Octal D-type Latch | 50 † | 4 † |
| 74ABCT11374 | Octal D-type Flip-Flop | 50 † | 4 † |
| 74ABCT11533 | Octal D-type Latch | 50 † | 4 † |
| 74ABCT11534 | Octal D-type Flip-Flop | 50 † | 4 † |
| 74ABCT11543 | Octal Registered Transceiver | 50 † | 4 † |
| 74ABCT11544 | Octal Registered Transceiver | 50 † | 4 † |
| 74ABCT11620 | Octal Bus Transceiver | 53 † | 4 † |
| 74ABCT11623 | Octal Bus Transceiver | 53 † | 4 † |
| 74ABCT11646 | Octal Registered Bus Transceiver | 50 † | 4 † |
| 74ABCT11648 | Octal Registered Bus Transceiver | 50 † | 4 † |
| 74ABCT11651 | Octal Registered Bus Transceiver | 50 † | 4 † |
| 74ABCT11652 | Octal Registered Bus Transceiver | 50 † | 4 † |
| 74ABCT11821 | 10-Bit Register | 30 † | 3 † |
| 74ABCT11822 | 10-Bit Register | 30 † | 3 † |
| 74ABCT11823 | 9-Bit Register | 30 † | 3 † |
| 74ABCT11824 | 9-Bit Register | 30 † | 3 † |
| 74ABCT11825 | 8-Bit Register | 30 † | 3 † |
| 74ABCT11826 | 8-Bit Register | 30 † | 3 † |
| 74ABCT11841 | 10-Bit Latch | 30 † | 3 † |
| 74ABCT11842 | 10-Bit Latch | 30 † | 3 † |
| 74ABCT11843 | 9-Bit Latch | 30 † | 3 † |
| 74ABCT11844 | 9-Bit Latch | 30 † | 3 † |
| 74ABCT11845 | 8-Bit Latch | 30 † | 3 † |
| 74ABCT11846 | 8-Bit Latch | 30 † | 3 † |

† Preliminary data

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# TEXAS INSTRUMENTS EPIC™ ACL

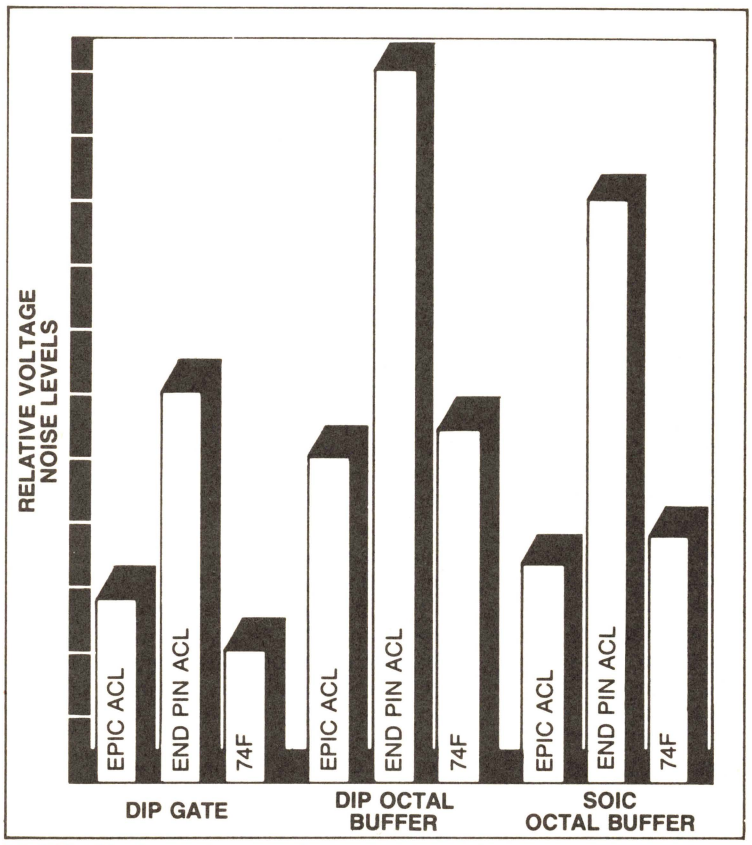
## OVERVIEW

Texas Instruments offers the first advanced CMOS logic (ACL) family designed to improve system performance while reducing simultaneous switching noise. TI's EPIC™ ACL not only provides advanced speed, high drive, and low CMOS power consumption, but gives you reliable system-level operation as well.

Designated 54/74AC/ACT, components in the new EPIC ACL family have speeds comparable to advanced bipolar 74F. In addition, EPIC ACL provides 24 mA of sink/source current to drive 50-ohm transmission lines. Along with the traditional low power consumption of CMOS, TI's EPIC ACL devices feature flow-through architecture to simplify board layout.

Innovative packaging and design allow EPIC ACL to provide all this performance and still reduce noise levels by more than 50% over conventionally-packaged ACL. EPIC ACL noise levels are even less than those of advanced bipolar products.

A wide variety of traditionally bipolar logic applications will benefit from the more than 100 EPIC ACL functions. All functions are offered with both CMOS (74AC) and TTL (74ACT) level inputs, and alternate sourcing of the entire family is provided by co-developer Philips/Signetics. TI's EPIC ACL family will extend the applications of CMOS technology to such traditionally advanced bipolar markets as office automation systems, computer peripherals, mini-/personal computers, and telecommunications systems.




*TI's EPIC ACL reduces simultaneous switching noise levels by more than 50% over conventional ACL and still provides advanced speed, high drive, and low CMOS power consumption. EPIC ACL noise levels are even 10% below those associated with bipolar devices.*

| FEATURES | BENEFITS |
|---|---|
| • OEC™ (Output Edge Control) and center-pin design | • Reduced simultaneous switching noise and a "flow through" pinout structure for easier design |
| • Performance comparable to advanced bipolar 74F | • Improved throughput without power penalty |
| • Low CMOS power consumption (essentially zero standby) | • Minimum system power required |
| • 24-mA sink/source currents | • High drive capability (50-ohm transmission line) |
| • 'AC and 'ACT options | • CMOS and TTL interface capability |
| • High-frequency operation (to 150 MHz) | • 3X improvement over HCMOS |
| • DIP and SOIC package offerings | • Flexibility of design across product family |

# EPIC™ ACL
# PRODUCT INDEX

| DEVICE | FUNCTION |
|---|---|
| 74AC/ACT11000 | Quad 2-input NAND Gate |
| 74AC/ACT11002 | Quad 2-input NOR Gate |
| 74AC/ACT11004 | Hex Inverter |
| 74AC/ACT11008 | Quad 2-input AND Gate |
| 74AC/ACT11010 | Triple 3-input NAND Gate |
| 74AC/ACT11011 | Triple 3-input AND Gate |
| 74AC/ACT11013 | Dual 4-input NAND Schmitt-Trigger |
| 74AC/ACT11014 | Hex Schmitt-Trigger Inverter |
| 74AC/ACT11020 | Dual 4-input NAND Gate |
| 74AC/ACT11021 | Dual 4-input AND Gate |
| 74AC/ACT11027 | Triple 3-input NOR Gate |
| 74AC/ACT11030 | 8-input NAND Gate |
| 74AC/ACT11032 | Quad 2-input OR Gate |
| 74AC/ACT11034 | Hex Non-inverter |
| 74AC/ACT11074 | Dual D-Type Flip-Flop |
| 74AC/ACT11109 | Dual J-K Flip-Flop |
| 74AC/ACT11112 | Dual J-K Flip-Flop |
| 74AC/ACT11132 | Quad 2-input NAND Schmitt-Trigger |
| 74AC/ACT11138 | 3-to-8 Decoder/Demultiplexer |
| 74AC/ACT11139 | 2-to-4 Decoder/Demultiplexer |
| 74AC/ACT11151 | 8-to-1 Multiplexer |
| 74AC/ACT11153 | Dual 4-to-1 Multiplexer |
| 74AC/ACT11157 | Quad 2-to-1 Multiplexer |
| 74AC/ACT11158 | Quad 2-to-1 Multiplexer |
| 74AC/ACT11160 | 4-Bit Synchronous Decade Counter |
| 74AC/ACT11161 | 4-Bit Synchronous Binary Counter |
| 74AC/ACT11162 | 4-Bit Synchronous Decade Counter |
| 74AC/ACT11163 | 4-Bit Synchronous Binary Counter |
| 74AC/ACT11168 | 4-Bit Synchronous Decade Counter |
| 74AC/ACT11169 | 4-Bit Synchronous Binary Counter |
| 74AC/ACT11174 | Hex D-type Flip-Flop |
| 74AC/ACT11175 | Quad D-type Flip-Flop |
| 74AC/ACT11181 | 4-Bit Arithmetic Logic Unit |
| 74AC/ACT11190 | 4-Bit Synchronous Decade Counter |
| 74AC/ACT11191 | 4-Bit Synchronous Binary Counter |
| 74AC/ACT11192 | 4-Bit Synchronous Decade Counter |
| 74AC/ACT11193 | 4-Bit Synchronous Binary Counter |
| 74AC/ACT11194 | 4-Bit Universal Shift Register |
| 74AC/ACT11238 | 3-to-8 Decoder/Demultiplexer |
| 74AC/ACT11239 | Dual 2-to-4 Decoder/Demultiplexer |
| 74AC/ACT11240 | Octal Bus Driver |
| 74AC/ACT11241 | Octal Bus Driver |
| 74AC/ACT11244 | Octal Bus Driver |
| 74AC/ACT11245 | Octal Bus Transceiver |
| 74AC/ACT11251 | 8-to-1 Multiplexer |
| 74AC/ACT11253 | Dual 4-to-1 Multiplexer |
| 74AC/ACT11257 | Quad 2-to-1 Multiplexer |
| 74AC/ACT11258 | Quad 2-to-1 Multiplexer |
| 74AC/ACT11269 | 8-Bit Binary Counter |
| 74AC/ACT11280 | 9-Bit Parity Generator/Checker |
| 74AC/ACT11286 | 9-Bit Parity Generator/Checker |

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# EPIC™ ACL
# PRODUCT INDEX

| DEVICE | FUNCTION |
|---|---|
| 74AC/ACT11299 | 8-Bit Universal Shift/Storage Register |
| 74AC/ACT11323 | 8-Bit Universal Shift/Storage Register |
| 74AC/ACT11352 | Dual 4-to-1 Multiplexer |
| 74AC/ACT11353 | Dual 4-to-1 Multiplexer |
| 74AC/ACT11373 | Octal D-type Latch |
| 74AC/ACT11374 | Octal D-type Flip-Flop |
| 74AC/ACT11378 | Parallel D-type Register |
| 74AC/ACT11379 | Quad Parallel Register |
| 74AC/ACT11520 | 8-Bit Identity Comparator |
| 74AC/ACT11521 | 8-Bit Identity Comparator |
| 74AC/ACT11533 | Octal D-type Latch |
| 74AC/ACT11534 | Octal D-type Flip-Flop |
| 74AC/ACT11568 | 4-Bit Synchronous Decade Counter |
| 74AC/ACT11569 | 4-Bit Synchronous Binary Counter |
| 74AC/ACT11579 | 8-Bit Synchronous Binary Counter |
| 74AC/ACT11620 | Octal Bus Transceiver |
| 74AC/ACT11623 | Octal Bus Transceiver |
| 74AC/ACT11640 | Octal Bus Transceiver |
| 74AC/ACT11643 | Octal Bus Transceiver |
| 74AC/ACT11646 | Octal Registered Bus Transceiver |
| 74AC/ACT11648 | Octal Registered Bus Transceiver |
| 74AC/ACT11651 | Octal Registered Bus Transceiver |
| 74AC/ACT11652 | Octal Registered Bus Transceiver |
| 74AC/ACT11657 | Octal Transceiver |
| 74AC/ACT11818 | Pipeline Register |
| 74AC/ACT11819 | Pipeline Register |
| 74AC/ACT11821 | 10-Bit D-type Flip-Flop |
| 74AC/ACT11822 | 10-Bit D-type Flip-Flop |
| 74AC/ACT11823 | 9-Bit Register |
| 74AC/ACT11824 | 9-Bit Register |
| 74AC/ACT11825 | 8-Bit Register |
| 74AC/ACT11826 | 8-Bit Register |
| 74AC/ACT11827 | 10-Bit Buffer |
| 74AC/ACT11828 | 10-Bit Buffer |
| 74AC/ACT11833 | Registered Transceiver |
| 74AC/ACT11834 | Registered Transceiver |
| 74AC/ACT11841 | 10-Bit D-type Latch |
| 74AC/ACT11842 | 10-Bit D-type Latch |
| 74AC/ACT11843 | 9-Bit Latch |
| 74AC/ACT11844 | 9-Bit Latch |
| 74AC/ACT11845 | 8-Bit Latch |
| 74AC/ACT11846 | 8-Bit Latch |
| 74AC/ACT11853 | Latched Transceiver |
| 74AC/ACT11854 | Latched Transceiver |
| 74AC/ACT11861 | 10-Bit Transceiver |
| 74AC/ACT11862 | 10-Bit Transsceiver |
| 74AC/ACT11863 | 9-Bit Transceiver |
| 74AC/ACT11864 | 9-Bit Transceiver |
| 74AC/ACT11873 | Dual 4-Bit D-type Latch |
| 74AC/ACT11874 | Dual 4-Bit D-type Flip-Flop |
| 74AC/ACT11881 | 4-Bit Arithmetic Logic Unit |
| 74AC/ACT11882 | 32-Bit Fast Carry Look-Ahead |

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# EPIC™ ACL
# DC CHARACTERISTICS

## recommended operating conditions for AC devices

| | | | 54AC11XXX | | | 74AC11XXX | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage (see Note 2) | | 3 | 5 | 5.5 | 3 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 2.1 | | | 2.1 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | 3.15 | | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | | 3.85 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | | | 0.9 | | | 0.9 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | | | 1.35 | |
| | | $V_{CC}$ = 5.5 V | | | 1.65 | | | 1.65 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3 V | | | −4 | | | −4 | mA |
| | | $V_{CC}$ = 4.5 V | | | −24 | | | −24 | |
| | | $V_{CC}$ = 5.5 V | | | −24 | | | −24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3 V | | | 12 | | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | | 24 | | | 24 | |
| | | $V_{CC}$ = 5.5 V | | | 24 | | | 24 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| dt/dv | Input transition rise or fall rate | | 0 | | 10 | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |

NOTE 2: No electrical or switching characteristics are specified at $V_{CC}$ < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) for AC devices

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | 54AC11XXX | | 74AC11XXX | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 μA | 3 V | 2.9 | | | 2.9 | | 2.9 | | V |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | $I_{OH}$ = −4 mA | 3 V | 2.58 | | | 2.4 | | 2.48 | | |
| | $I_{OH}$ = −24 mA | 4.5 V | 3.94 | | | 3.7 | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.7 | | 4.8 | | |
| | $I_{OH}$ = −50 mA† | 5.5 V | | | | 3.85 | | | | |
| | $I_{OH}$ = −75 mA† | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 3 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 5.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 12 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | | 1.65 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 3.5 | | | | | | pF |

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

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# DC CHARACTERISTICS

## recommended operating conditions for ACT devices

| | | 54ACT11XXX | | 74ACT11XXX | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −24 | | −24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | | 24 | mA |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| dt/dv | Input transition rise or fall rate | 0 | 10 | 0 | 10 | ns/V |
| $T_A$ | Operating free-air temperature | −55 | 125 | −40 | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) for ACT devices

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | 54ACT11XXX | | 74ACT11XXX | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 μA | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | V |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | $I_{OH}$ = −24 mA | 4.5 V | 3.94 | | | 3.7 | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.7 | | 4.8 | | |
| | $I_{OH}$ = −50 mA† | 5.5 V | | | | 3.85 | | | | |
| | $I_{OH}$ = −75 mA† | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 5.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | | 1.65 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | | 0.9 | | 1 | | 1 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 3.5 | | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

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# MAX RATINGS AND ORDERING INSTRUCTIONS

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

| | |
|---|---|
| Supply voltage, $V_{CC}$ | −0.5 V to 6 V |
| Input voltage, $V_I$ (see Note 1) | −0.5 V to $V_{CC}$ +0.5 V |
| Output voltage, $V_O$ (see Note 1) | −0.5 V to $V_{CC}$ +0.5 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) | ±20 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) | ±50 mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | ±50 mA |
| Continuous current through $V_{CC}$ or GND pins | ±100 mA |
| Storage temperature range | −65°C to 150°C |

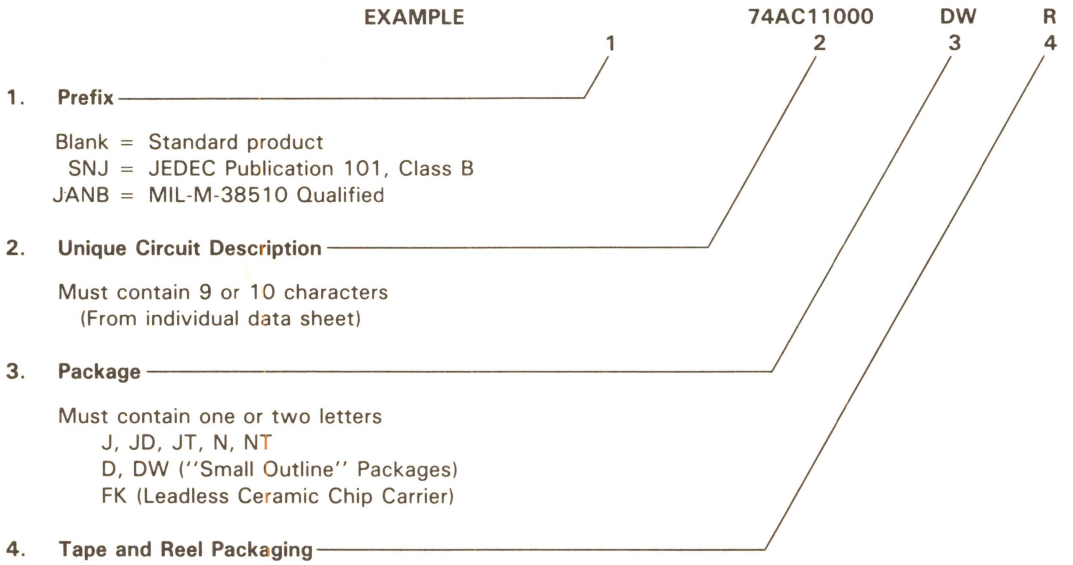
†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

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# TI MOS MEMORY PRODUCTS

## MOS EPROM

| DENSITY (BITS) | ORGANIZATION (WORDS × BITS) | TYPE | MAX ACCESS TIME (ns) | POWER SUPPLY (V) | MAX POWER DISSIPATION | | PACKAGES | COMMENTS | DOCUMENT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | ACTIVE (mW) | STANDBY (mW) | | | |
| 16K | 2K × 8<br>High Speed | TMS27C292 | 35<br>45<br>45<br>50 | 5±5%<br>5±5%<br>5±10%<br>5±10% | 394<br>315<br>330<br>303 | N/A | J | High Speed CMOS EPROM | SMLS291A |
| 32K | 4K × 8 | TMS2732A | 170<br>200<br>250<br>450 | 5±5% | 657 | 158 | J | NMOS, JEDEC Standard Pinout | SMYD006 |
| 64K | 8K × 8 | TMS2764 | 170<br>200<br>250<br>450 | 5±5% | 788 | 184 | J | NMOS | SMYD006 |
| | | TMS27C64 | 150<br>150<br>200<br>200<br>250<br>250<br>300<br>300<br>450<br>450 | 5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10% | 158<br>165<br>158<br>165<br>158<br>165<br>158<br>165<br>158<br>165 | 1.4 | J | CMOS | SMLS064 |
| 128K | 16K × 8 | TMS27C128 | 150<br>150<br>200<br>200<br>250<br>250<br>300<br>300<br>450<br>450 | 5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10% | 158<br>165<br>158<br>165<br>158<br>165<br>158<br>165<br>158<br>165 | 1.4 | J | CMOS | SMLS128A |
| 256K | 32K × 8 | TMS27C256 | 150<br>170<br>170<br>200<br>200<br>250<br>250<br>300<br>300<br>450<br>450 | 5±5%<br>5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10% | 158<br>158<br>165<br>158<br>165<br>158<br>165<br>158<br>165<br>158<br>165 | 1.4 | J | CMOS | SMLS256A |
| 512K | 64K × 8 | TMS27C512 | 200<br>200<br>250<br>250<br>300<br>300<br>450<br>450 | 5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10%<br>5±5%<br>5±10% | 158<br>165<br>158<br>165<br>158<br>165<br>158<br>165 | 1.4 | J | CMOS | SMLS512A |

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## MOS EPROM (Continued)

| DENSITY (BITS) | ORGANIZATION (WORDS × BITS) | TYPE | MAX ACCESS TIME (ns) | POWER SUPPLY (V) | MAX POWER DISSIPATION | | PACKAGES | COMMENTS | DOCUMENT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | ACTIVE (mW) | STANDBY (mW) | | | |
| 1024K | 64K × 16 | TMS27C210 | 200 | 5 ± 5% | TBD | TBD | J | CMOS | SMLS210 |
| | | | 200 | 5 ± 10% | | | | | |
| | | | 250 | 5 ± 5% | | | | | |
| | | | 250 | 5 ± 10% | | | | | |
| | | | 300 | 5 ± 5% | | | | | |
| | | | 300 | 5 ± 10% | | | | | |
| | 128K × 8 | TMS27C010 | 200 | 5 ± 5% | TBD | TBD | J | CMOS | SMLS010 |
| | | | 200 | 5 ± 10% | | | | | |
| | | | 250 | 5 ± 5% | | | | | |
| | | | 250 | 5 ± 10% | | | | | |
| | | | 300 | 5 ± 5% | | | | | |
| | | | 300 | 5 ± 10% | | | | | |

## MOS PROM (One-Time Programmable)

| DENSITY (BITS) | ORGANIZATION (WORDS × BITS) | TYPE | MAX ACCESS TIME (ns) | POWER SUPPLY (V) | MAX POWER DISSIPATION | | PACKAGES | COMMENTS | DOCUMENT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | ACTIVE (mW) | STANDBY (mW) | | | |
| 64K | 8K × 8 | TMS27PC64 | 150 | 5 ± 5% | 158 | 1.4 | N | CMOS | SMLS064 |
| | | | 150 | 5 ± 10% | 165 | | | | |
| | | | 200 | 5 ± 5% | 158 | | | | |
| | | | 200 | 5 ± 10% | 165 | | | | |
| | | | 250 | 5 ± 5% | 158 | | | | |
| | | | 250 | 5 ± 10% | 165 | | | | |
| | | | 300 | 5 ± 5% | 158 | | | | |
| | | | 300 | 5 ± 10% | 165 | | | | |
| | | | 450 | 5 ± 5% | 158 | | | | |
| | | | 450 | 5 ± 5% | 165 | | | | |
| 128K | 16K × 8 | TMS27PC128 | 200 | 5 ± 5% | 158 | 1.4 | FM, N | CMOS | SMPS128A |
| | | | 200 | 5 ± 10% | 165 | | | | |
| | | | 250 | 5 ± 5% | 158 | | | | |
| | | | 250 | 5 ± 10% | 165 | | | | |
| | | | 300 | 5 ± 5% | 158 | | | | |
| | | | 300 | 5 ± 10% | 165 | | | | |
| | | | 450 | 5 ± 5% | 158 | | | | |
| | | | 450 | 5 ± 10% | 165 | | | | |
| 256K | 32K × 8 | TMS27PC256 | 200 | 5 ± 5% | 158 | 1.4 | FM, N | CMOS | SMPS256A |
| | | | 200 | 5 ± 10% | 165 | | | | |
| | | | 250 | 5 ± 5% | 158 | | | | |
| | | | 250 | 5 ± 10% | 165 | | | | |
| | | | 300 | 5 ± 5% | 158 | | | | |
| | | | 300 | 5 ± 10% | 165 | | | | |
| | | | 450 | 5 ± 5% | 158 | | | | |
| | | | 450 | 5 ± 10% | 165 | | | | |
| 512K | 64K × 8 | TMS27PC512 | 200 | 5 ± 5% | 158 | 1.4 | FM, N | CMOS | SMPS512 |
| | | | 200 | 5 ± 10% | 165 | | | | |
| | | | 250 | 5 ± 5% | 158 | | | | |
| | | | 250 | 5 ± 10% | 165 | | | | |
| | | | 300 | 5 ± 5% | 158 | | | | |
| | | | 300 | 5 ± 10% | 165 | | | | |
| | | | 450 | 5 ± 5% | 158 | | | | |
| | | | 450 | 5 ± 10% | 165 | | | | |

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## MOS DRAM

| DENSITY (BITS) | ORGANIZATION (WORDS × BITS) | TYPE | MAX ACCESS TIME (ns) | POWER SUPPLY (V) | MAX POWER DISSIPATION | | PACKAGES | COMMENTS | DOCUMENT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | ACTIVE (mW) | STANDBY (mW) | | | |
| 256K | 256K × 1 | TMS4256 | 100<br>120<br>150 | 5 | 385<br>358<br>330 | 25<br>25<br>25 | FM, N | Page Mode | SMQS256B |
| | | TMS4257 | 100<br>120<br>150 | 5 | 385<br>358<br>330 | 25<br>25<br>25 | FM, N | Nibble Mode | |
| | 64K × 4 | TMS4464 | 100<br>120<br>150 | 5 | 385<br>358<br>330 | 28<br>28<br>28 | FM, N | | SMBS464B |
| | | TMS4461 | 120<br>150 | 5 | 935<br>770 | 110<br>110 | N, SD | Multiport Video RAM | SMVS011A |
| 1M | 1M × 1 | TMS4C1024 | 100<br>120<br>150 | 5 | 413<br>385<br>385 | 28 | DJ, N | Enhanced Page Mode | SMGS024A |
| | | TMS4C1025 | 100<br>120<br>150 | 5 | 413<br>385<br>385 | 28 | DJ, N | Nibble Mode | SMGS025 |
| | | TMS4C1027 | 100<br>120<br>150 | 5 | 413<br>385<br>385 | 28 | DJ, N | Static Column Decode | SMGS027 |
| | 256K × 4 | TMS44C256 | 100<br>120<br>150 | 5 | 413<br>385<br>385 | 28 | DJ, N | Enhanced Page Mode | SMGS256 |
| | | TMS44C257 | 100<br>120<br>150 | 5 | 413<br>385<br>385 | 28 | DJ, N | Static Column Decode | SMGS257 |



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## Dynamic RAM Modules

| DENSITY (BITS) | ORGANIZATION (WORDS × BITS) | TYPE | MAX ACCESS TIME (ns) | POWER SUPPLY (V) | MAX POWER DISSIPATION | | PACKAGES | COMMENTS | DOCUMENT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | ACTIVE (mW) | STANDBY (mW) | | | |
| 1024K | 1M × 1 | TM4256FC1 | 100<br>120<br>150 | 5 | 385<br>358<br>330 | 99<br>99<br>99 | Leaded | 22-Pin | SMMS561A |
| | 256K × 4 | TM4256EC4 | 100<br>120<br>150 | 5 | 1540<br>1432<br>1320 | 99<br>99<br>99 | Leaded | 22-Pin | SMMS564B |
| 2048K | 256K × 8 | TM4256FL8 | 100<br>120<br>150 | 5 | 3080<br>2864<br>2640 | 198<br>198<br>198 | Leaded | 30-Pin | SMMS568A |
| | | TM4256GU8 | 100<br>120<br>150 | 5 | 3080<br>2864<br>2640 | 198<br>198<br>198 | Socketable | 30-Lead | |
| 2304K | 256K × 9 | TM4256EL9 | 100<br>120<br>150 | 5 | 3465<br>3218<br>2970 | 226<br>226<br>226 | Leaded | 30-Pin | SMMS569A |
| | | TM4256GU9 | 100<br>120<br>150 | 5 | 3465<br>3218<br>2970 | 226<br>226<br>226 | Socketable,<br>Presence<br>Detect | 30-Lead | |
| 4096K | 1 MEG × 4 | TM024HAC4 | 100<br>120<br>150 | 5 | 1652<br>1540<br>1540 | 110<br>110<br>110 | Leaded | CMOS,<br>24-Pin | SMMS104 |
| 8192K | 1 MEG × 8 | TM024GAD8 | 100<br>120<br>150 | 5 | 3304<br>3080<br>3080 | 220<br>220<br>220 | Socketable,<br>Presence<br>Detect | CMOS,<br>30-Lead | SMMS102B |
| 9216K | 1 MEG × 9 | TM024EAD9 | 100<br>120<br>150 | 5 | 3717<br>3465<br>3465 | 248<br>248<br>248 | Socketable | CMOS<br>30-Lead | SMMS102B |



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THOMSON COMPONENTS MOSTEK

# MK48Z02/12(B)-12/15/20/25

2K x 8 ZEROPOWER RAM

MEMORY COMPONENTS

## FEATURES

- ☐ Predicted worst case battery life of 11 years @ 70°C
- ☐ Data retention in the absence of power
- ☐ Data security provided by automatic write protection during power failure
- ☐ +5 Volt only Read/Write
- ☐ Conventional SRAM write cycles
- ☐ Full CMOS-440 mW active; 5.5 mW standby
- ☐ 24-Pin Dual in Line package, JEDEC pinouts
- ☐ Read-cycle time equals write-cycle time
- ☐ Low-Battery Warning
- ☐ Two power-fail deselect trip points available
  MK48Z02 $4.75V \geq V_{PFD} \geq 4.50V$
  MK48Z12 $4.50V \geq V_{PFD} \geq 4.20V$

| Part Number | Access Time | R/W Cycle Time |
|---|---|---|
| MK48ZX2-12 | 120 ns | 120 ns |
| MK48ZX2-15 | 150 ns | 150 ns |
| MK48ZX2-20 | 200 ns | 200 ns |
| MK48ZX2-25 | 250 ns | 250 ns |

## TRUTH TABLE (MK48Z02/12)

| $V_{CC}$ | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | MODE | DQ |
|---|---|---|---|---|---|
| $<V_{CC}$ (Max)<br>$>V_{CC}$ (Min) | $V_{IH}$<br>$V_{IL}$<br>$V_{IL}$<br>$V_{IL}$ | X<br>X<br>$V_{IL}$<br>$V_{IH}$ | X<br>$V_{IL}$<br>$V_{IH}$<br>$V_{IH}$ | Deselect<br>Write<br>Read<br>Read | High-Z<br>$D_{IN}$<br>$D_{OUT}$<br>High-Z |
| $<V_{PFD}$ (Min)<br>$>V_{SO}$ | X | X | X | Power-Fail Deselect | High-Z |
| $\leq V_{SO}$ | X | X | X | Battery Back-up | High-Z |

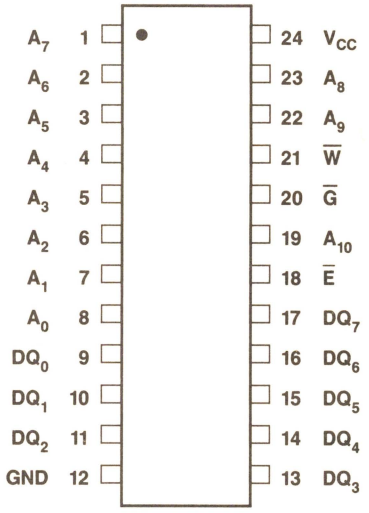


**Figure 1. Pin Connections**

## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_{10}$ | Address Inputs | $V_{CC}$ | System Power (+5 V) |
| $\overline{E}$ | Chip Enable | $\overline{W}$ | Write Enable |
| GND | Ground | $\overline{G}$ | Output Enable |
| $DQ_0$—$DQ_7$ Data In/Data Out | | | |

## DESCRIPTION

The MK48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted

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Thomson/Mostek

# MK48T02/12(B)-12/15/20/25

## 2K x 8 ZEROPOWER /TIMEKEEPER RAM

MEMORY COMPONENTS

Thomson/Mostek

### FEATURES

- ☐ Integrated Ultra Low Power SRAM, Real Time Clock, Crystal, Power-fail Control Circuit and Battery
- ☐ BYTEWIDE™ RAM-like Clock Access
- ☐ BCD Coded Year, Month, Day, Date, Hours, Minutes and Seconds
- ☐ Software Controlled Clock Calibration for High Accuracy Applications
- ☐ Predicted Worst Case Battery Storage Life of 11 years @ 70°C
- ☐ Pin and Function Compatible with JEDEC Standard 2K x 8 SRAMs
- ☐ Automatic Power-fail Chip Deselect/Write Protection
- ☐ Two Power-fail Deselect Trip Points Available
  MK48T02: 4.75 V ≥ $V_{PFD}$ ≥ 4.50 V
  MK48T12: 4.50 V ≥ $V_{PFD}$ ≥ 4.20 V

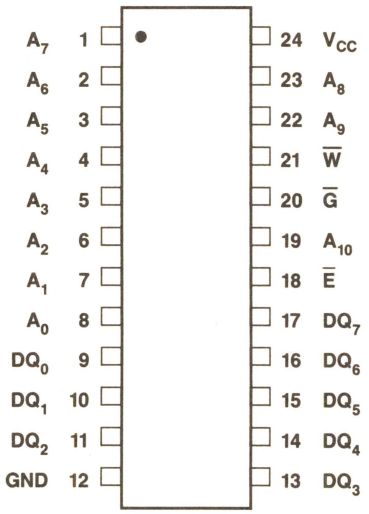


**Figure 1. Pin Connections**

| Part Number | Access Time | R/W Cycle Time |
|---|---|---|
| MK48TX2-12 | 120 ns | 120 ns |
| MK48TX2-15 | 150 ns | 150 ns |
| MK48TX2-20 | 200 ns | 200 ns |
| MK48TX2-25 | 250 ns | 250 ns |

### PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_{10}$ | Address Input | $V_{CC}$ | +5 Volts |
| $\overline{E}$ | Chip Enable | $\overline{W}$ | Write Enable |
| GND | Ground | $\overline{G}$ | Output Enable |
| $DQ_0$ - $DQ_7$ Data In/Data Out | | | |

### TRUTH TABLE (MK48T02/12)

| $V_{CC}$ | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | MODE | DQ |
|---|---|---|---|---|---|
| < $V_{CC}$ (Max)<br>> $V_{CC}$ (Min) | $V_{IH}$<br>$V_{IL}$<br>$V_{IL}$<br>$V_{IL}$ | X<br>X<br>$V_{IL}$<br>$V_{IH}$ | X<br>$V_{IL}$<br>$V_{IH}$<br>$V_{IH}$ | Deselect<br>Write<br>Read<br>Read | High-Z<br>$D_{IN}$<br>$D_{OUT}$<br>High-Z |
| < $V_{PFD}$ (Min)<br>> $V_{SO}$ | X | X | X | Power-Fail Deselect | High-Z |
| ≤ $V_{SO}$ | X | X | X | Battery Back-up | High-Z |

### DESCRIPTION

The MK48T02/12 combines a 2K x 8 full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery, all in a single plastic DIP package. The MK48T02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM, such as the 6116 or 5517. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.


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THOMSON COMPONENTS MOSTEK

# MK48Z08/18/09/19(B)-15/20/25

8K × 8 ZEROPOWER RAM

MEMORY COMPONENTS

## FEATURES

- ☐ Predicted Worst Case Battery Life of 11 years @ 70°C
- ☐ Data retention in the absence of power
- ☐ Power Fail Interrupt Output (MK48Z09/19) Open Drain
- ☐ Extra data security provided by early write protection during power failure (MK48Z08/09)
- ☐ Direct replacement for volatile 8K x 8 Byte Wide Static RAM
- ☐ +5 Volt only Read/Write
- ☐ Unlimited write cycles
- ☐ JEDEC standard 28 pin memory pinout
- ☐ Read-cycle time equals write-cycle time
- ☐ Two power-fail deselect trip points available
  MK48Z08/09: $4.75V \geq V_{PFD} \geq 4.50V$
  MK48Z18/19: $4.50V \geq V_{PFD} \geq 4.20V$

| Part Number | Access Time | R/W Cycle Time |
|---|---|---|
| MK48Z08B-25 | 250 ns | 250 ns |
| MK48Z08B-20 | 200 ns | 200 ns |
| MK48Z08B-15 | 150 ns | 150 ns |
| MK48Z18B-25 | 250 ns | 250 ns |
| MK48Z18B-20 | 200 ns | 200 ns |
| MK48Z18B-15 | 150 ns | 150 ns |
| MK48Z09B-25 | 250 ns | 250 ns |
| MK48Z09B-20 | 200 ns | 200 ns |
| MK48Z09B-15 | 150 ns | 150 ns |
| MK48Z19B-25 | 250 ns | 250 ns |
| MK48Z19B-20 | 200 ns | 200 ns |
| MK48Z19B-15 | 150 ns | 150 ns |

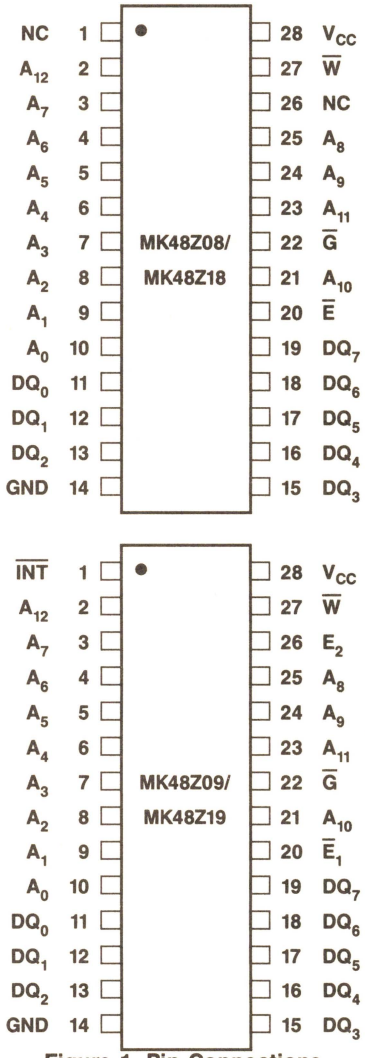


**Figure 1. Pin Connections**

## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_{12}$ | Address Inputs | $V_{CC}$ | System Power (+5 V) |
| $\overline{E_1}$, $E_2$ | Chip Enable | $\overline{W}$ | Write Enable |
| GND | Ground | $\overline{G}$ | Output Enable |
| $DQ_0$ - $DQ_7$ | Data In/Data Out | $\overline{INT}$ | Power Fail Interrupt Output |
| NC | No Connect | | |

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Thomson/Mostek

# MK41H66/MK41H67(N,P)-20/25/35

16K × 1 CMOS STATIC RAM

MEMORY COMPONENTS



## FEATURES

- ☐ 20, 25, and 35 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 20-pin, 300 mil Plastic and Ceramic DIP
- ☐ All input and output pins TTL compatible, low capacitance, and protected against static discharge
- ☐ 50 μA CMOS Standby Current (MK41H67)
- ☐ High speed chip select (MK41H66)
- ☐ JEDEC standard pinout

## MK41H66 TRUTH TABLE

| $\overline{CS}$ | $\overline{WE}$ | Mode | Q | Power |
|---|---|---|---|---|
| H | X | Deselect | High Z | Active |
| L | L | Write | High Z | Active |
| L | H | Read | Data Out | Active |

X = Don't Care

## MK41H67 TRUTH TABLE

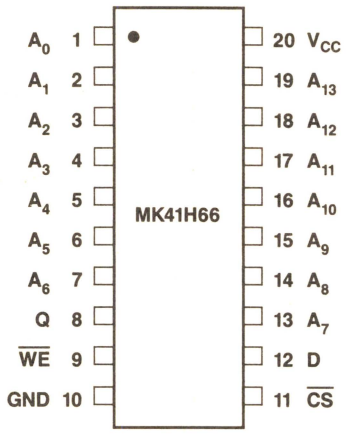
| $\overline{CE}$ | $\overline{WE}$ | Mode | Q | Power |
|---|---|---|---|---|
| H | X | Deselect | High Z | Standby |
| L | L | Write | High Z | Active |
| L | H | Read | Data Out | Active |

## DESCRIPTION

The MK41H66 and MK41H67 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Both require only a single +5V ± 10 percent power supply. Both devices are fully TTL compatible.

The MK41H67 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

The MK41H66 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.



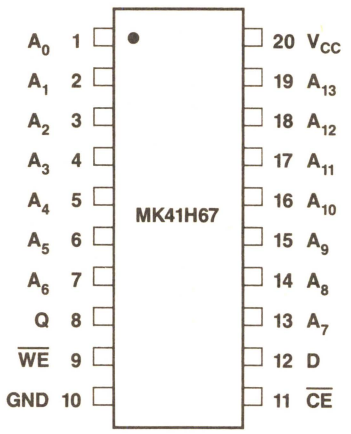




**Figure 1. Pin Connections**

## PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{13}$ - Address | $\overline{WE}$ - Write Enable |
| $\overline{CE}$ - Chip Enable (MK41H67) | GND - Ground |
| $\overline{CS}$ - Chip Select (MK41H66) | $V_{CC}$ - + 5 volts |
| | D - Data In |
| | Q - Data Out |



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# MK41H68/MK41H69(N,P)-20/25/35

4K × 4 CMOS STATIC RAM

MEMORY COMPONENTS

## FEATURES

- ☐ 20, 25, and 35 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 20-pin, 300 mil Plastic and Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ 50 $\mu$A CMOS Standby Current (MK41H68)
- ☐ TTL Standby Current unaffected by address activity (MK41H68)
- ☐ High speed chip select (MK41H69)
- ☐ JEDEC standard pinout

## MK41H68 TRUTH TABLE

| $\overline{CE}$ | $\overline{WE}$ | Mode | DQ | Power |
|---|---|---|---|---|
| H | X | Deselect | High Z | Standby |
| L | L | Write | $D_{IN}$ | Active |
| L | H | Read | $D_{OUT}$ | Active |

## MK41H69 TRUTH TABLE

| $\overline{CS}$ | $\overline{WE}$ | Mode | DQ | Power |
|---|---|---|---|---|
| H | X | Deselect | High Z | Active |
| L | L | Write | $D_{IN}$ | Active |
| L | H | Read | $D_{OUT}$ | Active |

X = Don't Care

## DESCRIPTION

The MK41H68 and MK41H69 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Both require only a single +5V ± 10 percent power supply. Both devices are fully TTL compatible.

The MK41H68 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by raising the $\overline{CE}$ pin to the full $V_{CC}$ voltage.

The MK41H69 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

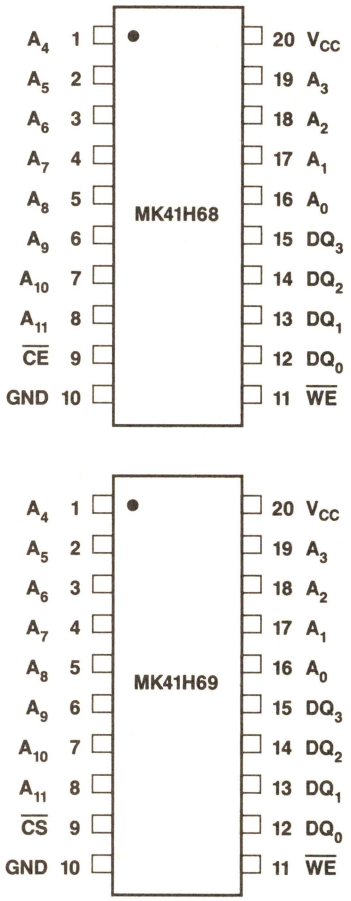





**Figure 1. Pin Connections**

## PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{11}$ - Address | $\overline{WE}$ - Write Enable |
| $DQ_0$ - $DQ_3$ - Data I/O | GND - Ground |
| $\overline{CE}$ - Chip Enable (MK41H68) | $V_{CC}$ - + 5 volts |
| $\overline{CS}$ - Chip Select (MK41H69) | |

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## FEATURES

- ☐ 25, 35, and 45 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 22-pin, 300 mil Plastic and Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ Low Power CMOS Standby Current
- ☐ Battery Backup Operation
- ☐ JEDEC standard pinout

## MK41H87 TRUTH TABLE

| $\overline{CE}$ | $\overline{WE}$ | Mode | Q | Power |
|---|---|---|---|---|
| H | X | Deselect | High Z | Standby |
| L | L | Write | High Z | Active |
| L | H | Read | Data Out | Active |

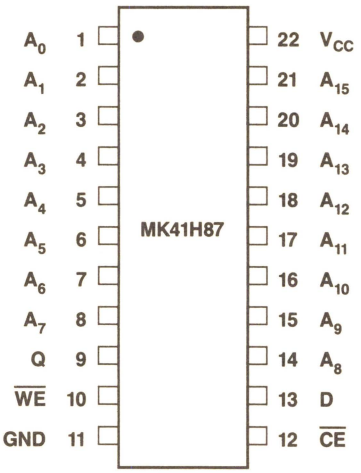


**Figure 1. Pin Connections**

## PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{15}$ - Address | $V_{CC}$ - + 5 volts |
| $\overline{CE}$ - Chip Enable | D - Data In |
| $\overline{WE}$ - Write Enable | Q - Data Out |
| GND - Ground | |

## DESCRIPTION

The MK41H87 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The MK41H87 requires only a single +5V ± 10 percent power supply, and it is fully TTL compatible.

The MK41H87 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

## OPERATIONS

### READ MODE

The MK41H87 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from one of 65,536 locations in the static storage array. Valid data will be available at the Data Output pin (Q) within $t_{AA}$ after the last address input signal is stable, providing that the $\overline{CE}$ access time is satisfied. If $\overline{CE}$ access time is not met, data access will be measured from the limiting parameter ($t_{CA}$) rather than the address. The state of the Data Output pin is controlled by the CE and $\overline{WE}$ control signals. The Q may be in an indeterminate state at $t_{CL}$, but the Q will always have valid data at $t_{AA}$.



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# MK41H79(N,P)-20/25/35

4K × 4 CMOS STATIC RAM

PRELIMINARY

MEMORY COMPONENTS

## FEATURES

- ☐ 20, 25, and 35 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 22-pin, 300 mil Plastic and Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ TTL Standby Current unaffected by address activity
- ☐ Separate Output Enable control
- ☐ Flash Clear Function

## TRUTH TABLE

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{CLR}$ | Mode | DQ | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | Deselect | High Z | Standby |
| L | X | L | H | Write | $D_{IN}$ | Active |
| L | L | H | H | Read | $D_{OUT}$ | Active |
| L | H | H | H | Read | High Z | Active |
| L | X | L | L | Flash Clear | High Z | Active |
| L | L | H | L | Flash Clear | Low Z | Active |
| L | H | H | L | Flash Clear | High Z | Active |

X = Don't Care

## DESCRIPTION

The MK41H79 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. It requires a single +5V ± 10 percent power supply and is fully TTL compatible.

The device has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced by raising the $\overline{CE}$ pin to the full $V_{CC}$ voltage. An Output Enable ($\overline{OE}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus.

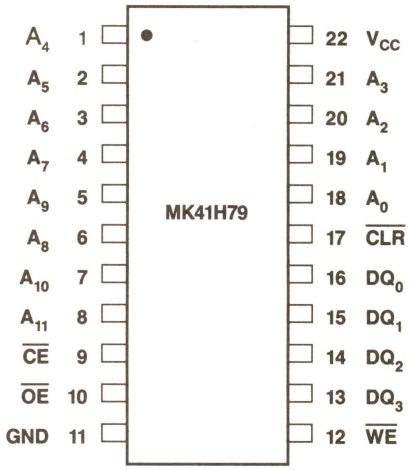



**Figure 1. Pin Connections**

## PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{11}$ - Address | $\overline{OE}$ - Output Enable |
| $DQ_0$ - $DQ_3$ - Data I/O | $\overline{WE}$ - Write Enable |
| $\overline{CLR}$ - Flash Clear | GND - Ground |
| $\overline{CE}$ - Chip Enable | $V_{CC}$ - + 5 volts |

Flash Clear operation is provided on the MK41H79 via the $\overline{CLR}$ pin, and $\overline{CE}$ active (low). A low applied to the $\overline{CLR}$ pin clears all RAM bits to zero, making it especially useful for high speed cache and buffer storage applications.

## OPERATIONS

### READ MODE

The MK41H79 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Thomson/Mostek

# MK4501(N,K)-50/65/80/10/12/15/20

## 512 x 9 CMOS BiPORT™ FIFO

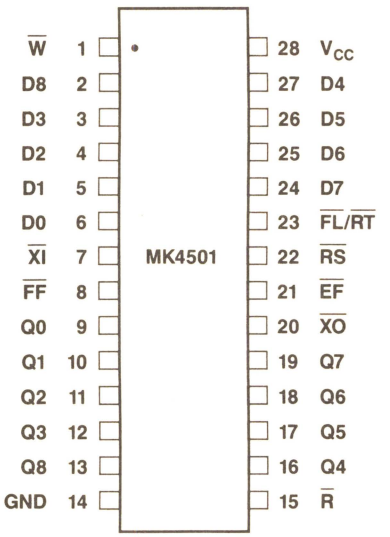
MEMORY COMPONENTS



### FEATURES

- ☐ First-In, First-Out Memory Based Architecture
- ☐ Flexible 512 x 9 organization
- ☐ Low Power HCMOS technology
- ☐ Asynchronous and simultaneous read/write
- ☐ Bidirectional applications
- ☐ Fully expandable by word width or depth
- ☐ Empty and full warning flags
- ☐ Retransmit capability
- ☐ High performance

| Part No. | Access Time | R/W Cycle Time |
|---|---|---|
| MK4501-50 | 50 ns | 65 ns |
| MK4501-65 | 65 ns | 80 ns |
| MK4501-80 | 80 ns | 100 ns |
| MK4501-10 | 100 ns | 120 ns |
| MK4501-12 | 120 ns | 140 ns |
| MK4501-15 | 150 ns | 175 ns |
| MK4501-20 | 200 ns | 235 ns |



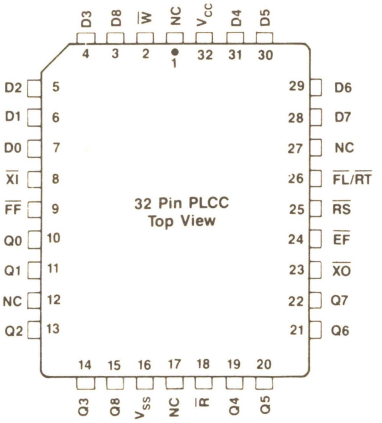




**Figure 1. Pin Connections**

### PIN NAMES

| | | | |
|---|---|---|---|
| W̄ | = Write | XI | = Expansion In |
| R̄ | = Read | XO | = Expansion Out |
| RS | = Reset | FF | = Full Flag |
| FL/RT | = First Load/ Retransmit | EF | = Empty Flag |
| D | = Data In | $V_{CC}$ | = 5 Volts |
| Q | = Data Out | GND | = Ground |

### DESCRIPTION

The MK4501 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

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# MK4511(N/K)-12/15/20

512 × 9 CMOS BiPORT RAM

MEMORY COMPONENTS

## FEATURES

- ☐ Single Chip Bi-directional Message Passing
- ☐ Software Controlled Interrupt Outputs
- ☐ Addressable Status/Control Flags
- ☐ Identical Ports, 3-wire Controlled I/O

## PIN NAMES

| | |
|---|---|
| AD - Address/Data I/O | $\overline{INT}$ - Interrupt Output |
| $\overline{CE}$ - Chip Enable | GND - Ground |
| $\overline{OE}$ - Output Enable | $V_{CC}$ - +5 Volts |
| $\overline{WE}$ - Write Enable | NC - No Connection |

| Part Number | Access Time | Cycle Time | Cycle Rate |
|---|---|---|---|
| MK4511-12 | 120 ns | 150 ns | 6.67 MHz |
| MK4511-15 | 150 ns | 190 ns | 5.26 MHz |
| MK4511-20 | 200 ns | 250 ns | 4.00 MHz |

## DESCRIPTION

The MK4511 dual port RAM contains a single 512 x 9 CMOS memory matrix that can be accessed simultaneously from both of the input/output ports. Dual port operation is achieved through the use of a memory array composed of BiPORT memory cells. Each memory cell is accessible from both ports at all times.

Pin count is kept low through the use of address/data multiplexing. This technique is being used on advanced microprocessors and other devices to keep pin counts and package sizes down.

The MK4511 incorporates all functions required for dual port operations, including software controlled interrupt outputs. Use of the interrupt outputs is optional, allowing both polled and interrupt controlled applications.

## SINGLE PORT OPERATIONS

The MK4511 may be viewed from either port as an ordinary three wire controlled 512 x 9 static RAM. Timing of read and write operations is altogether conventional; the presence of the other port is effectively transparent to the accessing processor. Therefore, all timing parameters are specified without references that differentiate between the ports.

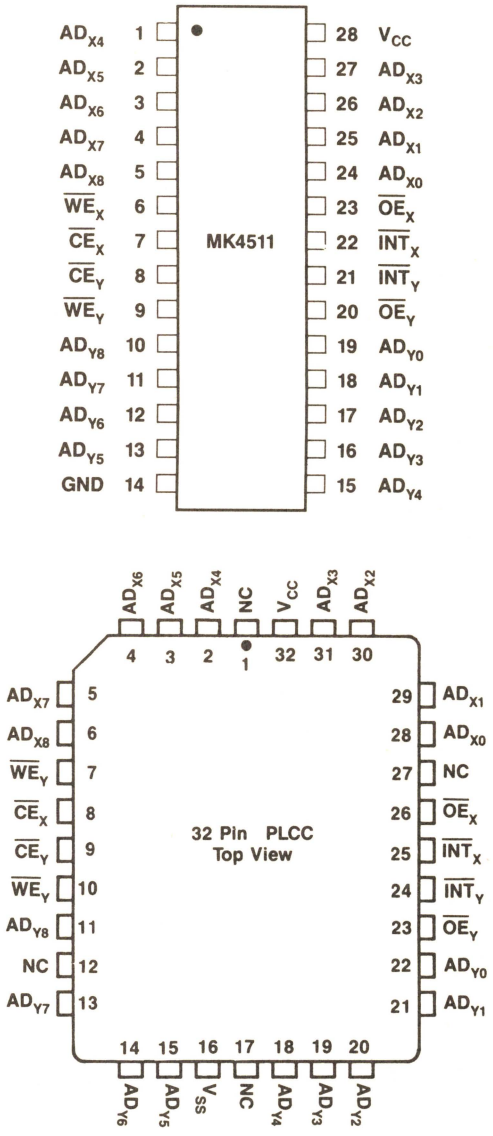


**Figure 1. Pin Connections**

Thomson/Mostek

# MK4532 • MK4542(N,K)-55,70,90

2K x 8 CMOS DUAL-PORT RAM

ADVANCE INFORMATION

MEMORY COMPONENTS



## FEATURES

- ☐ High speed:
  — 55, 70, and 90 ns access
- ☐ Fully static operation
- ☐ Full contention arbitration
- ☐ VT7142 slave for bus expansion
- ☐ Output enable function
- ☐ Separate port power-down
- ☐ Advanced CMOS technology
- ☐ Dual interrupt flags in PLCC
- ☐ Low power:
  — 60 mA (max) operating
- ☐ 48-pin DIP or 52-pin PLCC

## DESCRIPTION

The MK4532 and MK4542 are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The MK4532 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "master" dual-port RAM with the MK4542A "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

The MK4532/MK4542 feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and/or write from either port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete.

When used in the 52-pin PLCC package, a dual-level interrupt function is available. The interrupt function acts like writable flags and is provided to allow communication between systems. When the flag's location is written from one side, the other side's INT pin goes low until the flag location is read by that side.

MK4532 • MK4542

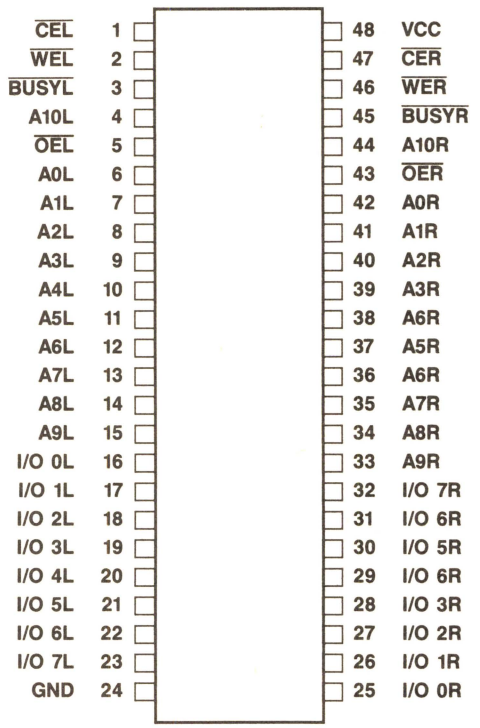


**Figure 1. Pin Connections**



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# MK4503(N/K)-50/65/80/10/12/15/20

2048 x 9 CMOS BiPORT FIFO

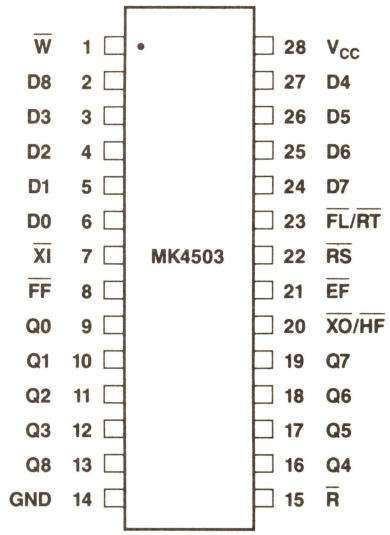
PRELIMINARY

MEMORY COMPONENTS

## FEATURES

- ☐ First-In, First-Out Memory Based Architecture
- ☐ Flexible 2048 x 9 organization
- ☐ Low Power HCMOS technology
- ☐ Asynchronous and simultaneous read/write
- ☐ Bidirectional applications
- ☐ Fully expandable by word width and depth
- ☐ Empty and full warning flags
- ☐ Retransmit capability
- ☐ High performance
- ☐ Half full flag in single device mode

| Part No. | Access Time | R/W Cycle Time |
|---|---|---|
| MK4503-50 | 50 ns | 65 ns |
| MK4503-65 | 65 ns | 80 ns |
| MK4503-80 | 80 ns | 100 ns |
| MK4503-10 | 100 ns | 120 ns |
| MK4503-12 | 120 ns | 140 ns |
| MK4503-15 | 150 ns | 175 ns |
| MK4503-20 | 200 ns | 235 ns |




28 Pin Plastic DIP

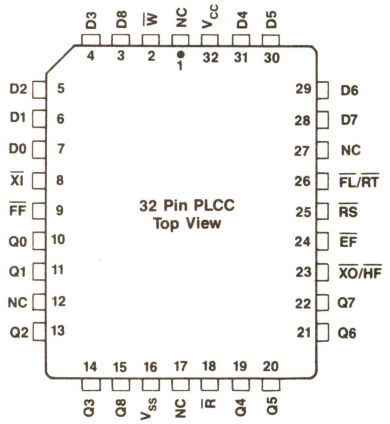



Figure 1. Pin Connections

## DESCRIPTION

The MK4503 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, half full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4503 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The

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## PIN NAMES

| | | | |
|---|---|---|---|
| W̄ | = Write | XI | = Expansion In |
| R̄ | = Read | XO/HF | = Expansion Out Half Full Flag |
| RS | = Reset | FF | = Full Flag |
| FL/RT | = First Load/ Retransmit | EF | = Empty Flag |
| D | = Data In | $V_{CC}$ | = 5 Volts |
| Q | = Data Out | GND | = Ground |
| | | NC | = No Connection |

Thomson/Mostek

THOMSON COMPONENTS MOSTEK

# MK4505M/4505S(N,K)-25,33,50

VERY HIGH SPEED CMOS CLOCKED FIFO

PRELIMINARY

MEMORY COMPONENTS

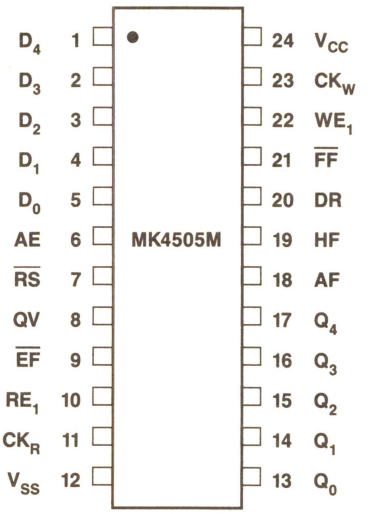
Thomson/Mostek

## FEATURES

- ☐ 1024 x 5 Organization
- ☐ Very high performance

| Part No. | Cycle Time | Cycle Frequency | Access Time |
|---|---|---|---|
| 4505-25 | 25 ns | 40 MHz | 15 ns |
| 4505-33 | 33 ns | 30 MHz | 20 ns |
| 4505-50 | 50 ns | 20 MHz | 25 ns |

- ☐ Rising edge triggered clock inputs
- ☐ Supports free-running 40% to 60% Duty Cycle Clock Inputs
- ☐ Separate Read and Write Enable Inputs
- ☐ BiPORT™ RAM architecture allows fully asynchronous and simultaneous Read/Write operation
- ☐ Cascadable to any depth with no additional logic
- ☐ Width Expandable to more than 40 bits with no additional logic
- ☐ Half Full Status Flag
- ☐ Full and Empty Flags, Almost Full, Almost Empty, Input Ready, Output Valid Status Flags (4505M)
- ☐ Fully TTL Compatible
- ☐ 3 State Outputs



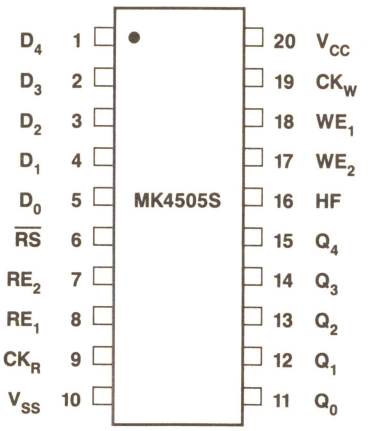




**Figure 1. Pin Configuration, 300 mil DIP**

## PIN NAMES

| | |
|---|---|
| $D_0$ - $D_4$ | - Data Input |
| $Q_0$ - $Q_4$ | - Data Output |
| $CK_W$, $CK_R$ | - Write and Read Clock |
| $WE_1$ | - Write Enable Input 1 |
| $\overline{RE_1}$ | - Read Enable Input 1 |
| $\overline{RS}$ | - Reset (Active Low) |
| HF | - Half Full Flag |
| $V_{CC}$, $V_{SS}$ | - +5 Volt, Ground |

**(4505M Only)**

| | |
|---|---|
| $\overline{FF}$, $\overline{EF}$ | - Full and Empty Flag (Active Low) |
| AF, AE | - Almost Full, Almost Empty Flag |
| DR, QV | - Input Ready, Output Valid |

**(4505S Only)**

| | |
|---|---|
| $WE_2$ | - Write Enable Input 2 |
| $RE_2$ | - Read Enable Input 2 (Rising Edge Triggered 3 State Control) |

Supersedes Publication No. 4420972 for Jan. 1987 and May 1987.

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# MK41H80(N/P)-20/25/35

## 4K × 4 CMOS TAGRAM

## MEMORY COMPONENTS

### FEATURES

- ☐ 4K × 4 SRAM with onboard 4 bit Comparator
- ☐ 20, 25, and 35ns Address to Compare Access Time
- ☐ 12, 15, and 20 ns Tag Data to Compare Access Time
- ☐ Equal Access, Read and Write Cycle Times
- ☐ Flash Clear Function
- ☐ 22-pin, 300 mil Plastic and Ceramic Dip
- ☐ All Inputs and Outputs are TTL compatible, low capacitance, and protected against static discharge
- ☐ Word Width Expandable

### TRUTH TABLE

| $\overline{WE}$ | $\overline{OE}$ | $\overline{CLR}$ | MATCH | MODE |
|---|---|---|---|---|
| H | H | H | Valid | Compare Cycle |
| L | X | H | Invalid | Write Cycle |
| H | L | H | Invalid | Read Cycle |
| X | X | L | Invalid | Flash Clear Cycle |

X = Don't Care

### DESCRIPTION

The MK41H80 is a member of Mostek's 4K × 4 CMOS Static RAM family featuring fully static operation requiring no external clocks or timing strobes. Cycle Time and Compare Access Time are equal. The MK41H80 is powered by a single +5V ±10% power supply and the inputs and outputs are fully TTL compatible.

The MK41H80 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high match on the MATCH pin or an active low miss on the MATCH pin. The MATCH pins of several MK41H80's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

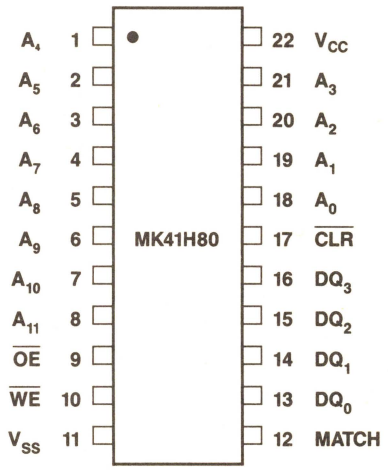


**Figure 1. Pin Connections**

### PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{11}$ | - Address Inputs |
| $DQ_0$ - $DQ_3$ | - Data Input/Output |
| MATCH | - Comparator Output |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |
| $\overline{CLR}$ | - Flash Clear |
| $V_{CC}$ | - Power (+5V) |
| $V_{SS}$ | - Ground |

Tag data can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs ($DQ_0$-$DQ_3$).

Flash Clear operation is provided on the MK41H80 via the ($\overline{CLR}$) pin. A low applied to the $\overline{CLR}$ pin clears all RAM bits to a logic zero.

Thomson/Mostek

THOMSON COMPONENTS MOSTEK

# MK48H74(N,P,E)-35/45/55

## 64K (8K x 8-BIT) CMOS TAGRAM™

ADVANCE INFORMATION

MEMORY COMPONENTS

Thomson/Mostek

### FEATURES

- ☐ 8K × 8 CMOS SRAM with onboard 8-bit comparator
- ☐ Address to Compare Access 35/45/55ns
- ☐ Fast Chip Select to Compare Access 20/25/30ns
- ☐ MATCH Output (open drain) with fast Tag Data to compare access of 25/30/35ns (max.)
- ☐ Static Operation - no clocks or timing strobes required
- ☐ All inputs and outputs are fully TTL compatible
- ☐ Full CMOS for low power operation
- ☐ Flash Clear Function
- ☐ Three-state output
- ☐ Standard 28-pin package in 600 mil DIP and 32-pin LCC
- ☐ High Speed asynchronous RAM Clear (Cycle time = 2 × $t_{AVAV}$)

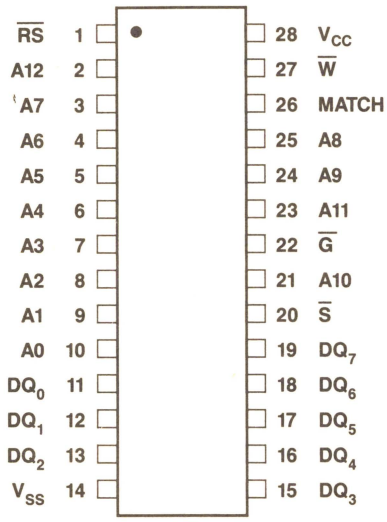


**Figure 1. Pin Connections**

### DESCRIPTION

The MK48H74 is a 65,636-bit fast static cache TAGRAM organized as 8K × 8 bits. It is fabricated using Thomson-Mostek's low power, high performance, CMOS technology. The MK48H74 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The device requires a single +5V ±10 percent supply, and is fully TTL compatible.

### PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{12}$ | - Address Inputs |
| $DQ_0$ - $DQ_7$ | - Data Input/Output |
| $\overline{S}$ | - Chip Select |
| $\overline{W}$ | - Write Enable |
| $\overline{G}$ | - Output Enable |
| $V_{CC}$ | - +5V |
| $V_{SS}$ | - Ground |
| $\overline{RS}$ | Reset Flash Clear |
| MATCH | Match Output |

### MK48H74 TRUTH TABLE

| $\overline{W}$ | $\overline{S}$ | $\overline{G}$ | $\overline{RS}$ | MODE | DQ | MATCH |
|---|---|---|---|---|---|---|
| X | X | X | L | Reset Clear | — | High |
| X | H | X | H | Deselect | High-Z | High |
| H | L | H | H | Miss-NOmatch | $D_{IN}$ | Low |
| H | L | H | H | Match | $D_{IN}$ | High |
| H | L | L | H | Read | $Q_{OUT}$ | High |
| L | L | X | H | Write | $D_{IN}$ | High |



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THOMSON COMPONENTS MOSTEK

# MK48H64/MK48H65(N/P)-35,45,55,70

64K (8K x 8-BIT) CMOS FAST STATIC RAM

ADVANCE INFORMATION

MEMORY COMPONENTS

## FEATURES

- ☐ 35, 45, 55, and 70 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ Static Operation - no clocks or timing strobes required
- ☐ Low $V_{CC}$ Data Retention 2 volts
- ☐ All inputs and outputs are CMOS and TTL compatible
- ☐ Low Power Operation, 10$\mu$A CMOS Standby Current utilizing Full CMOS 6-T cell
- ☐ Three state output
- ☐ Standard 28-pin package in 600 mil Plastic or 600 mil Ceramic DIP. MK48H65 available in 300 mil Plastic DIP.

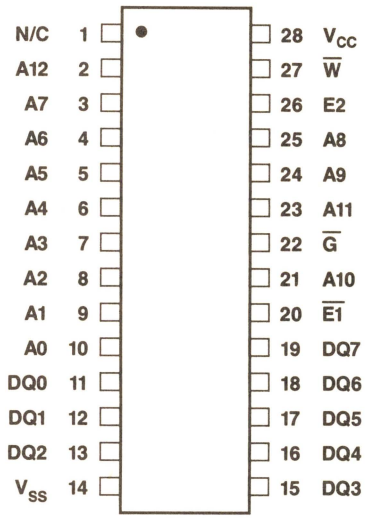



**Figure 1. Pin Connections**

## MK48H64/MK48H65 TRUTH TABLE

| $\overline{W}$ | $\overline{E1}$ | E2 | $\overline{G}$ | MODE | DQ | POWER |
|---|---|---|---|---|---|---|
| X | H | X | X | Deselect | High-Z | Standby |
| X | X | L | X | Deselect | High-Z | Standby |
| H | L | H | H | Read | High-Z | Active |
| H | L | H | L | Read | $Q_{OUT}$ | Active |
| L | L | H | X | Write | $D_{IN}$ | Active |

| PIN NAMES | |
|---|---|
| A0-A12 | Address Inputs |
| DQ0-DQ7 | Data Input/Output |
| $\overline{E1}$, E2 | Chip Enable |
| $\overline{W}$ | Write Enable |
| $\overline{G}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| N/C | No Connection |

## DESCRIPTION

The MK48H64 and MK48H65 are 65,536-bit fast static RAMs organized as 8K × 8 bits. They are fabricated using Thomson-Mostek's low power, high performance, CMOS technology. The devices feature fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. They require a single +5V ± 10 % supply, and are fully TTL compatible.

The MK48H64 and MK48H65 have a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive ($\overline{E1}$ goes high or E2 goes low). An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, $\overline{E1}$, and E2, as summarized in the truth table.

The MK48H65 is a space saving 300 mil plastic DIP. The MK48H64 offers the standard 600 mil Plastic or Ceramic DIP.

Thomson/Mostek

# MK45264/45265(N)-55/70

CMOS (64x5)x2

BIDIRECTIONAL BiPORT FIFO/TRANSCEIVER

Thomson/Mostek

## FEATURES

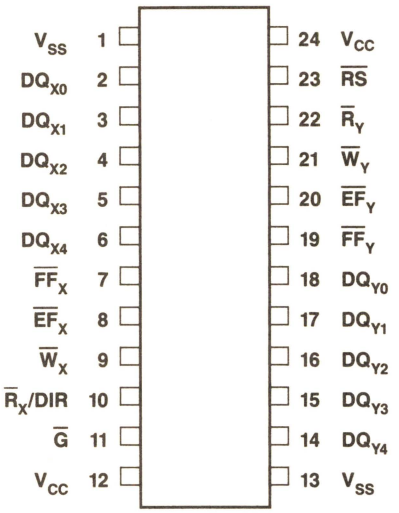
- ☐ Dual 64x5 FIFOs plus a 245-type Transceiver function
- ☐ Fully asynchronous dual port operation
- ☐ Empty, Full, Almost Full and Almost Empty Status Flags
- ☐ Spare bits for Parity and Beginning/End-of-Message Flags
- ☐ +/− 12mA Output Drive capability
- ☐ Dual $V_{CC}$ and $V_{SS}$ for improved margin and drive
- ☐ 300 mil DIP package
- ☐ Application: Arbitration-free $\mu$P-to-$\mu$P Message Passing

| PART NUMBER | ACCESS TIME | CYCLE TIME | CYCLE RATE |
|---|---|---|---|
| MK45264N-55 | 55 ns | 75 ns | 13.3 MHz |
| MK45264N-70 | 70 ns | 95 ns | 10.5 MHz |
| MK45265N-55 | 55 ns | 75 ns | 13.3 MHz |
| MK45265N-70 | 70 ns | 95 ns | 10.5 MHz |

## PIN NAMES

$V_{CC}$, $V_{SS}$ = +5V, GND
$DQ_{X0}$-$DQ_{X4}$ = X Port Data I/O
$DQ_{Y0}$-$DQ_{Y4}$ = Y Port Data I/O
$\overline{W}_X$, $\overline{W}_Y$ = X & Y Port Write Enables
$\overline{R}_X$/DIR = X Port Read Enable and Transceiver Direction Control
$\overline{G}$ = Transceiver Enable
$\overline{R}_Y$ = Y Port Read Enable
$\overline{RS}$ = Master Reset
$\overline{EF}_X$, $\overline{FF}_Y$ = Y-to-X FIFO Empty/Full Flag
$\overline{EF}_Y$, $\overline{FF}_X$ = X-to-Y FIFO Empty/Full Flag
$\overline{AE}_Y$, $\overline{AF}_X$ = X-to-Y FIFO Almost Empty/Full
$\overline{AE}_X$, $\overline{AF}_Y$ = Y-to-X FIFO Almost Empty/Full

MK45264




MK45265

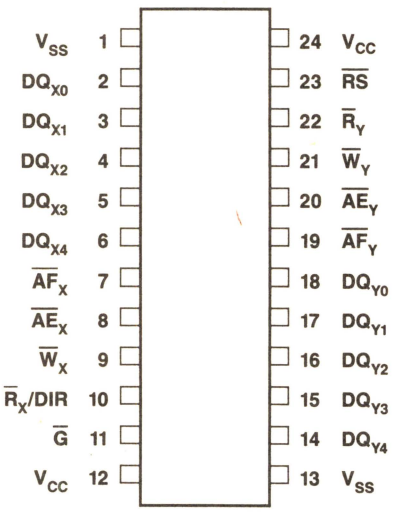



**Figure 1. Pinout. 24 Pin, 300 mil DIP**



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THOMSON COMPONENTS MOSTEK

# MK45DP8(N/K)-60/70

## 1K x 16. 2K x 8 CMOS DUAL PORT RAM

ADVANCE INFORMATION

MEMORY COMPONENTS

### FEATURES

- ☐ Organization
  Left Port 1024 x 16
  Right Port 2048 x 8
- ☐ High Speed
  60 ns Access
- ☐ Fully Static Operation
- ☐ Full Contention Arbitration
- ☐ Simple Microprocessor Interface
- ☐ Output Enable Function
- ☐ Separate Port Power Down
- ☐ Advanced CMOS technology
- ☐ Two Interrupt Flags
- ☐ Low Power: 70 mA Max. Operating
- ☐ 68 pin PLCC

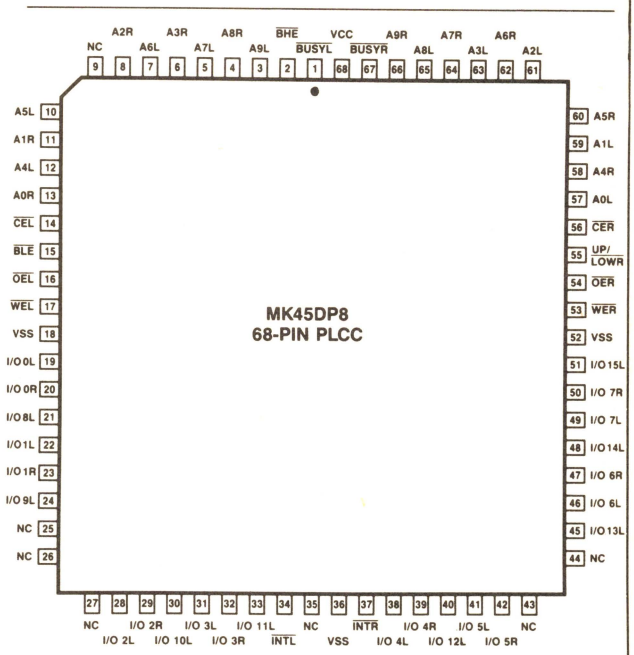


**Figure 1. Pin Diagram for PLCC**

### DESCRIPTION

The MK45DP8 is a 16,384-bit dual port static random access memory. Its left port is organized as 1,024 16-bit words and its right port as 2,048 8-bit words. It is designed to facilitate the transfer of data between 16- and 8-bit microprocessors.

The MK45DP8 features two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and or write from either the 16-bit or the 8-bit port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location. Two modes of operation are provided. One mode allows contention to be ignored and both operations are allowed to proceed. In the other mode the on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete.

The 16-bit port is designed to allow easy interface to all 16-bit microprocessors by the inclusion of the ability to read and write in either a word or a byte mode. The $\overline{BHE}$ and $\overline{BLE}$ control lines enable the upper byte or the lower byte, respectively. When both lines are active, the MK45DP8 is in word mode.

### FUNCTIONAL DESCRIPTION

The MK45DP8 is a 16,384-bit dual port RAM that features two separate I/O ports. One port (the left) is organized as 1,024 16-bit words and the other (the right) as 2,048 8-bit words. Each allows independent access for reading or writing to any location in the memory.

### PORT ENABLING

The MK45DP8 features separate left- and right-left port chip enable controls ($\overline{CEL}$ and $\overline{CER}$) that activate their respective ports when they go low (see Table 1). When a port is active, it is allowed access to the entire memory array. When a chip enable signal is high, its side of the device remains in a standby power mode as long as it does not change state. Each $\overline{CE}$ also controls automatic power-down circuitry that is associated only with its port.

Thomson/Mostek

# MK45AM8(K)-60/70

1K x 16, 2K x 8 CMOS DUAL-PORT RAM

ADVANCE INFORMATION

MEMORY COMPONENTS



## FEATURES

- ☐ Organization
  - — Left Port: 1,024 x 16
  - — Right Port: 2,048 x 8
- ☐ High speed:
  - — 60 ns access
- ☐ Address/data 8-bit bus
- ☐ Fully static operation
- ☐ Full contention arbitration
- ☐ Simple microprocessor interface
- ☐ Output enable function
- ☐ Separate port power-down
- ☐ Advanced CMOS technology
- ☐ Low power:
  - — 60 mA (max) operating
- ☐ 52-pin PLCC

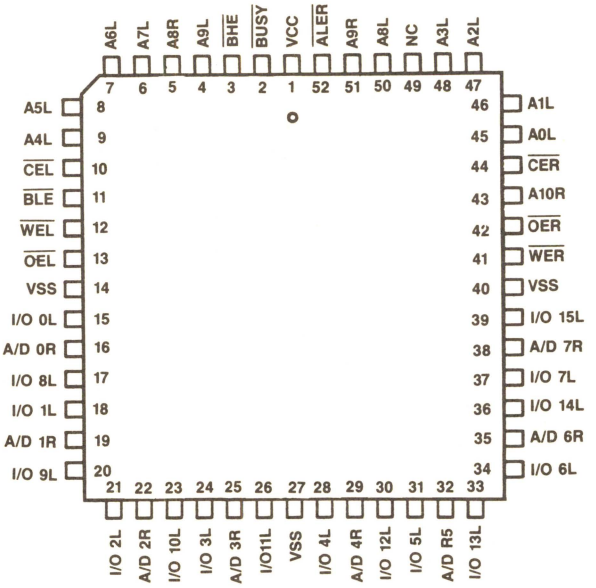


**Figure 1. Pin Configuration**

## DESCRIPTION

The MK45AM8 is a 16,384-bit dual-port static random access memory. Its left port is organized as 1,024 16-bit words and its right port as 2,048 8-bit words. The right port has been organized with an address/data multiplexed bus to allow easy interfacing with most of the standard processors. It is designed to facilitate the transfer of data between 16- and 8-bit microprocessors.

The MK45AM8 features two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and/or write from either the 16-bit or the 8-bit port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location. Two modes of operation are provided. One mode allows contention to be ignored and both operations to proceed. In the other mode, the on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the 16-bit port takes priority.

The 16-bit port is designed to allow easy interface to all 16-bit microprocessors by the inclusion of the ability to read and write in either a word or a byte mode. The $\overline{BHE}$ and $\overline{BLE}$ control lines enable the upper byte or the lower byte, respectively. When both control lines are active, the word mode is invoked.

Busy flags are open-drain for simple wired-OR operation.

Automatic power-down for each port is controlled independently by their chip enable inputs.



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THOMSON COMPONENTS MOSTEK

# MK68230

## PARALLEL INTERFACE/TIMER (PI/T)

PRELIMINARY

MICROCOMPUTER COMPONENTS

### FEATURES

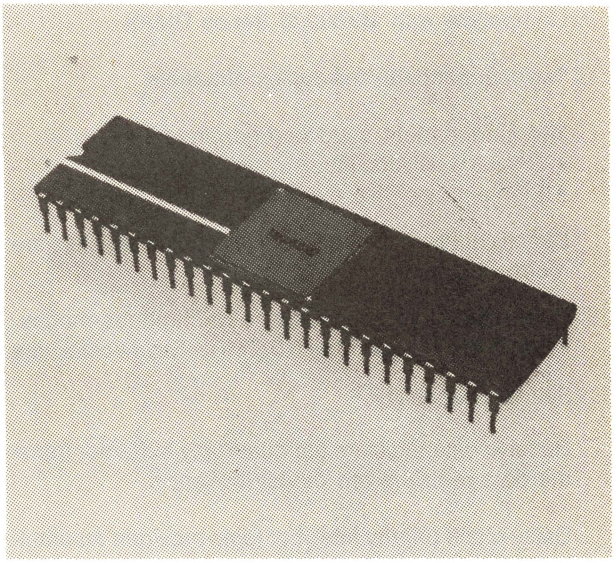
- ☐ 68000 Bus Compatible
- ☐ Port Modes Include:
  - Bit I/O
  - Unidirectional 8-bit and 16-bit
  - Bidirectional 8-bit and 16-bit
- ☐ Programmable Handshaking Options
- ☐ 24-bit Programmable Timer Modes
- ☐ Five Separate Interrupt Vectors
- ☐ Separate Port and Timer Interrupt Service Requests
- ☐ Registers are Read/Write and Directly Addressable
- ☐ Registers are Addressed for MOVEP (Move Peripheral) and DMAC Compatibility

### GENERAL DESCRIPTION

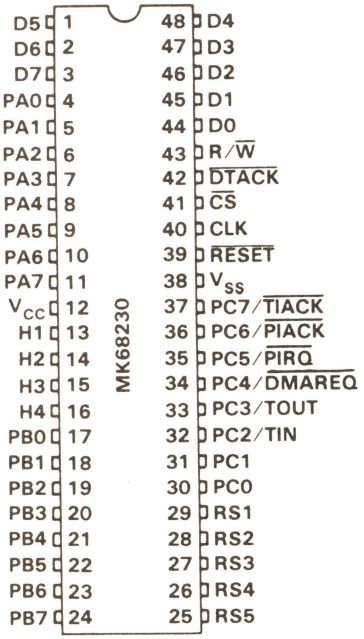
The MK68230 Parallel Interface/Timer (PI/T) provides versatile double-buffered parallel interfaces and an operating system oriented timer to MK68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether the port pins are inputs or outputs. In the bidirectional modes, the data direction registers are ignored, and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a DMA request pin for connection to the Direct Memory Access Controller or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), with the option of using a 5-bit prescaler. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed timer period. Also, it can be used for elapsed time measurement or as a device watchdog.

The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of Port

**MK68230**
**Figure 1**



### PIN ASSIGNMENT
**Figure 2**

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THOMSON COMPONENTS MOSTEK

# MK68564

## SERIAL INPUT/OUTPUT CONTROLLER

PRELIMINARY

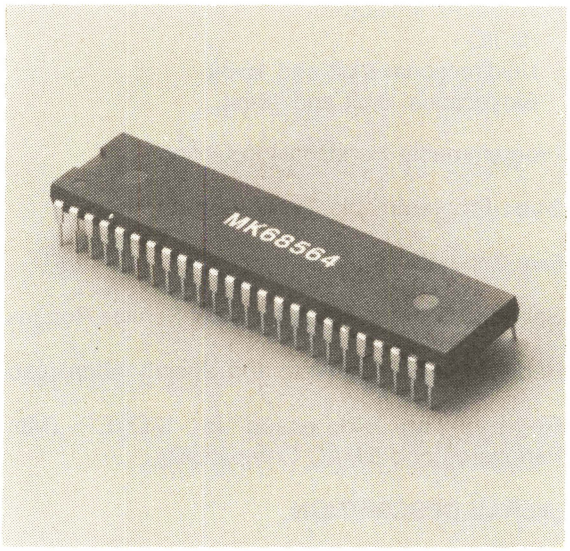
MICROCOMPUTER COMPONENTS



## FEATURES

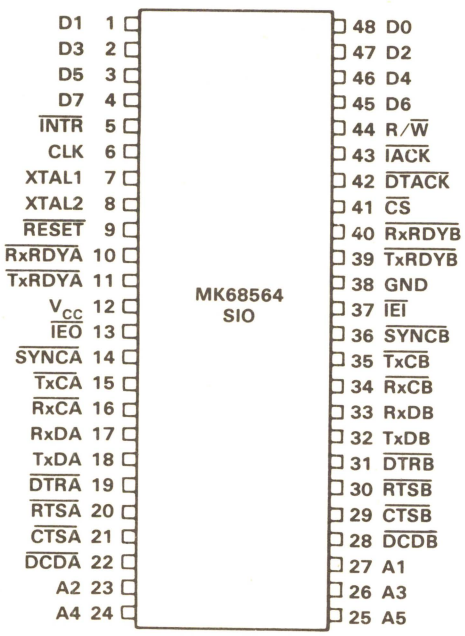
- ☐ Compatible with MK68000 CPU
- ☐ Compatible with MK68000 Series DMA's
- ☐ Two independent, full-duplex channels
- ☐ Two independent baud rate generators
  - Crystal oscillator input
  - Single-phase TTL clock input
- ☐ Directly addressable registers (all control registers are read/write)
- ☐ Data rate in synchronous or asynchronous modes
  - 0-1.25 M bits/second with 5.0 MHz system clock rate
- ☐ Self-test capability
- ☐ Receive data registers are quadruply buffered; transmit data registers are doubly buffered
- ☐ Daisy-chain priority interrupt logic provides automatic interrupt vectoring without external logic
- ☐ Modem status can be monitored
  - Separate modem controls for each channel
- ☐ Asynchronous features
  - 5, 6, 7, or 8 bits/character
  - 1, 1½, or 2 stop bits
  - Even, odd, or no parity
  - x1, x16, x32, and x64 clock modes
  - Break generation and detection
  - Parity, overrun, and framing error detection
- ☐ Byte synchronous features
  - Internal or external character synchronization
  - One or two sync characters in separate registers
  - Automatic sync character insertion
  - CRC-16 or CRC-CCITT block check generation and checking
- ☐ Bit synchronous features
  - Abort sequence generation and detection
  - Automatic zero insertion and deletion
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - Valid receive messages protected from overrun
  - CRC-CCITT block check generation and checking

**MK68564**
**Figure 1**




## PIN DESCRIPTION

**Figure 2**



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THOMSON COMPONENTS MOSTEK

# TS68000

## 16/32-BIT MICROPROCESSOR

ADVANCE INFORMATION

MICROCOMPUTER COMPONENTS

**ADVANCE INFORMATION**

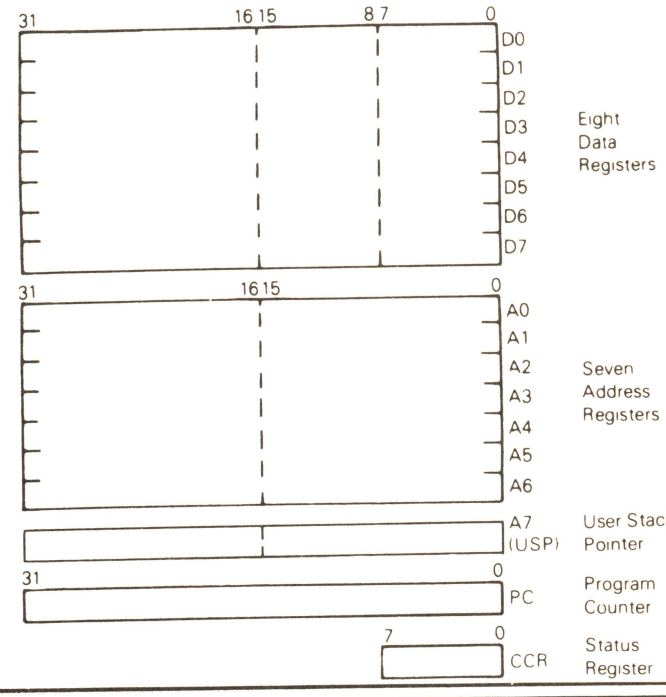
### 16-/32-BIT MICROPROCESSOR

The TS68000 is the first implementation of the 68000 16/32 microprocessor architecture. The TS68000 has a 16-bit data bus and 24-bit address bus while the full architecture provides for 32-bit address and data buses. It is completely code-compatible with the TS68008 8-bit data bus implementation of the 68000 and is downward code-compatible with the TS68020 32-bit implementation of the architecture. Any user-mode programs written using the TS68000 instruction set will run unchanged on the TS68008 and TS68020. This is possible because the user programming model is identical for all three processors and the instruction sets are proper sub-sets of the complete architecture.
The resources available to the TS68000 user consist of the following :

- 16 32-bit data and address registers
- 16 megabyte direct addressing range
- 56 powerful instruction types
- Operations on five main data types
- Memory mapped I/O
- 14 addressing modes
- 4 available versions : 8 MHz, 10 MHz, 12.5 MHz and 16 MHz.

As shown in the user programming model, the TS68000 offers 16 32-bit registers and a 32-bit program counter. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) operations. The second set of seven registers (A0-A6) and the user stack pointer (USP) may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long word operations. All of the 16 registers may be used as index registers.

**PROGRAMMING MODEL**

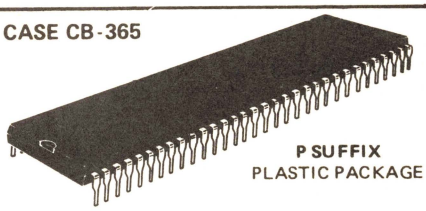



**HMOS**

HIGH-DENSITY, N-CHANNEL, SILICON-GATE, DEPLETION LOAD

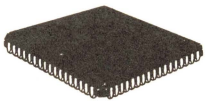
16-/32-BIT MICROPROCESSOR

**CASE CB-365**



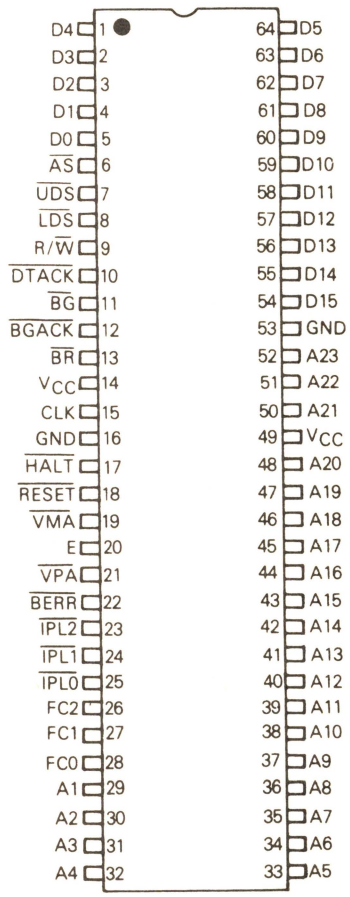
**P SUFFIX**
PLASTIC PACKAGE

**CASE CB-523**



**FN SUFFIX**
PLCC 68

**PIN ASSIGNMENT**

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THOMSON COMPONENTS MOSTEK

# MK5025

PRELIMINARY

COMMUNICATIONS PRODUCTS

Thomson/Mostek

## FEATURES

- ☐ CMOS
- ☐ Fully compatible with both 8 or 16 bit systems.
- ☐ System clock rate to 10 MHz.
- ☐ Data rate up to 7 MBPS with 64 byte FIFOs in each direction.
- ☐ Complete Data Link Layer Implementation.
- ☐ Compatible with X.25 LAPB, ISDN LAPD, X.32, and X.75 Link Level Protocols.
- ☐ 48-pin DIP nearly pin-for-pin compatible with the Mostek LANCE chip (MK68590).
- ☐ Buffer Management includes:
  - — Initialization Block
  - — Separate Receive and Transmit Rings
  - — Variable Descriptor Ring and Window Size.
- ☐ On chip DMA control and programmable burst length.
- ☐ Selectable single or extended control field.
- ☐ Programmable 1 or 2 byte address field and Global Address.
- ☐ Handles all HDLC (ADCCP) frame formatting:
  - — Zero bit insert and delete
  - — FCS generation and detection
  - — Frame delimiting with flags.
- ☐ Handles all error recovery, sequencing, and S and U frame control.
- ☐ Transparent mode with or without address filtering allows disabling X.25 processing for customized applications.
- ☐ Selectable FCS of 16 or 32 bits.
- ☐ Data Link Services:
  - — Compatible with ISO Data Link Services
  - — Compatible with LAPD Data Link Services.
- ☐ Testing Facilities:
  - — Internal Loopback
  - — Silent Loopback
  - — Optional Internal Data Clock Generation
  - — Self Test.

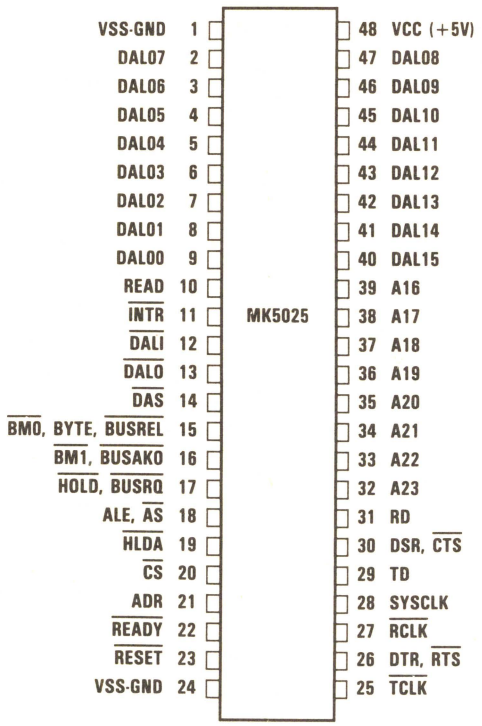


**Figure 1. Pin Connection**

- ☐ All inputs and outputs are TTL compatible.
- ☐ Programmable for Full or Half Duplex operation.
- ☐ Programmable minimum frame spacing on transmit (flags between frames).

## DESCRIPTION

The Thomson Components - Mostek X.25 Link Level Controller (MK5025) is a VLSI semiconductor device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. This includes frame formatting, transparency (so-called "bit-stuffing"), error recovery by retransmission, sequence number control, U (unnumbered) frame control, and S (supervisory) frame control. The MK5025 also supports X.32 (XID), X.75, and ISDN LAPD. The MK5025 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI-11, 8086, 8088, 8080, etc.


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THOMSON COMPONENTS MOSTEK

# MK5030P,K

## StarLAN HUB CHIP

COMMUNICATIONS PRODUCTS

### FEATURES

- ☐ Complete Hub Logic device which conforms to StarLAN specification.
- ☐ Supports Multi-point extension (MPE).
- ☐ Auto compensation for wiring reversal.
- ☐ 12 port HUB.
- ☐ Optional retime circuit.
- ☐ Cascadable. Two levels may be cascaded and still appear to the network as one yielding up to a 121 port HUB.
- ☐ Supports up to a 10 layer network.
- ☐ Auto preamble generation to eliminate bit loss.
- ☐ Selectable active carrier polarity sense.
- ☐ Jabber function isolates network failures.
- ☐ Optional minimum frame length enforcement.
- ☐ Collision detection:
  - multiple inputs
  - missing mid-bit transition
  - transitions too close together
  - transitions too far apart
  - AT&T release 1 collision presence signal.
- ☐ Digital phase lock loop.
- ☐ 6X clock yields 162 nS jitter tolerance.
- ☐ Transmit Data Trailer enforcement.
- ☐ Input protection at end of frame (20 $\mu$s).
- ☐ Pin selectable high-end HUB versus intermediate HUB.
- ☐ Optional internal pulse stretcher for carrier sense squelch.
- ☐ UPLINK and DOWNLINK active status outputs.

*NOTE: Crystal inputs have CMOS thresholds.

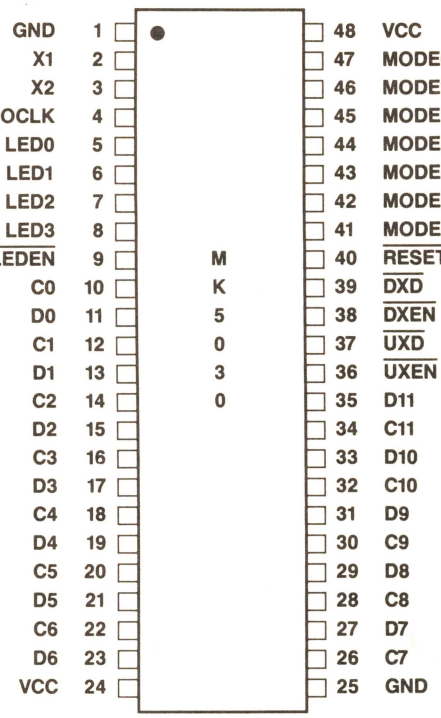


**Figure 1. MK5030 Pin Assignment**

- ☐ UPLINK and DOWNLINK collision status outputs.
- ☐ Per port jabber status output.
- ☐ On chip crystal oscillator circuitry.
- ☐ 35 mW typical power dissipation.
- ☐ CMOS technology.
- ☐ 48 pin DIP.
- ☐ Single 5-volt supply.
- ☐ All inputs and outputs TTL compatible.*
- ☐ Industrial version available.

### GENERAL DESCRIPTION

The MK5030-HUB is a 48 pin CMOS VLSI device that simplifies the design and implementation of a StarLAN compatible HUB. This chip provides all the digital logic necessary in a HUB.

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THOMSON COMPONENTS MOSTEK

# MK5033N

## MANCHESTER ENCODER/DECODER

COMMUNICATIONS PRODUCTS

Thomson/Mostek

### FEATURES

- ☐ Conforms to StarLAN specifications.
- ☐ Supports multi-point extension.
- ☐ Auto compensation for line reversal.
- ☐ Compatible with most Ethernet controller chips.
- ☐ Data rates DC to 2.66Mbps supported.
- ☐ Manchester or Differential Manchester data encoding/decoding.
- ☐ Full duplex or half duplex operation.
- ☐ Supports Star, Bus, or Point-to-Point network topologies.
- ☐ Collision detection circuitry with the following features:
  - Detects missing mid-bit transitions
  - Transitions too close together
  - Transitions too far apart
  - External collision input pin
  - Carrier dropout
  - Watchdog timer
  - AT&T Release 1 collision presence signal
  - Echo timeout
- ☐ Optional end-of-frame detection.
  - Input protection at end-of-frame
- ☐ Loopback capability.
- ☐ Receive carrier automatically converted to a level signal.
- ☐ Optional Watchdog timer to prevent continuous transmission.
- ☐ Optional Echo timer to signal error if transmitted frame is not received.
- ☐ Optional Heartbeat generation.
- ☐ In 82586/82588 mode, insensitive to extra bits ahead of preamble.

*Crystal inputs have CMOS thresholds.

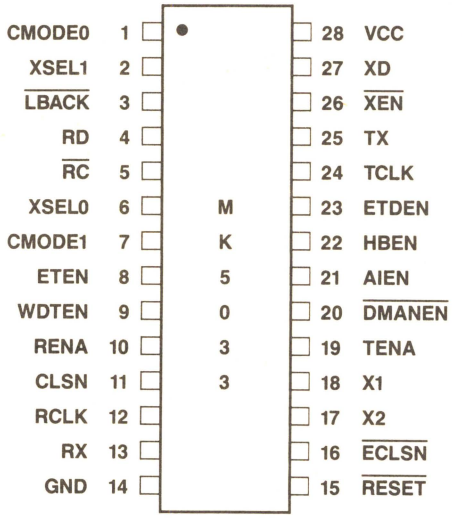


**Figure 1. MK5033 Pin Assignment**

- ☐ Digital phase-locked loop.
- ☐ On chip crystal oscillator, 16, 10, 8, or 6X operation.
- ☐ CMOS technology.
- ☐ 28-pin DIP.
- ☐ Single 5-volt supply.
- ☐ All inputs and outputs TTL compatible.*
- ☐ Outputs are also CMOS compatible.
- ☐ Industrial version available.

### GENERAL DESCRIPTION

The MK5033 is a general purpose Manchester Encoder/Decoder. It incorporates several features that make it an ideal StarLAN station chip. The MK5033 performs three functions. It encodes data from a controller chip into Manchester or Differential data. It decodes Manchester or Differential Manchester data from the line transceiver and produces NRZ data and clock for the controller chip. It also detects collision and signals the controller chip that a collision has occurred.



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THOMSON COMPONENTS MOSTEK

# MK5035N

## StarLAN ENCODER DECODER

COMMUNICATIONS PRODUCTS

### FEATURES

- ☐ Conforms with StarLAN specification.
- ☐ Supports multi-point extension.
- ☐ Auto compensation for line reversal.
- ☐ Compatible with Mostek MK68590 LANCE and Intel 82586/82588.
- ☐ Close pin compatibility with SEEQ8023.
- ☐ Data rates to 2.66Mbps supported.
- ☐ Manchester data encoding/decoding.
- ☐ Collision detection circuitry with the following features:
  - Detects missing mid-bit transitions
  - Transitions too close together
  - Transitions too far apart
  - External collision input pin
  - Carrier dropout
  - Watchdog timer
  - AT&T Release 1 collision presence signal
  - Echo timeout
- ☐ Receive end-of-frame detection.
  - Input protection at end-of-frame
- ☐ Loopback capability.
- ☐ Receive carrier automatically converted to a level signal.
- ☐ Echo timer to signal error if transmitted frame is not received.
- ☐ Heartbeat generation.
- ☐ In 82586 mode, insensitive to extra bits ahead of preamble
- ☐ Digital phase-locked loop.
- ☐ On chip crystal oscillator, 8X or 6X operation.

*Crystal inputs have CMOS thresholds.

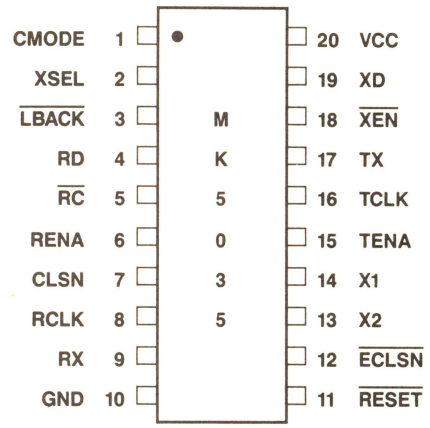


**Figure 1. MK5035 Pin Assignment**

- ☐ CMOS technology.
- ☐ 20-pin DIP.
- ☐ Single 5-volt supply.
- ☐ All inputs and outputs TTL compatible.*
- ☐ Outputs are also CMOS compatible.
- ☐ Industrial version available.

### GENERAL DESCRIPTION

The MK5035 is a Manchester Encoder/Decoder chip incorporating several features that make it an ideal StarLAN station chip. The MK5035 performs three functions. It encodes data from a controller chip into Manchester data. It decodes Manchester data from the line transceiver and produces NRZ data and clock for the controller chip. It also detects collisions and signals the controller chip that a collision has occurred.

The MK5035 has several enhancements for StarLAN and Multi-Point extension (MPE) StarLAN. These include auto compensation for wiring reversal, echo timer, external collision detect, watchdog timer, and heartbeat, among others.

Thomson/Mostek

THOMSON COMPONENTS MOSTEK

# MK68590 (P,N)

LOCAL AREA NETWORK CONTROLLER FOR ETHERNET

COMMUNICATIONS PRODUCTS

Thomson/Mostek

## FEATURES

- ☐ 100% compatible with Ethernet and IEEE 802.3 specifications
- ☐ Data packets moved by block transfers over a processor bus (on-board DMA controller 24-bit linear address space)
- ☐ Buffer management
- ☐ Packet framing
- ☐ Preamble and Cyclic Redundancy Check (CRC) insertion
- ☐ Preamble stripping and CRC verification
- ☐ General 16-bit microprocessor bus interface compatible with popular processors (68000, 8086, Z8000, LSI-11)
- ☐ Cable fault detection
- ☐ Multicast logical address filtration
- ☐ Collision handling and retry
- ☐ Scaled N-channel MOS VLSI technology
- ☐ 48-pin DIP
- ☐ Single 5-volt power supply
- ☐ Single phase TTL level clock
- ☐ All inputs and outputs TTL compatible
- ☐ Completely compatible with companion Serial Interface Adapter (SIA) chip MK68591/2.

## DESCRIPTION

The MK68590-LANCE™ (Local Area Network Controller for Ethernet) is a 48-pin VLSI device that simplifies the interfacing of a microcomputer or a minicomputer to an Ethernet Local Area Network. This chip operates in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several microprocessors.

LANCE is a trademark of Thomson Components - Mostek Corporation.

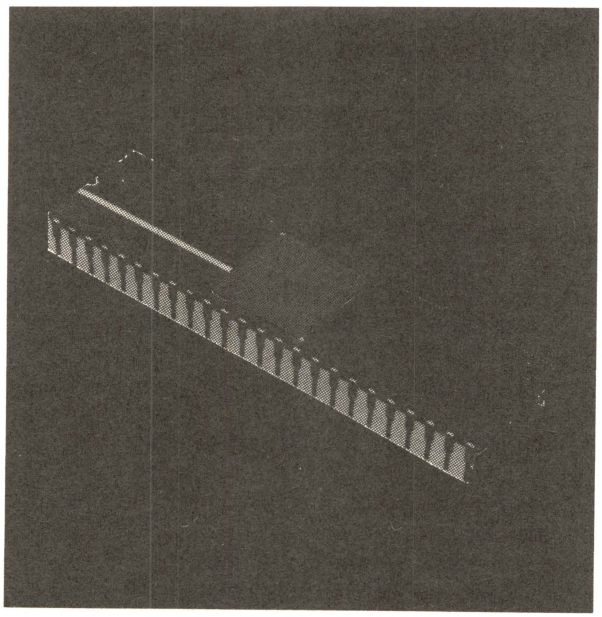

**Figure 1. MK68590**

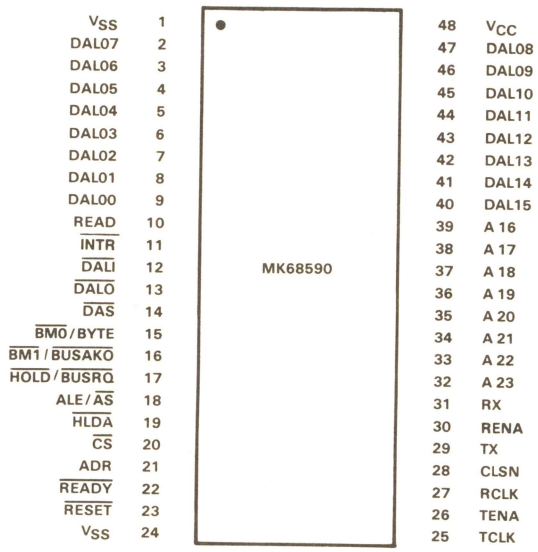


**Figure 2. LANCE Pin Assignment**



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THOMSON COMPONENTS MOSTEK

# TS68930 • TS68931

## PROGRAMMABLE SIGNAL PROCESSOR

ADVANCE INFORMATION

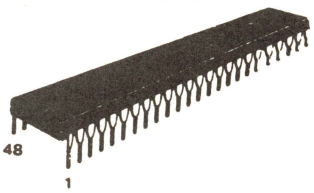
The TS68930/1 (Programmable Signal Processor) is a high-speed general purpose signal and arithmetic processor with on-chip memory, multiplier, ALU, accumulators and I/Os. It is organized in a parallel/pipeline structure to execute simultaneously one ALU, function, multiplication, two reads and one write operation and associated address calculation every 160 ns.

- Parallel/pipeline Harvard architecture
- 3 data-bus structure
- 3 data types : 16-bit real, 32-bit real
  : 16 + 16-bit complex number
- 2 versions : TS68930 (internal ROMs) 48-pin
  : TS68931 (external ROMs) 84-pin
- Pipeline complex multiplier
- 2 × 128 × 16-bit RAM
- 512 × 16-bit coefficient ROM
- 32-bit instruction bus
- 64 k × 32-bit external program space
- 68000 family compatibility
- Dual external buses : local/system

**HMOS2**

**PROGRAMMABLE SIGNAL PROCESSOR**

CASE CB-229



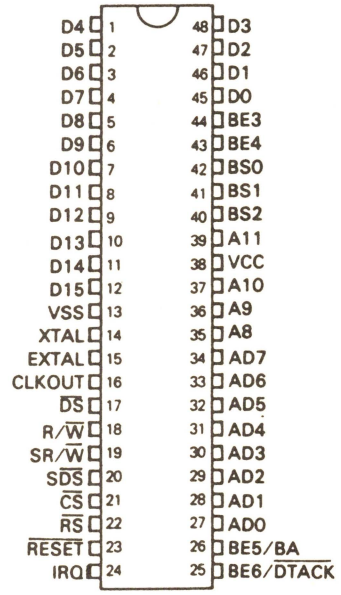

**TS68930**
**P SUFFIX**
PLASTIC PACKAGE

**TS68931**
**E SUFFIX**
LCCC 84

### TYPICAL APPLICATIONS

- Adaptive processing
- Complex numbers
- Digital filtering
- Fast Fourier transform
- Voice grade communication systems
- High-speed modems
- Speech processing
- Audio Frequencies
- Sonar/radar
- Image processing
- Robotics
- Graphics processing

**PIN ASSIGNMENT**




**TS68930**

Thomson/Mostek

THOMSON COMPONENTS MOSTEK

# TS68950/1/2

## MODEM TRANSMIT ANALOG INTERFACE

COMMUNICATIONS PRODUCTS

DATA SHEET

The TS68950 is a transmit (Tx) analog front-end circuit designed to implement high speed voice-grade modems up to 19200 bps according to the CCITT V.22, V.26, V.27, V.29, V.32 and V.33 recommendations or the BELL 212A, 208 and 209 standards. This circuit is particularly suited to work with the TS68951 receive (Rx) analog front-end circuit, the TS68952 clock generator and the TS68930/31 digital signal processors (DSPs).

Main features

- Two-channel digital to analog converter (DAC) for Tx and echo-cancelling signals.
- 6th-order low-pass filter (switched-capacitor filter with output continuous-time smoothing cell).
- Programmable attenuation over a 22 dB range with 2 dB steps.
- Direct interface with MPU standard 8 bit bus.

The TS68951 is the receive section of a MODEM analog front-end. The MODEM consists of TS68950/51/52 analog front-end chip sets and TS68930/31 digital signal processor; it is able to run voice-grade applications, which conforms to CCITT V.22/BIS, V.26/TER, V.27, V.29, V.32 and V.33 recommendations as well as BELL 212A, 208 and 209 standards.

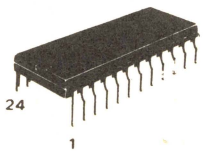
The TS68952 generates all the clock frequencies needed to implement standard voice-grade MODEMS up to 19200 bps according to the CCITT V.22, V.26, V.27, V.29, V.32 and V.33 or BELL 212A, 208 and 209 recommendations.

It can be associated with the TS68950 and the TS68951 to give a MODEM Analog Front-End Chip Set.

**CMOS**

**MODEM TRANSMIT ANALOG INTERFACE**

**CASE CB-68**

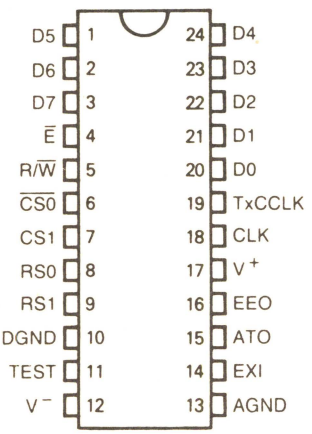



**P SUFFIX**
PLASTIC PACKAGE

**ALSO AVAILABLE**
**C SUFFIX**
CERAMIC PACKAGE

**J SUFFIX**
CERDIP PACKAGE

**PIN ASSIGNMENT**

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# TSG7515

## SINGLE CHIP DPSK AND FSK MODEM

## SINGLE CHIP DPSK AND FSK MODEM (BELL 212A - BELL 103 - V22 A/B)

The TSG7515 is a single chip DPSK and FSK voiceband modem, compatible with the applicable BELL and CCITT recommended standards for 212A sets including BELL 103 and V22 A-B type modems.

- Monolithic device includes both transmit and receive filters.
- Mixing analog and digital technics.
- Standard low cost crystal (4.9152 MHz).
- Available clock for microprocessor at 4.9152 MHz.
- Low power consumption - CMOS technology.
- Sharp adjacent channel rejection.
- Fixed equalization in transmitter and receiver.
- Test loops.
- Carrier detect output.
- CCITT and BELL signaling tone.
- 1200 bps and 600 bps bit synchronous format in DPSK.
- 1200 bps and 600 bps +1%, −2.5% or +2.3%, −2.5% character asynchronous format (8, 9, 10 or 11 bits) in DPSK.
- 0 to 300 bps in FSK.
- Break signal supervision.
- External voice band tone filtering available (i.e. 550 Hz or DTMF).
- CMOS and TTL compatible.
- Direct interface to THOMSON SEMICONDUCTEURS microprocessor family.
- Special line monitoring facility.

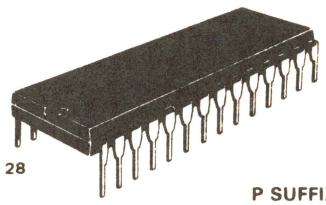
### MAIN OPERATING MODES

- Standard selection (BELL 212A/BELL 103/V22).
- Answer tone selection.
- Low speed mode selection.
- Channel selection (Answer/Originate).
- Synchronous/Asynchronous mode selection.
- 8 bits to 11 bits word length selection in character asynchronous format mode.
- Overspeed selection in character asynchronous format mode.
- Scrambler selection.
- 1800 Hz guard tone selection in V22.
- Test loop selection (Digital/Analog).

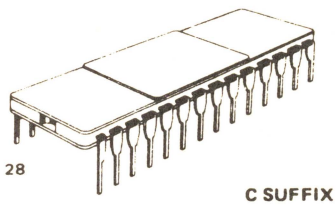
## CMOS

### SINGLE CHIP DPSK AND FSK MODEM

CASE CB-132

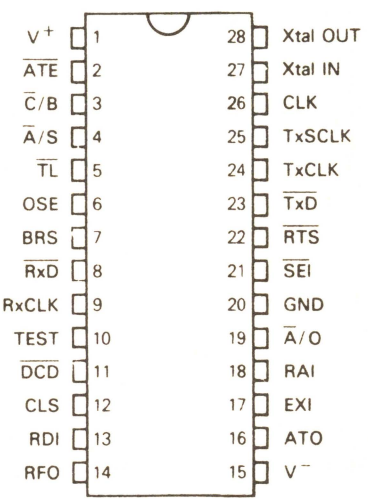



P SUFFIX
PLASTIC PACKAGE




C SUFFIX
CERAMIC PACKAGE

### PIN ASSIGNMENT




Thomson/Mostek

THOMSON COMPONENTS MOSTEK

# TS5070 • TS5071

MONOLITHIC PROGRAMMABLE CODEC/FILTER

COMBO 2ND GENERATION

ADVANCE INFORMATION

COMMUNICATIONS PRODUCTS

## ADVANCE INFORMATION

The TS5070 series are second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber and trunk line cards. Using advanced switched capacitor techniques, COMBO IIG combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and $\mu$-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable COMBO IIG to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output. The TS5070 provides 6 latches and the TS5071 5 latches.

- Complete CODEC and FILTER system including:
  - Transmit and receive PCM channel filters
  - $\mu$-law or A-law companding coder and decoder
  - Receive power amplifier drives 300 Ω
  - 4.096 MHz serial PCM data (max)
- Programmable Functions:
  - Transmit gain: 25.4 dB range, 0.1 dB steps
  - Receive gain: 25.4 dB range, 0.1 dB steps
  - Hybrid balance cancellation filter
  - Time-slot assignment: up to 64 slots/frame
  - 2 port assignment (TS5070)
  - 6 interface latches (TS5070)
  - A or $\mu$-law
  - Analog loopback
  - Digital loopback
- Direct interface to solid-state SLICs
- Simplifies transformer SLIC, single winding secondary
- Standard serial control interface
- 70 mW operating power (typ)
- 5 mW standby power (typ)
- Meets or exceeds all CCITT and LSSGR specifications
- TTL and CMOS compatible digital interfaces
- Second source of TP3070, TP3071

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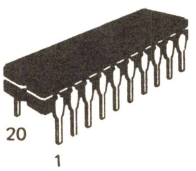
## CMOS

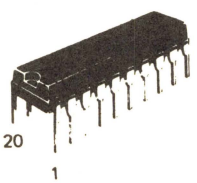
### CASES

**J20A**




**J SUFFIX**
CERDIP PACKAGE

**CB-194**




**P SUFFIX**
PLASTIC PACKAGE

**CB-520**

**FN SUFFIX**
PLCC PACKAGE

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THOMSON COMPONENTS MOSTEK

# ETC5057 • ETC5054

## MONOLITHIC SERIAL INTERFACE CODEC/FILTER

COMMUNICATIONS PRODUCTS

## MONOLITHIC SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

The ETC5064 ($\mu$-law) and ETC5067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in Figure 1, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

Similar to the ETC5050 family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capacity. The receive gain can be adjusted by means of two external resistors for an output level of up to ±6.6 V across a balanced 600 Ω load.

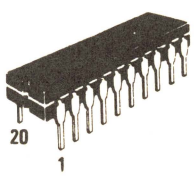
Also included is an Analog Loopback switch and $\overline{TS_X}$ output.

- Complete CODEC and filtering system including :
  - Transmit high-pass and low-pass filtering.
  - Receive low-pass filter with sin x/x correction.
  - Active RC noise filters.
  - $\mu$-law or A-law compatible COder and DECoder.
  - Internal precision voltage reference.
  - Serial I/O interface.
  - Internal auto-zero circuitry.
  - Receive push-pull power amplifiers.
- $\mu$-law ETC5064
- A-law ETC5067
- Meets or exceeds all D3/D4 and CCITT specifications.
- ±5 V operation.
- Low operating power - typically 70 mW
- Power-down standby mode - typically 3 mW
- Automatic power-down.
- TTL or CMOS compatible digital interfaces.
- Maximizes line interface card circuit density.

## CMOS

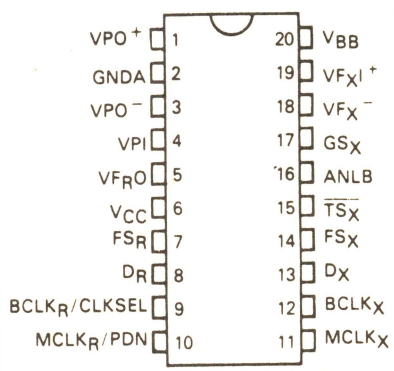
### MONOLITHIC SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

**CASE J20A**




20 Lead Cavity
**J SUFFIX**
CERDIP PACKAGE

**PIN ASSIGNMENT**

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THOMSON COMPONENTS MOSTEK

# ETC5067 • ETC5064

## MONOLITHIC SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

COMMUNICATIONS PRODUCTS

Thomson/Mostek

### MONOLITHIC SERIAL INTERFACE CODEC/FILTER

The ETC5057/ETC5054 family consists of A-law and μ-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in Figure 1, and a serial PCM interface. The devices are fabricated using double-poly CMOS process.

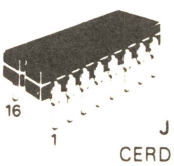
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ- law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both indrustry standard formats.

- Complete CODEC and filtering system (COMBO) including :
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with sin x/x correction
  - Active RC noise filters
  - A-law or μ-law compatible COder and DECoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
- A-law, 16-pins - ETC5057
- μ-law without signaling, 16-pins - ETC5054
- Meets or exceeds all D3/D4 and CCITT specifications
- ± 5V operation
- Low operating power - typically 60 mW
- Power-down standby - typically 3 mW
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Second source of TP3057, TP3054.

## CMOS

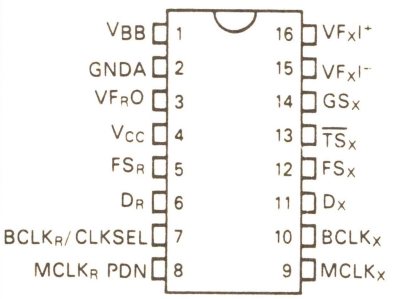
### MONOLITHIC SERIAL INTERFACE CODEC/FILTER

CASE J16A




J SUFFIX
CERDIP PACKAGE

### PIN ASSIGNMENT



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THOMSON COMPONENTS MOSTEK

# MK53762

REPERTORY DIALER

COMMUNICATIONS PRODUCTS

## FEATURES

- ☐ Single chip DTMF and pulse dialer.
- ☐ Stores 10 18-digit telephone numbers, including last number dialed.
- ☐ Softswitch changes signaling mode from pulse to tone.
- ☐ Single button redial of all ten memories.
- ☐ Flash key input initiates timed hook flash.
- ☐ 8 Tones Per Second dialing in Tone Mode and 10 PPS in Pulse Mode.
- ☐ DTMF active until key release.
- ☐ Minimum DTMF duration/separation guaranteed (74/54 ms).
- ☐ Pacifier tone provides audible indication of a valid key input for non-DTMF key entries.
- ☐ Powered from telephone line, low operating voltage for long loop applications.

## DESCRIPTION

The MK53762 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53762 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch, Flash, and 9 memories. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed, and the MEM keys provide single key access to all memory locations for auto-dialing.

The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

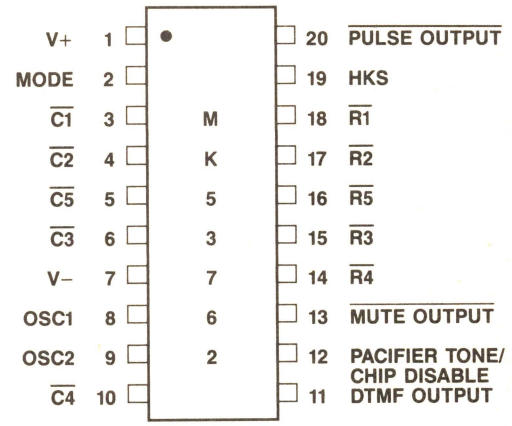


**Figure 1. Pin Connection**

| | | | | |
|---|---|---|---|---|
| 1 | 2 | 3 | FLASH | MEM 9 |
| 4 | 5 | 6 | PROG | MEM 8 |
| 7 | 8 | 9 | PAUSE | MEM 7 |
| * SOFTSWITCH | 0 | # | LND | MEM 6 |
| MEM 1 | MEM 2 | MEM 3 | MEM 4 | MEM 5 |

**Figure 2. Keypad Configuration**

The PAUSE key allows the user to insert a delay in dialing for functions such as the pause in accessing an outside line when redialing from a PABX.

The PROG key provides an easy way to program a number into any memory location (MEM 1 - MEM 9) whether on-hook or off-hook.

Thomson/Mostek

THOMSON COMPONENTS MOSTEK

# MK53721

## SINGLE NUMBER TONEPULSE WORLD DIALER

ADVANCE INFORMATION

COMMUNICATIONS PRODUCTS

### FEATURES

- ☐ Two select pins allow the user to select 16 different country options.
- ☐ Single chip mixed mode dialer allows dialing in either tone or pulse modes. A * or "SOFTSWITCH" key input can also be used to switch from Pulse to Tone mode operation and is stored in memory.
- ☐ 28 digit storage with LNR (last number redial)
- ☐ P.I.N. (personal identify number) protection method
- ☐ Hookswitch debounce, transients due to line reversals and drop-outs can be masked for a period determined by external RC.
- ☐ Powered from telephone line, low standby current and operating voltage.
- ☐ DTMF signal consistent with key entry period.
- ☐ Minimum DTMF signal duration/separation guaranteed.
- ☐ Timed PABX pause may be stored in Memory.
- ☐ Timed FLASH for extended timed Break recall.

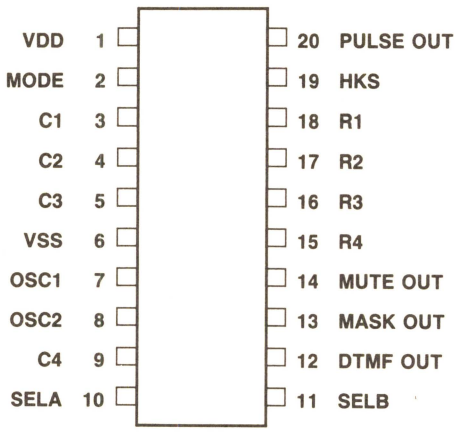


**Figure 1. MK53721 Pinout**

| | | | |
|---|---|---|---|
| 1 | 2 | 3 | FLASH |
| 4 | 5 | 6 | SS |
| 7 | 8 | 9 | PAUSE |
| * | 0 | # | LNR |

**Figure 2. MK53721 Keypad Configuration**





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THOMSON COMPONENTS MOSTEK

# MKB45F56(P,E)-80/81/82

262,144 x 1-BIT DYNAMIC RAM

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B

PRELIMINARY

GOVERNMENT PRODUCTS

## FEATURES

- ☐ Military temperature range ($-55°C \leq T_C \leq +110°C$)
- ☐ Recognized industry standard 16-pin configuration
- ☐ Single +5V (±10%) supply operation
- ☐ On-chip substrate bias generator for optimum performance
- ☐ 100 ns access time, 175 ns cycle time (MKB45F56-80)
  120 ns access time, 230 ns cycle time (MKB45F56-81)
  150 ns access time, 260 ns cycle time (MKB45F56-82)
- ☐ Fast page mode cycle time, 110 ns for -80
- ☐ Internal refresh counter, $\overline{CAS}$ before $\overline{RAS}$ refresh
- ☐ Extended $D_{OUT}$ hold using $\overline{CAS}$ control (Hidden Refresh)
- ☐ Common I/O capability using "early write"
- ☐ Read, Write, Read-Write, Read-Modify-Write, and Page-Mode capability
- ☐ All inputs TTL-compatible, low capacitance, and protected against static discharge
- ☐ 256 refresh cycles (4.0 ms)
  Pin 1 is not needed for refresh
- ☐ Desc Drawing 85152

## PIN FUNCTIONS

| | | | |
|---|---|---|---|
| $A_0$-$A_8$ | Address Inputs | $\overline{RAS}$ ($\overline{RE}$) | Row, Address Strobe |
| $\overline{CAS}$ ($\overline{CE}$) | Column Address Strobe | $\overline{WRITE}$ ($\overline{W}$) | Read/Write |
| $D_{IN}$(D) | Data In | $V_{CC}$ | Power (5V) |
| $D_{OUT}$(Q) | Data Out | $V_{SS}$ | GND |

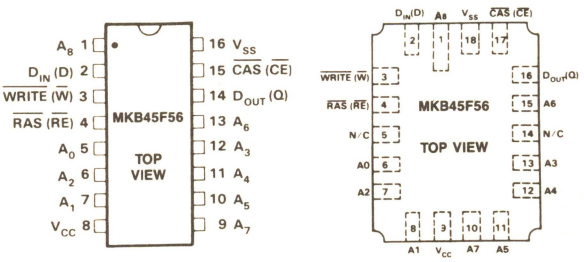


**Figure 1. Pin Connections**

## DESCRIPTION

The MKB45F56 is a 256K dynamic RAM, organized as 262,144 words by 1 bit. It is optimized for high speed, minimum cycle-time applications such as video and graphics memory, buffer memory, and mainframe memory. The MKB45F56 utilizes Mostek's latest scaled NMOS process technology for maximum circuit density, wide operating margins, and optimum reliability. Some features of this process include silicon gate, double-layer metal and poly interconnects, 1.5 micrometer channel lengths, and 150 Angstrom capacitor oxide for maximum critical charge.

Multiplexed address inputs permit the MKB45F56 to be packaged in a standard 16-pin DIP. The MKB45F56 is compatible with JEDEC standards for the 256K x 1 dynamic RAM.

The output of the MKB45F56 can be held valid up to 10$\mu$s by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

Thomson/Mostek

THOMSON COMPONENTS MOSTEK

# MKB4501(P,E)-88/80/81/82/83

512 WORD x 9 BIT BiPORT PARALLEL IN-OUT FIFO

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B

GOVERNMENT PRODUCTS

Thomson/Mostek

## FEATURES

- ☐ First-In, First-Out Memory Based Architecture
- ☐ Flexible 512 x 9 organization
- ☐ Low Power HCMOS technology
- ☐ Asynchronous and simultaneous read/write
- ☐ Bidirectional applications
- ☐ Fully expandable by word width or depth
- ☐ Empty and full warning flags
- ☐ Retransmit capability
- ☐ High performance
- ☐ Military temperature range ($-55°C \leq T_C \leq +125°C$)
- ☐ JAN Version (MIL-M-38510/250)

| Part No. | Access Time | R/W Cycle Time |
|---|---|---|
| MKB4501-88 | 80 ns | 100 ns |
| MKB4501-80 | 100 ns | 120 ns |
| MKB4501-81 | 120 ns | 140 ns |
| MKB4501-82 | 150 ns | 175 ns |
| MKB4501-83 | 200 ns | 235 ns |

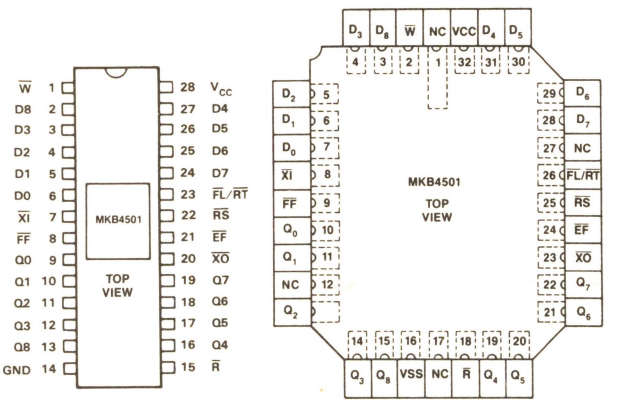


**Figure 1. Pin Connections**

## PIN NAMES

| | | | |
|---|---|---|---|
| $\overline{W}$ | = Write | $\overline{XI}$ | = Expansion In |
| $\overline{R}$ | = Read | $\overline{XO}$ | = Expansion Out |
| $\overline{RS}$ | = Reset | $\overline{FF}$ | = Full Flag |
| $\overline{FL}/\overline{RT}$ | = First Load/ Retransmit | $\overline{EF}$ | = Empty Flag |
| | | $V_{CC}$ | = 5 Volts |
| D | = Data In | GND | = Ground |
| Q | = Data Out | | |

## DESCRIPTION

The MKB4501 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MKB4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

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THOMSON COMPONENTS MOSTEK

# MKB4564(P,E)-82/83

65,536 x 1-BIT DYNAMIC RAM

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B

GOVERNMENT PRODUCTS

## FEATURES

- ☐ Military temperature range ($-55°C \leq T_C \leq +110°C$)
- ☐ Recognized industry standard 16-pin configuration from Mostek
- ☐ Single +5V (±10%) supply operation
- ☐ On-chip substrate bias generator for optimum performance
- ☐ Low power: 330 mW active, max
  27.5 mW standby, max
- ☐ 150 ns access time, 260 ns cycle time (MKB4564-82)
  200 ns access time, 345 ns cycle time (MKB4564-83)
- ☐ Extended $D_{OUT}$ hold using CAS control (Hidden Refresh)
- ☐ Common I/O capability using "early write"
- ☐ Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- ☐ All inputs TTL compatible, low capacitance, and protected against static charge
- ☐ Scaled POLY 5™ technology
- ☐ 128 refresh cycles (2 ms)
  Pin 9 is not needed for refresh
- ☐ JAN Version (MIL-M-38510/244)

## PIN FUNCTIONS

| | | | |
|---|---|---|---|
| $A_0$-$A_7$ | Address Inputs | $\overline{RAS}$ ($\overline{RE}$) | Row Address Strobe |
| $\overline{CAS}$ ($\overline{CE}$) | Column Address Strobe | $\overline{WRITE}$ ($\overline{W}$) | Read/ Write Input |
| $D_{IN}$(D) | Data In | $V_{CC}$ | Power (5V) |
| $D_{OUT}$(Q) | Data Out | $V_{SS}$ | GND |
| | | N/C | Not Connected |

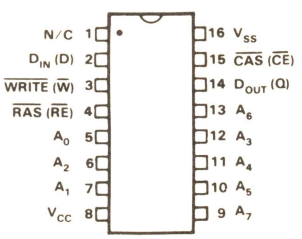
## DESCRIPTION

Organized 65,536 words by 1 bit, the MKB4564 is the successor to the industry standard MK4116. The MKB4564 utilizes Mostek's Scaled POLY 5™ process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal or external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permit the MKB4564 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MKB4564 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

The output of the MKB4564 can be held valid up to 10 $\mu$s by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as hidden refresh.

**DUAL-IN-LINE PACKAGE**




**LEADLESS CHIP CARRIER**

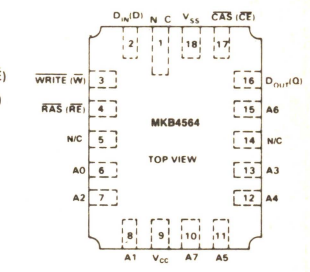



**Figure 1. Pin Connections**

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THOMSON COMPONENTS MOSTEK

# MKB41H87(P)-835/845/855

64K x 1 CMOS STATIC RAM

PROCESSED TO MIL-STD-883, CLASS B

PRELIMINARY

GOVERNMENT PRODUCTS

Thomson/Mostek

## FEATURES

- ☐ 35, 45, and 55 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 22-pin, 300 mil Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ JEDEC standard pinout
- ☐ Military temperature range ($-55°C \leq T_C \leq +125°C$)
- ☐ DESC Drawing 86015

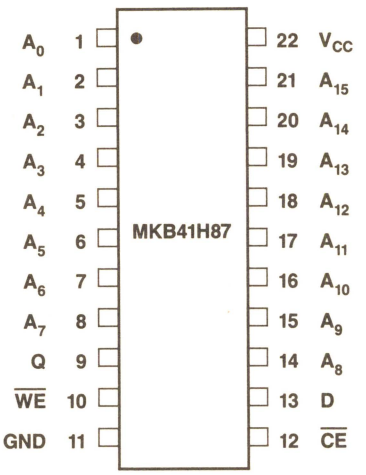


**Figure 1. Pin Connections**

## MKB41H87 TRUTH TABLE

| $\overline{CE}$ | $\overline{WE}$ | Mode | Q | Power |
|---|---|---|---|---|
| H | X | Deselect | High Z | Standby |
| L | L | Write | High Z | Active |
| L | H | Read | Data Out | Active |

## PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{15}$ - Address | $V_{CC}$ - + 5 volts |
| $\overline{CE}$ - Chip Enable | D - Data In |
| $\overline{WE}$ - Write Enable | Q - Data Out |
| GND - Ground | |

## DESCRIPTION

The MKB41H87 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The MKB41H87 requires only a single +5V ± 10 percent power supply, and it is fully TTL compatible.

The MKB41H87 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

## OPERATIONS

### READ MODE

The MKB41H87 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from one of 65,536 locations in the static storage array. Valid data will be available at the Data Output pin (Q) within $t_{AA}$ after the last address input signal is stable, providing that the $\overline{CE}$ access time is satisfied. If $\overline{CE}$ access time is not met, data access will be measured from the limiting parameter ($t_{CA}$) rather than the address. The state of the Data Output pin is controlled by the $\overline{CE}$ and $\overline{WE}$ control signals. The Q may be in an indeterminate state at $t_{CL}$, but the Q will always have valid data at $t_{AA}$.



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THOMSON COMPONENTS MOSTEK

# MKB45H64(P,E)-81/82/83

65,536 x 1-BIT DYNAMIC RAM

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B

PRELIMINARY

GOVERNMENT PRODUCTS

## FEATURES

- ☐ Military temperature range ($-55\,°C \leq T_C \leq +110\,°C$)
- ☐ Recognized industry standard 16-pin configuration from Mostek
- ☐ Single +5V (±10%) supply operation
- ☐ On-chip substrate bias generator for optimum performance
- ☐ Low power: 330 mW active, max
  27.5 mW standby, max
- ☐ 120 ns access time, 230 ns cycle time (MKB45H64-81)
  150 ns access time, 250 ns cycle time (MKB45H64-82)
  200 ns access time, 330 ns cycle time (MKB45H64-83)
- ☐ Extended $D_{OUT}$ hold using CAS control (Hidden Refresh)
- ☐ Common I/O capability using "early write"
- ☐ Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- ☐ All inputs TTL compatible, low capacitance, and protected against static charge
- ☐ 128 refresh cycles (4 ms)
  Pin 9 is not needed for refresh
- ☐ JAN Version (MIL-M-38510/244)
- ☐ DESC Drawing 82010

## PIN FUNCTIONS

| | | | |
|---|---|---|---|
| $A_0$-$A_7$ | Address Inputs | $\overline{RAS}$ ($\overline{RE}$) | Row Address Strobe |
| $\overline{CAS}$ ($\overline{CE}$) | Column Address Strobe | $\overline{WRITE}$ ($\overline{W}$) | Read/ Write Input |
| $D_{IN}$(D) | Data In | $V_{CC}$ | Power (5V) |
| $D_{OUT}$(Q) | Data Out | $V_{SS}$ | GND |
| | | N/C | Not Connected |

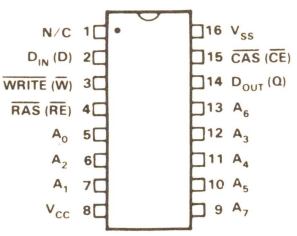
## DESCRIPTION

The MKB45H64 is a 64K dynamic RAM organized as 65,536 words by 1 bit. It utilizes Mostek's latest scaled NMOS process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal or external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permit the MKB45H64 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MKB45H64 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

The output of the MKB45H64 can be held valid up to 10 $\mu$s by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as hidden refresh.

DUAL-IN-LINE PACKAGE




LEADLESS CHIP CARRIER

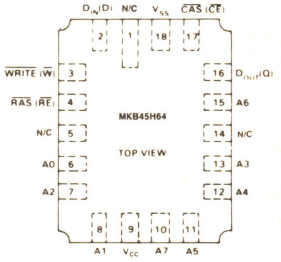



**Figure 1. Pin Connections**

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THOMSON COMPONENTS MOSTEK

# MKB4505M/4505S(J)-25,33,50

1K x 5 CMOS FIFO

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B

PRELIMINARY

GOVERNMENT PRODUCTS

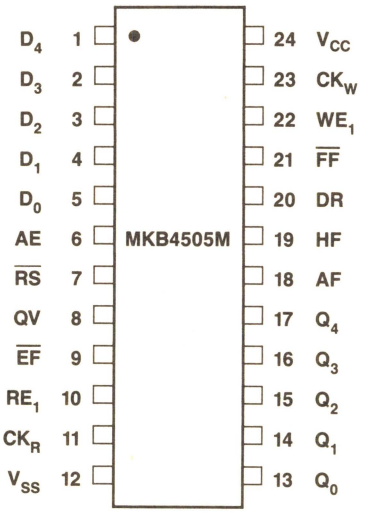


## FEATURES

- ☐ Military temperature range ($-55°C \leq T_C \leq 125°C$)
- ☐ 1024 x 5 Organization
- ☐ Very high performance

| Part No. | Cycle Time | Cycle Frequency | Access Time |
|---|---|---|---|
| 4505-25 | 25 ns | 40 MHz | 15 ns |
| 4505-33 | 33 ns | 30 MHz | 20 ns |
| 4505-50 | 50 ns | 20 MHz | 25 ns |

- ☐ Rising edge triggered clock inputs
- ☐ Supports free-running 40% to 60% Duty Cycle Clock Inputs
- ☐ Separate Read and Write Enable Inputs
- ☐ BiPORT™ RAM architecture allows fully asynchronous and simultaneous Read/Write operation
- ☐ Cascadable to any depth with no additional logic
- ☐ Width Expandable to more than 40 bits with no additional logic
- ☐ Half Full Status Flag
- ☐ Full and Empty Flags, Almost Full, Almost Empty, Input Ready, Output Valid Status Flags (4505M)
- ☐ Fully TTL Compatible
- ☐ 3 State Outputs



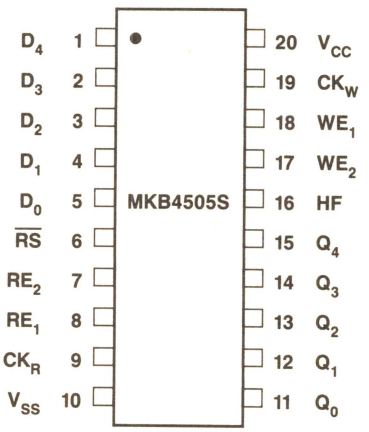




**Figure 1. Pin Configuration, 300 mil DIP**

## PIN NAMES

| | |
|---|---|
| $D_0$ - $D_4$ | - Data Input |
| $Q_0$ - $Q_4$ | - Data Output |
| $CK_W$, $CK_R$ | - Write and Read Clock |
| $WE_1$ | - Write Enable Input 1 |
| $\overline{RE_1}$ | - Read Enable Input 1 |
| $\overline{RS}$ | - Reset (Active Low) |
| HF | - Half Full Flag |
| $V_{CC}$, $V_{SS}$ | - +5 Volt, Ground |

**(4505M Only)**

| | |
|---|---|
| $\overline{FF}$, $\overline{EF}$ | - Full and Empty Flag (Active Low) |
| AF, AE | - Almost Full, Almost Empty Flag |
| DR, QV | - Input Ready, Output Valid |

**(4505S Only)**

| | |
|---|---|
| $WE_2$ | - Write Enable Input 2 |
| $RE_2$ | - Read Enable Input 2 (Rising Edge Triggered 3 State Control) |

Supersedes Publication No. 4420972 for Jan. 1987 and May 1987.

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# TOPAZ SEMICONDUCTOR

## CMOS/D-MOS ANALOG SWITCHES WITH DRIVERS

| TYPE NO. | CONFIG. | LOGIC RANGE (V) | ANALOG RANGE (V) | SWITCH(1) ON RESISTANCE (ohms) | SWITCH(2) OFF ISOLATION (dB) | SWITCH(2) BANDWIDTH (MHz) | $t_{ON}/t_{OFF}$ (nSec) | TEMP. RANGE | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|
| CDG201AK | 4xSPST | 0.8-2.4 | ±10 | 45 | 66 | 250 | 400/70 | MILITARY | 16-CDIP |
| CDG201BJ | 4xSPST | 0.8-2.4 | ±10 | 45 | 66 | 250 | 400/70 | INDUSTRIAL | 16-PDIP |
| CDG201BK | 4xSPST | 0.8-2.4 | ±10 | 45 | 66 | 250 | 400/70 | INDUSTRIAL | 16-CDIP |
| CDG201CJ | 4xSPST | 0.8-2.4 | ±10 | 45 | 66 | 250 | 400/70 | COMMERCIAL | 16-PDIP |
| CDG211CJ | 4xSPST | 0.8-2.4 | ±10 | 45 | 66 | 250 | 400/70 | COMMERCIAL | 16-PDIP |
| CDG211DY | 4xSPST | 0.8-2.4 | ±10 | 45 | 64 | 250 | 400/70 | INDUSTRIAL | S0-16 SMD |
| CDG308AK | 4xSPST | 1.0-4.5 | ±10 | 45 | 66 | 250 | 140/80 | MILITARY | 16-CDIP |
| CDG308BJ | 4xSPST | 1.0-4.5 | ±10 | 45 | 66 | 250 | 140/80 | INDUSTRIAL | 16-PDIP |
| CDG308BK | 4xSPST | 1.0-4.5 | ±10 | 45 | 66 | 250 | 140/80 | INDUSTRIAL | 16-CDIP |
| CDG308CJ | 4xSPST | 1.0-4.5 | ±10 | 45 | 66 | 250 | 140/80 | COMMERCIAL | 16-PDIP |
| CDG309AK | 4xSPST | 1.0-4.5 | ±10 | 45 | 66 | 250 | 140/80 | MILITARY | 16-CDIP |
| CDG309BJ | 4xSPST | 1.0-4.5 | ±10 | 45 | 66 | 250 | 140/80 | INDUSTRIAL | 16-PDIP |
| CDG309BK | 4xSPST | 1.0-4.5 | ±10 | 45 | 66 | 250 | 140/80 | INDUSTRIAL | 16-CDIP |
| CDG309CJ | 4xSPST | 1.0-4.5 | ±10 | 45 | 66 | 250 | 140/80 | COMMERCIAL | 16-PDIP |
| CDG2214BJ | 1xSPST | 1.0-4.5 | ±10 | 50 | 80 | 250 | 40/20 | INDUSTRIAL | 8-PDIP |
| CDG2269CJ | 2xSPDT | 1.0-4.5 | ±10 | 25/50 | 80 | 125 | 140/80 | COMMERCIAL | 16-PDIP |
| CDG2269CY | 2xSPDT | 1.0-4.5 | ±10 | 25/50 | 80 | 125 | 140/80 | COMMERCIAL | S0-16 SMD |
| CDG4308BJ | 4xSPST | 1.0-4.5 | ±10 | 45 | 72 | 250 | 140/80 | INDUSTRIAL | 20-PDIP |
| CDG4309BJ | 4xSPST | 1.0-4.5 | ±10 | 45 | 72 | 250 | 140/80 | INDUSTRIAL | 20-PDIP |
| CDG5341AK | 2xSPST | 1.0-4.5 | ±10 | 110 | 80 | 125 | 150/120 | MILITARY | 14-CDIP |
| CDG5341BJ | 2xSPST | 1.0-4.5 | ±10 | 110 | 80 | 125 | 150/120 | INDUSTRIAL | 14-PDIP |
| CDG5341BK | 2xSPST | 1.0-4.5 | ±10 | 110 | 80 | 125 | 150/120 | INDUSTRIAL | 14-CDIP |
| CDG5341CJ | 2xSPST | 1.0-4.5 | ±10 | 110 | 80 | 125 | 150/120 | COMMERCIAL | 14-PDIP |

V± = ±15V (1) typical @ $V_{ANALOG}$ = +2.0V (2) typical @ f = 10MHz, $R_L$ = 50 ohms

## CMOS/D-MOS ANALOG MULTIPLEXERS WITH ENABLE

| TYPE NO. | CONFIG. | LOGIC RANGE (V) | ANALOG RANGE (V) | SWITCH(1) ON RESISTANCE (ohms) | ALL CHANNEL(2) CROSS TALK (dB) | SWITCH(2) BANDWIDTH (MHz) | $t_{ON}/t_{OFF}$ (nSec) | TEMP. RANGE | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|
| CDG4500AK | 4-Channel | 1.0-4.5 | ±10 | 40 | 66 | 250 | 150/120 | MILITARY | 16-CDIP |
| CDG4500BJ | 4-Channel | 1.0-4.5 | ±10 | 40 | 66 | 250 | 150/120 | INDUSTRIAL | 16-PDIP |
| CDG4500BK | 4-Channel | 1.0-4.5 | ±10 | 40 | 66 | 250 | 150/120 | INDUSTRIAL | 16-CDIP |
| CDG4500CJ | 4-Channel | 1.0-4.5 | ±10 | 40 | 66 | 250 | 150/120 | COMMERCIAL | 16-PDIP |

V± = ±15V (1) typical @ $V_{ANALOG}$ = +2.0V (2) typical @ f = 10MHz, $R_L$ = 50 ohms

## D-MOS ANALOG SWITCHES WITHOUT DRIVERS

| TYPE NO. | CONFIG. | ANALOG RANGE (V) | SWITCH ON(1) RESISTANCE (ohms) | CHANNEL-TO-CHANNEL(2) CROSS TALK (dB) | $t_{ON}/t_{OFF}$ (nSec) | TEMP. RANGE | PACKAGE |
|---|---|---|---|---|---|---|---|
| SD5000N | 4xSPST | ±10 | 70 | 80 | 1.5/2.0 | COMMERCIAL | 16-PDIP |
| SD5001N | 4xSPST | ±5.0 | 70 | 80 | 1.5/2.0 | COMMERCIAL | 16-PDIP |
| SD5002N | 4xSPST | ±7.5 | 70 | 80 | 1.5/2.0 | COMMERCIAL | 16-PDIP |
| SD5400CY | 4xSPST | ±10 | 70 | 80 | 1.5/2.0 | COMMERCIAL | S0-14 SMD |
| SD5401CY | 4xSPST | ±5.0 | 70 | 80 | 1.5/2.0 | COMMERCIAL | S0-14 SMD |
| SD5402CY | 4xSPST | ±7.5 | 70 | 80 | 1.5/2.0 | COMMERCIAL | S0-14 SMD |

(1) maximum @ $V_{GS}$ = 5.0V, $I_D$ = 1mA, $V_{SB}$ = 0 (2) typical @ f = 10 MHz, $R_L$ = 50 ohms

***TOPAZ SEMICONDUCTOR INC.***
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# Toshiba.
# World Leader in 1MB and 256K DRAMs.

**Toshiba was the first to introduce the 1MB DRAM and is now the world's leading supplier.** We offer fast page, nibble or static column operating modes in CMOS. Production quantities of these devices are available in DIP, SOJ and ZIP packages.

**1,048,576 WORDS × 1 BIT DYNAMIC RAM**
SILICON GATE CMOS
*This is advanced information and specifications are subject to change without notice.

**TC511000P/J/Z-85**
**TC511000P/J/Z-10**
**TC511000P/J/Z-12**

The TC511000P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000P/J/Z utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000P/J/Z to be packaged in a standard 18 pin plastic DIP, 20 pin plastic SOJ and 20 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

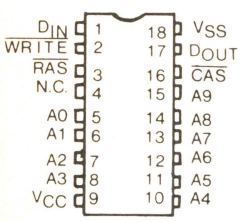
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

| | | TC511000P/J/Z-85 | TC511000P/J/Z-10 | TC511000P/J/Z-12 |
|---|---|---|---|---|
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 85ns | 100ns | 120ns |
| $t_{AA}$ | Column Address Access Time | 45ns | 50ns | 60ns |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 25ns | 25ns | 30ns |
| $t_{RC}$ | Cycle Time | 165ns | 190ns | 220ns |
| $t_{PC}$ | Fast Page Mode Cycle Time | 50ns | 55ns | 70ns |

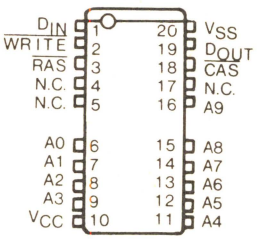
- Single power supply of 5V ± 10% with a built-in $V_{BB}$ generator
- Low Power
  330mW MAX. Operating (TC511000P/J/Z-10)
  275mW MAX. Operating (TC511000P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Fast Page Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511000P
  Plastic SOJ: TC511000J
  Plastic ZIP: TC511000Z

## PIN CONNECTION (TOP VIEW)

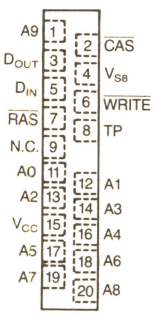
- Plastic DIP




- Plastic SOJ



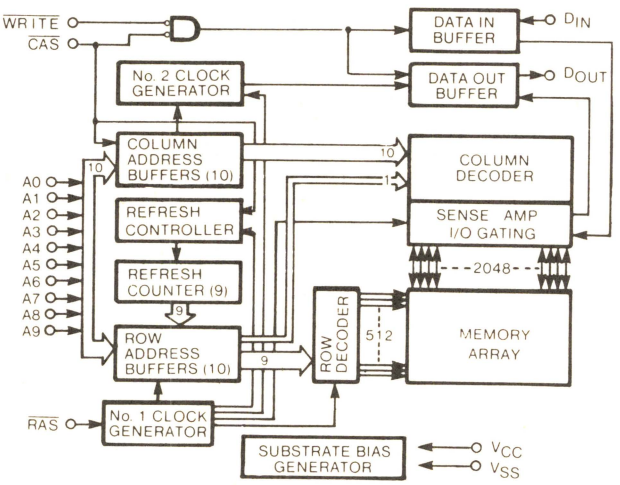

- Plastic ZIP




## PIN NAMES

| | |
|---|---|
| A0~A9 | Address Inputs |
| $\overline{RAS}$ | Row Address Strobe |
| $D_{IN}$ | Data In |
| $D_{OUT}$ | Data Out |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WRITE}$ | Read/Write Input |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| N.C. | No Connection |

## BLOCK DIAGRAM

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# Toshiba.
# World Leader in 256K SRAMs.

**Toshiba is the world leader in CMOS and NMOS Static RAMs and was one of the first suppliers of the 256K CMOS SRAM.**

32,768 WORDS × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

**TC55257APL-85/AFL-85/APL-85L/AFL-85L**
**TC55257APL-10/AFL-10/APL-10L/AFL-10L**
**TC55257APL-12/AFL-12/APL-12L/AFL-12L**

The TC55257APL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.) and minimum cycle time of 85ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is typical 2μA. The TC55257APL has two control inputs: Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus theTC55257APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

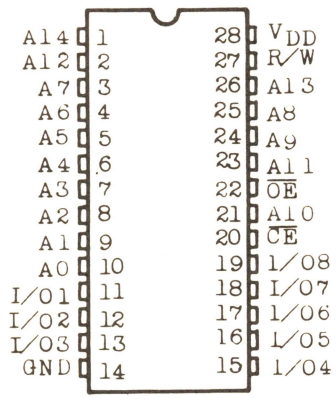
The TC55257APL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

- Low Power Dissipation
  27.5 mW/MHz(Max.) Operating
- Standby Current
  100μA(Max.): TC55257APL-85/AFL-85
  APL-10/AFL-10
  APL-12/AFL-12
  2μA(Max.): TC55257APL-85L/AFL-85L
  (Ta = 25°C) APL-10L/AFL-10L
  APL-12L/AFL-12L
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$
- Data Retention Supply Voltage: 2.0~5.5V
- Access Time

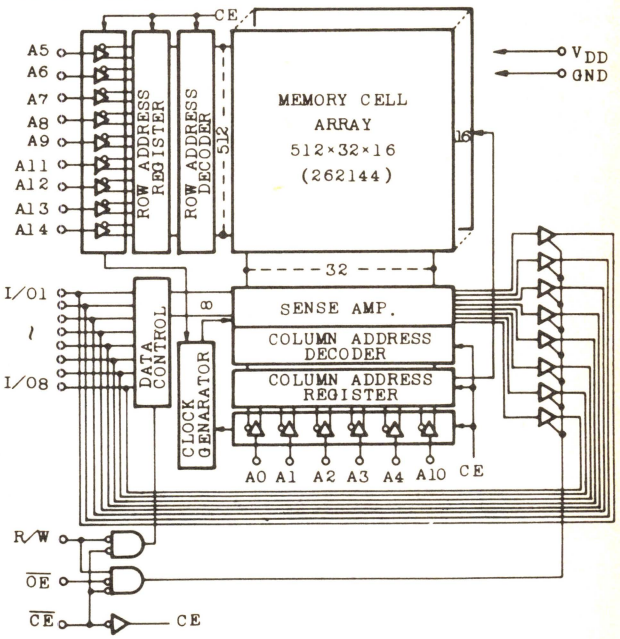
| | TC55257APL-85 /AFL-85/APL-85L /AFL-85L | TC55257APL-10 /AFL-10/APL-10L /AFL-10L | TC55257APL-12 /AFL-12/APL-12L /AFL-12L |
|---|---|---|---|
| Access Time (MAX.) | 85ns | 100ns | 120ns |
| $\overline{CE}$ Access Time (MAX.) | 85ns | 100ns | 120ns |
| Output Enable Time (MAX.) | 45ns | 50ns | 60ns |

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic FP Package

PIN CONNECTION (TOP VIEW)




BLOCK DIAGRAM




PIN NAMES

| | |
|---|---|
| $A_0$~$A_{14}$ | Address Inputs |
| R/W | Read/Write Control Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{CE}$ | Chip Enable Input |
| $I/O_1$~$I/O_8$ | Data Input/Output |
| $V_{DD}$ | Power (+5V) |
| GND | Ground |

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# Toshiba.
# World Leader in 1MB EPROMs.

**Toshiba has the EPROMs you need in the densities you want: 256K and 1MB in CMOS – 64K, 128K and 512K in NMOS.**

**1 MEGABIT (131,072 WORD × 8 BIT)**
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

**TC571000D-20, TC571000D-25**
**TC571001D-20, TC571001D-25**

The TC571000D/TC571001D is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571000D uses a JEDEC standard pin configuration while the TC571001D is compatible with 28 pin 1M bit Mask ROM. Both products are packed in a 32 pin standard cerdip package.

TC571000D/TC571001D is fabricated with the CMOS technology.

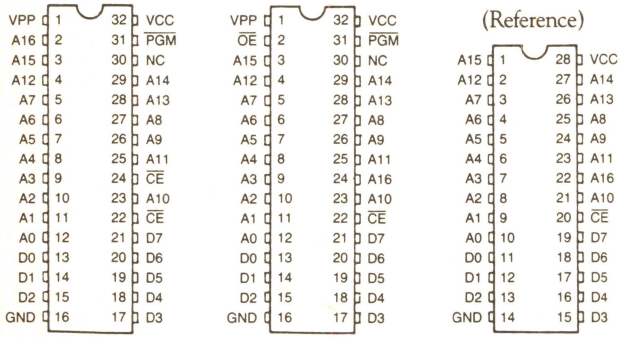
- Peripheral circuit: CMOS
- Memory cell: NMOS
- Fast access Time
  TC571000D-20/TC571001D-20: 200ns
  TC571000D-25/TC571001D-25: 250ns

Advanced circuit technique provides both high speed and low power features with a maximum operating current of 30mA 15.0MHz and an access time of 200ns/250ns.

The programming times of the TC571000D/TC571001D excluding overhead times of the EPROM programmer is only 14 seconds by using the high speed programming algorithm.

- Low power dissipation
  Active: 30mA/5.0MHz
  Standby: 100μA (Ta = 85°C)
- Single 5V power supply
- Wide operating temperature range: −40~85°C
- Full static operation
- High speed programming operation: tpw 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin: TC571000D
- 1M MROM compatible: TC571001D
- Standard 32 pin DIP cerdip package

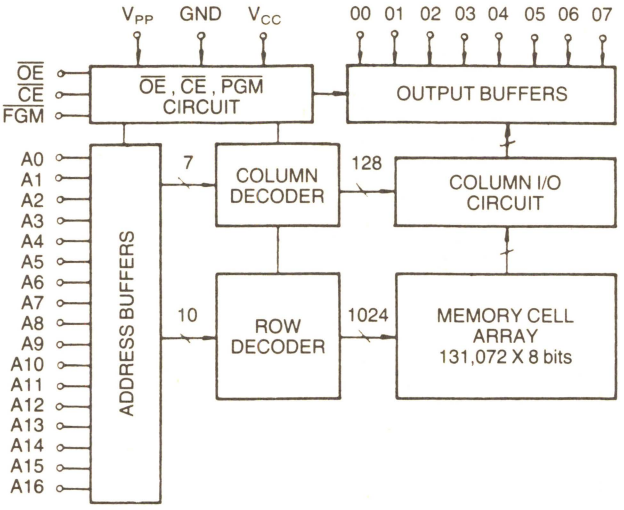
## PIN CONNECTION (TOP VIEW)




## PIN NAMES

| | |
|---|---|
| $A_0 \sim A_{16}$ | Address inputs |
| $D_0 \sim D_7$ | Outputs (Inputs) |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{PGM}$ | Program Control Input |
| $V_{CC}$ | $V_{CC}$ Supply Voltage |
| $V_{PP}$ | Program Supply Voltage |
| GND | Ground |
| N.C. | No connection |

## BLOCK DIAGRAM

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# World's Fastest 2MB and 1MB ROMs.

**Toshiba leads the world in high-speed, high-density mask ROMs: 1MB and 2MB in CMOS . . . 256K in NMOS and CMOS.**

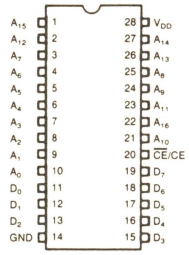
## 1MB (128K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE CMOS — TC531000AP

The TC531000AP is a 1,048,576 bit read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in microprocessor program memory and especially character generation. The TC531000AP, using CMOS technology, is most suitable for low power applications where battery operations are required.

The TC531000AP has one chip enable input $\overline{CE}$/CE, programmable for device selection.

The TC531000AP is molded in a 28 pin standard plastic package and is 0.6 inch in width.

### PIN CONNECTION – 28 PIN (TOP VIEW)




### PIN NAMES

| | |
|---|---|
| $A_0 \sim A_{16}$ | Address Inputs |
| $D_0 \sim D_7$ | Data Outputs |
| $\overline{CE}$/CE | Chip Enable Input |
| $V_{DD}$ | Power Supply |
| GND | Ground |

- Single 5V Power Supply
- Access Time: 150ns (Max.)
- Power Dissipation
  Operating Current: 40mA (Max.)
  Standby Current: 20μA (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 28 pin 600 mil width DIP Plastic Package
- Fully Static Operation
- Programmable Chip Enable

## 2MB (256K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE CMOS — TC532000P

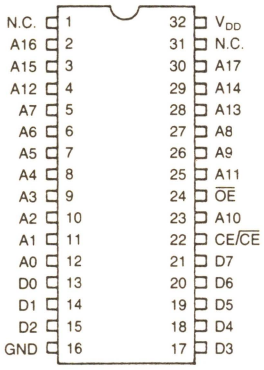
The TC532000P is a 2,097,152 bit read only memory organized as 262,144 words by 8 bits with a low bit cost, thus being suitable for use in microprocessor program memory, data memory, and especially character generation. The TC532000P, using CMOS technology, is most suitable for low power applications where battery operations are required.

The TC532000P has one programmable chip enable input $\overline{CE}$/CE for device selection.

The TC532000P is molded in a 32 pin standard plastic package and is 0.6 inch in width.

- Single 5V Power Supply
- Access Time: 200 ns (Max.)
- Power Dissipation
  Operating Current: 30mA (Max.)
  Standby Current: 20μA (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 32 pin 600 mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

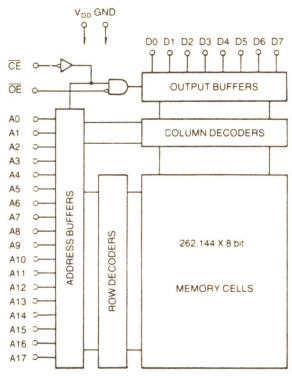
### PIN CONNECTION – 32 PIN (TOP VIEW)




### PIN NAMES

| | |
|---|---|
| $A_0 \sim A_{17}$ | Address Inputs |
| $D_0 \sim D_7$ | Data Outputs |
| $\overline{OE}$ | Output Enable Input |
| CE/$\overline{CE}$ | Chip Enable Input |
| $V_{DD}$ | Power Supply |
| GND | Ground |
| N.C. | No connection |

### BLOCK DIAGRAM (2MB)

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# Toshiba.
# The Power in MPUs.

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## MICROCONTROLLER 8048/8049

| DEVICE | PKG | DESCRIPTION |
|---|---|---|
| TMP8049A | P,T | 8 BIT MCU, RAM, ROM, I/O - 11 MHz |
| TMP8048A | P,T | 8 BIT MCU, RAM, ROM, I/O - 11 MHz |
| TMP8243 | P | I/O EXPANDER |
| TMP80C50A | P,F,T | 8 BIT CMOS MCU, RAM, ROM, I/O - 6MHz, 11 MHz |
| TMP80C49A | P,F,T | 8 BIT CMOS MCU, RAM, ROM, I/O - 6MHz, 11 MHz |
| TMP80C48A | P,F,T | 8 BIT CMOS MCU, RAM, ROM, I/O - 11 MHz |
| TMP82C43 | P | CMOS I/O EXPANDER |
| TMP8039 | P | ROMLESS VERSION OF TMP8049 - 6MHz, 11MHz |
| TMP8035 | P | ROMLESS VERSION OF TMP8048 - 6MHz, 11MHz |
| TMP80C40A | P | ROMLESS VERSION OF TMP80C50A - 6MHz, 11MHz |
| TMP80C39A | P | ROMLESS VERSION OF TMP80C49A - 6MHz, 11MHz |
| TMP80C35A | P | ROMLESS VERSION OF TMP80C48A - 6MHz, 11MHz |

## SPEECH PRODUCTS

### ADM – SPEECH RECORDING & REPRODUCTION

| PART NUMBER | FUNCTION |
|---|---|
| T6668 | RECORDING/REPRODUCTION, DRAM TYPE |
| TC8831F | RECORDING/REPRODUCTION 1 MEG DRAM TYPE* |
| TC8830F | RECORDING/REPRODUCTION, SRAM/EPROM |
| T6667 | REPRODUCTION ONLY, BUILT-IN MROM |

*Available Dec. '87

### VOICE RECOGNITION

| | |
|---|---|
| T6658A | SPEAKER DEPENDENT WORK RECOGNITION |

### PARCOR – SPEECH SYNTHESIS

| | |
|---|---|
| T6803 | SPEECH SYNTHESIS, BUILT IN 64K MROM |
| T6721 | SPEECH SYNTHESIS |
| T6772 | 64K MASKED ROM |
| T6684 | 128K MASKED ROM |

## OTHER PERIPHERALS

| TYPE NUMBER | | DESCRIPTION |
|---|---|---|
| TC8250AP | RTC | REAL TIME CLOCK/CALENDAR |
| TC8505AP | CRTC | CRT DISPLAY CONTROLLER |
| TC8505AF | | |
| TMPZ80C47C | HDC | HARD DISK CONTROLLER |
| TC8565AP/AF | FDC | FLOPPY DISK CONTROLLER INCLUDES VFO |
| TC8566AF | | |
| TC8570P | UART | UART FOR PC |
| TC8570F | | |
| TC8576AF | CPC | CENTRONICS I/O + RS232C |
| TC8577AP | | CENTRONICS OUTPUT + RS232C |
| TC8578AP | | CENTRONICS INPUT + RS232C |
| TC8600F | FDMC | 5.25" FD MECHANISM CONTR'L |
| TC8601F | | 3.5" FD MECHANISM CONTR'L |
| TC8602F | | 3.5" FD MECHANISM CONTR'L |
| T7779* | LCD/CRTC | LCD/CRTC CONTROLLER 640 x 400 DOT MATRIX |
| BAC84110 | MULTIBUS II BUS ARBITER CONTROLLER | |
| MIC84120 | MULTIBUS II MESSAGE INTERRUPT CONTROLLER | |

*OTHER LCD DISPLAY CONTROLLERS ARE ALSO AVAILABLE

## MICROPROCESSOR AND PERIPHERALS 8085

| DEVICE | PKG | DESCRIPTION |
|---|---|---|
| TMP8085A/A-2/AH/AH-2 | P | 8 BIT MICROPROCESSOR 3/5MHz |
| TMP8155/-2 | P | 256 BYTE RAM WITH I/O AND TIMER 3/5MHz |
| TMP8156/-2 | P | 256 BYTE RAM WITH I/O AND TIMER 3/5MHz |
| TMP8237A/A-5 | P | PROG. DMA CONTROLLER 3/5MHz |
| TMP8251A | P | PROG. COMMUNICATION INTERFACE 3MHz |
| TMP8253-5 | P | PROG. INTERVAL TIMER 2.5MHz |
| TMP8255A-5 | P | PROG. PERIPHERAL INTERFACE 3MHz |
| TMP8259A | P | PROG. INTERRUPT CONTROLLER 3MHz |
| TMP8279-5 | P | PROG. KEYBOARD/DISPLAY CONTROLLER 3MHz |
| TMP8355 | P | 2 BYTE ROM, I/O PORTS 3MHz |
| TMP82C79-2 | P,F | PROG. KEYBOARD/DISPLAY CONTROLLER 5MHz, CMOS |
| TMP82C59A-2 | P | PROG. INTERRUPT CONTROLLER 8MHz, CMOS |
| TMP82C55A-5/2/10 | P,F | PROG. PERIPHERAL INTERFACE 3/5/10MHz, CMOS |
| TMP82C54/-2 | P | PROG. INTERVAL TIMER 8/10MHz, CMOS |
| TMP82C53-2 | P | PROG. INTERVAL TIMER 5MHz, CMOS |
| TMP82C51A-2/-8 | P,F | PROG. COMMUNICATION INTERFACE 5/8MHz, CMOS |
| TMP82C37A-5 | P,F | DMA CONTROLLER 5MHz, CMOS |

## CMOS Z80 FAMILY

| DEVICE | PKG | FREQ. | DESCRIPTION |
|---|---|---|---|
| TMPZ84C00A | P,T,F | 4MHZ | MICROPROCESSOR-Z80A |
| TMPZ84C00A-6 | P,T,F | 6MHZ | MICROPROCESSOR-Z80B |
| TMPZ84C00A-8 | P,T | 8MHZ | MICROPROCESSOR-Z80H |
| TMPZ84C10A | P,T,F | 4MHZ | DIRECT MEMORY ACCESS CONTROLLER |
| TMPZ84C10A-6 | P,T,F | 6MHZ | DIRECT MEMORY ACCESS CONTROLLER |
| TMPZ84C20A | P,T,F | 4MHZ | PARALLEL I/O CONTROLLER |
| TMPZ84C20A-6 | P,T,F | 6MHZ | PARALLEL I/O CONTROLLER |
| TMPZ84C30A | P,T,F | 4MHZ | COUNTER TIMER CIRCUIT |
| TMPZ84C30A-6 | P,T,F | 6MHZ | COUNTER TIMER CIRCUIT |
| TMPZ84C40A | P | 4MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C40A-6 | P | 6MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C41A | P | 4MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C41A-6 | P | 6MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C42A | P | 4MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C42A-6 | P | 6MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C43A | F | 4MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C43A-6 | F | 6MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C44A | T | 4MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C44A-6 | T | 6MHZ | SERIAL I/O CONTROLLER |
| TMPZ84C60 | P | 4MHZ | CLOCK GENERATOR CONTROLLER |
| TMPZ84C61A | P | 6/8MHZ | CLOCK GENERATOR CONTROLLER |
| TMPZ84C01 | F | 4MHZ | MICROPROCESSOR + CGC |
| TMPZ84C02A-6 | F | 6MHZ | MICROPROCESSOR + CGC |

## NEW APPLICATION SPECIFIC STANDARD PRODUCTS (ASSPs)

Toshiba now uses Super Integration to combine a CMOS microprocessor and several peripheral devices into a single, space-saving monolithic silicon die.

### ASSP PRODUCTS

| TYPE NUMBER | PKG | DESCRIPTION |
|---|---|---|
| TMPZ84C011A | F | Z80 MPU (4MHz) + CGC + CTC + I/O (8×5) |
| TMPZ84C011A-6 | F | Z80 MPU (6MHz) + CGC + CTC + I/O (8×5) |
| TMPZ84C015A | F | Z80 MPU (4MHz) + CGC + CTC + PIO + SIO |
| TMPZ84C015A-6 | F | Z80 MPU (6MHz) + CGC + CTC + PIO + SIO |
| TMPZ84C013A | T | Z80 MPU (4MHz) + CGC + CTC + SIO |
| TMPZ84C013A-6 | T | Z80 MPU (6MHz) + CGC + CTC + SIO |

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# Toshiba. World's Largest Supplier of CMOS.

**Toshiba offers the most comprehensive CMOS LOGIC line available – from our standard 4000 series up to our new Advanced High Speed 74AC series.** The Advanced High Speed series has typical prop delay times of 3.5ns and maximum clock frequencies of 150 megahertz. That's 33% faster than the original 74HC series. With high noise margin, high speed and low power consumption, these devices create opportunities for designers of high speed portable instruments, telecommunications or any digital system.

TOSHIBA HIGH SPEED (HC) AND ADVANCED HIGH SPEED (AC) CMOS FUNCTION SELECTION GUIDE

| FUNCTION | | | HIGH SPEED (P/N TC74HC -) | ADVANCED HIGH SPEED (P/N TC74AC -) |
|---|---|---|---|---|
| GATE | NAND<br>NOR<br>AND<br>OR<br>INVERTER | | 00, 03, 10, 20, 30, 133<br>02, 27, 4002, 4078<br>08, 11, 21<br>32, 4075, 4072, 4078<br>U04, 04, T04 | 00, 10, 20<br>02<br>08, 11<br>32<br>04 |
| | SCHMITT TRIGGER | | 14, 132 | |
| | MULTIFUNCTION | | 51, 86, 386, 7266 | 86 |
| BUFFER | | | 4049, 4050, T7007 | |
| | 3-STATE | | 125, 126, 240, T240, 241, T241, 244, T244, 365, 366, 367, 368, 540, T540, 541, T541 | 240, 241, 244, 367, 368, 540, 541 |
| | BIDIRECTIONAL | | 242, 243, 245, T245, 620<br>623, 640, T640, 643, T643 | 245, 620, 640, 643 |
| FLIP-FLOP | J-K, FLIP-FLOP | | 73, 76, 107, 109, 112, 113 | 109, 112 |
| | D FLIP-FLOP | | 74, 174, 175, 273, 377 | 74, 174, 175, 273 |
| | | 3-STATE | 374, T374, 534, 564, T564, 574, T574, 646, T646, 648, T648, 651, T651, 652, T652 | 374, 534, 564, 574, 646, 648 |
| LATCH | | | 75, 77, 259, 279, 375 | |
| | | 3-STATE | 373, T373, 533, 563, T563, 573, T573 | 373, 533, 563, 573 |
| MULTIVIBRATOR | | | 123, 221, 423, 4538 | |
| DECODER | | | 42, 131, 137, T137, 138, T138, 139, 154, 155, 237, 238, 4028, 4514, 4515 | 138, 139 |
| | | 7-SEGMENT | 4511, 4543 | |
| ENCODER | | | 147, 148 | |
| REGISTER | | | 164, 165, 166, 173, 194, 195, 299, 323, 595, 597, 670, 4094 | 299, 323 |
| COUNTER | | BINARY | 161, 163, 191, 193, 393, 590, 592, 593, 691, 693, 697, 699, 4520 | 161, 163, 393 |
| | | DECADE | 160, 162, 190, 192, 390, 690, 692, 696, 698, 4518 | 160, 162, 390 |
| | | DIVIDER | 4017, 4020, 4022, 4024, 4040, 4060, 40102, 40103, 7292, 7294 | |
| MULTIPLEXER | | ANALOG | 4051, 4052, 4053, 4066 | |
| | | DIGITAL | 151, 153, 157, 158, 251, 253, 257, 258, 298, 354, 356 | 151, 153, 157, 158, 251, 253, 257, 258 |
| OTHERS | COMPARATOR | | 85, 688 | |
| | ADDER | | 283 | |
| | ALU | | 181, 182 | |
| | PARITY TREE | | 280 | |

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## TOSHIBA STANDARD $C^2MOS$ FUNCTION SELECTION GUIDE

| FUNCTION | | | TYPE NUMBER |
|---|---|---|---|
| GATE BUFFERS | NAND | | TC4011BP/BF, TC4011UBP, TC4012BP/BF, TC4023BP/BF, TC4068BP/BF, TC7400BP |
| | NOR | | TC4000BP, TC4001BP/BF, TC4001UBP, TC4002BP/BF, TC4025BF/BP, TC4078BP/BF |
| | AND | | TC4068BP/BF, TC4073BP/BF, TC4081BP/BF, TC4082BP |
| | OR | | TC4071BP/BF, TC4072BP/BF, TC4075BP/BF, 4078BP/BF |
| | INVERTER | | TC4007UBP/UBF, TC4009UBP, TC4049BP/BF, TC4069UBP/UBF, TC7404UBP |
| | BUFFERS | | TC4009UBP, TC4010BP, TC4049BP/BF, TC4050BP/BF |
| | | 3-STATE | TC4502BP, TC5012BP/BF, TC5024BP, TC5025BP |
| | | OPEN DRAIN | TC40107BP, TC5029BP, TC5064BP, TC5065BP, TC5066BP, TC5067BP |
| | MULTIFUNCTION | | TC4019BP/BF, TC4030BP/BF, TC4077BP/BF, TC4085BP, TC4086BP, TC4501BP, TC4519BP, TC4530BP, TC4572BP/BF |
| | SCHMITT TRIGGER | | TC4093BP/BF, TC4583BP, TC4584BP/BF |
| | LEVEL SHIFTER | | TC4009UBP, TC4010BP, TC4049BP/BF, TC4050BP/BF, TC5020BP |
| FLIP-FLOP | | | TC4013BP/BF, TC4027BP/BF, TC40174BP/BF, TC40175BP/BF, TC7476BP |
| LATCHES | | | TC4042BP/BF, TC4043BP, TC4044BP/BF, TC4099BP/BF, TC4508BP |
| MULTIVIBRATORS | | | TC4047BP, TC4528BP/BF, TC4538BP/BF |
| DECODERS | | | TC4028BP/BF, TC4514BP, TC4515BP, TC4555BP, TC4556BP/BF |
| DISPLAY DRIVER | LED | | TC4511BP/BF, TC5002BP, TC5022BP |
| | LCD | | TC4054BP/BF, TC4055BP, TC4056BP/BF, TC4543BP/BF |
| | DIGITRON | | TC5068BP, TC5069BP |
| ENCODER | | | TC4532BP |
| REGISTERS | SHIFT | | TC4006BP, TC4014BP, TC4015BP/BF, TC4021BP, TC4034BP, TC4035BP, TC4094BP/BF, TC40104BP, TC40194BP, TC5050P |
| | STORAGE | | TC4076BP |
| COUNTERS | BINARY | | TC4029BP/BF, TC40161BP, TC40163BP, TC40193BP, TC4516BP/BF, TC4520BP/BF, TC5018BP, TC5027BP |
| | DECADE | | TC4029BP/BF, TC40160BP, TC40162BP, TC40192BP, TC4510BP/BF, TC4518BP/BF, TC5026BP |
| | DIVIDER | | TC4020BP/BF, TC4024BP/BF, TC4040BP/BF, TC4521BP, TC5036P, TC5048P |
| | DIVIDE-BY-"N" | | TC4018BP, TC40102BP, TC40103BP, TC4522BP, TC4526BP/BF |
| | N-DIGIT DECADE | | TC5001P, TC5032P, TC5037P, TC5051P, TC5052P, TC5053P, TC5054P, TC5070P |
| | OTHER | | TC4017BP/BF, TC4022BP |
| TIMERS | | | TC5043P, TC5071P, TC5072P |
| MULTI-PLEXERS | ANALOG | | TC4051BP/BF, TC4052BP/BF, TC4053BP/BF |
| | DIGITAL | | TC4512BP/BF, TC4539BP/BF, TC5023BP |
| ARITHMETIC CIRCUITS | ADDER | | TC4008BP, TC4032BP, TC4038BP, TC4560BP |
| | COMPARATOR | | TC4063BP/BF, TC4585BP |
| | PARITY TREE | | TC4531BP |
| | RATE MULTIPLIER | | TC4527BP |
| | 9's COMPLEMENTER | | TC4561BP |
| MEMORIES (RAM) | | | TC4036BP, TC4039BP |
| A/D CONVERTERS | | | TC5090AP, TC5091AP, TC5092AP, TC5093AP |
| ANALOG SWITCH | | | TC4016BP/BF, TC4066BP/BF |
| OTHER | | | TC40117BP |

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## Foundry Products and Services

### *GaAs IC Technologies*

- GaAs 1D/1A: 1 um GHz digital/analog process
- GaAs HA: 0.5 um Microwave process
- GaAs Q-ED: LSI E/D process
- GaAs Q-ED/A: Low power Microwave Process

### *Engineering Services*

- Design Manuals
- Proven cell libraries
- Design Review & Consulting
- GaAs IC Design Classes

### *Ancillary Services*

- Mask making
- Wafer thinning
- Device packaging
- Special testing

## Standard Catalog Components

### *Interface/Linear Std. Components*

- D/A Convertors
  - 8 - BIT resolution and accuracy
  - 1 Gs/s and 600 Ms/s conversion rates
- Pin Driver / Line Receiver
  - 100 pS rise time
  - ECL Input
  - 2 Gbit/sec
  - Programmable outputs

### *Q-Logic Std. Components*

- MSI/LSI
- Ultra-high-speed (toggle rates to 3 GHz)
- Counter series
- MUX/DEMUX series

### *Micro-S Std. Components*

- MMIC building block components for receiver & interstage applications
  - Amplification
  - Switching/Signal distribution
  - Mixing/modulation
  - Signal generation

## Gate Arrays and Standard Cells

### *TQ3000 Gate Array*

- 3000 Equivalent Gates
- Low power - 0.75mW per gate
- 64 dedicated high speed I/O's : ECL, TTL, and CMOS Programmable
- Single power supply
- High speed multi-layer ceramic package
- Workstation software support Daisy, Mentor & Tek/CAE

### *Customer Designed ASICs using Q-Logic Std. Cells*

- Customer workstation electrical design
- ECL compatible library
- TriQuint does place and route
- TriQuint delivers functionally tested, packaged parts

## TriQuint Designed ASICs

### *TriQuint Designed Linear and Digital ASIC's*

- Customer provides electrical specifications
- Designs can include custom cells
- TriQuint does design, simulation, layout
- TriQuint delivers functionally tested, packaged parts

### *TriQuint Designed Application Specific MMICs*

- Customer provides electrical specifications
- Designs can include both custom & MICRO-S standard MMIC functions
- TriQuint does design, simulation, and layout
- TriQuint delivers functionally tested, packaged parts

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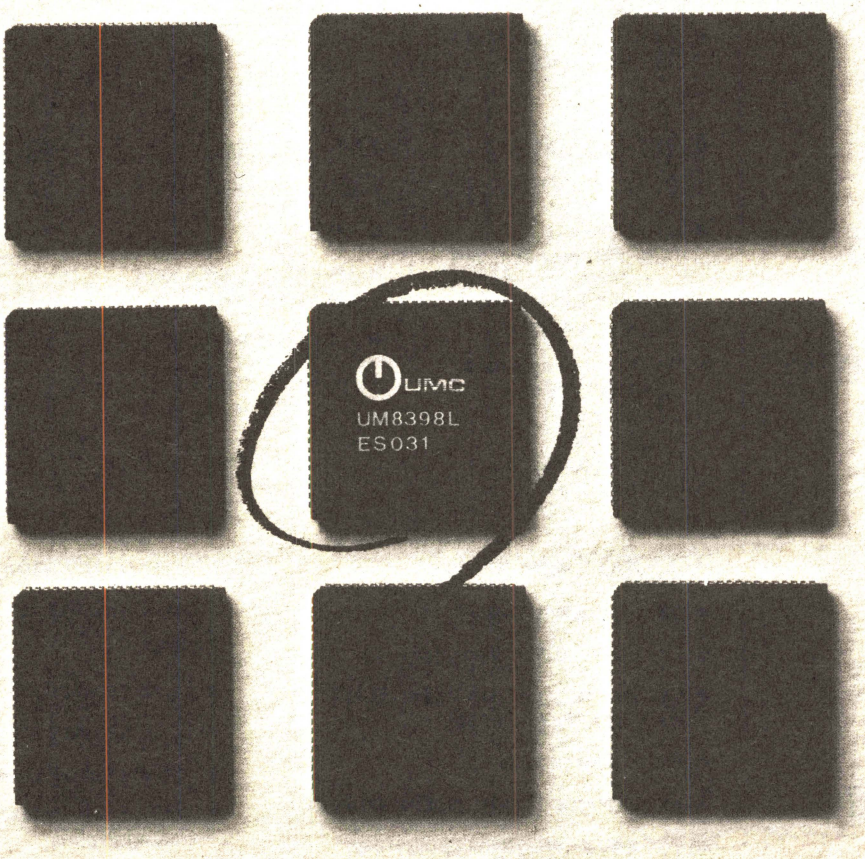


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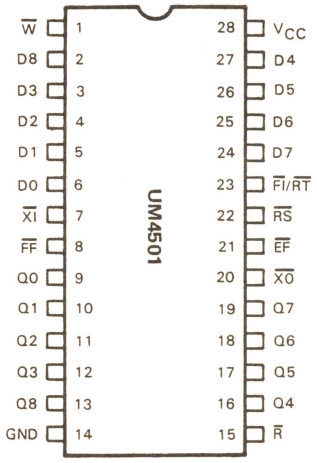
# UM4501 512x9–Bit CMOS Parallel FIFO

## FEATURES:

- First-in, First-out Dual Port Memory
- 512 x 9-bit Organization, 28-pin DIP
  Pin and Functionally Equivalent to MOSTEK MK4501
- Asynchronous and Simultaneous Read/Write
- Empty and Full Warning Flags
- Auto Retransmit Capability
- Multiple Device Expansion Modes
- TTL-compatible Interface
- Very Low CMOS Power Consumption:
  $V_{CC}$ = 5V ± 10%, T = 0 – 70°C
  Typical Power Consumption: 50 mW
  Average Operating Current: 10 mA
  Maximum Standby Current: 10 μA
- High Performance Architecture:
  High Throughout Dual Port RAM Architecture Eliminates 1-2μsec Fallthrough Delays of Shift Register Type FIFOs.
  10-20 MHz Operation: 50 – 100 ns Access Times.
- 2μ CMOS Double-Metal Technology
  Electrostatic Discharge Tolerance to 2000V. Latch-up Protection to 100 mA.

## PIN CONFIGURATION

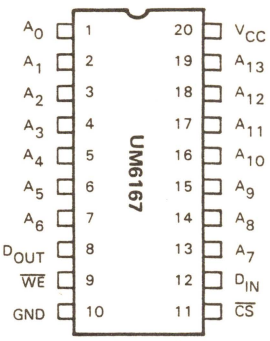



# UM6167 16Kx1 High–Speed CMOS SRAM

## FEATURES:

- High-speed – 45/55/70 ns Access Times
- Low Power Dissipation
  – 150mW (Typ.) Operating
  – 100μW (Typ.) Standby
- Single 5V Power Supply
- Fully Static Operation
- All Inputs and Outputs Directly TTL Compatible
- Three-State Outputs
- Data Retention Supply Voltage: 2.0 – 5.5V

## PIN CONFIGURATION



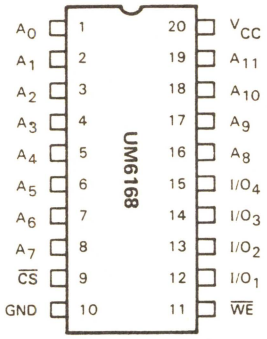

United Microelectronics

# UM6168 4Kx4 High-Speed CMOS SRAM

## FEATURES:

- High-speed – 45/55/70 ns Access Times
- Low Power Dissipation
  - 225mW (Typ.) Operating
  - 100μW (Typ.) Standby
- Single 5V Power Supply
- Fully Static Operation
- All Inputs and Outputs Directly TTL Compatible
- Three-State Outputs
- Data Retention Supply Voltage: 2.0 – 5.5V

## PIN CONFIGURATION




United Microelectronics

# UM53C80 SCSI Bus Controller

## FEATURES:

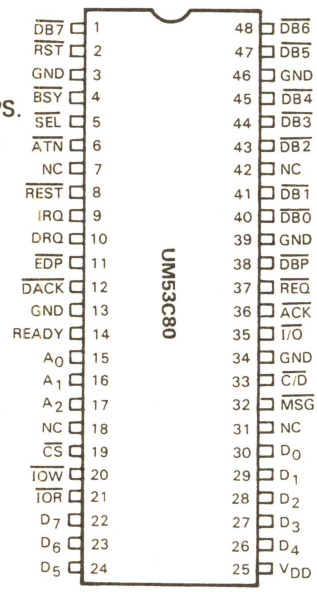
SCSI Interface:

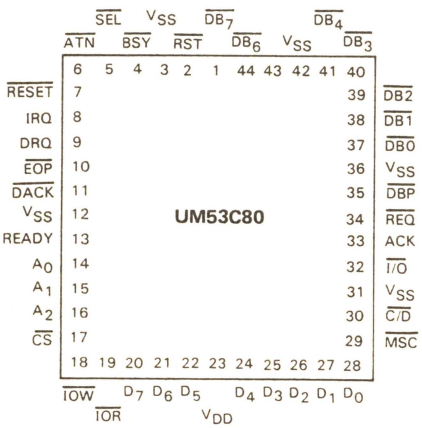
- Supports ANSI X3T9.2 SCSI Standard.
- Asynchronous Data Transfers to 1.5M BPS.
- Supports Both Initiator and Target Roles
- Parity Generation W/optional Checking.
- Supports Priority Arbitration
- Controls All Bus Signals Except Reset.
- Single-buffered Data Register.

MPU Interface:

- Memory or I/O Mapped MPU Interface.
- DMA or Programned I/O Transfer
- No Transfer Counter
- Programmable (Re) Selection Timeouts
- Interrupts MPU on All Bus Conditions Requiring Service

## PIN CONFIGURATION



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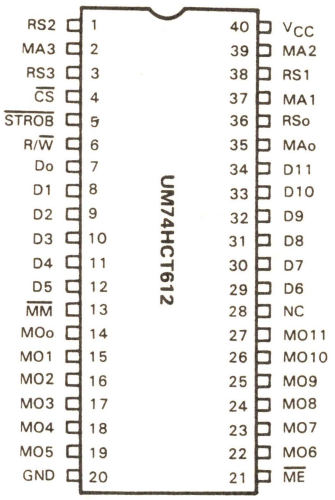
# UM74HCT612 Memory Mapper

## FEATURES:

- Fully Compatible with TTL, NMOS and CMOS Devices
- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- High-current 3-state Outputs

## PIN CONFIGURATION

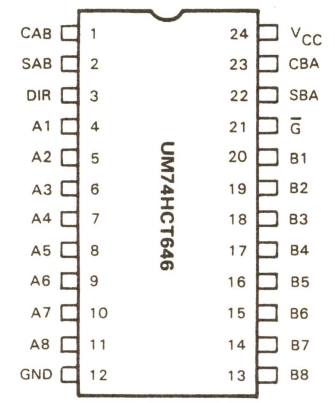



# UM74HCT646 Octal Bus Transceivers and Register

## FEATURES:

- 8 Bi-directional Data Bus
- Transmits Directly Read-time Data or Stored Data to the Internal Register in Either Direction
- 3-state Outputs with Driving Capability for Direct Bus Interface
- Low Power Consumption with Function, Pin-out, Speed and Drive Compatibility with 74LS Logic Family. Interfaces Directly with TTL, NMOS and CMOS Dovices

## PIN CONFIGURATION

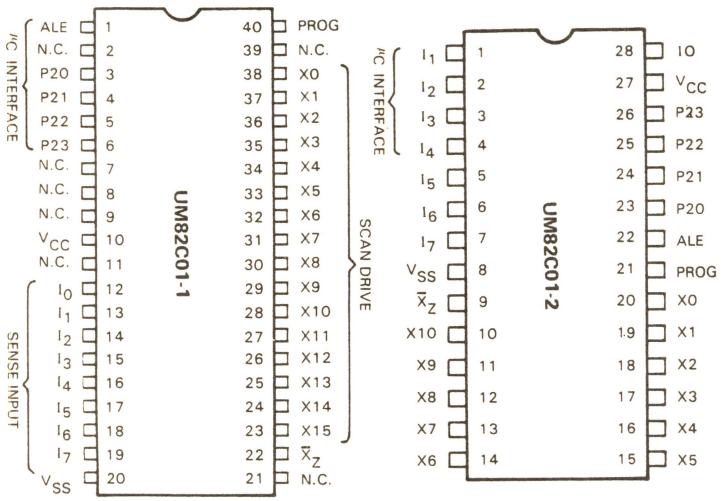


# UM82C01 Capacitance Keyboard Encoder (CKE)

## FEATURES:

- 16x8 Matrix, can Build up to 128-Key Capacitance Keyboard
- Single Chip with 16 Scan Drive Outputs and 8 Sense Inputs.
- Two Types of Package: 28 Pin for 88-Key KB and 40 Pin for 128-Key KB.
- Keyboard Scanning and Encoding under Complete Control of the User's Computer, Especially UM8048 $\mu$C.
- Single 5V Supply.
- High-speed CMOS Technology.
- Serves as Easy Interface to UM8048.
- New CMOS Sense Technology, CMOS Analog Sense Circuit is Built in.
- Byte-Wide Sense, Higher Performance than Serial Sense Technology
- Wide UM8048 Frequency Range, 1M to 11MHz UM8048 can be used.

## PIN CONFIGURATION

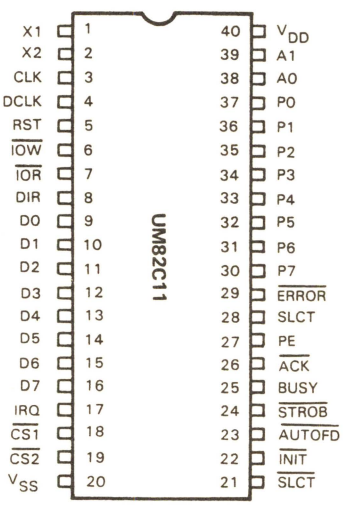



# UM82C11 Printer Adapter Interface (PAI)

## FEATURES:

- Programmable Parallel Printer Interface
- TTL Compatible Input/Output to Printer
- User-controlling Interrupt Request
- High Driving Capability
- Z-80 and 8088 Interface Capability
- On-Chip Oscillator can be used to Generate 1.5 to 20 MHz Oscillation
- Single 5V Power Supply
- Silicon Gate CMOS LSI

## PIN CONFIGURATION

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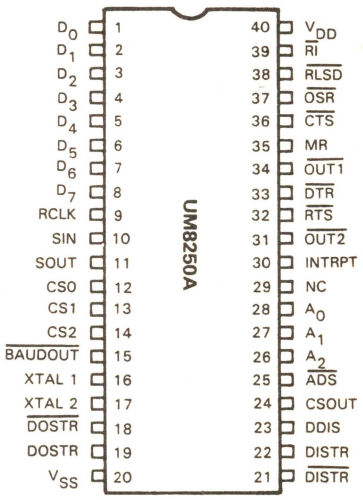
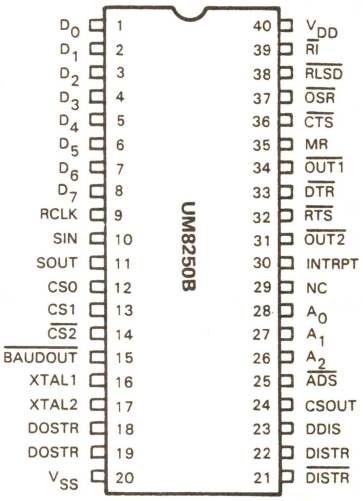
# UM8250A/B Asynchronous Communication Element (ACE)

## FEATURES:

- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to ($2^{16}$ −1) and Generates the Internal 16X Clock
- Independent Receiver Clock Input
- Modem Control Functions (CTS, RTS, DSR, DTR, RI, and Carrier Detect)
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Single +5 Volt Power Supply
- Fully Programmable Serial Interface Characteristics
  - 5, 6, 7, or 8-bit Characters
  - Even, Odd, or No-parity Bit Generation and Detection
  - 1, 1½, or 2 Stops Bit Generation
  - Baud Rate Generation (DC to 56K Baud)
- INS 8250A Spec. Compatible
- False Start Bit Detection
- Complete Status Reporting Capabilities
- Easily Interfaces with Most Popular Microprocessors
- Line-Break Generation and Detection
- Fully Prioritized Interrupt System Controls.

## PIN CONFIGURATION

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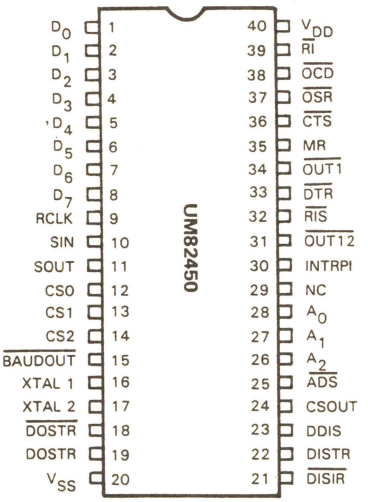
# UM82450 Asynchronous Communication Element (ACE)

## FEATURES:

- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to ($2^{16}$—1) and Generates the Internal 16X Clock
- Independent Receiver Clock Input
- Modem Control Functions (CTS, RTS, DSR, DTR, RI and Carrier Detect)
- Fully Prioritized Interrupt System Controls
- Single +5 Volt Power Supply
- Fully Programmable Serial Interface Characteristics
  - 5, 6, 7, or 8-bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1, 1½, or 2 Stops Bit Generation
  - Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- Easily Interfaces to Most Popular Micro Processors
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation

## PIN CONFIGURATION

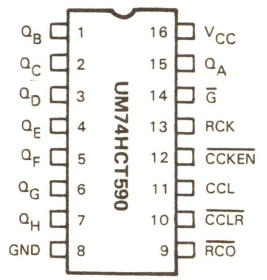



# UM74HCT590 8-Bit Binary Counters with Output Registers

## FEATURES:

- 8-bit Binary Counter with Parallel Register Output
- 3-state Register Output
- Direct Clear to Counter
- High Speed Counter with Guaranteed Frequency: DC to 20 MHz
- High Driving Capability ($I_{OL}$ = 24mA, $V_{OL}$ = 0.5V) for Direct Interface with TTL, NMOS and CMOS Devices
- Can Drive up to 20 TTL Load at Least

## PIN CONFIGURATION

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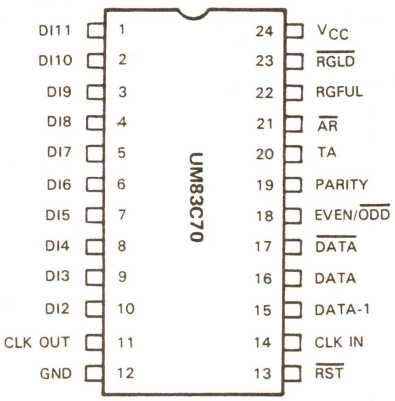
# UM83C70 Serial Bi–Phase Transmitter/Encoder

## FEATURES:

- 10-Bits Per Data Byte Transmission
- Single-byte or Multi-byte Transmission
- Internal Parity Generation (Even or Odd)
- Input Data Holding Register
- Automatic Clear Status Response (TT/AR)
- Transmitter Drives the Line Driver Directly
- Standard TTL Input/Output Compatibility
- Functionally Compatible with DP8340
- Single +5V Supply
- CMOS Technology

## PIN CONFIGURATION

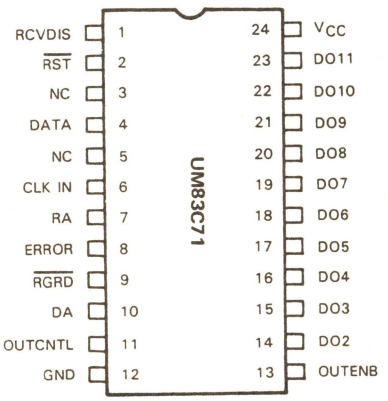



# UM83C71 Serial Bi–Phase Receiver/Decoder

## FEATURES:

- UM83C71 Detects 10-Bit Data Bytes Which Conform to the IBM 3270 Information Transmission Protocol.
- Even Parity Detection
- Standard TTL Input/Output Compatibility
- Output Data Holding Register
- Single-byte or Multi-Byte Transfer
- TRI-STATE Receiver Data Outputs
- Both Error Detection and Error Type Identification
- Functionally Compatible with DP8341
- Single +5V Supply
- CMOS Technology

## PIN CONFIGURATION



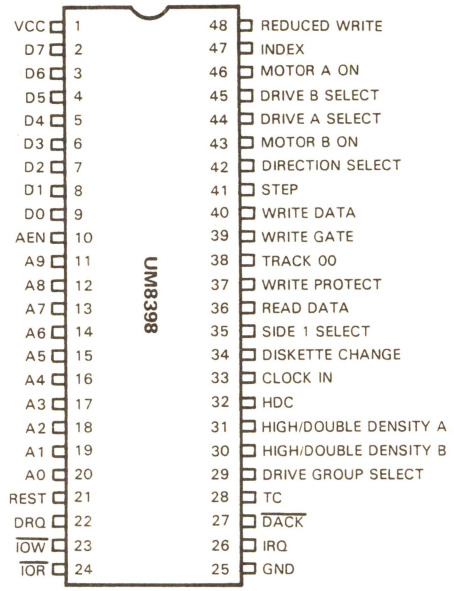

United Microelectronics

# UM8398 Single–Chip Floppy Disk Controller

## FEATURES:

- IBM PC XT/AT Drive System Compatible
- Supports 2 Drives (MS-DOS Support)
- 1.2M/360K Format Selectable
- IBM PC Drive System Address Decoder.
- Only 3 Components in the Drive System
- Internal Write Precompensation Circuit; Precompensation Values: 250-125 ns
- Internal Data Separator Circuit

## PIN ASSIGNMENT



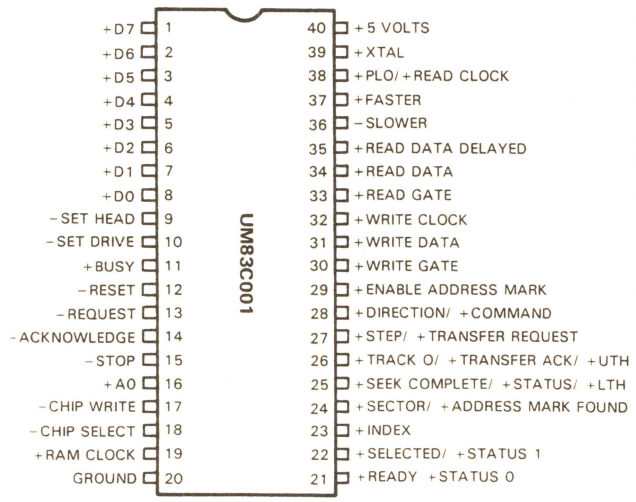

United Microelectronics

# UM83C001 Hard Disk Controller

## FEATURES:

- Serializer-Deserializer
- Programmable Track Format
- External Drive Select and Head Select Registers for Expandability
- Internal Phase Detector for Phase Lock Oscillator
- Interface Options: ST-506, ST-412, ST-412HP, ESDI, FLOPPY, and QIC-36 TAPE
- Sector Options: SOFT, HARD, ESDI ADDRESS MARKS, ESDI BYTE and ESDI BYTE CLOCKS
- Recording Options: UNENCODED, FM, MFM or RLL
- Error Checking and Correcting Options: ECC or CRC
- Write Data Options: PULSE, NRZ or NRZI
- Read Data Options: PULSE, NRZ or NRZI
- TTL Compatible Inputs and Outputs. Outputs Drive 8 LSTTL Loads

## PIN CONFIGURATION





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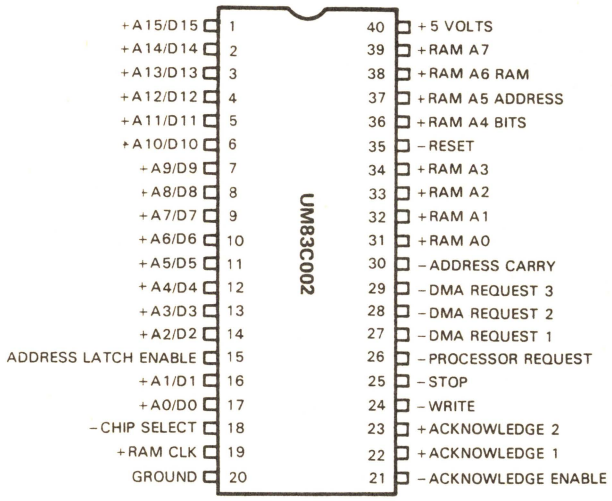
# UM83C002 RAM Buffer Controller

## FEATURES:

- 3 DMA Channels
- Host Processor Port
- Refresh for Dynamic RAMs Built in
- RAM Access Priority Network
- Address Multiplexing for Dynamic RAMs
- Multiplexed Address and Data Lines from Processor
- Pins Arranged for Easy Integration Into 8088/8086 System
- No Lost RAM Cycles for DMA Break-in
- DMA Carry Output Permits DMA Across 64K Boundaries
- 24-Bit Timer or Baud Rate Generator
- TTL Compatible Inputs and Outputs Outputs Drive 8 LSTTL Loads

## PIN CONFIGURATION

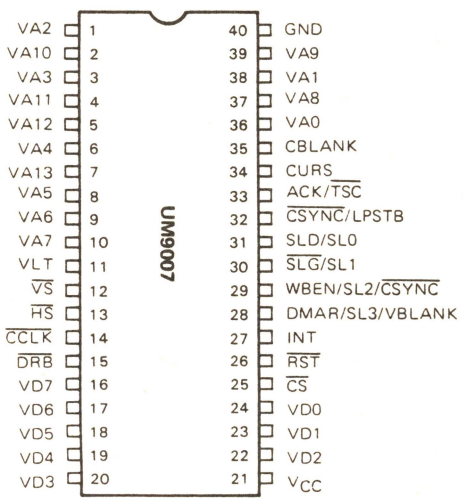



# UM9007 CRT Controller

## FEATURES:

- Fully Programmable Display Format
- Programmable Monitor Sync Format
- Direct Outputs to CRT Monitor
- Binary, Row-Table Driven or Sequential Video Addressing Modes
- Programmable Status Row Position and Address Registers
- Bidirectional Partial or Full-Page Smooth Scroll
- Attribute Assemble Mode
- Double Height, Double Width Data Row Mode
- Programmable DMA Burst Mode
- Configurable with a Variety of Memory Contention Arrangements
- Light Pen Register
- Maskable Processor Interrupt Line
- Three-state Video Memory Address Bus
- Partial or Full Page Blank Capability
- Two Interlace Modes: Enhanced Video and Alternate Scan Line
- Programmable for Horizontal Split Screen Applications

## PIN CONFIGURATION




- Graphics Compatible
- VT-100 Compatible
- RS-170 Interlaced Composite Sync Available

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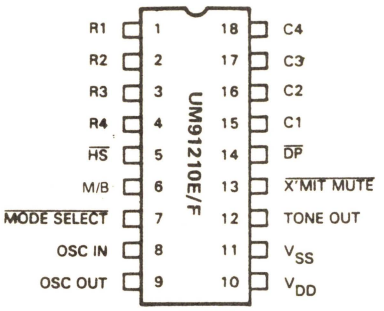
# UM91210E/F Tone/Pulse Dialer

## FEATURES:

- Tone/Pulse Switchable (Slide Switch)
- 32-Digit Capacity for Redialing
- Automatic Mix Redialing (Last Number Redial) of Pulse ⟶ DTMF with Multiple Automatic Access Pause
- PABX Auto-Pause for 3.6 sec
- Low Power CMOS Process (2.0 to 5.5V)
- Numbers Dialed Manually after Redial are Cascadable and Stored as Additional Numbers for Next Redialing
- Uses Inexpensive TV Crytal (3.58 MHz)
- Make/Break Ratio (33 1/3 : 66 2/3 / 40:60) Pin Selectable
- Touch Key Hooking (580ms)
- 4 x 4 or 2 of 8 Keyboard Available
- Low Standby Current

## PIN CONFIGURATION




## ORDERING INFORMATION

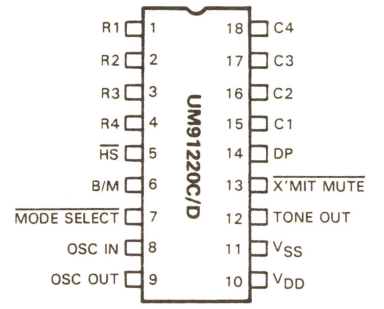
| Type | Dial Pulse | Dial Pulse Rate |
|---|---|---|
| 91210E | DP | 10 PPS |
| 91210F | DP | 20 PPS |

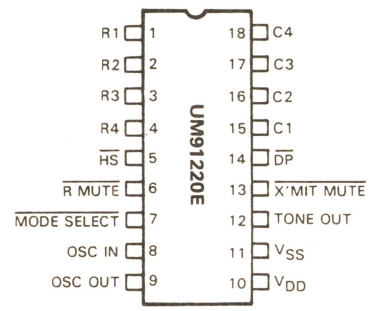
# UM91220C/D/E Tone/Pulse Dialer

## FEATURES:

- Tone/Pulse Switchable (Touch Key or Slide Switch)
- 32-Digit Capacity for Redialing
- Automatic Mix Redialing (Last Number Dial) of "Pulse to DTMF" with Multiple Automatic Access Pause
- PABX Auto-pause for 4.0 Sec
- Low Power CMOS Process (1.8 to 6.0 V)
- Numbers Dialed Manually After Redial are Cascadable and Stored as Additional Numbers for Next Redialing
- Used 480KHz Ceramic Resonator
- For UM91220C/D: Make/Break Ratios (33 1/3 : 66 2/3 / 40 : 60) are Pin Selectable. Pulse Dial Rate is 10pps for UM91220C and 20pps for UM91220D
- For UM91220E: Make/Break Ratio is Fixed to 40/60; 10pps
- Touch-key Hooking (600ms)
- 4 x 4 Keyboard Available
- Low Standby Current, Typically 0.1μA at $V_{DD}$ = 1.0 Volt
- Automatic Power on Reset

## PIN CONFIGURATION

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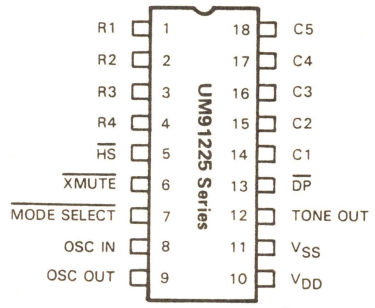
# UM91225 SERIES 5 Memory Tone/Pulse Dialer

## FEATURES:

- Tone/Pulse Switchable (Slide Switch or Touch Key)
- 32-Digit Redial Memory, 16-Digit x 3, 32-Digit x 1 One Touch Memory
- Automatic Mix Redialing (Last Number Redial) of Pulse → DTMF with Multiple Automatic Access Pause
- Low Power CMOS Process (2.0 to 5.5V)
- Numbers Dialed Manually after Redial Are Cascadable and Stored as Additional Numbers for Next Redialing
- Uses Inexpensive 480K Ceramic Resonator
- Tone/Pulse (33 1/3 : 66 2/3 / 40:60) by Mode Selection Pin
- 4 x 4 or 2 of 8 Keyboard Available
- Low Standby Current

## PIN CONFIGURATION




## ORDERING INFORMATION

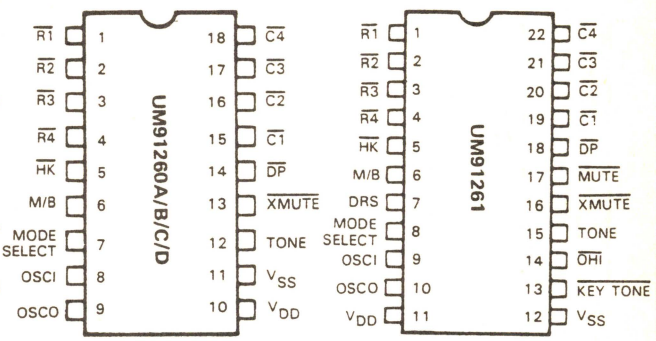
| Type | Pause | Flash | Store Mode | Dial Rate |
|---|---|---|---|---|
| UM91225A | 2.0S | 600ms | Off Hook | 10 PPS |
| UM91225B | 2.0S | 600ms | On/Off Hook | 10 PPS |
| UM91225C | 3.6S | 70ms | On/Off Hook | 10 PPS |
| UM91225D | 3.6S | 70ms | Off Hook | 10 PPS |

# UM91260 SERIES/91261 10 Memory Tone/Pulse Dialer

## FEATURES:

- 32-Digit Redial Memory
- 10 Number by 16-Digit Repertory Memory
- Tone/Pulse Switchable Via Slide Switch, and Inserts a Pause (4.08 Sec.) Automatically
- Low Operating Voltage:1.8V to 6.0V
- Uses 480 KHz Ceramic Resonator
- Low Standby Voltage and Current: 1.0V; and 0.1μA at 3.0V, 40°C
- Low Off-Hook Standby Current and Operating Current
- Make/Break Ratio Pin Selectable (1/2, 2/3)
- Dialing Rate Pin Selectable:10 pps/20 pps (UM91261 Only)
- Two-Key Single-Tone Operation
- Redial Memory Cascadable with Normal Dialling
- Fully Debounced 4 x 4 Keyboard
- Power on Reset On-Chip
- Minimum Tone Output Duration: 106.5 ms; and Minimum Inter-Digit Interval: 106.5 ms at Normal Dialing

## PIN CONFIGURATION




- All Pins Protected Against Electrostatic Charges and Latch-up
- 22-pin/18-pin Versions
- On/Off Hook Store; 10/20 pps Dialing Rate Available:

| Part No. | Dialling Rate | Storage Mode |
|---|---|---|
| UM91260A | 10 PPS | Off Hook Only |
| UM92160B | 20 PPS | On/Off Hook |
| UM92160C | 10 PPS | On/Off Hook |
| UM92160D | 20 PPS | Off Hook Only |

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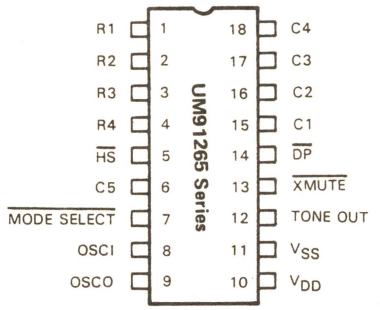
# UM91265 SERIES 15 Memory Tone/Pulse Dialer

## FEATURES:

- 32-Digit Redial Memory and Save Function
- 10 Number by 16-Digit Indirect Repertory Memory, and 3 by 16-Digit Direct Repertory Memory
- DTMF/Pulse Switchable Via Slide Switch and Keyboard, a Pause (1.6 sec) Will be Inserted Automatically
- Memory Retention Current: 0.1μA (max), $V_{DD}$ = 1.0V at 25°C
- Low Off-Hook Standby Current and Operating Current
- Make/Break Ratio Pin Selectable (1/2, 2/3)
- Key Accesable Flash for 560ms
- Two-Key Single-Tone Operation
- Redial Memory Cascadable with Normal Dialling
- Fully Debounced 4 x 5 Keyboard
- Power-on Reset on Chip
- Minimum Tone Output Duration 106 ms; and Minimum Interdigit Interval 106ms
- 18 Pin DIP
- On/off Hook Store; 10/20 pps Dialling Rate are Available

## PIN CONFIGURATION




## ORDERING INFORMATION

| Part No. | Dialling Rate | On/Off Hook Store |
|---|---|---|
| UM91265A | 10 pps | Off Hook Store Only |
| UM91265B | 20 pps | On Hook Store Only |
| UM91265C | 10 pps | On Hook Store Only |
| UM91265D | 20 pps | Off Hook Store Only |

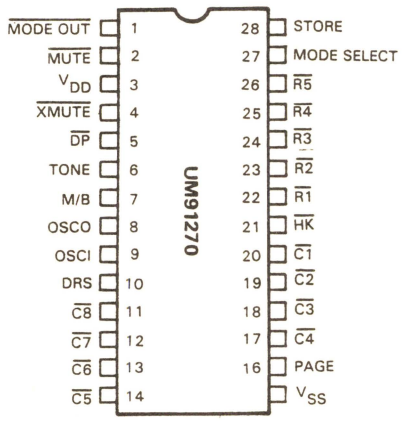
United Microelectronics

# UM91270 20 Memory Tone/Pulse Dialer

## FEATURES:

- 32-Digit Redial Memory
- 20 Number by 18-Digit Repertory Memory with Direct Access Keys
- 28-pin Package
- Tone/Pulse Modes, Tone Capability in Pulse Mode Using DTMF Key
- Low Operating Voltage: 1.8V to 6.0V
- Uses 480 KHz Ceramic Resonator
- Low Standby Voltage and Current: 1.0V, and 0.1μA at 3.0V, 40°C
- Low Off-Hook Standby Current and Operating Current
- Make-Break Ratio Pin Selectable: (1/2, 2/3)
- Dialing Rate Pin Selectable: 10pps/20pps
- Flash Can be Stored as a Digit, 0.533 Second Flash, 1.7 Second Pause
- Two-Key Single-Tone Operation
- Fully Debounced 5 x 8 Keyboard
- Power on Reset and Inhibit Redial/Repertory Dial
- Off-Hook Store Via Switch, On-Hook Store Via Application
- Off-Hook Store Via Keyboard
- Page Mode: M1 to M10 First Page, M11 to M20 Second Page

## PIN CONFIGURATION




- Access Pause 4.0 Seconds
- Minimum Tone Duration and Also Inter-Digit Pause for 106ms
- All Pins Protected Against Electrostatic Charges and Latch-up
- Memory Transfer from Repertory Memory to Redial Memory in Dialing Mode
- Overflow in Normal Dialing Allowed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# POWER SUPPLY CIRCUITS

## Switching Regulator Control ICs

Note: Most series available screened to /883B Rev. C.

UNITRODE

| TYPE | Voltage Reference ± 4% | Voltage Reference ± 1% | Soft Start | PWM Latch | Under-Voltage Lockout | Pulse-by-Pulse Current Limiting | Shutdown Terminal | Output Current | Feed Forward | Maximum Frequency Oscillator | Dual Outputs | Single-Ended Output | Totem Pole Outputs | Separate Oscillator Sync Terminal | Adjustable Deadtime Control | Latch Off or Continuous Retry Mode | Double Pulse Suppression | Low Current Start Up | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Regulating PWMs** UC1524/2524/3524 | X | | | | | | X | 100mA | | 300kHz | X | | | | | | | | 16 Pin DIP |
| **Advanced Regulating PWMs** UC1524A/2524A/3524A | | X | | X | X | X | X | 200mA | | 500kHz | X | | | | | | X | | 16 Pin DIP |
| **Advanced Regulating PWMs** UC1525A/2525A/3525A UC1527A/2527A/3527A | | X | X | X | X | | X | 100mA 0.4A Pulse | | 500kHz | | | X | X | X | | | | 16 Pin DIP |
| **Regulating PWM** UC1526/2526/3526 | | X | X | X | X | X | X | 100mA | | 400kHz | | | X | X | X | | X | | 18 Pin DIP |
| **Advanced Regulating PWMs** UC1526A/2526A/3526A | | X | X | X | X | X | X | 100mA | | 550kHz | | | X | X | X | | X | | 18 Pin DIP |
| **Regulating PWMs** UC493/UC494/ | X | | | | | | | 200mA | | 300kHz | X | | | | X | | X | | 16 Pin DIP |
| UC495 | | | | | | | | | | | | | | | | | | | 18 Pin DIP |
| **Advanced Regulating PWMs** UC493A/UC493AC UC494A/UC494AC | | X | | | X | | | 200mA | | 300kHz | X | | | | X | | X | | 16 Pin DIP |
| UC495A/UC495AC UC495B/UC495BC | | | | | | | | | | | | | | | | | | | 18 Pin DIP |
| **Current Mode PWM Controllers** UC1846/2846/3846 UC1847/2847/3847 | | X | X | X | X | X | X | 200mA | X | 500kHz | | | X | X | X | X | X | | 16 Pin DIP |
| **Programmable Primary Side PWMs** UC1840/2840/3840 | | X | X | X | X | X | X | 200mA | X | 500kHz | | X | | | X | X | N/A | X | 18 Pin DIP |
| **Programmable Primary Side PWMs** UC1841/2841/3841 | | X | X | X | X | X | X | 200mA | X | 500kHz | | X | | | X | X | N/A | X | 18 Pin DIP |
| **Economy Primary Side PWMs** UC1842/2842/3842 UC1843/2843/3843 UC1844/2844/3844 UC1845/2845/3845 | | X | | X | X | X | | 100mA 1A Pulse | X | 500kHz | | X | | | X | | N/A | X | 8 Pin DIP |
| **High Frequency PWM Controllers** UC1823/2823/3823 | | X | X | X | X | X | | 500mA 1.5A Pulse | X | 2MHz | | X | X | X | X | | X | X | 16 Pin DIP |
| UC1825/2825/3825 | | X | X | X | X | X | | | | | X | | X | X | X | | X | X | |
| **Power Supply Control System** UC2850/3850 | X | | X | X | X | X | X | 50mA | | 200kHz | X | | | X | X | | X | | 24 Pin DIP |
| **High Current Buck Regulator** L296 | | X | X | X | | X | X | 4A | | 200kHz | | X | | | | | X | | 15 Pin Multiwatt® |
| **Resonant Mode Controller** UC1860/2860/3860 | | X | X | | X | | X | 1.5A | | 3MHz | X | | X | X | X | X | X | | 24 Pin DIP |

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## Power Supply Support Functions

| TYPE | DESCRIPTION | KEY FEATURES | PACKAGE |
|---|---|---|---|
| UC1543/2543/3543<br>UC1544/2544/3544 | Power Supply Supervisory Circuit, Monitors and Controls Power Supply Output | • Over/Under-Voltage, and Current Sensing Circuits<br>• Programmable Time Delays<br>• SCR "Crowbar" Drive of 300mA<br>• Optional Over-Voltage Latch<br>• Internal 1% Accurate Reference<br>• Remote Activation Capability<br>• Uncommitted Comparator<br>• Inputs for Low Voltage Sensing (UC1544 Series only) | 16 Pin DIL (1543 Series)<br><br>18 Pin DIL (1544 Series) |
| UC1705/2705/3705<br>UC1706/2706/3706<br>UC1707/2707/3707 | See Power Driver & Interface Circuit Section | | |
| UC1834/2834/3834 | High Efficency Linear Regulator, Low Input-Output Differential | • Minimum $V_{IN}$—$V_{OUT}$ less than 0.5V at 5A Load with External Pass Device<br>• Equally Usable for either Positive or Negative Regulator Design<br>• Adjustable Low Threshold Current Sense Amplifier<br>• Under- and Over-Voltage Fault Alert with Programmable Delay<br>• Over-Voltage Fault Latch with 100mA Crowbar Drive Output | 16 Pin DIL |
| UC1835/2835/3835<br>UC1836/2836/3836 | High Efficiency Regulator Controllers<br>5V Fixed (1835 Series)<br>Adjustable (1836 Series) | • Complete Control for High Current Low Dropout Linear Regulator<br>• Accurate 2.5A Current Limiting with Foldback<br>• Internal Current Sense<br>• External Shutdown | 8 Pin DIL |
| UC1838/2838/3838 | Magnetic Amplifier Controller | • Independent 1% Reference<br>• Two Uncommitted, Identical Op Amps<br>• 100mA Reset Current Source | 16 Pin DIL Power Pkg. |
| UC1901/2901/3901 | Isolated Feedback Generator<br>Stable and Reliable Alternative to an Optical Coupler | • An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal<br>• Internal 1% Reference and Error Amplifier<br>• Loop Status Monitor<br>• Low-Cost Alternative to Optical Couplers<br>• Internal Carrier Oscillator Usable to 5MHz<br>• Modulator Synchronizable to an External Clock | 14 Pin DIL |
| UC1903/2903/3903 | Quad Supply and Line Monitor<br>Precision System | • Monitor Four Power Supply Output Voltage Levels<br>• Both Over- and Under-Voltage Indicators<br>• Internal Inverter for Negative Level Sense<br>• Adjustable Fault Window<br>• Additional Input for Early Line Fault Sense<br>• On Chip, High-Current General Purpose OP-AMP | 18 Pin DIL |

## Product Applications Circuits

| PRODUCT SERIES | TYPICAL APPLICATIONS |
|---|---|
| UC1611/2611/3611<br>Quad Schottky Array | • Matched, Four Diode Monolithic Array<br>• High Peak Current<br>• Low Cost MINIDIP Package<br>• Low Forward Voltage<br>• Parallelable for Lower $V_F$ or Higher $V_F$<br>• Fast Recovery Time<br>• Military Temperature Range |
| UC1906/2906<br>Lead-Acid Battery Charger | "IC Circuitry that results in optimized charge cycles for specific battery applications."<br>• Uninterruptable Power Supplies<br>• Portable Electrical Equipment<br>• Emergency Power and Light Systems<br>• Volatile Data Handling Computers—Power Back-Up |

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# POWER SUPPLY CIRCUITS

## 3 Terminal Fixed and Adjustable Regulators

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### Three Terminal Voltage Regulators, Adjustable

| TYPE | OUTPUT CURRENT (A) | POLARITY | REGULATED OUTPUT VOLTAGE (V) | PACKAGE |
|---|---|---|---|---|
| †*UC117K/LM117K | 1.5A | Pos. | Adjustable from 1.2V to 37V | TO-3 |
| UC217K/LM217K | 1.5A | Neg. | | TO-3 |
| UC317K/LM317K | | | | TO-3 |
| *UC137K/LM137K | 1.5A | Neg. | Adjustable from −1.2V to −37V | TO-3 |
| UC237K/LM237K | | | | TO-3 |
| UC337K/LM337K | | | | TO-3 |
| *UC150K/LM150K | 3.0A | Pos. | Adjustable from 1.2V to 33V | TO-3 |
| UC250K/LM250K | | | | TO-3 |
| UC350K/LM350K | | | | TO-3 |

### Three Terminal Voltage Regulators, Fixed, Positive

| TYPE | OUTPUT CURRENT (A) | POLARITY | REGULATED INPUT VOLTAGE (V) | | | PACKAGE |
|---|---|---|---|---|---|---|
| *UC7800AK/LM140AK SERIES | 1.5A | Pos. | 5V ± 1% | 12V ± 1% | 15V ± 1% | TO-3 |
| UC7800ACK/LM340AK SERIES | | | | | | TO-3 |
| *UC7800K/LM140K SERIES | 1.5A | Pos. | 5V ± 4% | 12V ± 4% | 15V ± 4% | TO-3 |
| UC7800CK/LM340K SERIES | | | | | | TO-3 |

### Three Terminal Voltage Regulators, Fixed, Negative

| TYPE | OUTPUT CURRENT (A) | POLARITY | REGULATED INPUT VOLTAGE (V) | | | PACKAGE |
|---|---|---|---|---|---|---|
| *UC7900AK/LM120K SERIES | 1.5A | Neg. | −5V ± 1% | −12V ± 1% | −15V ± 1% | TO-3 |
| UC7900ACK SERIES | | | | | | TO-3 |
| *UC7900K SERIES | 1.5A | Neg. | −5V ± 4% | −12V ± 4% | −15V ± 4% | TO-3 |
| UC7900CK/LM320K SERIES | | | | | | TO-3 |

*All TO-3 Fixed and Adjustable Regulators available in /883B screened versions.

PACKAGE NOTE: Both Plastic or Ceramic Surface Mount Packaging are available. Contact factory for details.

† Available in /38510 version. Contact factory for details.



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# MOTION CONTROL CIRCUITS

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| TYPE | DESCRIPTION | TYPICAL APPLICATION | $V_C$ | $V_{SS}$ | $I_{OUT}$ | $P_D$ | $f_c$ | $\theta_{JC}$ | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|
| L292 | H-Bridge Transconductance amplifier with PWM current control. | DC Motors, torque control, stepping motors, microstepping solenoid controlled valves. | 18 to 36 Volts | | 2.0 Amp Cont. | 25 Watts MAX | 30 kHz MAX | 3.0 °C/W | 15 Pin Power Tab |
| L293 | Four Totem-Pole Drivers | DC Motors<br>Stepping Motors | 36 Volts | 4.5 to 36 Volts | 1.0 Amp Cont. | 5.0 Watts MAX | | 14.0 °C/W | 16 Pin DIP "BATWING" |
| L293D | L293 with eight bridge diodes; reduced $I_{OUT}$ | DC Motors<br>Stepping Motors | 36 Volts | 4.5 to 36 Volts | 0.6A Amp Cont. | 5.0 Watts MAX | | 14.0 °C/W | 16 Pin DIP "BATWING" |
| L295 | Dual solenoid driver with current control. | Hammer driver in matrix printers<br>Solenoid drivers<br>Motors | See Power Driver & Interface Circuits. | | | | | | |
| L298<br>L298D | Dual Full-Bridge with individual logic inputs for each bridge.<br>(L298D has on board diodes) | Power stage for motor and solenoid drivers. Low standby power drain makes it ideal for battery operated equipment. | $V_{SS}$ to 46 Volts | 4.5 to 7.0 Volts | 2.0 Amp Cont.<br>1.0A Cont. | 25 Watts MAX | | 3.0 °C/W | 15 Pin Power Tab |
| UC1610<br>UC3610 | Dual diode bridge with eight Schottky diodes. ($V_f$ = 1V @ 2A) | Use as circulating diodes with motor or solenoid drivers. | 40 Volts MAX | | 3.0 Amp MAX | | | | 8 Pin DIP |
| UC3620 | Brushless DC motor with switching current control. | Drive brushless DC motors. Includes Hall decode logic and fixed off-time current control switching. | 40 Volts MAX | | 2.0 Amp Cont. | 25 Watts MAX | 30 kHz | 3.0 °C/W | 15 Pin Power Tab |
| UC3622 | Brushless DC motor with voltage mode control. | Drives brushless DC motors in fast responding, position feedback systems. | 40 Volts MAX | | 2.0 Amp Cont. | 25 Watts | 30 kHz | 30 °C/W | 15 Pin Power Tab |
| UC1633<br>UC1634 | Phase Locked Controller | Speed control for DC motors with crystal oscillator, phase detector and lock indicator. | 8 to 15 Volts | | 16mA | 1 Watt | | | 16 Pin DIP |
| UC1637<br>UC2637<br>UC3637 | PWM Driver for DC Servomotors; Current Limit, Under-Voltage Lock-Out. | Drive Bipolar or MOSFET Power H-Bridge in DC Velocity and Position Servo-Loops. | 40 Volts MAX | | 500mA Peak | 2.0W MAX | | | 18 Pin DIP |
| UC1705*<br>UC3705*<br>UC1706<br>UC3706<br>UC1707<br>UC3707 | Dual driver for power MOSFETs; 40nS into 1000pF, 1.5A peak. TTL compatible inputs. | Interface between low-level control functions and high power control devices, particularly power MOSFETs. | See Power Driver & Interface Circuits. | | | | | | |
| UC1717<br>UC3717<br>UC3717A | Stepping motor phase driver; TTL compatible inputs. Pulse-by-pulse current control, and full output H-Bridge with diodes. | Stepping motor driver in full-step, half-step, or microstep mode. Separate digital control sets current at 100%, 60%, 19%, or zero Bipolar operation. | 10 to 40 Volts | 4.75 to 5.25 Volts | 1.0 Amp Peak | 2.0 Watts MAX | 30 kHz Typ. | 11.0 °C/W | 16 Pin DIP "BATWING" |
| UC3517 | Stepping modor driver, unipolar, bilevel. Minimal RFI. Activates both motor phases. | Driver for stepping motors in applications requiring least possible RFI. Internal logic for STEP, FWD/REV, and FULL STEP/HALF STEP. High voltage pulse width set by single RC. | 10 to 40 Volts | 4.75 to 5.25 Volts | 350 mA Cont. | 1.6 Watts MAX | | | 16 Pin DIP |
| UC2950 | Half Bridge Bipolar Switch | 2-Phase Steppers<br>Brush Type Motors<br>3-Phase Brushless | See Power Driver & Interface Circuits. | | | | | | |
| UC1657<br>UC3657 | Triple Half Bridge Power Driver | 3-Phase Brushless Motors | 40 Volts MAX | | 2.0 Amp Cont. | 2.5 Watts | 30 kHz | 3.0 °C/W | 15 Pin Power Tab |
| UC3176 | Voice-Coil Driver | Head Positioning | 25 Volts MAX | | 3.0 Amp MAX | | | | 15 Pin Power Tab |
| UC3720 | Smart Switch | Any Load Switching Feedback System | See Power Driver & Interface Circuits. | | | | | | |

*UC1705/3705 are single drivers.

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# POWER DRIVER & INTERFACE CIRCUITS

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| TYPE | DESCRIPTION | KEY FEATURES | PACKAGE |
|---|---|---|---|
| L295 | Dual Solenoid Driver with Current Control | • High Current Capability (Up to 2.5A per channel)<br>• High Voltage Operation (Up to 46V for Power Stage)<br>• High Efficiency Switchmode Operation<br>• Regulated Output Current (Adjustable)<br>• Few External Components<br>• Separate Logic Supply<br>• Thermal Protection | 15 Pin Power Tab |
| UC195/295/395 | Smart Power Switch | The UC195/395 family of devices are ultra reliable, fast, monolithic power transistors with complete overload protection. These devices act as high gain power transistors and have on-chip, current limiting, power limiting, and thermal overload protection, making them virtually impossible to destroy. The UC195/395 offers a significant increase in reliability and simplifies power circuitry designs.<br>• Greater than 1.0A Output<br>• 3.0μA Typical Base Current<br>• 500ns Switching Time<br>• 2.0V Saturation Voltage<br>• Directly Interfaces with CMOS or TTL<br>• Internal Thermal Limiting | TO-5<br><br><br><br><br>TO-220 |
| UC1704/3704 | Bridge Transducer Switch | • Dual Matched Current Sources<br>• High-Gain Differential Sensing Circuit<br>• Wide Common-Mode Input Capability<br>• Complimentary Digital Open-Collector Outputs<br>• Externally Programmable Time Delay<br>• Optional Output Latch with Reset<br>• Built-In Diagnostic Activation<br>• Wide Supply Voltage Range<br>• High Current Heater Power Source Driver | 16 Pin DIL |
| UC1705/3705 | High Speed Power Driver (Single ended) | • 1.5A Totem Pole Output<br>• High Speed MOSFET Compatible<br>• Low Quiescent Current<br>• Low Cost Package | 8 Pin DIL<br>5 Pin TO-220 |
| UC1706/3706<br><br><br><br><br><br>UC1707/3707 | Dual High Current MOSFET Compatible Output Driver<br><br><br><br><br><br>Dual Uncommitted High Current MOSFET Compatible Output Driver | • Dual, 1.5A, Totem Pole Outputs<br>• Parallel or Push-Pull Operations<br>• Single-Ended to Push-Pull Conversion (1706 Series)<br>• Internal Overlap Protection<br>• Analog, Latched Shutdown<br>• High-Speed, Power MOSFET Compatible<br>• Thermal Shutdown Protection<br>• 5 to 40V Operation<br>• Low Quiescent Current | 16 Pin DIL "Batwing" |
| UC1728/3728 | PWM Dual Driver | Load Control and Status monitoring for two inductive loads) up to 1 amp each.<br>• PWM Current Control<br>• Dual, Floating Switches<br>• Supply Voltage up to 60V<br>• Tri-State Status Outputs<br>• 60V Operation | 28 Pin DIL<br>28 PLCC |
| UC2950 | Half-Bridge Bipolar Switch | • Source or Sink 4.0A<br>• Supply Voltage to 35V<br>• High-Current Output Diodes<br>• Tri-State Operation<br>• TTL and CMOS Input Compatibility<br>• Thermal Shutdown Protection<br>• 300kHz Operation | 5 Pin TO-220 |



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# POWER DRIVER & INTERFACE CIRCUITS (cont.)

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| TYPE | DESCRIPTION | KEY FEATURES | PACKAGE |
|---|---|---|---|
| UC3657 | Triple Half Bridge Power Driver | See Motor Control Section | 15 Pin Power Tab |
| UC3720 | Smart Switch | Independent high and low side switching, up to 2.5A capability.<br>• Full Protection<br>• Over- and Under-Current Fault Indication<br>• 50V Operation | 15 Pin Power Tab |
| UC3722 | Five Channel Programmable Current Switch | • Five Current-Sinking Switches<br>• Programmable Currents from .5 to 2.5A<br>• Internal Current Sensing<br>• 40V Operation<br>• Protection Features | 15 Pin Power Tab |
| UC5170 | Octal Single Ended Line Driver | Suited for data transmission systems.<br>• Eight Driver in One Package<br>• Meets EIA Standards<br>• Single External Resistor Controls Slew Rate<br>• Tri-State Outputs<br>• Low Power Consumption<br>• TTL Compatible | 28 Pin DIL<br>28 PLCC |
| UC5180/5181 | Octal Line Receiver | Suited for digital communication requirements.<br>• Eight Receivers in One Package<br>• Meets EIA Standards<br>• Single 5V Supply<br>• Differential Inputs Withstand ±25V<br>• Low Noise Filter (5180 Only) | 28 Pin DIL<br>28 PLCC |

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# OP AMPS & COMPARATORS

| TYPE | DESCRIPTION | KEY FEATURES | PACKAGE |
|---|---|---|---|
| UCOP01 | High Speed - High Slew Rate Op Amp | • Low Power<br>• Fast Settling Time<br>• Internally Compensated<br>• Pin Compatible with 741, OP01 | 8 Pin DIL |
| UCOP02 | High Performance General Purpose Op Amp | • Low Power<br>• Low Offset Voltage Drift<br>• Internally Compensated<br>• Pin Compatible with 741 | 8 Pin DIL |
| UC161 | Quad Comparator with Programmable AC & DC Parameters | • Wide Input Common Mode Range<br>• Low Power<br>• Directly Compatible with CMOS Logic<br>• Output Drive Level Programmability<br>• Outputs Can Be Wire Or'd | 16 Pin DIL |
| UC542 | High Slew Rate Operational Amplifier | • High Slew Rate 150V/μs tvd<br>• Fast Settling Time: 1% in 75ns<br>• Open Loop Gain: 70dB min.<br>• Low Offset Voltage Drift 10μV/°C max.<br>• Wide Bandwidth: DC to 100MHz at 10dB Gain | 8 Pin DIL |
| UC1704/3704 | Bridge Transducer Switch for Monitoring Systems | See Power Driver & Interface Circuits. | |

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# VL16C450 • VL82C50A • VL82C50

## ASYNCHRONOUS COMMUNICATIONS ELEMENT

### FEATURES

- Full double buffering
- Independent control of transmit, receive, line status and data set interrupts
- Modem control signals include $\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$ and $\overline{DCD}$.
- Programmable serial interface characteristics:
  - —5-,6-,7- or 8-bit characters
  - —Even-, odd- or no-parity bit generation and detection
  - —1-, 1½- or 2-stop bit generation
  - —Baud rate generation (dc to 56K baud)
- Full status reporting capabilities
- 3-state TTL drive capabilities for bidirectional data bus and control bus

### DESCRIPTION

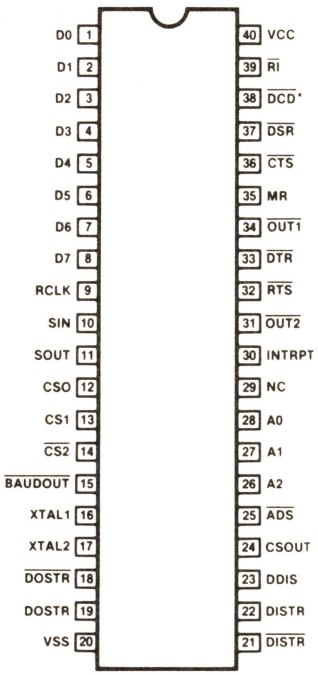
The VL16C450 is an asynchronous communications element (ACE) that is functionally equivalent to the VL82C50A, but is an improved-specification version of that part. The improved specifications provide ensured compatibility with state-of-the-art CPUs.

The VL16C450, VL82C50A, and VL82C50 ACEs serve as serial data input/output interfaces in microcomputer systems. They perform serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing or break interrupt.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and ($2^{16}$-1).

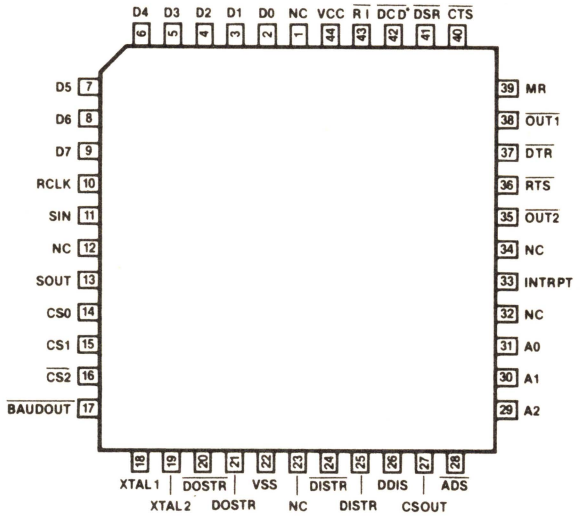
### PIN DIAGRAMS

**VL16C450**
**VL82C50A**
**VL82C50**




*ON THE VL82C50, PIN 38 (PIN 42 ON THE PLCC PACKAGE) IS ALSO CALLED $\overline{RLSD}$

**VL16C450**
**VL82C50A**
**VL82C50**




### ORDER INFORMATION

| Part Number | Maximum External Clock Frequency | Package |
|---|---|---|
| VL16C450-PC | 3.1 MHz | Plastic DIP |
| VL16C450-CC | | Ceramic DIP |
| VL16C450-QC | | Plastic Leaded Chip Carrier (PLCC) |
| VL82C50A-PC | 3.1 MHz | Plastic DIP |
| VL82C50A-CC | | Ceramic DIP |
| VL82C50A-QC | | Plastic Leaded Chip Carrier (PLCC) |
| VL82C50-PC | 3.1 MHz | Plastic DIP |
| VL82C50-CC | | Ceramic DIP |
| VL82C50-QC | | Plastic Leaded Chip Carrier (PLCC) |

**Note:**
Operating temperature range: 0°C to +70°C.



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# VL16C451

## PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

### FEATURES

- IBM PC/AT-compatible
- VL16C450 with on-board Centronix printer interface
- Completely pin- and upward-compatible with the dual serial channel VL16C452
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable serial interface characteristics:
  - 5-,6-,7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus

### DESCRIPTION

The VL16C451 is an enhanced version of the popular VL16C450 asynchronous communications element (ACE). The serial channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the Parallel/Asynchronous Communications Element (P/ACE) can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions. It is fully pin- and upward-compatible with the dual serial channel VL16C452. The second serial channel of the VL16C452 occupies pins that are VCC, GND, or N.C. (not connected) on the VL16C451.

The VL16C451 also provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the P/ACE. The parallel port, together with the serial port, provide IBM PC/AT-compatible computers with a single device to serve the two system ports.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and ($2^{16}$ -1).

The VL16C451 is housed in a 68-pin plastic leaded chip carrier.

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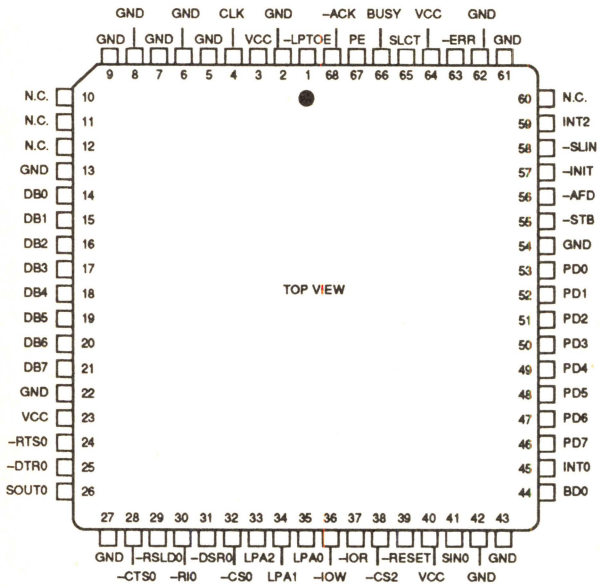
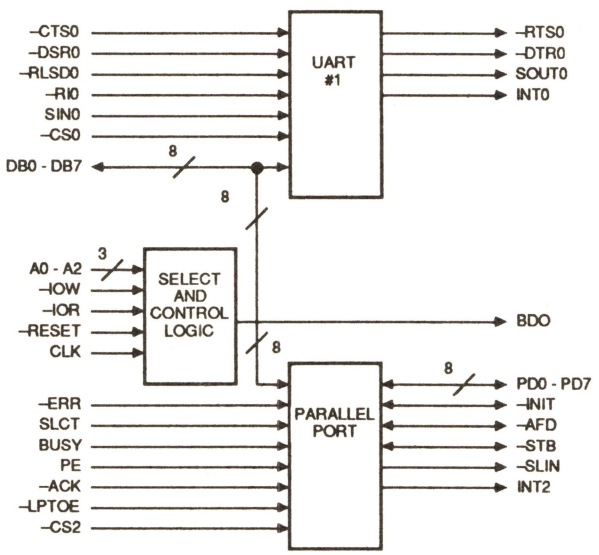
### PIN DIAGRAM

VL16C451




### BLOCK DIAGRAM




### ORDER INFORMATION

| Part Number | Maximum Clock Frequency | Package |
|---|---|---|
| VL16C451-QC | 3.1 MHz | Plastic Leaded Chip Carrier (PLCC) |

**Note:** Operating temperature range is 0°C to +70°C.

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# VL16C452

## DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT

### FEATURES

- IBM PC/AT compatible
- Dual-channel version of VL16C450
- Centronix printer interface
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
  - 5-,6-,7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive capabilities for bidirectional data bus and control bus

### DESCRIPTION

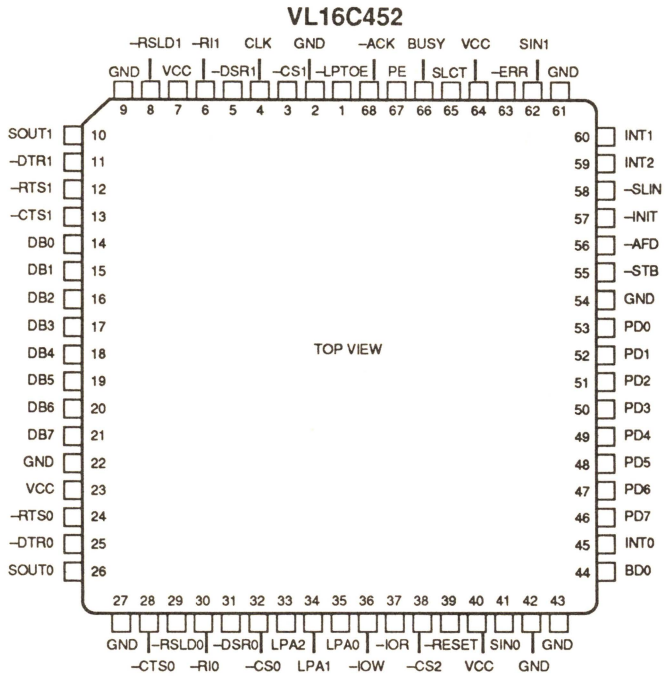
The VL16C452 is an enhanced dual-channel version of the popular VL16C450 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions.

In addition to its dual communications interface capabilities, the VL16C452 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the dual ACE. The parallel port, together with the two serial ports, provide IBM PC/AT compatible computers with a single device to serve the three system ports.

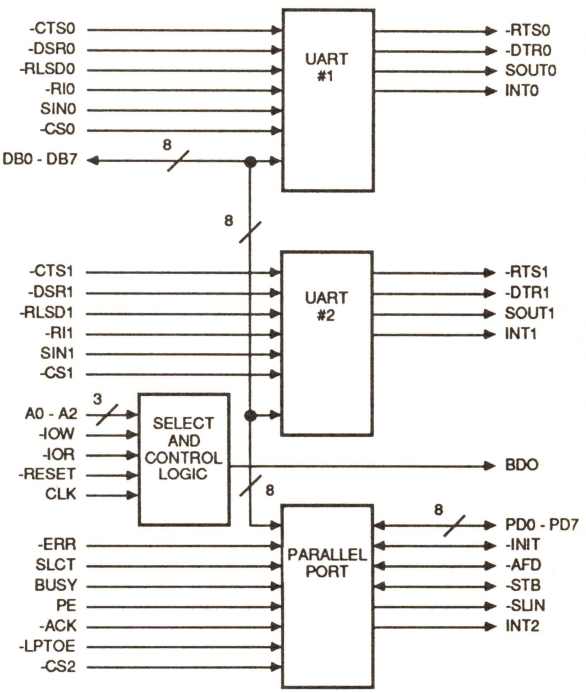
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and ($2^{16}$ -1).

The VL16C452 is housed in a 68-terminal plastic leaded chip carrier.

### PIN DIAGRAM




### BLOCK DIAGRAM




### ORDER INFORMATION

| Part Number | Maximum Clock Frequency | Package |
|---|---|---|
| VL16C452-QC | 3.1 MHz | Plastic Leaded Chip Carrier (PLCC) |

**Note:** Operating temperature range is 0°C to +70°C.

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# VL7C212A

## 300/1200 BIT-PER-SECOND MODEM

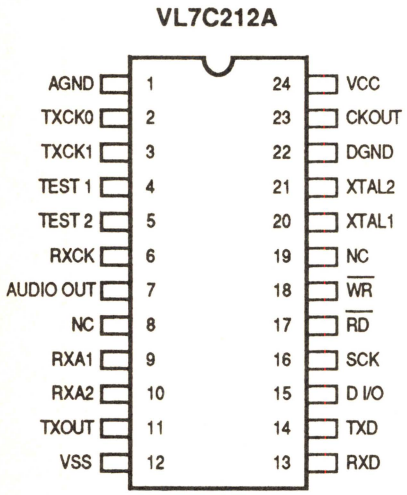
### FEATURES

- FSK and PSK modulators and demodulators, high-band and low-band filters with compromise ampli tude and group delay equalizers
- Built-in call progress mode and tone generators for DTMF V.21 and V.22 guard tones
- Bell 212A and CCITT V.21 and V .22 compatible; V.22 notch filters included
- Serial control interface
- Programmable audio output port
- Analog, digital and remote digital loopback capabilities
- 24-pin DIP and 28-terminal plastic leaded chip carrier available
- High level of integration provides a highly cost effective 300/1200 bit-per- second modems
- Eliminates external components, easing design of intelligent modems
- Usable in North American and European modem designs
- Simple board layout
- Simple speaker interface for monitoring phone line
- Testable signal path
- Reduced board area
- Direct replacement for Sierra SC11004 and SC11014

### DESCRIPTION

The VL7C212A is a complete 300/1200 bit-per-second modem. All of the signal processing functions needed for a full duplex, 300/1200 bit-per-second 212A (V.21 or V.22) modem, including both FSK and PSK modulators and demodulators and the high-band and low-band filters, are integrated on a single chip. It is built using a three-micron CMOS double-polysilicon process that allows analog and digital functions to be combined on the same chip. This design includes capabilities for progress monitoring and for generating DTMF as well as V.21 or V.22 guard tones. The two-to-four wire hybrid is also included, simplifying the interface to a DAA. The VL7C212A also includes analog loopback and remote digital loopback functions for self-testing.

### PIN DIAGRAM

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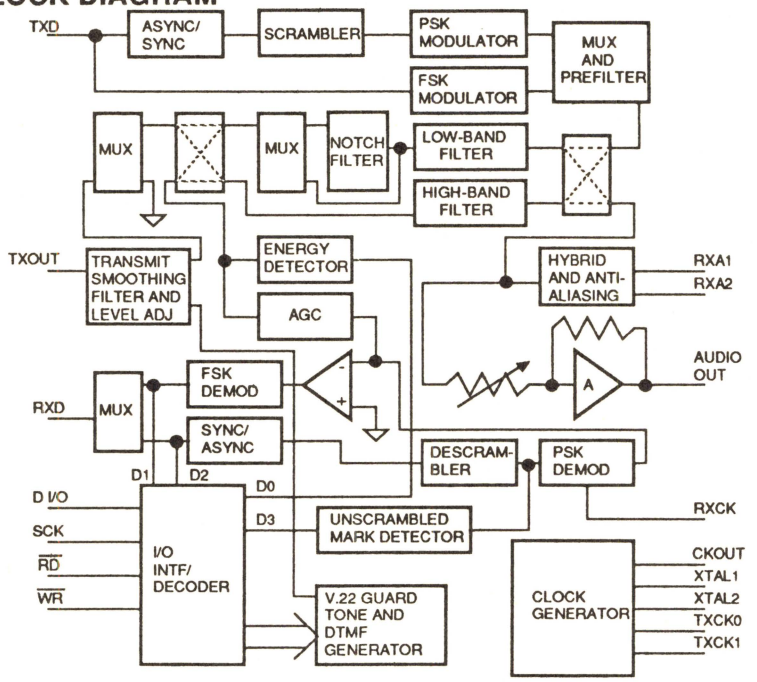


### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL7C212A-PC | Plastic DIP |
| VL7C212A-QC | Plastic Leaded Chip Carrier (PLCC) |

**Note:** Operating temperature range is 0°C to +70°C.

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# VL7C213

## PARALLEL BUS MODEM CONTROLLER

### FEATURES

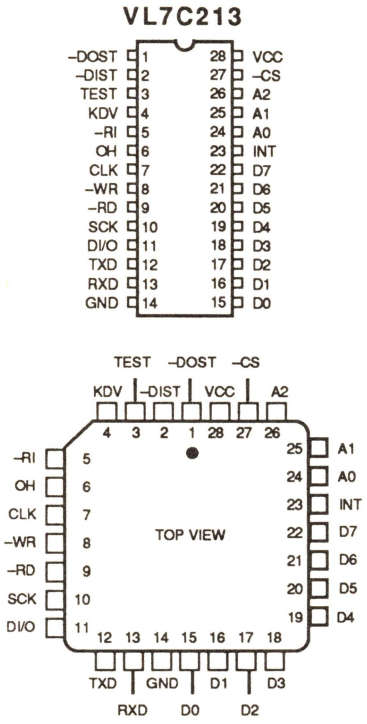
- Direct interface to VL7C212A single-chip modems
- Complete Hayes AT command set in firmware
- Built-in UART
- Direct IBM PC bus interface
- Two-micron CMOS process
- 28-pin DIP or PLCC package
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Replacement for Sierra SC11007
- Reduces board space and component count requirements

### DESCRIPTION

The VL7C213 Parallel Bus Modem Controller is specifically designed to control the VL7C212A single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C213 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the VL7C212A, with the addition of a data access arrangement (DAA), the VL7C213 implements a Hayes-type smart modem for board-level, integral-modem applications. Because the VL7C213 fully emulates the functionality of the VL82C50 UART and includes data bus transceivers, it can be directly interfaced to a computer's parallel data bus (in particular to the bus of the IBM PC, XT or AT). All of the popular communications software written for the PC will work with the VL7C213/VL7C212A chip set. In addition to including the functionality of the VL82C50 UART, the VL7C213 contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM.

For specific high-volume applications, the control program can be modified by VLSI to include additional command functions.

### PIN DIAGRAMS

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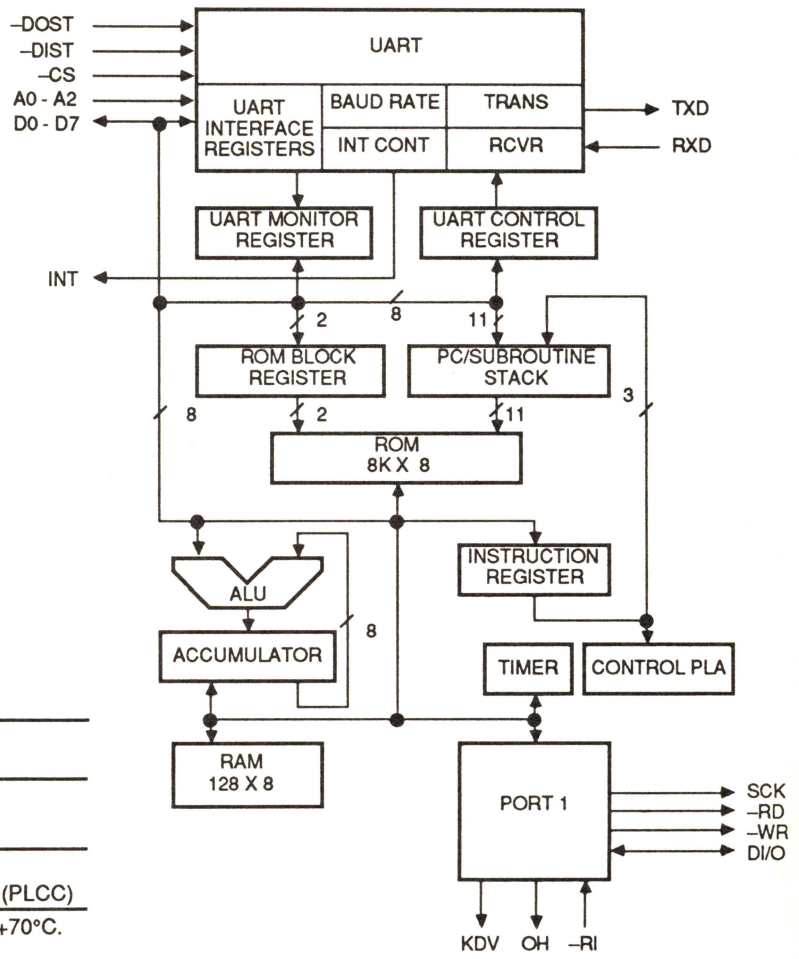


### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL7C213-PC | Plastic DIP |
| VL7C213-QC | Plastic Leaded Chip Carrier (PLCC) |

**Note:** Operating temperature range is 0°C to +70°C.

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# VL7C214

## STAND-ALONE MODEM INTERFACE CONTROLLER

### FEATURES

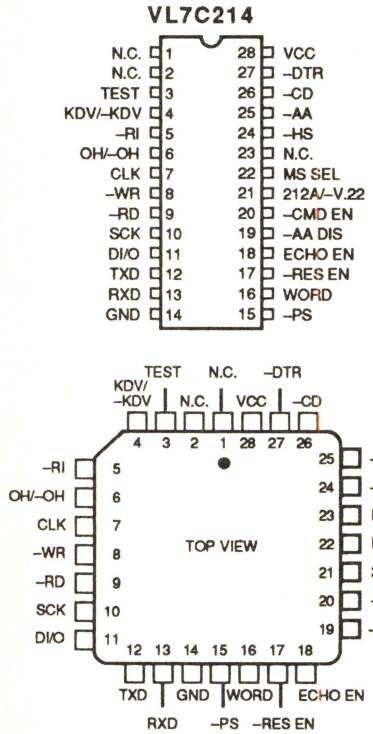
- Direct interface to VL7C212A single chip modems
- Complete Hayes AT command set in firmware
- Built-in UART for RS232C interface
- Two-micron CMOS process
- 28-pin DIP or PLCC package
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Reduces board space and component count requirements
- Low power consumption
- Replacement for Sierra SC11008

### DESCRIPTION

The VL7C214 Stand-Alone Modem Interface Controller is specifically designed to control the VL7C212A single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C214 provides a highly cost effective solution for interfacing a modem IC to a computer's RS232C port. When connected to the VL7C212A, with the addition of a data access arrangement (DAA), the VL7C214 implements a Hayes-type smart modem for stand-alone modem applications. All of the popular communications software written for the IBM PC will work with the VL7C214/VL7C212A chip set. The VL7C214 contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM. In order to support the stand-alone functionality of the device, an 8-bit switch input port allows immediate user access and manual control of the system. Either Bell 103 or CCITT V.22 may be selected in this manner.

For specific high volume applications, the control program can be modified by VLSI Technology, Inc. to include additional commands and functions.

### PIN DIAGRAMS

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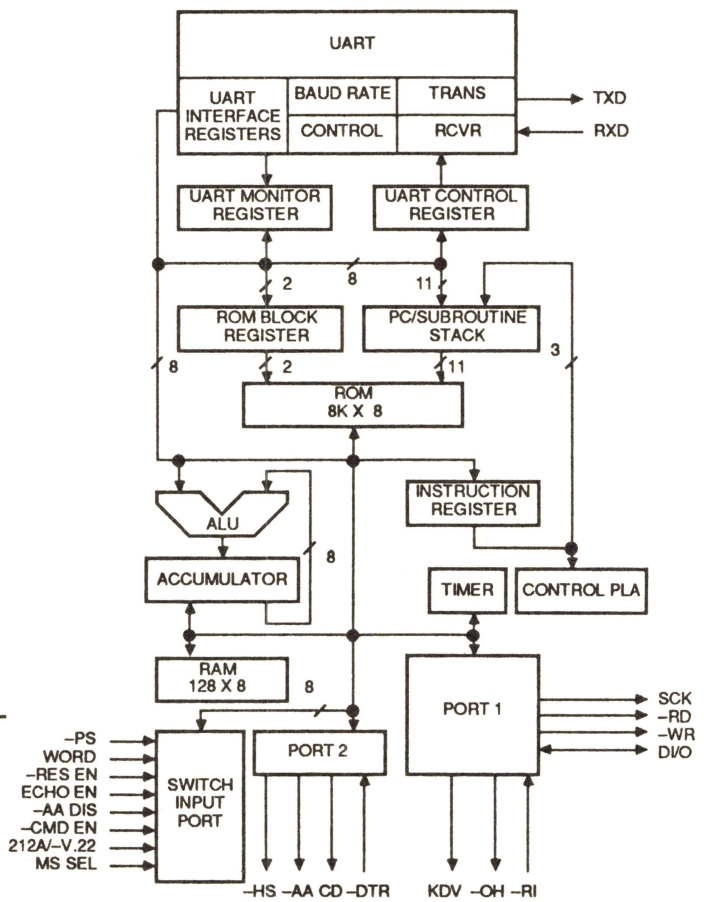


### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL7C214-PC | Plastic DIP |
| VL7C214-QC | Plastic Leaded Chip Carrier (PLCC) |

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# VL7C224A

## 2400 BIT-PER-SECOND MODEM

### FEATURES

- Complete 2400 bit-per-second modem conforming to V.22 bis specifications
- Compatible with CCITT V.22 bis, V.22, V.21 and BELL 212A and 103 standards
- Integrated DTMF/GUARD TONE GENERATOR, call progress monitor and contains an on-chip hybrid
- Analog, digital and remote digital loopback
- Programmable audio output port
- Three-micron CMOS technology
- DIP or PLCC package
- High-level of integration provides for economical 2400 bit-per-second modem solution
- Broadly adaptable to established worldwide standards at 2400, 1200 and 300 bits-per-second
- Minimizes need for external components simplifying design of intelligent modems
- Testable signal path diagnostics
- Audio interface for phone line monitoring
- Low power consumption

### DESCRIPTION

The VL7C224A is a complete 2400 bit-per-second modem IC containing all modem functions except the adaptive equalizer. It is used in conjunction with an external controller such as the VL7C235 (for parallel bus applications), the VL7C245 (for RS-232 applications) or a general purpose microcontroller such as 8096, to implement a 2400 bps full duplex modem, compatible with the CCITT V.22 bis recommendation. The controller performs all modem control and handshaking functions as well as the adaptive equalization.

The VL7C224A operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22 and V.22 bis standards. When used with the VL7C225, VL7C235, or VL7C245 controllers, the VL7C224A becomes an intelligent modem controlled by the industry standard "AT" command set. The interface between the VL7C224A modem and the controller (either the 8096 or the VL7C225/235/245) is a standard microcontroller interface that easily connects to an EEPROM for permanent storage of configuration settings and phone numbers.

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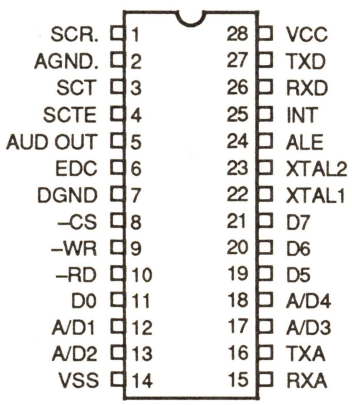
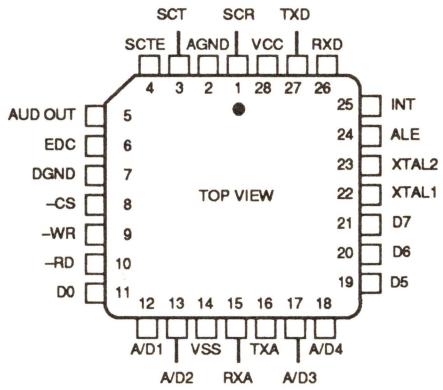
### PIN DIAGRAMS

**VL7C224A-PC**




**VL7C224A-QC**




### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL7C224A-PC | Plastic DIP |
| VL7C224A-QC | Plastic Leaded Chip Carrier (PLCC) |

**Note:** Operating temperature range is 0°C to +70°C.

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# VL7C225 • VL7C235 • VL7C245

## 2400 BIT-PER-SECOND MODEM ADVANCED COPROCESSOR FAMILY

### FEATURES

- Direct interface to the VL7C224A single-chip modem
- Complete "AT" command set in firmware
- Built-in 82C50B UART equivalent
- Direct IBM PC bus interface
- External ROM/RAM addressable
- Two-micron CMOS technology
- 2400 bps intelligent modem using just two chips
- Compatible with industry standard software
- No external buffers required

### DESCRIPTION

The VL7C225 family are specialized controllers that interface directly to the VL7C224A Modem to form a 2400 bps full duplex intelligent modem. The two-chip set performs all the modem functions as well as automatic control features compatible to the Hayes "AT" Command Set. The chip set is compatible to the CCITT V.22 BIS with V.22 fallback, Bell 212A with 103 fallback, as well as the V.21 standard.

The VL7C235 interfaces to a parallel system bus, such as the bus in the IBM PC, while the VL7C245 interfaces to an RS232 port.

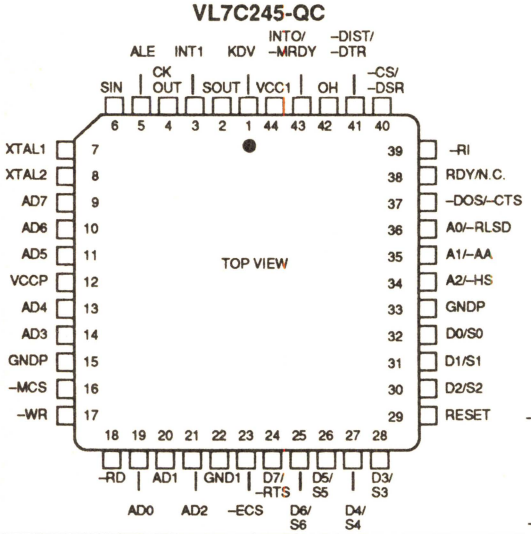
The controller receives 8-bit signal samples from the VL7C224A and performs adaptive equalization, Carrier phase recovery, data decode, and de-scrambling.

The VL7C225, VL7C235, and VL7C245 have identical hardware. However, they can be configured as a parallel (VL7C235), or serial (VL7C245) device by programming the internal ROM. The VL7C225 is the ROM-less version and is available in a 68-pin PLCC package. It is intended for use with external memory to accommodate customized firmware.

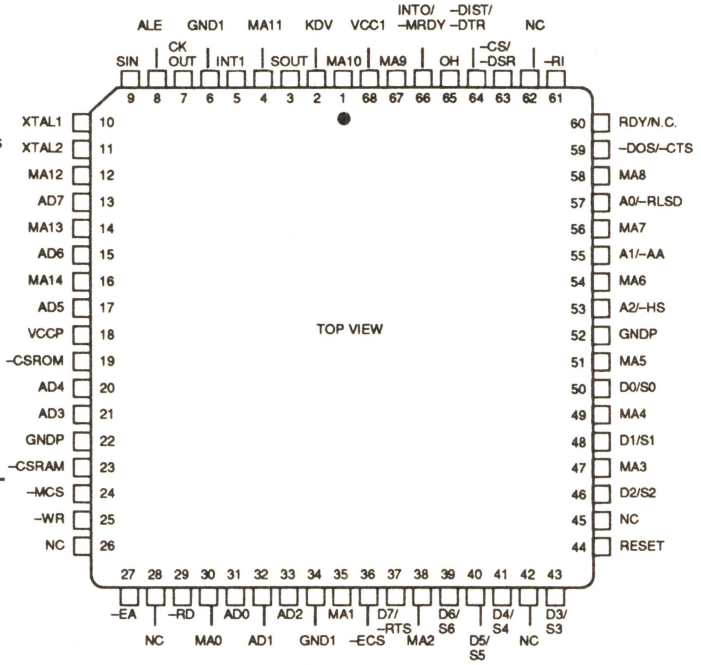
These controllers use a bit slice core processor to perform digital signal processing (DSP) and the control function. Its instruction set is a fast subset of the 8096 instruction set.

### PIN DIAGRAMS

**VL7C235-QC**
**VL7C245-QC**




**VL7C225-QC**




### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL7C235-PC | Plastic DIP |
| VL7C235-QC | Plastic Leaded Chip Carrier (PLCC) |
| VL7C245-PC | Plastic DIP |
| VL7C245-QC | Plastic Leaded Chip Carrier (PLCC) |
| VL7C225-QC | Plastic Leaded Chip Carrier (PLCC) |

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# VL82C37A

## CMOS DIRECT MEMORY ACCESS (DMA) CONTROLLER

### FEATURES

- Low-power CMOS version of popular 8237A DMA controller
- Four DMA channels
- Individual enable/disable control of DMA requests
- Directly expandable to any number of channels
- Independent auto-initialize feature for all channels
- High performance 8 MHz version available
- Transfers may be terminated by end-of-process input
- Software controlled DMA requests
- Independent polarity control for DREQ and DACK signals

### DESCRIPTION

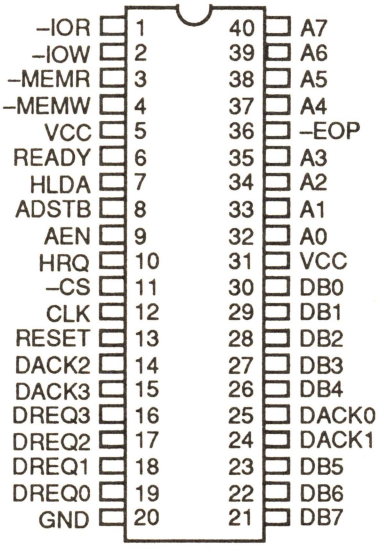
The VL82C37A Direct Memory Access (DMA) Controller serves as a peripheral interface circuit for microprocessor systems, and is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The VL82C37A DMA Controller offers many programmable control features that enhance data throughput and system performance. Dynamic reconfiguration is permitted under program control.

The VL82C37A is designed to be used with an external 8-bit address register such as the 8282. In addition to the four independent channels, the VL82C37A is expandable to any number of channels by cascading additional controller devices.

Three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to auto-initialize to its original condition following an end-of-process (EOP) input. Each channel also has a 64K address and word count handling ability.

The VL82C37A DMA Controller is available in 5 MHz and 8 MHz clock frequencies.

### PIN DIAGRAM

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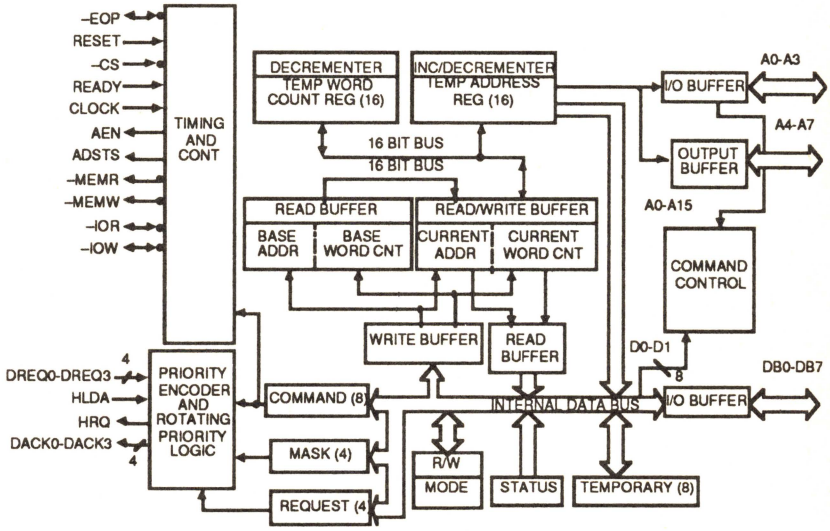


### ORDER INFORMATION

| Part Number | Clock Frequency | Package |
|---|---|---|
| VL82C37A-05PC | 5 MHz | Plastic DIP |
| VL82C37A-05CC | | Ceramic DIP |
| VL82C37A-05QC | | Plastic Leaded Chip Carrier (PLCC) |
| VL82C37A-08PC | 8 MHz | Plastic DIP |
| VL82C37A-08CC | | Ceramic DIP |
| VL82C37A-08QC | | Plastic Leaded Chip Carrier (PLCC) |

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# VL82C284

## CMOS CLOCK GENERATOR AND INTERFACE

### FEATURES

- Generates clock for Intel 286-type microprocessor-based systems
- External TTL source or crystal may be used as frequency source
  - On-board crystal oscillator
- Provides Local –READY signal for system synchronization
- Generates system reset
- Schmitt-trigger reset input assures stability and noise immunity
- Low power consuming CMOS technology

### DESCRIPTION

The VL82C284 is a clock generator and driver that provides clock and interface signals to Intel 286-type microprocessor-based systems. All device output signals are synchronized to the output clock signal.

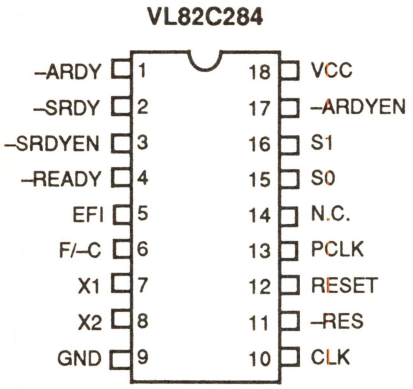
The clock input and output frequencies are twice the frequency used internally by the microprocessor in the system. To avoid confusion, the clock frequency in the order information represents the internal system microprocessor clock frequency (e.g., the devices listed as 8 MHz would actually have an input crystal or a TTL signal frequency of 16 MHz).

The VL82C284 also supplies the system with a high-noise-immunity reset, as well as a synchronous peripheral clock and a synchronous –READY to indicate the completion of the current bus cycle.

The peripheral clock is controlled by two status input signals, which may be left open if not used.

The VL82C284 is available in an 18-pin ceramic and plastic DIP, as well as in a plastic leaded chip carrier.

### PIN DIAGRAM

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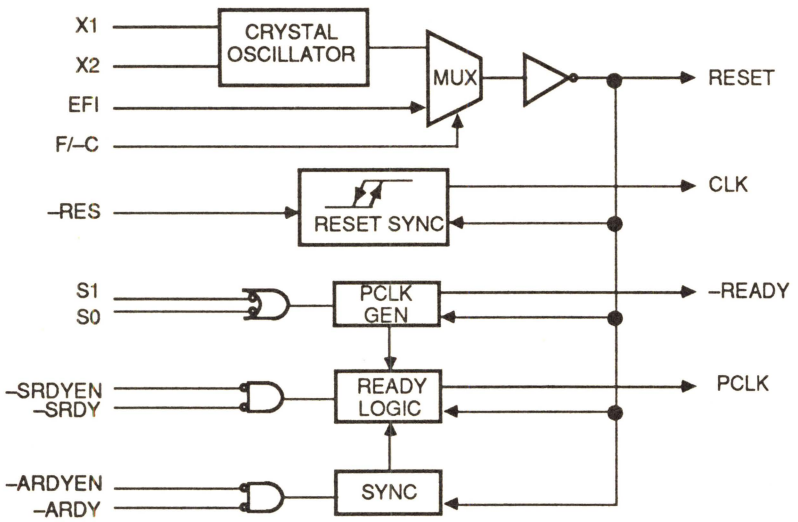


### ORDER INFORMATION

| Part Number | Clock Frequency | Package |
|---|---|---|
| VL82C284-08PC | 8 MHz | Plastic DIP |
| VL82C284-08QC | | Plastic Leaded Chip Carrier (PLCC) |
| VL82C284-08CC | | Ceramic DIP |
| VL82C284-10PC | 10 MHz | Plastic DIP |
| VL82C284-10QC | | Plastic Leaded Chip Carrier (PLCC) |
| VL82C284-10CC | | Ceramic DIP |

**Note:** Operating temperature range is 0°C to +70°C.



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VLSI TECHNOLOGY, INC.

# VL82C288

## CMOS BUS CONTROLLER

### FEATURES

- Both local and system bus commands and control are provided
- Supports both Multibus® and high-speed bus cycle operating modes
- High-current output drivers
- Flexible command timing
- High degree of system configuration flexibility
- Low power consuming CMOS technology
- Single 5 V power supply

### DESCRIPTION

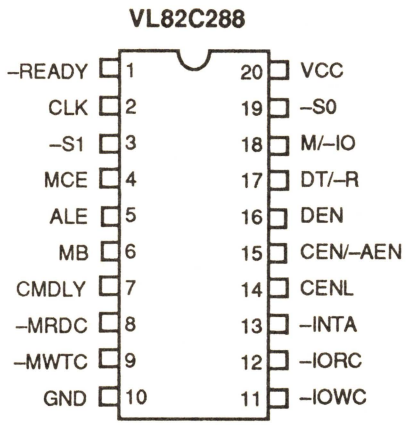
The VL82C288 is a CMOS bus controller for use in Intel 286-type microprocessor-based systems. A mode select pin allows strapping the device for Multibus operation or for short bus cycles. The device also provides separate command outputs for memory and I/O devices. The data bus is controlled by separate data direction and data enable signals.

A system clock provides the timing control required by the microprocessor-based system. The device clock input is twice the system clock speed. To avoid confusion, the clock frequency listed in the order information is the system clock frequency (e.g., the devices listed as 8 MHz Clock Frequency, would have an input clock of 16 MHz).

The VL82C288 meets the timing and drive requirements to satisfy the IEEE-796 standard for Multibus.

The VL82C288 is available in a 20-pin ceramic or plastic DIP, as well as in a plastic leaded chip carrier.

### PIN DIAGRAM

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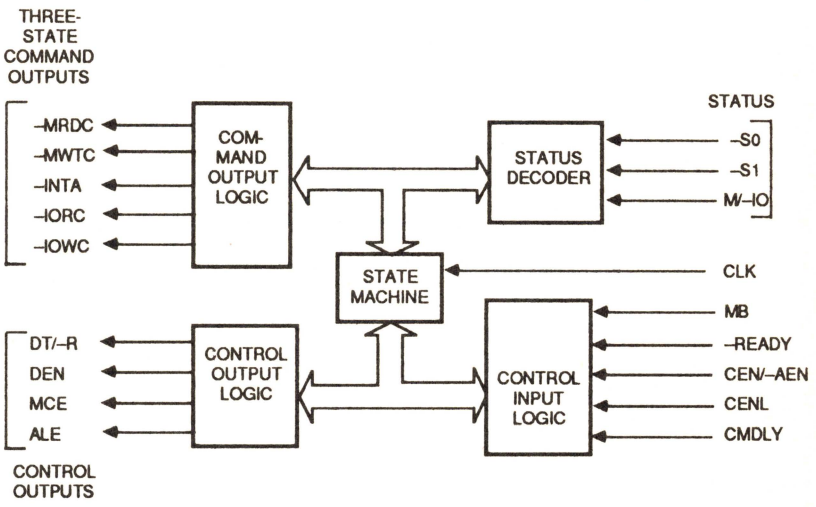


### ORDER INFORMATION

| Part Number | Clock Frequency | Package |
|---|---|---|
| VL82C288-06PC | 6 MHz | Plastic DIP |
| VL82C288-06QC | | Plastic Leaded Chip Carrier (PLCC) |
| VL82C288-06CC | | Ceramic DIP |
| VL82C288-08PC | 8 MHz | Plastic DIP |
| VL82C288-08QC | | Plastic Leaded Chip Carrier (PLCC) |
| VL82C288-08CC | | Ceramic DIP |

**Note:** Operating temperature range is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

# VL82C(PC/AT)

## IBM PC/AT COMPATIBLE CHIP SET

### FEATURES

- Fully compatible with IBM PC/AT-type designs
- High-Integration five-chip set
- Reduces non-memory system device count from 110 to 16
- Supports 12 MHz processor clock
- Devices are available as "cores" for user-specific designs
- All devices designed in CMOS for low power consumption

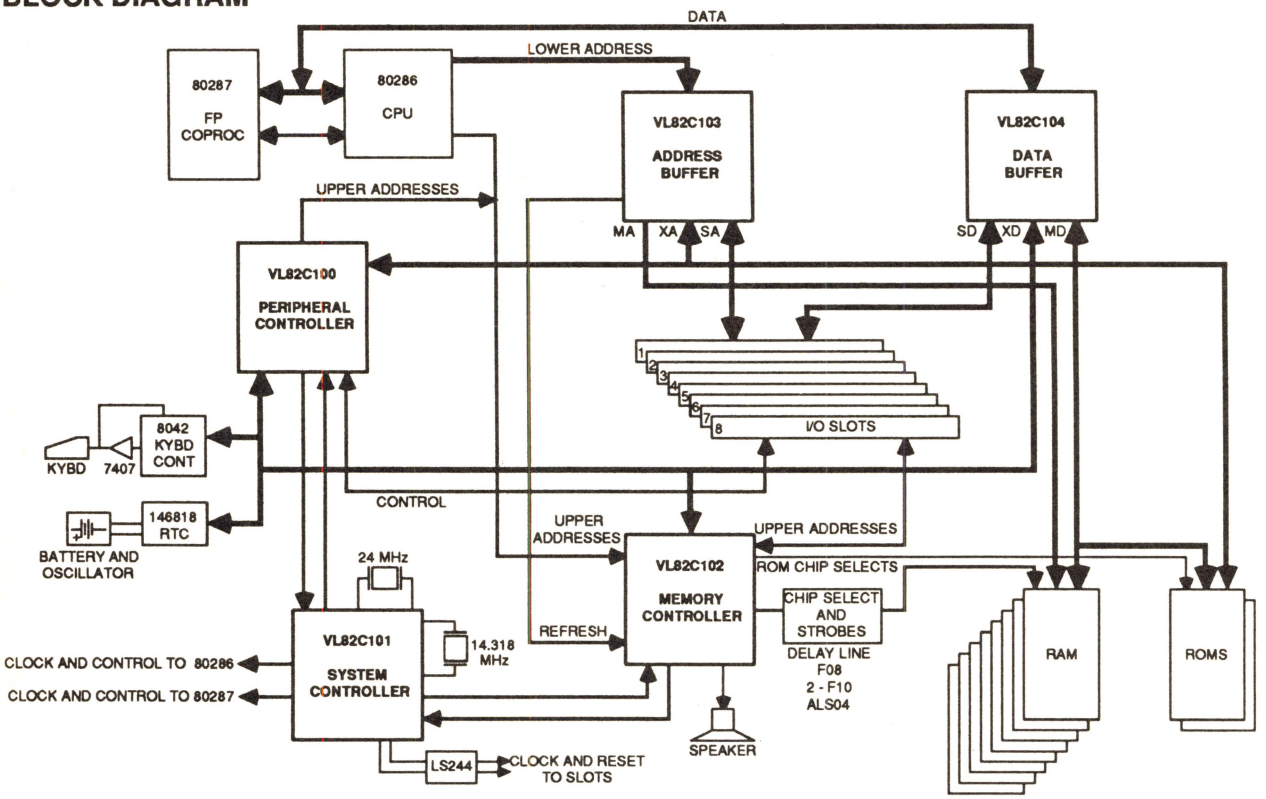
### DESCRIPTION

The IBM PC/AT compatible chip set from VLSI Technology, Inc. supports 1-Megabit dynamic RAMs, and is utilized in systems with clock speeds up to 12 MHz. The chip set provides the IBM PC/AT compatible system with a completely compatible low-cost board design solution. Further, since the devices were designed using VLSI's design tools, the devices can be quickly modified for use as cores in user-specific designs.

The five-device chip set has been designed using the highest integration consistent with economic and reliable system design. The VL82C103 Address Buffer and VL82C104 Data Buffer are offered in separate packages, although their circuitry is relatively small. If they were offered as a single device, the pin count would be extremely high, or some performance degradation would occur.

The devices are manufactured with VLSI's advanced high-performance CMOS process and all five are available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package.

### BLOCK DIAGRAM




### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL82C100-QC | Plastic Leaded Chip Carrier (PLCC) |
| VL82C101-QC | Plastic Leaded Chip Carrier (PLCC) |
| VL82C102-QC | Plastic Leaded Chip Carrier (PLCC) |
| VL82C103-QC | Plastic Leaded Chip Carrier (PLCC) |
| VL82C104-QC | Plastic Leaded Chip Carrier (PLCC) |

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VLSI TECHNOLOGY, INC.

# VL83C11

## GENERAL PURPOSE (SCSI) BUS TRANSCEIVER

### FEATURES

- Meets full Small Computer Systems Interface (SCSI) specifications for system cables up to six meters long
- Fully buffered, bidirectional data and control buses
- Interfaces directly to VL53C86 and NCR 5386 family
- Can be used with other interfaces requiring a 48 mA drive
- Low cost
- Two-micron CMOS technology
- Housed in a standard 52-pin PLCC

### DESCRIPTION

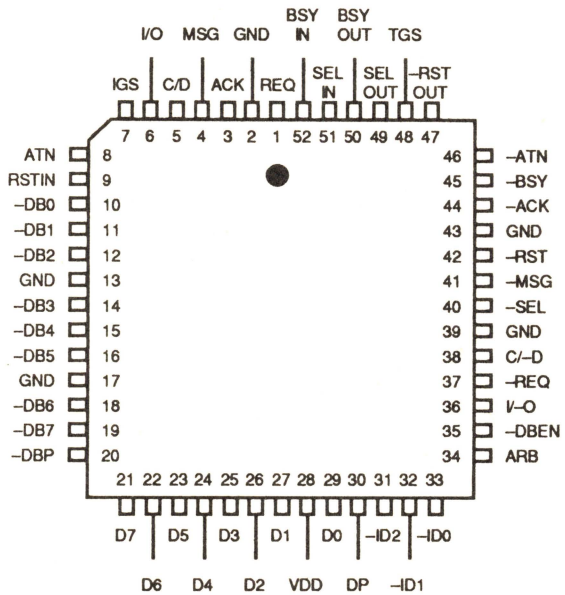
The VL83C11 General Purpose Bus Transceiver Chip, is a two-micron CMOS device designed as a 48 mA bus transceiver chip for all of the Small Computer System Interface (SCSI) bus signals. It incorporates high current single-ended drivers for the SCSI bus. The VL83C11 is specifically intended to be used with the VL53C86 or NCR 53C86 SCSI Protocol Controller families. It interfaces directly to those devices, with no additional circuits required. It can be used with other interfaces where a general purpose 48 mA bus transceiver is required. Logical and electrical flexibility also allow its use as a general pupose interface driver/ receiver chip.

The VL83C11 is functionally equivalent to the NMOS NCR 8310, but has been designed in CMOS technology. It meets the full electrical specifications of Small Computer Systems Interface (SCSI) for system cable lengths up to six meters long. Further, it has been optimized for connection to the standard SCSI connector.

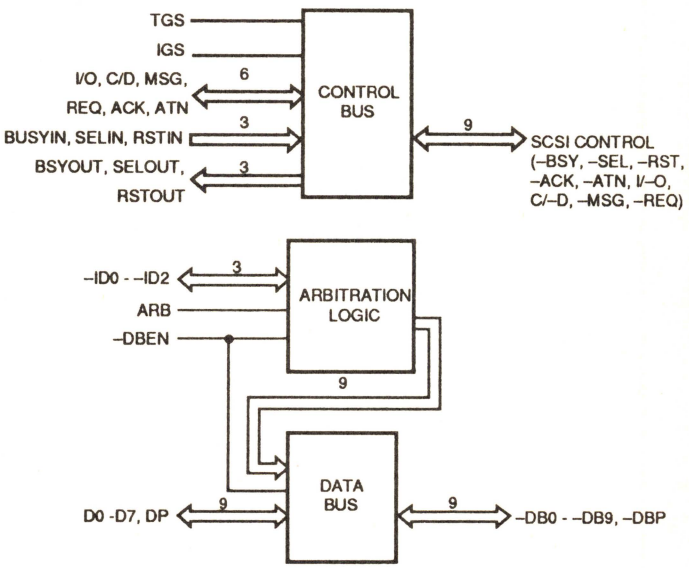
The VL83C11 General Purpose Tranceiver Chip is packaged in a 52-pin plastic leaded chip carrier (PLCC).

### PIN DIAGRAM

VL83C11-QC




### BLOCK DIAGRAM




### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL83C11-QC | Plastic Leaded Chip Carrier (PLCC) |

**Note:** Operating temperature range is 0°C to +70°C

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# ENHANCED SERIAL COMMUNICATIONS CONTROLLER (ESCC)

## FEATURES

- Enhanced SCC functions support DMA
  - 14-bit byte counter
  - 19-bit-wide FIFO
- Completely downward compatible with the NMOS 8530
- Two independent full-duplex channels
- Programmable clock factor
- Break generation and error detection
- Intelligent SDLC/HDLC
- Local loopback and auto echo modes
- Internal or external character synchronization
- Low power consuming CMOS

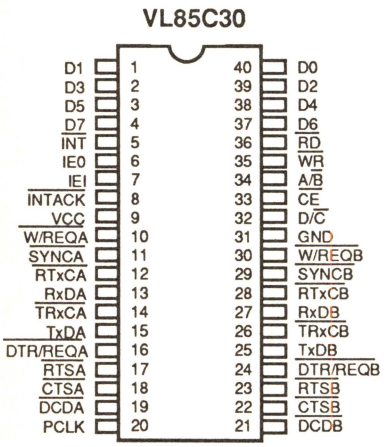
## DESCRIPTION

The VL85C30 CMOS Enhanced Serial Communications Controller (ESCC) is a dual-channel, multi-protocol data communications peripheral designed for use with non-multiplexed buses. The ESCC can be software configured for a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including all of the features of the NMOS 8530. In addition, the VL85C30 Enhanced SCC contains a 10 x 19-bit FIFO array and 14-bit byte counter. These features, in addition to the new higher clock frequency capabilities, allow the ESSC to be used with a direct memory access (DMA) controller.

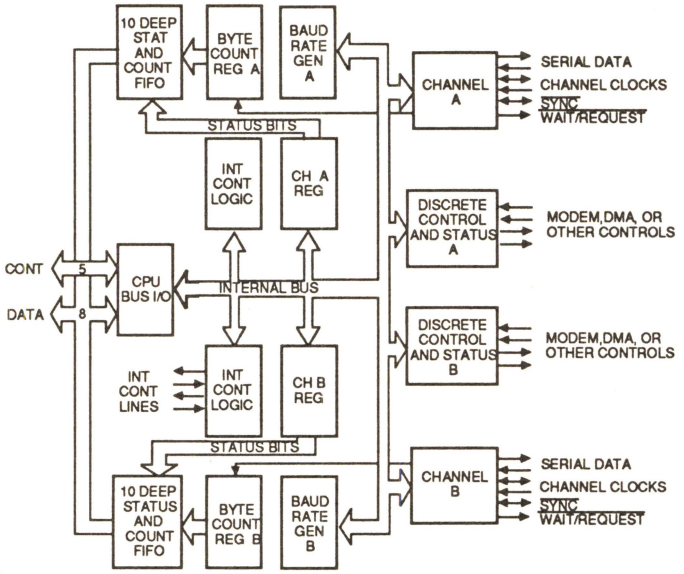
The ESCC handles asynchronous formats, such synchronous byte-oriented protocols as IBM Bisync and such synchronous bit-oriented protocols as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.), including DMA.

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels, in addition to its Byte - Counting Register and FIFO in SDLC mode.

## PIN DIAGRAM




## BLOCK DIAGRAM




## ORDER INFORMATION

| Part Number | Clock Frequency | Package |
|---|---|---|
| VL85C30-8PC<br>VL85C30-8QC<br>VL85C30-8CC | 8 MHz | Plastic DIP<br>Plastic Leaded Chip Carrier (PLCC)<br>Ceramic DIP |
| VL85C30-10PC<br>VL85C30-10QC<br>VL85C30-10CC | 10 MHz | Plastic DIP<br>Plastic Leaded Chip Carrier (PLCC)<br>Ceramic DIP |
| VL85C30-12PC<br>VL85C30-12QC<br>VL85C30-12CC | 12 MHz | Plastic DIP<br>Plastic Leaded Chip Carrier (PLCC)<br>Ceramic DIP |

**Note:** Operating temperature range is 0°C to +70°C.

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# VL86C010

## 32-BIT RISC MICROPROCESSOR

## DESCRIPTION

- 32-bit internal architecture
- 32-bit external data bus
- 64M-byte linear address space
- Bus timing optimized for standard DRAM usage with page mode operation
- 32M-byte/second bus bandwidth
- Simple/powerful instruction set providing an excellent high level language compiler target
- Hardware support for virtual memory systems
- Low interrupt latency for real-time application requirements
- Full CMOS implementation results in low power consumption
- Single 5 V ± 5% operation
- 84-pin JEDEC Type-B leadless chip carrier or plastic leaded chip carrier (PLCC)

## FEATURES

The VL86C010 Acorn RISC Machine (ARM) is a full 32-bit general-purpose microprocessor designed using reduced instruction set computer (RISC) methodologies. The processor is targeted for the microcomputer, graphics, industrial and controller markets for use in stand-alone or embedded systems. Applications in which the processor is useful include laser printers, graphics engines, N.C. machines and any other systems requiring fast real-time response to external interrupt sources and high processing throughput.

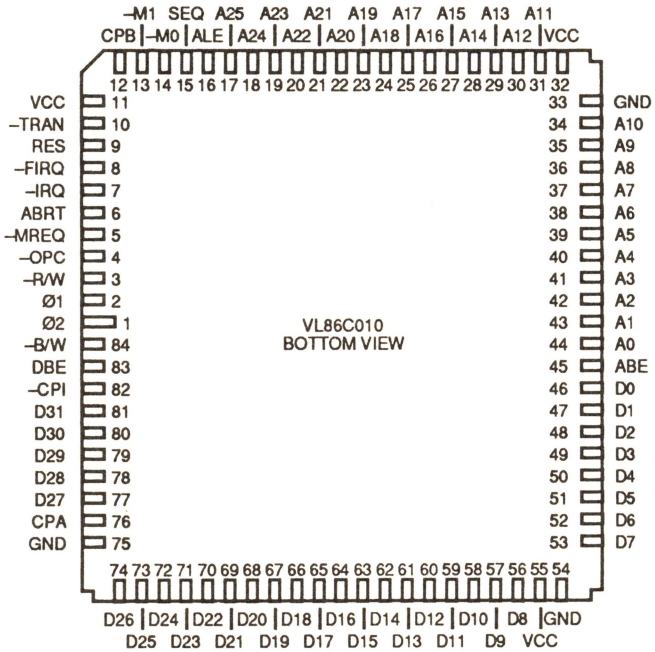
The VL86C010 features a 32-bit data bus, 27 registers of 32 bits each, a load-store architecture, a partially overlapping register set, 2.2 µs worst-case interrupt latency, conditional instruction execution, a 26-bit linear address space and an average instruction execution rate of from four to five million instructions per second (MIPS). Additionally, the processor supports two addressing modes: program counter (PC) and base register relative modes. The ability to do pre- and post-indexing allows stacks and queues to be easily implemented in software. All instructions are 32 bits long (aligned on word boundaries), with register-to-register operations executing in one cycle. The two data types supported are 8-bit bytes and 32-bit words.

Using a load-store architecture simplifies the execution unit of the processor, since only a few instructions deal directly with memory and the rest operate register-to-register. Load and store multiple register instructions provide enhanced performance, making context switches faster and exploiting sequential memory access modes.

The processsor supports two types of interrupts that differ in priority and register usage. The lowest latency is provided by the fast interrupt request (FIRQ) which is used primarily for I/O to peripheral devices. The other interrupt type (IRQ) is used for interrupt routines that do not demand low-latency service or where the overhead of a full context switch is small compared with the interrupt process execution time.

## PIN DIAGRAM

### JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER




## ORDER INFORMATION

| Part Number | Clock Frequency | Package |
|---|---|---|
| VL86C010-10QC | 10 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL86C010-10LC | | JEDEC Type-B Ceramic Carrier |
| VL86C010-12QC | 12 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL86C010-12LC | | JEDEC Type-B Ceramic Carrier |

**Note:** Operating temperature range is 0°C to +70°C.

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# VL86C110

## RISC MEMORY CONTROLLER (MEMC)

### FEATURES

- Drives up to 32 standard dynamic RAMs giving 4M bytes of real memory with 1M bit devices
- Logical-to-physical address translation (32M byte logical address space) supporting three protection levels:
  - Supervisor Mode
  - Operating System Mode
  - User Mode
- Uses fast page mode DRAM accesses to maximize bandwidth from commodity memories
- Internal DMA address generators for video, cursor and sound data buffers
- Various ROM speeds supported (access times of 450 ns, 325 ns, 200 ns)
- Provides all critical system timing including processor clocks, –RAS, –CAS, and DMA data transfer strobes
- Arbitrates memory between the processor and DMA systems

### DESCRIPTION

The memory controller (MEMC) acts as the interface between the ARM (Acorn RISC Machine) processor and other functions in the system. The four circuits in the RISC family: MEMC, ARM, VIDC-video controller, and IOC-I/O controller, can be used to implement a small computer system. MEMC uses a single clock input to derive timing information for the other components.

In addition to providing interface signals to the other controllers, MEMC generates all the control signals for several access times of read-only memory (ROM) plus high-resolution timing and refresh control for dynamic RAM (DRAM). The controller outputs can drive up to 32 memory devices directly in a wide variety of configurations using various architectures of standard DRAMs. A logical-to-physical address translator maps the 4M byte physical memory into the 32M byte logical address space with three levels of protection.

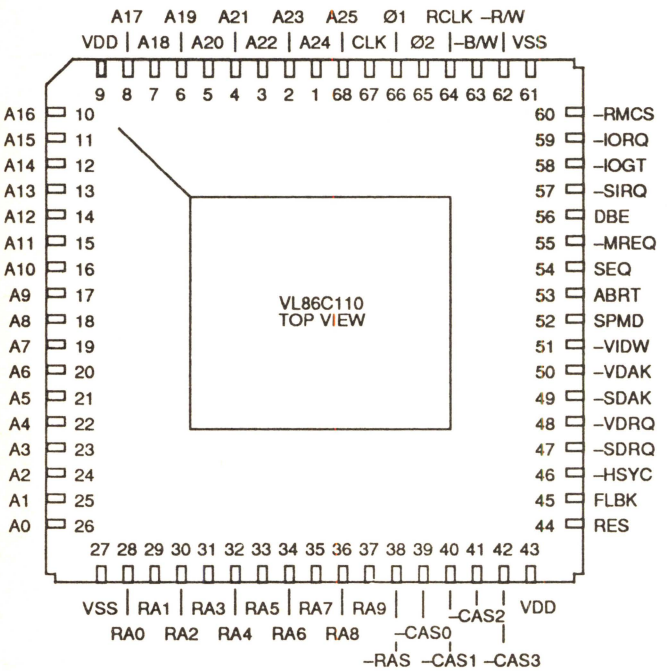
Address translation is performed by a simple 128 entry content-addressable memory (CAM). MEMC provides a descriptor entry for every page of physical memory which eliminates descriptor thrashing (address translation misses) from degrading system performance.

The simple structure allows memory address translation to be performed without increasing required memory access time or decreasing the system clock. MEMC allows virtual memory and multi-tasking operations to be implemented without the usual performance degradation associated with each function. Fast page mode DRAM accesses are used to maximize memory bandwidth from inexpensive commodity memory devices.

MEMC supports direct memory access (DMA) read operations with three programmable address generators. Video refresh is performed using a circular buffer to enhance scrolling capability plus a separate linear buffer for a cursor sprite. Sound data uses a double buffering system.

### PIN DIAGRAM

**JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER**




### ORDER INFORMATION

| Part Number | Clock Frequency | Package |
|---|---|---|
| VL86C110-10QC | 10 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL86C110-10LC | | JEDEC Type-B Ceramic Carrier |
| VL86C110-12QC | 12 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL86C110-12LC | | JEDEC Type-B Ceramic Carrier |

**Note:** Operating temperature range is 0°C to + 70°C.

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# VL86C310

## RISC VIDEO CONTROLLER (VIDC)

### FEATURES

- Pixel rate selectable as 8, 12, 16, or 24 MHz
- Serializes data to 1-, 2-, 4-, or 8- bits per pixel
- 16 x 13 bit words - 4096 color lookup palette
- Three 4-bit DACs (one for each CRT gun)
- Fully programmable screen parameters
- Screen border in any of the 4096 possible colors
- Flexible cursor sprite
- Support for interlaced display format
- External synchronization capability
- Very high resolution monochrome mode support
- High quality stereo sound generation

### DESCRIPTION

The Video Controller (VIDC) accepts video data from DRAM under DMA control, serializes and passes it through a color look-up palette, and converts it to analog signals for driving the CRT guns. The chip also controls all the display timing parameters plus the position and pattern of the cursor sprite. In addition, the VIDC includes an exponential DAC and stereo image table for the generation of high quality sound from data in the DRAM.

The VIDC requests data from the RAM when required, and buffers it in one of three first-in, first-out memories (FIFOs). Note that the addressing of the data in RAM is controlled elsewhere in the system (usually in the VL86C110 Memory Controller, MEMC). Data is requested in blocks of four 32-bit words, allowing efficient use of page-mode DRAM without locking up the system data bus for long periods.

The VIDC is a highly programmable device, offering a very wide choice of display formats. The pixel rate can be selected in a range between 8 and 24 MHz and the data can be serialized to either 8-, 4-, 2-, or 1-bit per pixel. The horizontal timing parameters can be controlled to units of two pixels, and the vertical timing parameters can be controlled in units of a raster. The color lookup palette which drives the three on-chip DACs is 13 bits wide, offering a choice from 4096 colors or an external video source.

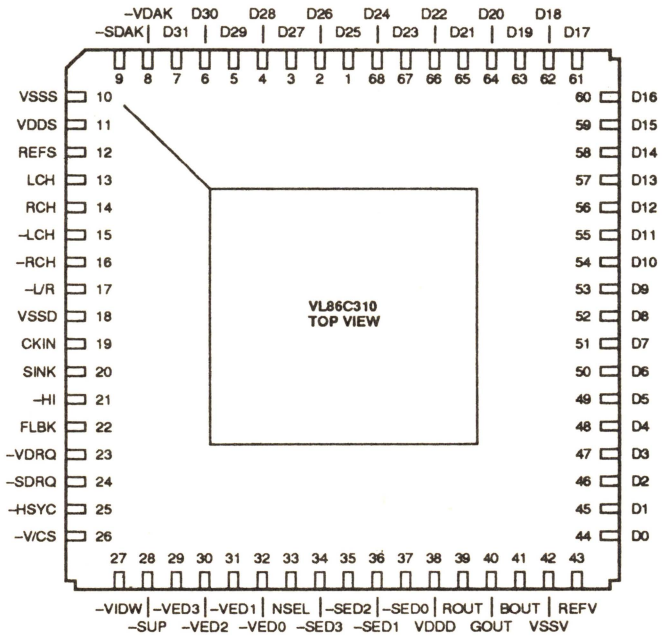
Extensive use is made of pipelining throughout the device.

The cursor sprite is 32 pixels wide, and any number of rasters high. Three simultaneous colors (from the 4096 possible) are supported, and any pixel can be defined as transparent, making possible cursors of many shapes. The cursor can be positioned anywhere on the screen.

The sound system implemented on the device can support up to eight channels, each with a separate stereo position.

### PIN DIAGRAM

**JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER**




### ORDER INFORMATION

| Part Number | Clock Frequency | Package |
|---|---|---|
| VL86C310-10QC | 10 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL86C310-10LC | | JEDEC Type-B Ceramic Carrier |
| VL86C310-12QC | 12 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL86C310-12LC | | JEDEC Type-B Ceramic Carrier |

**Note:** Operating temperature is 0°C to +70°C.

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# VL86C410

## RISC I/O CONTROLLER (IOC)

### FEATURES

- Power on reset control
- Four independent 16-bit programmable counters
  –Two timers
  –Two baud rate generators
- Bidirectional serial keyboard interface
- Six programmable bidirectional control pins
- Interrupt mask, request and status registers for –IRQ and –FIRQ
- 14 level triggered interrupt inputs
- Two edge triggered interrupt inputs
- Four programmable peripheral cycles
  – Slow
  – Medium
  – Fast
  – 2 MHz synchronous
- Seven external peripheral selects
- ARM/IO bus interface control
- Expansion bus buffer control

### DESCRIPTION

The VL86C410 Input/Output Controller (IOC) is designed to interface to the VL86C010/VL86C110/VL86C310 chip set to provide a unified view of interrupts and peripherals within an Acorn RISC Machine (ARM) based computer. It controls an 8-to-32 bit I/O data bus to which on-board peripherals and any I/O expansions are connected. It provides a set of internal functions, which are accessed without wait states, and programmable speed access to external peripherals.

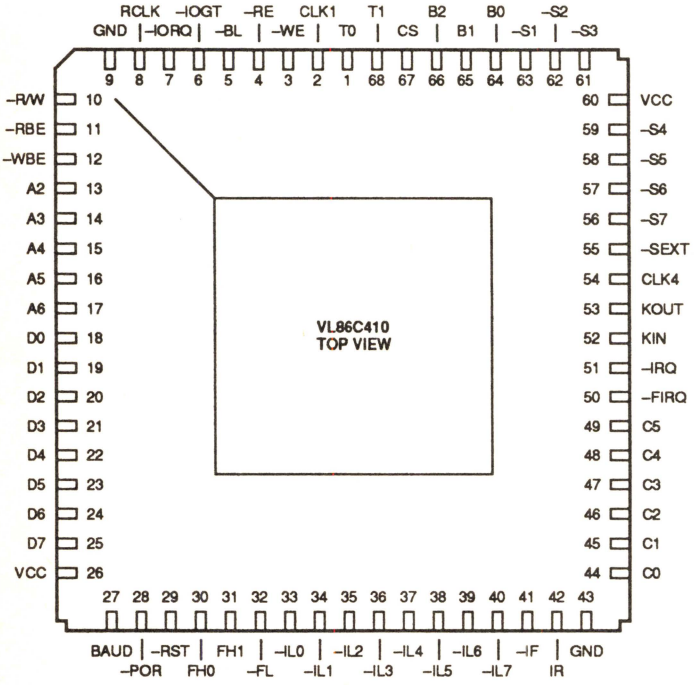
The VL86C410 provides system level I/O with six programmable control pins and a full-duplex, bidirectional serial keyboard interface. To support system timing requirements, the VL86C410 contains four independent programmable counters. Two of these counters are used as baud rate generators. One is dedicated to the keyboard and the other controls the BAUD output pin to generate a free-running clock. The other two counters can be used to generate system timing events.

The IOC serves as the interface between the very high-speed RISC system bus and the slower I/O or expansion bus. The part provides all the buffer control required between the two buses. The VL86C410 supports an interruptable I/O cycle thats allows the system to use slower, low-cost peripheral controllers such as the VL16C450 Asynchronous Communications Element and VL1772 Floppy Disk Controller without severe latency on the system bus.

Peripheral controllers are supported with 16 interrupt inputs (14 level sensitive and two edge-triggered), seven peripheral select outputs, and four programmable I/O cycle times.

### PIN DIAGRAM

**JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER**




### ORDER INFORMATION

| Part Number | Clock Frequency | Package |
|---|---|---|
| VL86C410-10QC | 10 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL86C410-10LC | | JEDEC Type-B Ceramic Carrier |
| VL86C410-12QC | 12 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL86C410-12LC | | JEDEC Type-B Ceramic Carrier |

**Note:** Operating temperature is 0°C to +70°C.

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# VT20C18 • VT20C19

## 2,048 × 8 SRAM

### FEATURES

- High-speed access and cycle times: 20, 25, and 35 ns
- Fast output enable control
- Fast chip select option (VT20C19)
- Automatic power-down when deselected (VT20C18)
- CMOS process for low power:
  — 600 mW (typical) active
  — 35 mW (typical) standby (VT20C18)
  — 100 $\mu$W (typical) CMOS standby
- Highly reliable six-transistor memory cell
- All pins capable of withstanding electrostatic discharge greater than 2,000 V
- 300-mil, 24-pin dual in-line, SOIC and SOJ packages

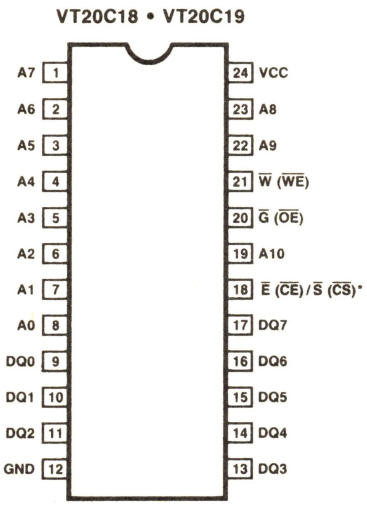
### DESCRIPTION

The VT20C18 and VT20C19 are high-speed static RAMs (SRAMs) that are organized as 2,048 words by 8 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power, making them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

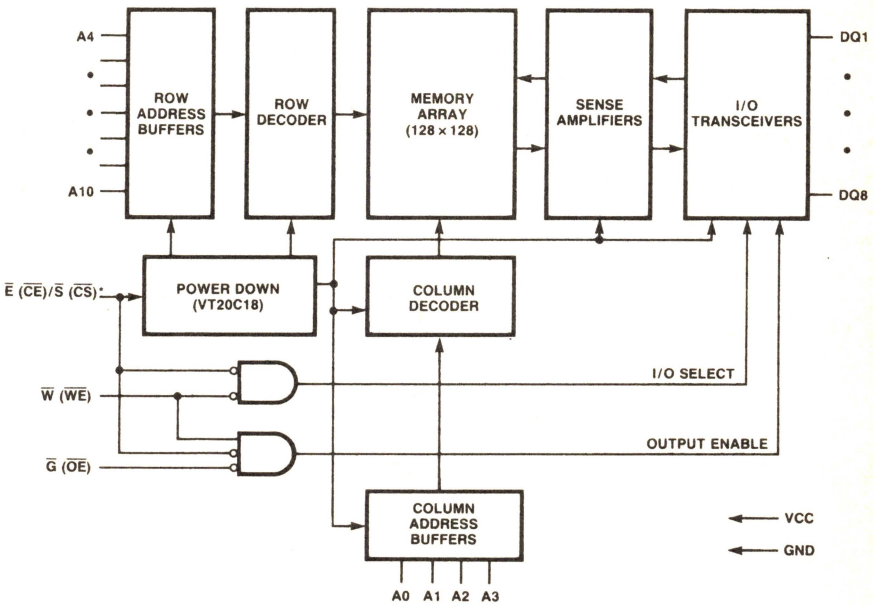
The VT20C18, with automatic power-down, offers standby current of only 7 mA (typical) when deselected. The VT20C19 offers a fast chip select option that provides data access in only 10 ns.

For easy memory expansion, both devices have active-LOW chip enable ($\overline{E}$), output enable ($\overline{G}$) and write enable ($\overline{W}$) signals, as well as three-state outputs. The VT20C18 and VT20C19 are packaged in 300-mil DIPs with industry-standard pinouts, but offer higher speeds for increased system performance.

### PIN DIAGRAM




### BLOCK DIAGRAM




### PIN NAMES

| | |
|---|---|
| A0–A10 | Address Inputs |
| DQ0–DQ7 | Data Inputs/Outputs |
| $\overline{E}$ ($\overline{CE}$)/$\overline{S}$ ($\overline{CS}$)* | Chip Enable/Chip Select* |
| $\overline{W}$ ($\overline{WE}$) | Write Enable |
| $\overline{G}$ ($\overline{OE}$) | Output Enable |
| VCC | Power (5 V) |
| GND | Ground (0 V) |

*VT20C19 only.

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PRELIMINARY **VT20C50**

# 1K x 4 CLEARABLE SRAM

## FEATURES

- High speed: 15 ns maximum access time
- 1K x 4 organization
- Memory reset (clear) function
- Separate data input/output
- Three-state output buffers
- High-reliability six-transistor memory cell
- Capable of withstanding greater than 2,000 V ESD
- Single 5 V ± 10% power supply
- 300-mil, 24-pin plastic dual in-line package
- 24-pin SOIC and SOJ packages

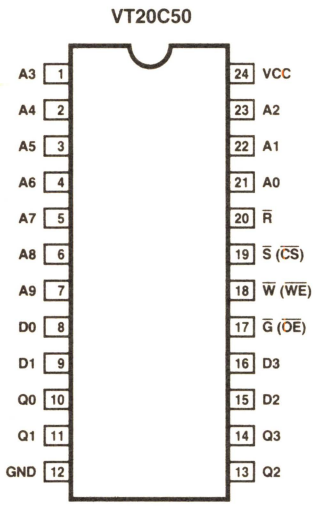
## DESCRIPTION

The VT20C50 Clearable SRAM is a high-performance static RAM with a 1,024 x 4 organization. It offers TTL-compatible input and output levels, and features separate input and output pins that enhance system performance and adaptability.

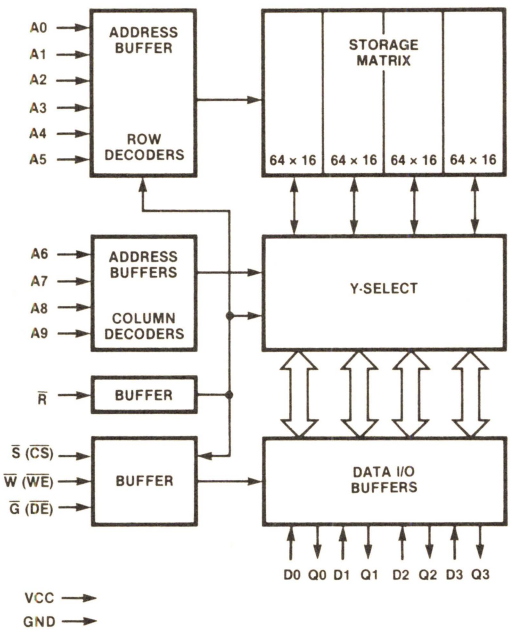
The contents of the VT20C50 can be cleared (all memory cells set to logic 0) within two cycles. To accomplish this, the user regulates the Reset ($\overline{R}$), Chip Select ($\overline{S}$) and Write Enable ($\overline{W}$) inputs.

The VT20C50 features 15 ns access time and a maximum operating current of only 100 mA. It is fabricated using VLSI Technology's CMOS process, and is available in a 24-pin 300-mil ceramic DIP, as well as 24-pin SOIC and SOJ packages.

## PIN DIAGRAM




## BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| A0 - A9 | Address Inputs |
| D0 - D3 | Data Input |
| Q0 - Q3 | Data Output |
| $\overline{S}$ ($\overline{CS}$) | Chip Select |
| $\overline{G}$ ($\overline{OE}$) | Output Enable |
| $\overline{W}$ ($\overline{WE}$) | Write Enable |
| $\overline{R}$ | Reset |
| VCC | Power (5 V) |
| GND | Ground (0 V) |

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# VT20C68 • VT20C69

## 4,096 × 4 SRAM

### FEATURES

- High-speed access and cycle times: 20, 25, and 35 ns
- Fast chip select option (VT20C69)
- Automatic power-down when deselected (VT20C68)
- CMOS process for low power:
  — 600 mW (typical) active
  — 35 mW (typical) standby (VT20C68)
  — 100 $\mu$W (typical) CMOS standby
- Highly reliable six-transistor memory cell
- Capable of withstanding electrostatic discharge greater than 2,000 V
- 300-mil, 20-pin dual in-line, 24-pin SOIC and SOJ packages
- Pin-compatible with standard 4K × 4 SRAMs

### DESCRIPTION

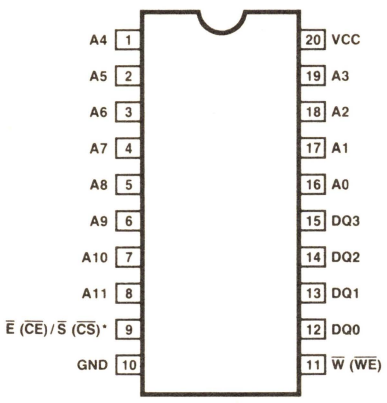
The VT20C68 and VT20C69 are high-speed static RAMs (SRAMs) that are organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power. This makes them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

The VT20C68, with automatic power-down, offers standby current of only 7 mA (typical) when deselected. The VT20C69 offers a fast chip select option that provides data access in only 10 ns.

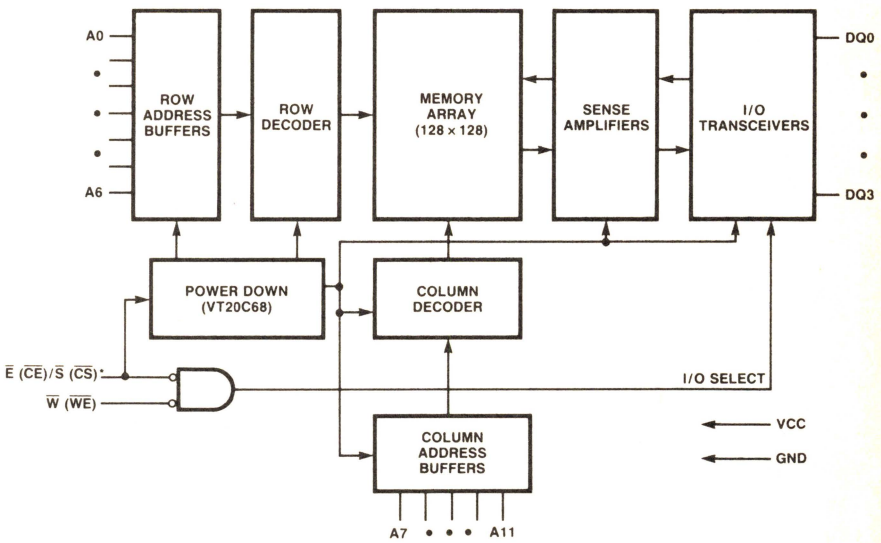
For easy memory expansion, both devices have active-LOW chip enable ($\overline{E}$) and write enable ($\overline{W}$) signals as well as three-state outputs. The VT20C68 and VT20C69 are packaged in 300-mil DIPs with industry-standard pinouts that are compatible with other static RAMs, but offer higher speeds for increased system performance.

### PIN DIAGRAM

VT20C68 • VT20C69




### BLOCK DIAGRAM




### PIN NAMES

| | |
|---|---|
| A0–A11 | Address Inputs |
| DQ0–DQ3 | Data Inputs/Outputs |
| $\overline{E}$ ($\overline{CE}$) /$\overline{S}$ ($\overline{CS}$)* | Chip Enable/Chip Select* |
| $\overline{W}$ ($\overline{WE}$) | Write Enable |
| VCC | Power (5 V) |
| GND | Ground (0 V) |

*VT20C69 only.



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PRELIMINARY **VT20C71 • VT20C72**

## 4,096 × 4 SEPARATE I/O SRAM

### FEATURES

- High-speed access and cycle times: 20, 25, 35 ns
- Automatic power-down at deselect
- Pin-compatible with standard 4K × 4 separate I/O SRAMs
- Low-power CMOS process: 600 mW active (typical) 35 mW standby (typical)
- High-reliability six-transistor memory cell
- Capable of withstanding greater than 2000 V ESD
- 300-mil, 24-pin ceramic and plastic dual in-line packages
- 24-pin SOIC and SOJ packages

### DESCRIPTION

The VT20C71 and VT20C72 are high-speed static RAMs organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability as well as low power, making them suitable for use in high-performance cache memory, writeable control store, and high-speed data buffer applications.

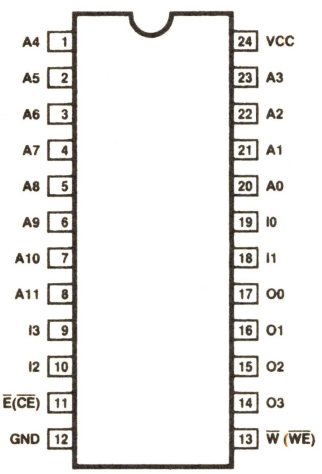
The VT20C71 and VT20C72 feature an automatic power-down that offers a standby current of only 7 mA (typical) when deselected.

For easy memory expansion, both devices have active-LOW Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) signals, as well as three-state outputs. The outputs may be placed in the high-impedance state with the Write Enable signal LOW (VT20C72 only) or with the Chip Enable HIGH.

The VT20C71 and VT20C72 are packaged in 300-mil dual in-line packages with industry-standard pinouts, and in 24-pin small-outline packages. They are compatible with other static RAMs, yet offer higher speeds for increased system performance.

### PIN DIAGRAM

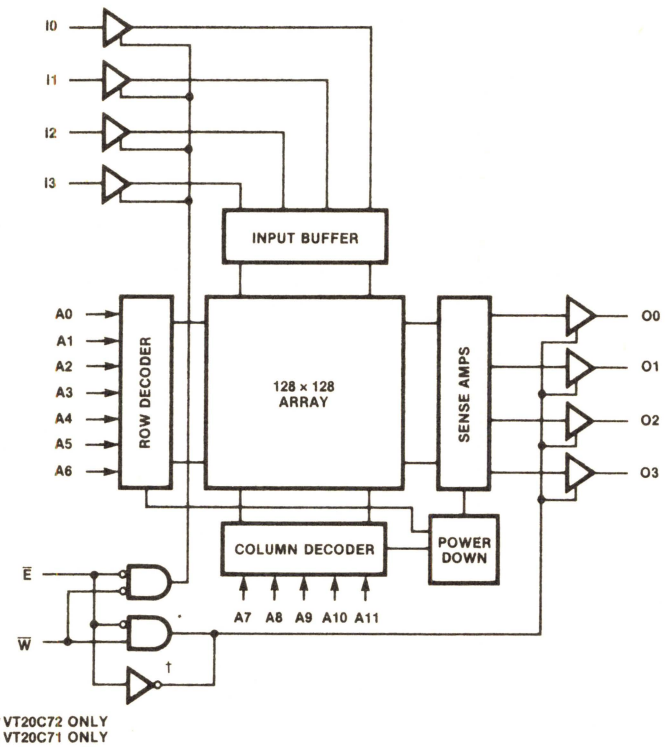
VT20C71 • VT20C72




### PIN NAMES

| | |
|---|---|
| A0 – A11 | Address Inputs |
| I0 – I3 | Data Input |
| O0 – O3 | Data Output |
| E ($\overline{CE}$) | Chip Enable |
| W ($\overline{WE}$) | Write Enable |
| VCC | Power (5 V) |
| GND | Ground (0 V) |

### BLOCK DIAGRAM




*VT20C72 ONLY
† VT20C71 ONLY

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# VT20C78 • VT20C79

## 4,096 × 4 SRAM

### FEATURES

- High-speed access and cycle times: 20, 25, and 35 ns
- Fast output enable control
- Fast chip select option (VT20C79)
- Automatic power-down when deselected (VT20C78)
- CMOS process for low power:
  — 600 mW (typical) active
  — 35 mW (typical) standby (VT20C78)
  — 100 $\mu$W (typical) CMOS standby
- Highly reliable six-transistor memory cell
- Capable of withstanding electrostatic discharge greater than 2,000 V
- 300-mil, 22-pin dual in-line, 24-pin SOIC and SOJ packages
- Pin-compatible with standard 4K × 4 SRAMs

### DESCRIPTION

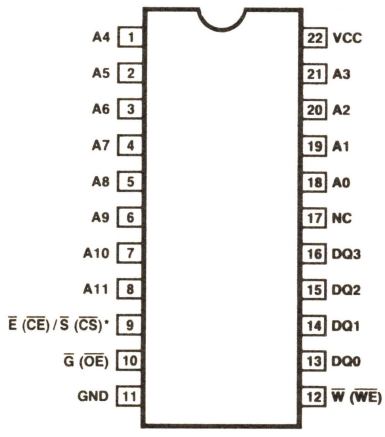
The VT20C78 and VT20C79 are high-speed static RAMs (SRAMs) that are organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power. This makes them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

The VT20C78, with automatic power-down, offers standby current of only 7 mA (typical) when deselected. The VT20C79 offers a fast chip select option that provides data access in only 10 ns.

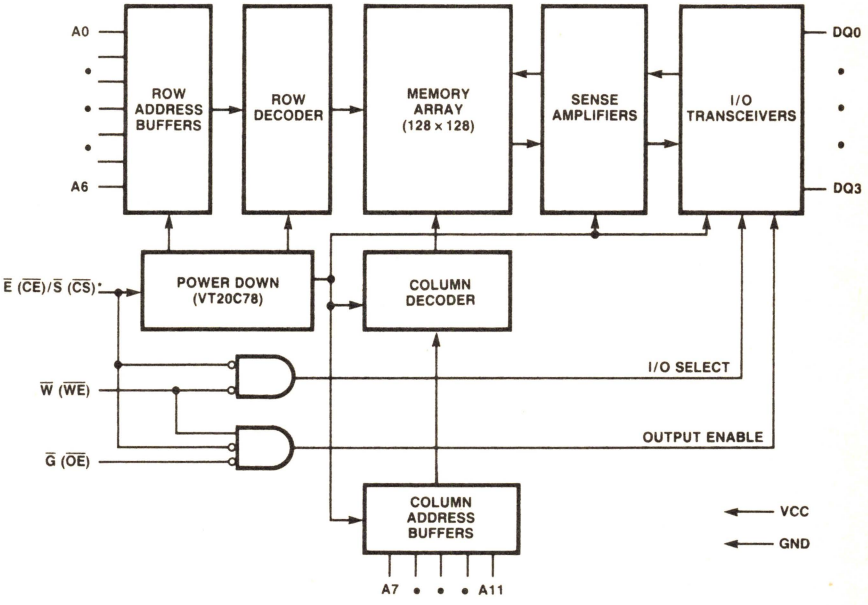
For easy memory expansion, both devices have active-LOW chip enable ($\overline{E}$), output enable ($\overline{G}$), and write enable ($\overline{W}$) signals, as well as three-state outputs. The VT20C78 and VT20C79 are packaged in 300-mil DIPs with industry-standard pinouts that are compatible with other static RAMs, but offer higher speeds for increased system performance.

### PIN DIAGRAM

VT20C78 • VT20C79




### BLOCK DIAGRAM




### PIN NAMES

| | |
|---|---|
| A0–A11 | Address Inputs |
| DQ0–DQ3 | Data Inputs/Outputs |
| $\overline{E}$ ($\overline{CE}$)/$\overline{S}$ ($\overline{CS}$)* | Chip Enable/Chip Select* |
| $\overline{W}$ ($\overline{WE}$) | Write Enable |
| $\overline{G}$ ($\overline{OE}$) | Output Enable |
| VCC | Power (5 V) |
| GND | Ground (0 V) |

*VT20C79 only.

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PRELIMINARY **VT20C98 • VT20C99**

**8,192 x 8 SRAM**

## FEATURES

- High speed access and cycle times: 25, 30 and 35 ns
- Fast chip select option: 15, 20 and 25 ns (VT20C99)
- Automatic power-down when not enabled (VT20C98)
- Highly reliable six-transistor memory cell
- Capable of withstanding electrostatic discharge greater than 2,000 V
- 300-mil, 28-pin dual in-line package
- Pin-compatible with standard 8K x 8 SRAMs

## DESCRIPTION

The VT20C98 and VT20C99 are high-speed static RAMs (SRAMs) that are organized as 8,192 words by 8 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power. This makes them suitable for use in high-performance cache memory, writable control store and high-speed data buffer applications.

The VT20C98, with automatic power-down, offers standby current of only 20 $\mu$A typical when not enabled. The VT20C99 offers a fast chip select option that provides data access in only 15 ns.

For easy memory expansion, both devices have active-HIGH chip enable (E2), active-LOW chip enable ($\overline{E1}$), output enable ($\overline{G}$), and write enable ($\overline{W}$) signals, as well as three-state outputs. Both of the two chip enable inputs ($\overline{E1}$ and E2) must be used to activate the SRAM.

The VT20C98 and VT20C99 are packaged in 300-mil DIPs with industry-standard pinouts that are compatible with other static RAMs, but offer higher speeds for increased system performance.

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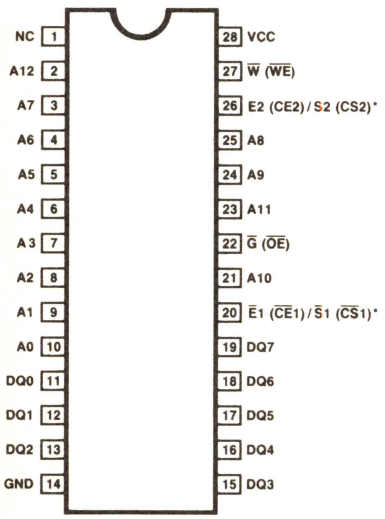
## PIN DIAGRAM

VT20C98 • VT20C99

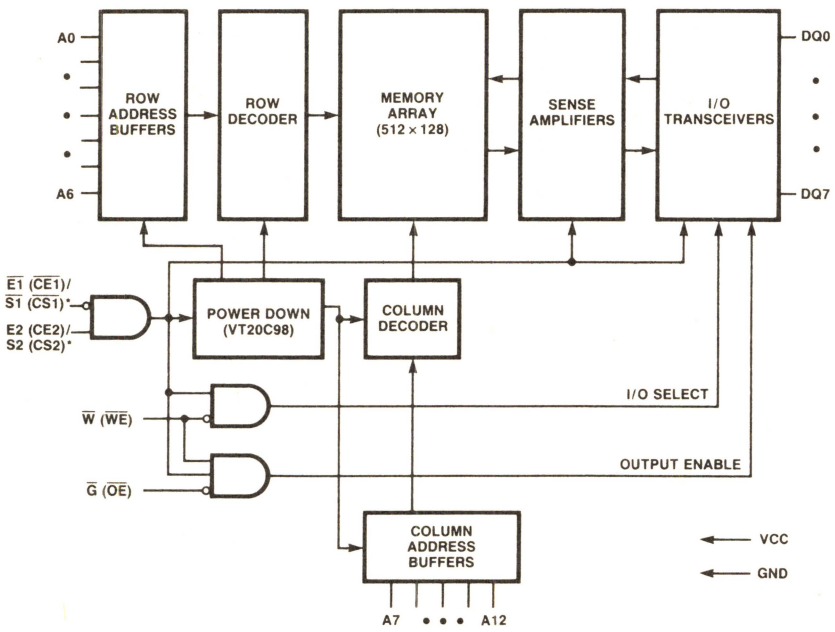



## PIN NAMES

| | |
|---|---|
| A0–A12 | Address Inputs |
| DQ0–DQ7 | Data Inputs/Outputs |
| $\overline{E1}$ ($\overline{CE1}$)/$\overline{S1}$ ($\overline{CS1}$)*<br>E2 (CE2)/S2 (CS2)* | Chip Enable/<br>Chip Select* |
| $\overline{W}$ ($\overline{WE}$) | Write Enable |
| $\overline{G}$ ($\overline{OE}$) | Output Enable |
| VCC | Power (5 V) |
| GND | Ground (0 V) |

*VT20C99 only.

## BLOCK DIAGRAM

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# VT7C122

## 256 × 4 STATIC RAM

### FEATURES

- High-speed access and cycle times: 15 ns
- CMOS process for low power: 330 mW (typical)
- Separate, TTL-compatible inputs and outputs
- All pins capable of withstanding electrostatic discharge greater than 2000 V.
- Industry-standard 22-pin dual in-line package
- 24-pin SOIC and SOJ packages

### DESCRIPTION

The VT7C122 is a high-speed static RAM (SRAM) that is organized as 256 words by 4 bits. If offers very high performance and reliability, as well as low power, making it ideally suited for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

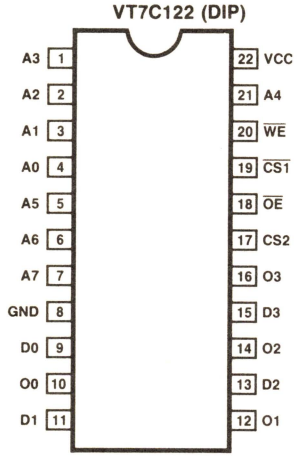
For easy memory expansion, the VT7C122 has an active-LOW chip select one ($\overline{CS1}$) input, an active-HIGH chip select two (CS2) input, and three-state outputs.

The read and write operations of the VT7C122 are controlled by an active-LOW write enable ($\overline{WE}$) input. When $\overline{WE}$ and chip select 1 ($\overline{CS1}$) are LOW and the chip select two (CS2) input is HIGH, information on the data input lines (D0 through D3) is written into the memory word addressed by the A0 through A7 inputs. Simultaneously, the output circuitry is preconditioned so that the correct data is available at the non-inverting output lines (O0 through O3) when the write cycle is complete. Preconditioning minimizes write recovery time by eliminating the "write recovery glitch."

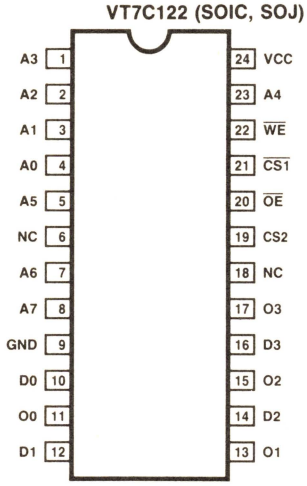
To read data from the VT7C122, the $\overline{CS1}$ and output enable ($\overline{OE}$) inputs must be LOW while CS2 and $\overline{WE}$ are HIGH. The data stored in the addressed memory word is then read out on O0 through O3.

### PIN DIAGRAMS

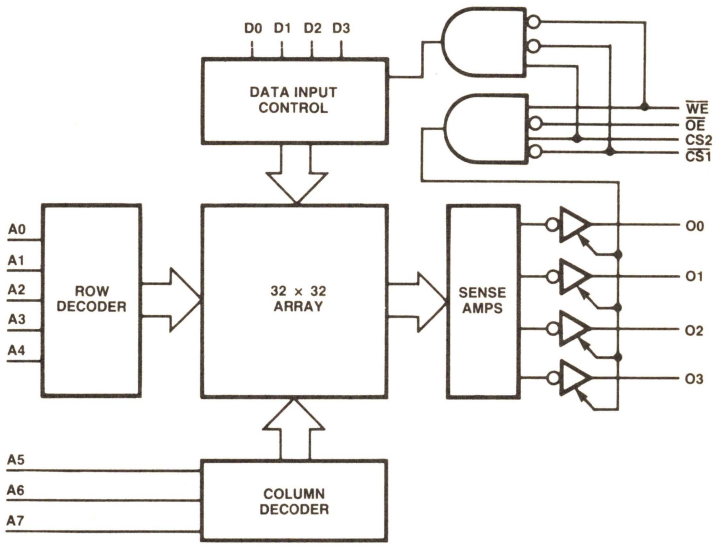
VT7C122 (DIP)




VT7C122 (SOIC, SOJ)




### BLOCK DIAGRAM




### PIN NAMES

| | |
|---|---|
| A0–A7 | Address Inputs |
| $\overline{CS1}$ | Chip Select 1 |
| CS2 | Chip Select 2 |
| D0–D3 | Data Inputs |
| GND | Ground (0 V) |
| O0–O3 | Data Outputs |
| $\overline{OE}$ | Output Enable |
| VCC | Power (5 V) |
| $\overline{WE}$ | Write Enable |

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PRELIMINARY **VT16AM8**

# 1K x 16, 2K x 8 DUAL-PORT RAM

## FEATURES

- Organization
  - — Left Port: 1,024 x 16
  - — Right Port: 2,048 x 8
- High speed:
  - — 60 ns access
- Address/data 8-bit bus
- Fully static operation
- Full contention arbitration
- Simple microprocessor interface
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Low power:
  - — 70 mA (max) operating
- 68-pin PLCC

## DESCRIPTION

The VT16AM8 is a 16,384-bit dual-port static random access memory. Its left port is organized as 1,024 16-bit words and its right port as 2,048 8-bit words. The right port has been organized with an address/data multiplexed bus to allow easy interfacing with most of the standard processors. It is designed to facilitate the transfer of data between 16- and 8-bit microprocessors.

The VT16AM8 features two separate I/O ports that each allow independent access to read or write to any location in the memory. The memory is designed to permit read and/or write operations to be performed at both the 16-bit and the 8-bit port at the same time. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location. Two modes of operation are provided on the 16-bit side. One mode allows contention to be ignored and both operations to proceed. In the other mode, the on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the 16-bit port takes priority.

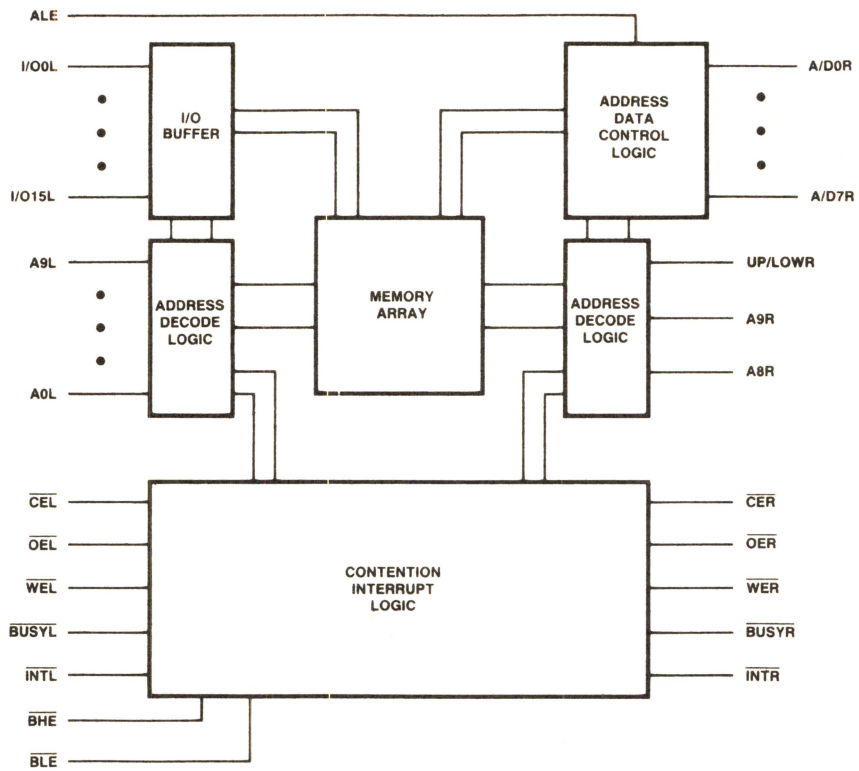
On the 8-bit side, the contention ignore mode is not available.

The 16-bit port is designed to allow easy interface to all 16-bit microprocessors by the inclusion of the ability to read and write in either a word or a byte mode. The $\overline{BHE}$ and $\overline{BLE}$ control lines enable the upper byte or the lower byte, respectively. When both control lines are active, the word mode is invoked.

Busy flags are open-drain for simple wired-OR operation.

Automatic power-down for each port is controlled independently by the chip enable inputs.

## BLOCK DIAGRAM

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PRELIMINARY **VT16DP8**

# 1K × 16, 2K × 8 DUAL PORT RAM

## FEATURES

- Organization:
  — Left port: 1,024 × 16
  — Right port: 2,048 × 8
- High speed:
  — 60 ns access (max)
- Fully static operation
- Full contention arbitration
- Simple microprocessor interface
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Two interrupt flags
- Low power:
  — 70 mA (max) operating
- 64-pin DIP or 68-pin PLCC

## DESCRIPTION

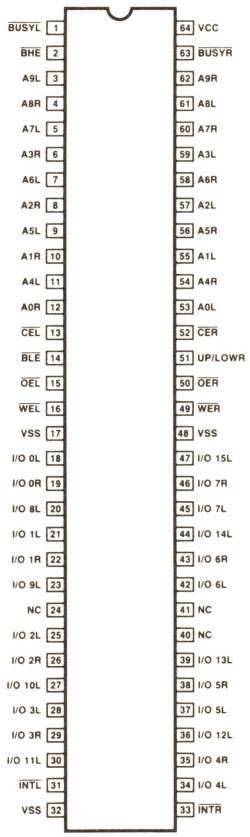
The VT16DP8 is a 16,384-bit dual port static random access memory. Its left port is organized as 1,024 16-bit words and its right port as 2,048 8-bit words. It is designed to facilitate the transfer of data between 16- and 8-bit microprocessors.

The VT16DP8 features two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and/or write from either the 16-bit or the 8-bit port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location. Two modes of operation are provided. One mode allows contention to be ignored and both operations to proceed. In the other mode, the on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the 16-bit port takes priority.

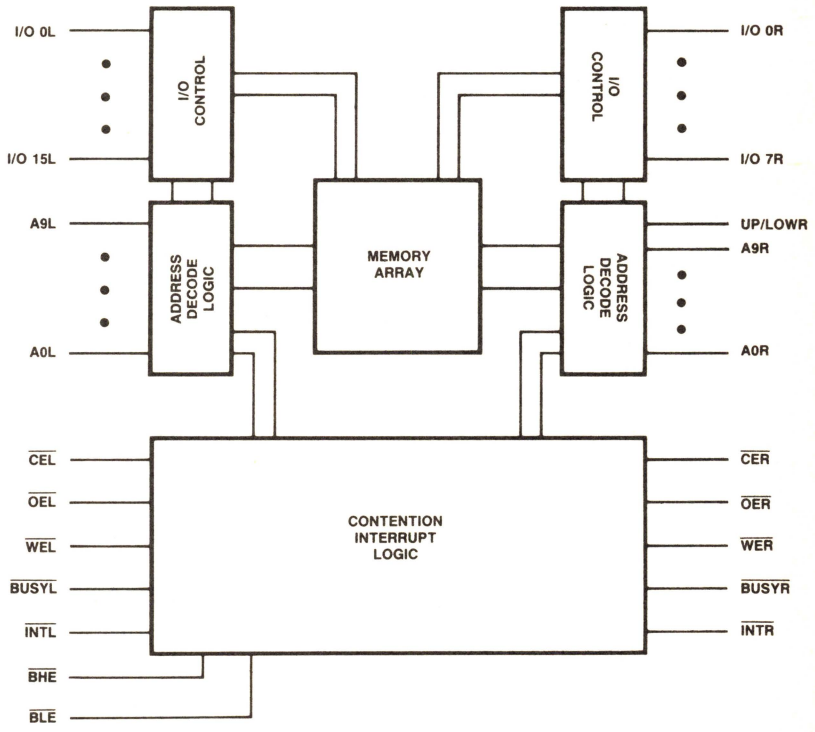
The 16-bit port is designed to allow easy interface to all 16-bit microprocessors by the inclusion of the ability to read and write in either a word or a byte mode. The $\overline{BHE}$ and $\overline{BLE}$ control lines enable the upper byte or the lower byte, respectively. When both lines are active, the VT16DP8 is in word mode.

## PIN DIAGRAM

VT16DP8




## BLOCK DIAGRAM

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PRELIMINARY **VT2KF9**

# 2K x 9 FIFO MEMORY

## FEATURES

- First-in, first-out dual-port memory
- Low-power 2.0-micron CMOS process
- Fully asynchronous operation
- Simultaneous read and write
- Fully expandable in depth and width
- Access time: 50 ns
- Dependable empty, half-full, and full warning flags
- Rate buffer applications
- Multi-processing master/slave applications
- 28-pin, 600-mil dual in-line package
- 32-pin PLCC package

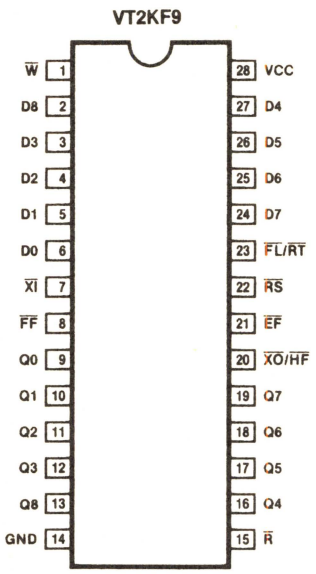
## DESCRIPTION

The VT2KF9 is a first-in, first-out (FIFO) memory that uses a high-performance static RAM array with internal logic to ensure totally asynchronous operation. Full, half-full, and empty flags are provided to allow the device to operate without external logic. The VT2KF9 also contains logic that allows for unlimited expansion in both word size and depth.

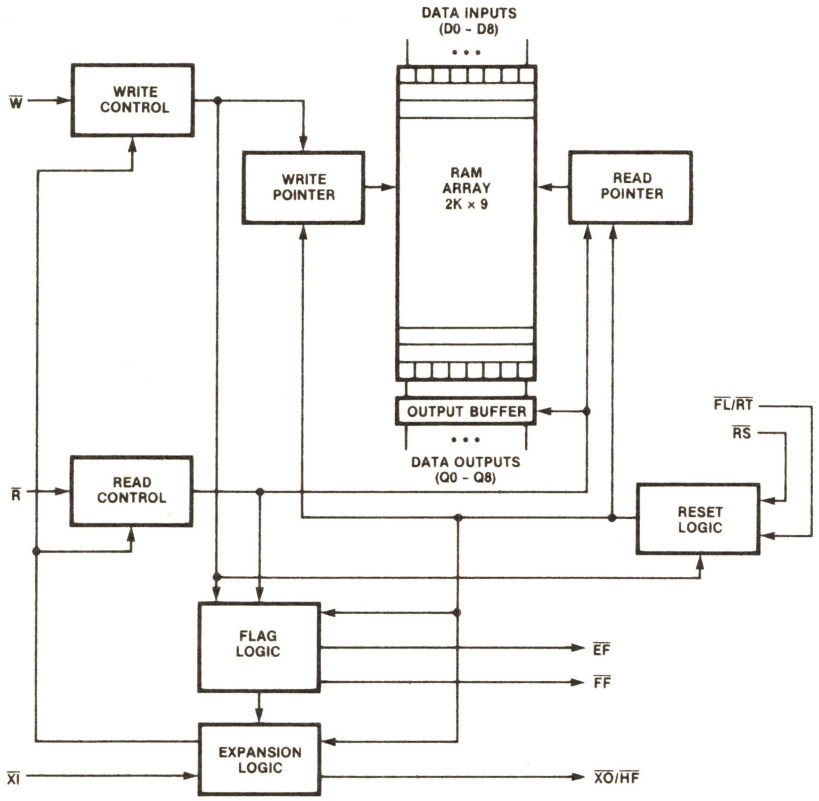
Although the VT2KF9 uses a static RAM array as its memory element, a system of read and write pointers has been included to sequence through the array. Data is toggled in and out of the device by means of the Write Enable ($\overline{W}$) and Read Enable ($\overline{R}$) signals. The VT2KF9 has an access time of 50 ns and a read/write cycle time of 65 ns (15 MHz). Its 2,064 x 9 organization permits the use of control or parity bits at the option of the user, and also allows a 2,064-deep word structure without the need for expansion.

The VT2KF9 is fabricated using VLSI Technology's high-performance 2-micron CMOS process. Its design is ideally suited to asynchronous and simultaneous reading and writing in multi-processing and rate buffer applications. The FIFO is available in both plastic dual in-line and plastic leaded chip carrier packages.

## PIN DIAGRAM




## BLOCK DIAGRAM

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PRELIMINARY **VT2KF91**

# 2K x 9 FIFO MEMORY

## FEATURES

- First-in, first-out dual-port memory
- Low-power 2.0-micron CMOS process
- Fully asynchronous operation
- Simultaneous read and write
- Fully expandable in depth and width
- Access time: 50 ns
- Dependable empty and full flags
- Almost-full and almost-empty flags 12 words away from full and empty
- Automatic retransmit capability in single-device mode
- 32-pin PLCC package

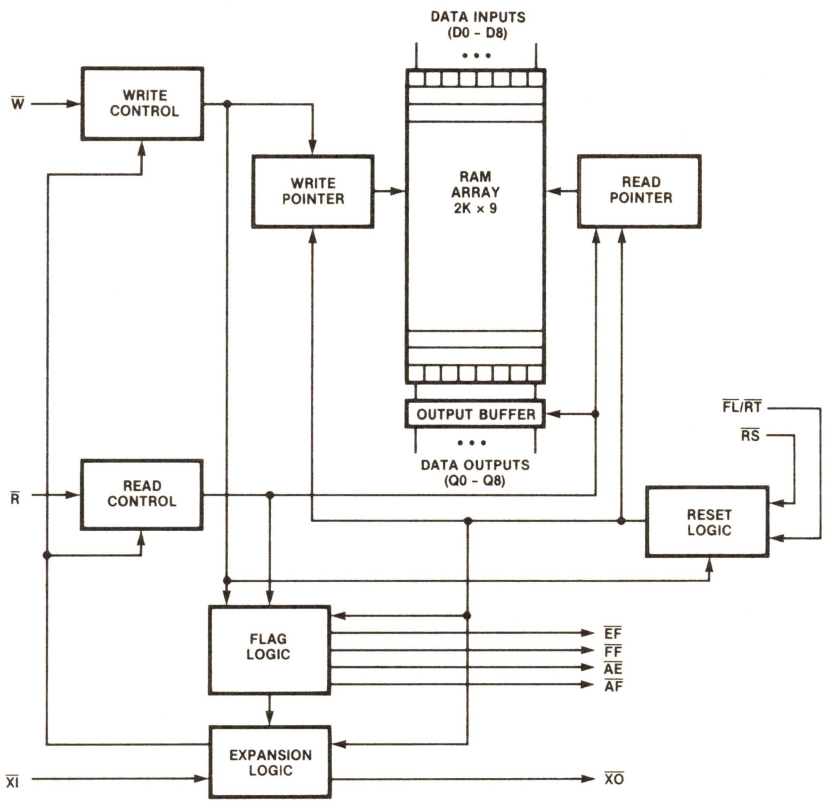
## DESCRIPTION

The VT2KF91 is a first-in, first-out (FIFO) memory that uses a high-performance static RAM array with internal logic to ensure totally asynchronous operation. Full, empty, almost-full, and almost-empty flags are provided to allow the device to operate without external logic. The VT2KF91 also contains logic that allows for unlimited expansion in both word size and depth.

Although the VT2KF91 uses a static RAM array as its memory element, a system of read and write pointers has been included to sequence through the array. Data is toggled in and out of the device by means of the Write Enable ($\overline{W}$) and Read Enable ($\overline{R}$) signals. The VT2KF91 has an access time of 50 ns and a read/write cycle time of 65 ns (15 MHz). Its 2,064 x 9 organization permits the use of control or parity bits at the option of the user, and also allows a 2,064-deep word structure without the need for expansion.

The VT2KF91 is fabricated using VLSI Technology's high-performance 2-micron CMOS process. Its design is ideally suited to asynchronous and simultaneous reading and writing in multi-processing and rate buffer applications.

## BLOCK DIAGRAM



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# VT2130 • VT2131

## 1,024 x 8 DUAL PORT RANDOM ACCESS MEMORY

### FEATURES

- 120 ns address access time
- Fully static operation
- Fully TTL compatible
- Interrupt function ($\overline{INT}$): open drain for OR-tied operation
- Easy microprocessor interface
- VM2130—Transparent power-down ($\overline{CE}$)
- VM2131—Non-power-down ($\overline{CS}$)
- Output Enable function ($\overline{OE}$)
- Both ports operate independently.
- Each port accesses entire memory.
- $\overline{BUSY}$ function to handle contention

### DESCRIPTION

The VT2130 and VT2131 are 8,192-bit Dual Port Static Random Access Memories organized 1,024 words by eight bits. They are designed using fully static circuitry and fabricated using n-channel double-poly silicon gate technology.

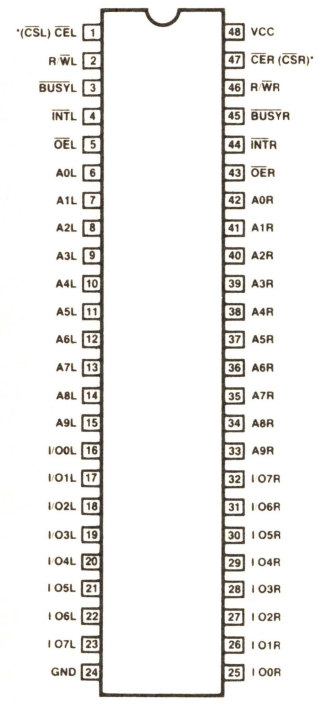
The VT2130 and VT2131 feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The only situation where contention occurs is when both ports are active and both addresses match. Two modes of operation are provided for this situation. In one mode, contention is ignored and both operations are allowed to proceed. In the other mode, on-chip control logic arbitrates delaying one port until the other port's operation is completed. A $\overline{BUSY}$ flag is sent to the side where the operation is delayed. $\overline{BUSY}$ is driven out at speeds that allow the port's processor to preserve its address and data.

An interrupt function ($\overline{INT}$) is provided to allow communication between systems. This function acts like a writable flag. When the flag's location is written from one side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side. The $\overline{INT}$s have open drain drivers to allow OR-tied operation.

The VT 2130 has an automatic power down feature which is controlled by the Chip Enable inputs. Each Chip Enable controls automatic power-down circuitry that allows its respective side of the device to remain in a standby power mode.

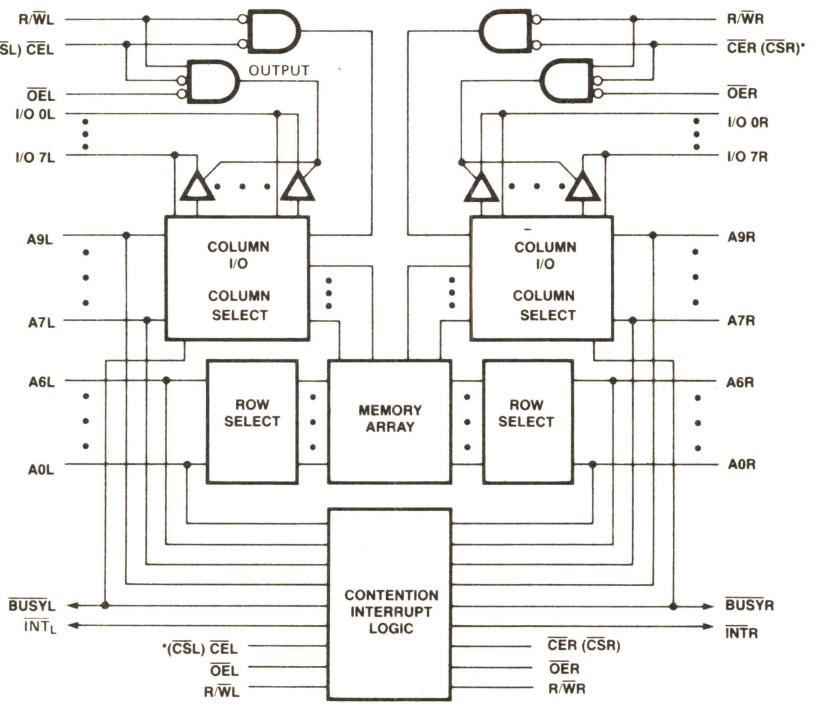
The VT2131 chip select (no power down) access has been designed to be faster than its address access so that the chip select decode time will not add to the memory's overall access time. This feature significantly improves system performance.

### PIN CONFIGURATION




*SYMBOL IN (PARENTHESES) APPLIES TO VT2131

### BLOCK DIAGRAM

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PRELIMINARY **VT7132 • VT7142**

# HIGH-SPEED 2K x 8 CMOS DUAL-PORT RAM

## FEATURES

- High speed:
  — 55, 70, and 90 ns access
- Fully static operation
- Full contention arbitration (VT7132)
- VT7142 slave for bus expansion
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Low power: 150 mA (max) operating
- 48-pin DIP or 52-pin PLCC

## DESCRIPTION

The VT7132 and VT7142 are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The VT7132 is designed to be used as a stand-alone "master" dual-port RAM with the VT7142 "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

The VT7132/VT7142 feature two separate I/O ports that each allow independent access to read or write to any location in the memory. The memory is designed to permit read and/or write operations to be performed at both ports at the same time. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

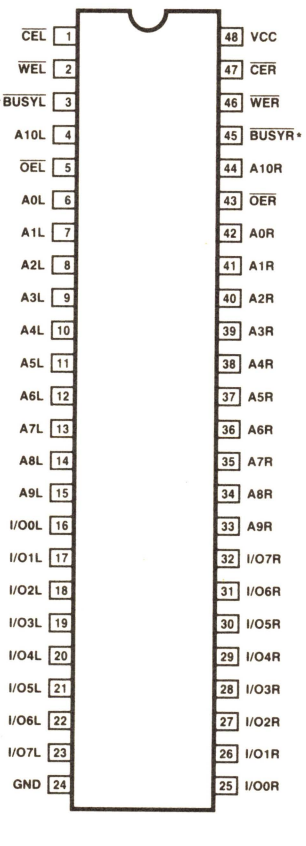
The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request access at exactly the same time, the left port takes priority.

Automatic power down for each port is controlled independently by its Chip Enable input.

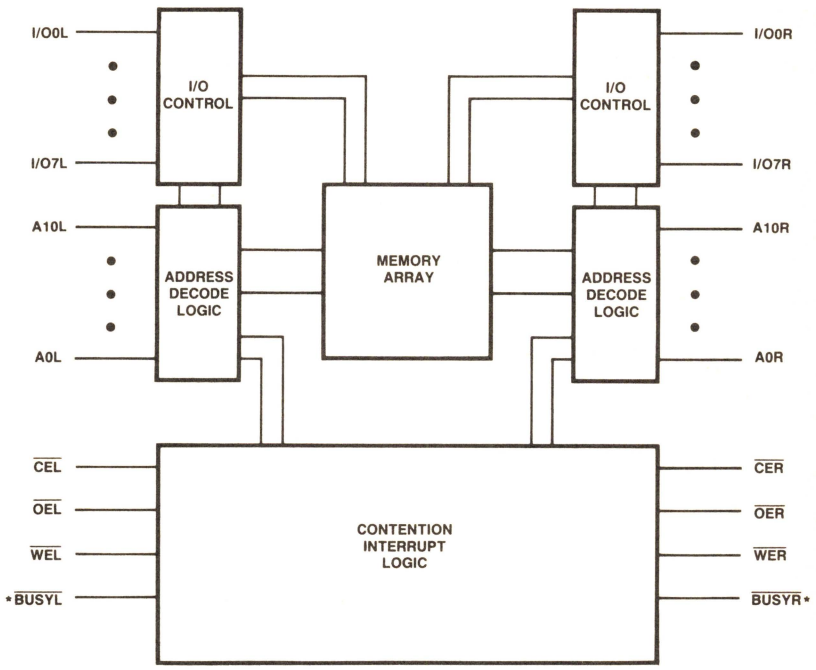
Interfacing to the VT7132/VT7142 is further simplified by the incorporation of an Output Enable control for each port.

## PIN DIAGRAM

VT7132/VT7142




## BLOCK DIAGRAM




* OPEN-DRAIN OUTPUTS FOR VT7132. INPUTS FOR VT7142.

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PRELIMINARY **VT7132A • VT7142A**

# HIGH-SPEED 2K x 8 CMOS DUAL-PORT RAM

## FEATURES

- High speed:
  — 30, 35, and 45 ns access
- Fully static operation
- Full contention arbitration
- VT7142A slave for bus expansion
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Dual interrupt flags in PLCC
- Low power: 150 mA (max) operating
- 48-pin DIP or 52-pin PLCC

## DESCRIPTION

The VT7132A and VT7142A are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The VT7132A is designed to be used as a stand-"master" dual-port RAM with the VT7142A "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

The VT7132A/VT7142A feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to permit read and/or write operations to be performed at both ports at the same time. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the left port takes priority.

When used in the 52-pin PLCC package, a dual-level interrupt function is available. The interrupt function acts like writable flags and is provided to allow communication between systems. When the flag's location is written from one side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side.

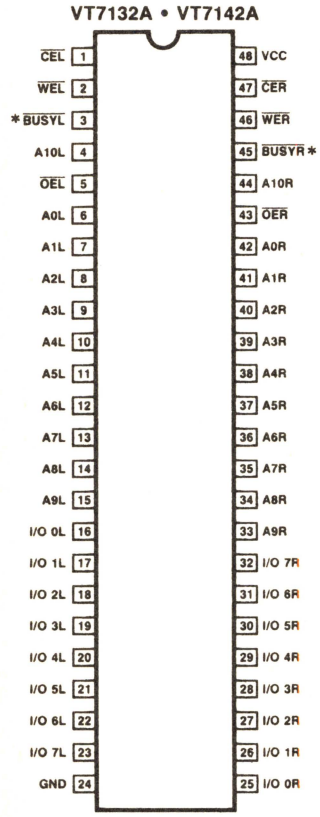
One flag is set during a write operation to any location and the other flag is set during a write to location 7FF/7FE.

Both Interrupt and Busy flags are open drain for simple wired OR operation.

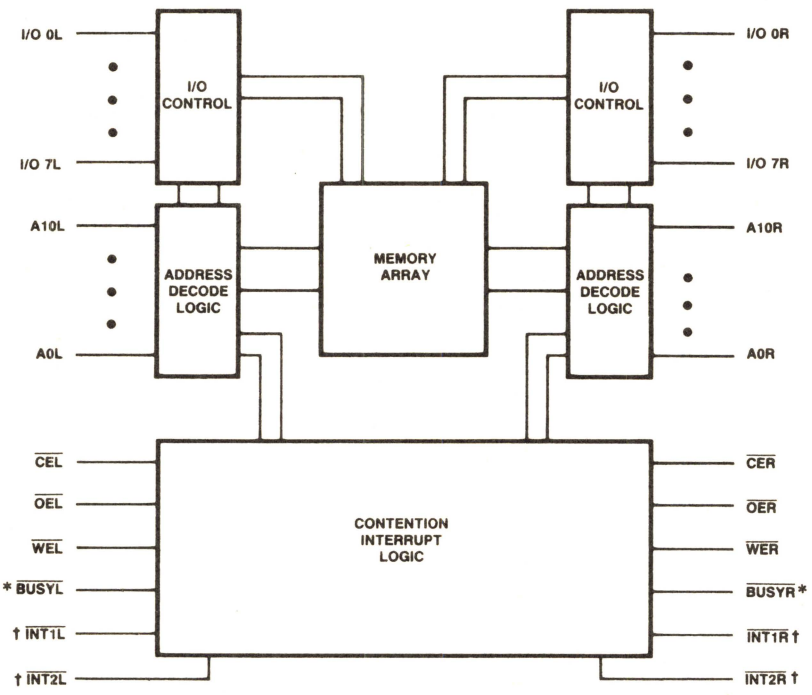
Automatic power down for each port is controlled independently by its Chip Enable input.

Interfacing to the VT7132A/VT7142A is further simplified by the incorporation of an Output Enable control for each port.

## PIN DIAGRAM




## BLOCK DIAGRAM




* OPEN-DRAIN OUTPUTS FOR VT7132A. INPUTS FOR VT7142A.
† AVAILABLE ONLY WITH 52-PIN PLCC.

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PRELIMINARY **VT7150**

# 512 x 8 CACHE TAG RAM

## FEATURES

- Fast address to match valid delay — three speed ranges: 20 ns, 25 ns, 35 ns
- 512 x 9 internal RAM
- On-chip parity generation and checking
- Parity error output/force parity error input
- On-chip address/data comparator
- Asynchronous, single-cycle reset
- Easily expandable
- Fully static
- Reliable CMOS technology
- TTL- and CMOS-compatible inputs and outputs
- 750 mW maximum power dissipation
- 300-mil, 24-pin plastic DIP or small outline (SOIC and SOJ) packages

## DESCRIPTION

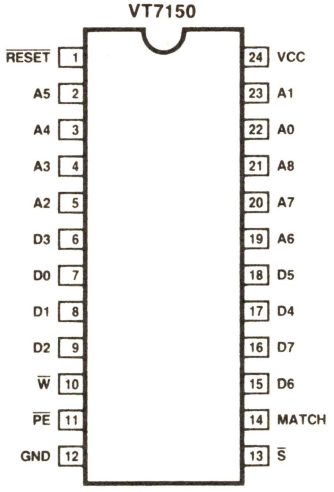
The VT7150 Cache Tag RAM contains a high-speed CMOS static RAM array that uses a full CMOS six-transistor cell for reliable high-speed and low-power operation. Also included on the chip are a parity generator, parity checker, and high-speed 9-bit comparator for comparing input tag data with stored tag data. The device is easily cascadable for wider addresses or deeper tag memories, and interfaces easily with TTL, MOS, and CMOS circuits.

In a compare cycle, the comparator compares the contents of the currently addressed RAM location, including the stored parity bit, with the data present at the data inputs together with the generated parity bit. When all 9 bits of each word match, the MATCH output is asserted. The parity checker checks the parity of the stored byte being accessed, 8 data bits plus 1 parity bit. A parity error is indicated when the number of 1's in the stored byte plus the stored parity bit add up to an odd number. A parity error on the stored tag data is indicated when $\overline{PE}$ and MATCH are both low. The parity generator generates the parity bit from the 8-bit data word at the data inputs.

In a write cycle, the data at the data inputs, plus the generated parity, is written into the memory location addressed by the address inputs.

When the $\overline{RESET}$ input goes LOW, all RAM bits are cleared to zero, and the MATCH output is forced HIGH.

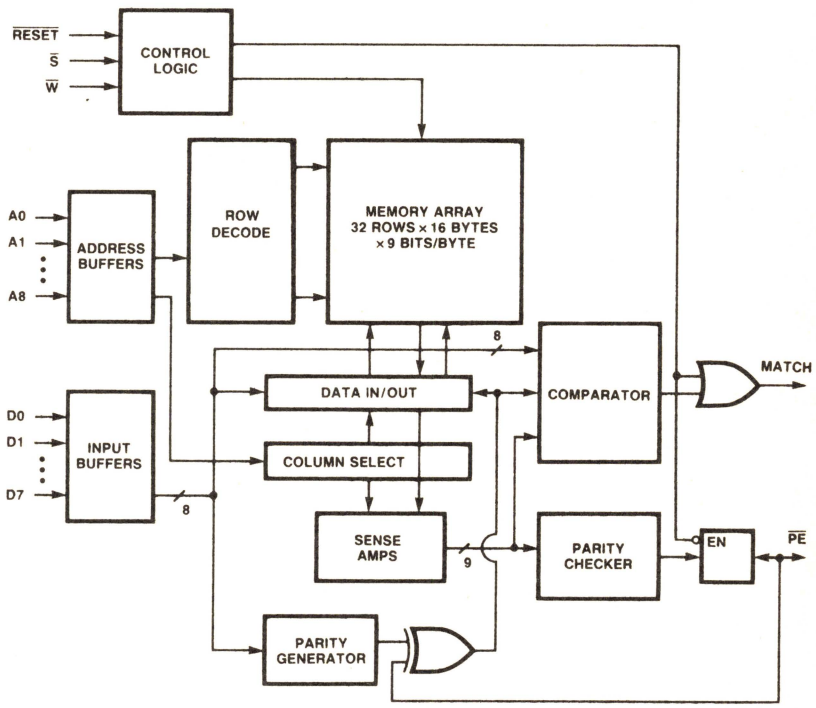
## PIN DIAGRAM




## PIN NAMES

| | |
|---|---|
| $\overline{RESET}$ | Reset Input |
| A0–A8 | Address Inputs |
| D0–D7 | Data Inputs |
| $\overline{W}$ | Write Control Input |
| $\overline{PE}$ | Parity Error I/O |
| $\overline{S}$ | Chip Select Input |
| MATCH | Comparator Output |
| VCC | Power (5 V) |
| GND | Ground (0 V) |

## BLOCK DIAGRAM

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PRELIMINARY **VT23512**

# 65,536 x 8 STATIC READ ONLY MEMORY

## FEATURES

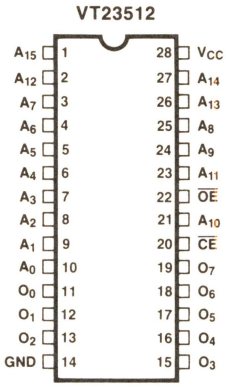
- 65,536 x 8 bit organization
- Access time – 150 ns max
- Current — Operating: 100 mA max
  Standby: 20 mA max
- Total static operation
- Static 5 V supply
- Automatic powerdown ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC approved pinout
- EPROMs accepted as program data input

## DESCRIPTION

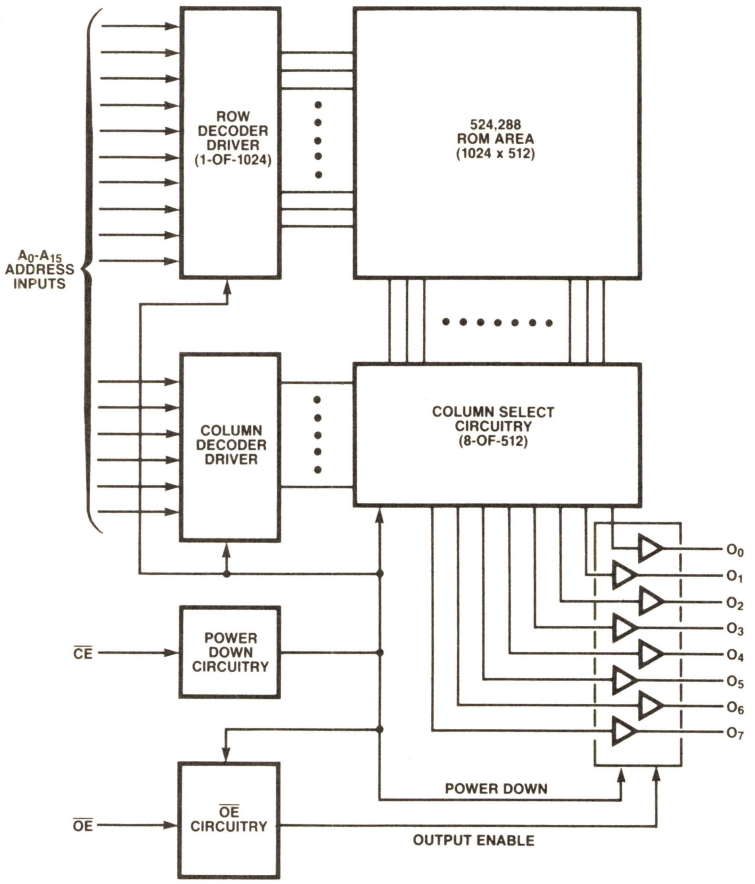
The VT23512 high performance Read Only Memory is organized 65,536 words by eight bits with an access time of 150 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

The VT23512 offers automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically powerdown and remain in a low-power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system level power savings of as much as 80%. The VT23512 also has an Output Enable ($\overline{OE}$) function to eliminate bus contention in multiple-bus microprocessor systems.

## PIN DIAGRAM




## BLOCK DIAGRAM

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# VT231024

## 131,070 × 8 STATIC READ ONLY MEMORY

### FEATURES

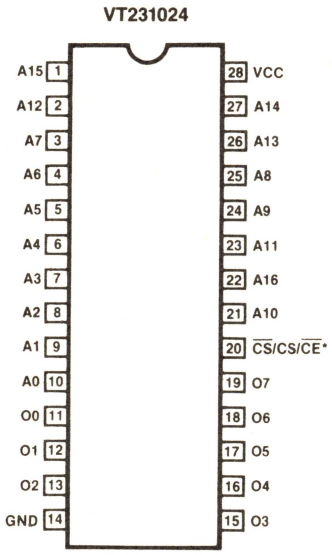
- 131,070 × 8-bit organization
- Access time—150 ns max
- Current—Operating: 100 mA max
  Standby: 20 mA max
- Total static operation
- Static 5 V supply
- Automatic powerdown [$\overline{CE}$]
- Complete TTL compatibility
- 3-State outputs for wired-OR expansion
- 28-pin JEDEC approved pinout
- EPROMs accepted as program data input

### DESCRIPTION

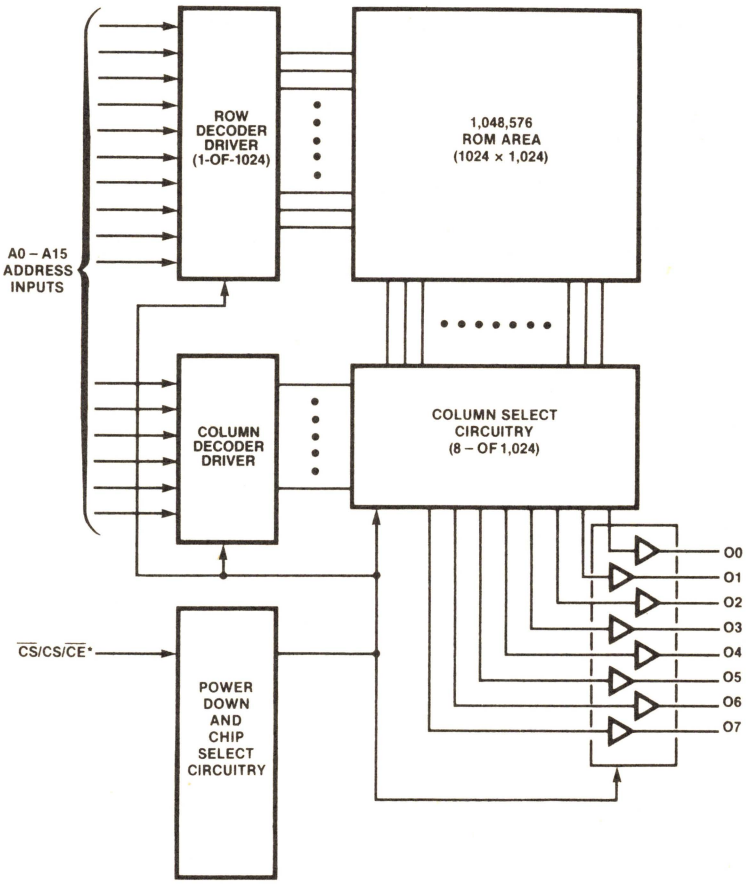
The VT231024 high performance Read Only Memory is organized 131,070 words by eight bits with an access time of 150 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

The VT231024 offers automatic power-down with powerdown controlled by the Chip Enable [$\overline{CE}$] input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system level power savings of as much as 80%. Pin 20 may also be programmed as CS (active HIGH or LOW) in order to eliminate bus contention in multiple-bus microprocessor systems.

### PIN CONFIGURATIONS




### BLOCK DIAGRAM




*THIS IS A MASK PROGRAMMABLE OPTION

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PRELIMINARY **VT231025**

# 131,070 × 8 STATIC READ ONLY MEMORY

## FEATURES

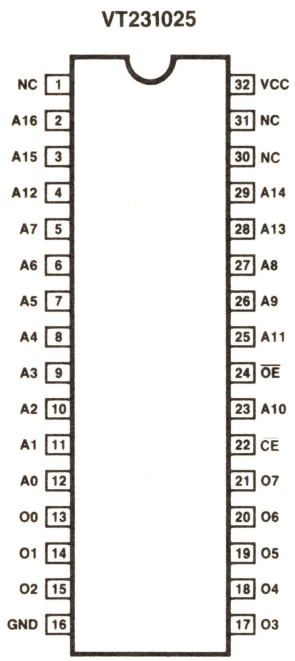
- 131,070 × 8-bit organization
- Access time—150 ns max
- 100 mA (max) operating current
- 20 mA (max) standby current
- Total static operation
- Static 5 V supply
- Automatic power-down
- Complete TTL compatibility
- Three-state outputs for wired-OR expansion
- 32-pin JEDEC-approved pinout
- EPROMs accepted as program data input
- Output enable ($\overline{OE}$) function

## DESCRIPTION

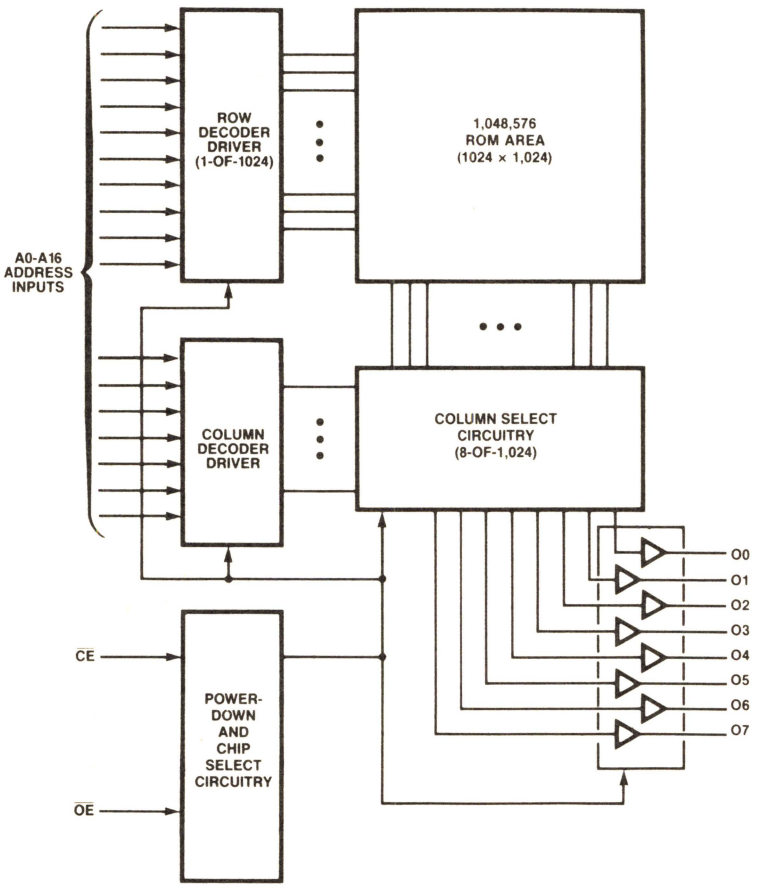
The VT231025 high-performance read only memory is organized 131,070 words by eight bits and has an access time of 150 ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

The VT231025 offers automatic power-down, with power-down controlled by the chip enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device automatically powers down and remains in a low-power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system-level power savings of as much as 80%.

## PIN DIAGRAM




## BLOCK DIAGRAM

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# APPLICATION SPECIFIC MEMORY PRODUCTS

## CROSS-REFERENCE GUIDE

| AMD | VLSI |
|---|---|
| AM2130 | VT2130 |
| AM2131 | VT2131 |
| AM9122 | VT7C122 |
| AM9150 | VT20C50 |
| AM99C68 | VT20C68 |

| CYPRESS | VLSI |
|---|---|
| CY7C122 | VT7C122 |
| CY7C128 | VT20C18 |
| CY7C129 | VT20C19 |
| CY7C132 | VT7132 |
| CY7C142 | VT7142 |
| CY7C150 | VT20C50 |
| CY7C168 | VT20C68 |
| CY7C169 | VT20C69 |
| CY7C170 | VT20C79 |
| CY7C171 | VT20C71 |
| CY7C172 | VT20C72 |
| CY7C185 | VT20C98 |

| FUJITSU | VLSI |
|---|---|
| MB83512 | VT23512 |
| MBM81C68A | VT20C68 |
| MBM81C69A | VT20C69 |
| MB831000 | VT231024 |

| HITACHI | VLSI |
|---|---|
| HM/HN6168 | VT20C68 |
| HM/HN6268 | VT20C69 |

| IDT | VLSI |
|---|---|
| IDT6168 | VT20C68 |
| IDT7130S | VT2130 |
| IDT7132 | VT7132 |
| IDT7164 | VT20C98 |
| IDT71681 | VT20C71 |
| IDT71682 | VT20C72 |
| IDT7203 | VT2KF9 |

| INMOS | VLSI |
|---|---|
| IMS1421 | VT20C69 |
| IMS1423 | VT20C68 |

| INTEL | VLSI |
|---|---|
| I51C68 | VT20C68 |
| I51C69 | VT20C69 |

| LATTICE | VLSI |
|---|---|
| SR16K4 | VT20C68 |
| SR16K8 | VT20C18 |

| MITSUBISHI | VLSI |
|---|---|
| MB/MBM81C68A | VT20C68 |
| MB/MBM81C69A | VT20C69 |

| MOTOROLA | VLSI |
|---|---|
| MCM2016 | VT20C18 |
| MCM6178 | VT20C78 |
| MCM6268 | VT20C68 |

| NEC | VLSI |
|---|---|
| μPD4314 | VT20C68 |

| TI | VLSI |
|---|---|
| TI2150 | VT7150 |
| TI2152 | VT7152 |

| TOSHIBA | VLSI |
|---|---|
| TC/TMM2018 | VT20C18 |
| TC/TMM2068 | VT20C68 |
| TC/TMM2078 | VT20C78 |
| TC/TMM531000P | VT23C1024 |

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## SRAMs

| Size | Device | Description | Access Times (ns) | Technology | Pins | Packages | Samples |
|---|---|---|---|---|---|---|---|
| 1K | VT7C122 | SRAM: 256 x 4 | 15, 25, 35 | CMOS | 22<br>24 | P<br>SO | Now<br>Now |
| 4K | VT20C50 | Clearable SRAM with Separate I/O: 1,024 x 4 | 15, 20, 25 | CMOS | 24 | P, SO | Q487 |
| 16K | VT20C18 | SRAM with Chip Enable, Auto Power Down: 2,048 x 8 | 20, 25, 35 | CMOS | 24 | P, SO | Now |
| 16K | VT20C19 | SRAM with Fast Chip Select: 2,048 x 8 | 20, 25, 35 | CMOS | 24 | P, SO | Now |
| 16K | VT20C68 | SRAM with Chip Enable, Auto Power Down: 4,096 x 4 | 20, 25, 35 | CMOS | 20 | P | Now |
| 16K | VT20C69 | SRAM with Fast Chip Select: 4,096 x 4 | 20, 25, 35 | CMOS | 20 | P | Now |
| 16K | VT20C71 | SRAM with Separate I/O; Outputs Track Inputs During Write: 4,096 x 4 | 20, 25, 35 | CMOS | 24 | P, SO | Now |
| 16K | VT20C72 | SRAM with Separate I/O; High-Impedance Outputs During Write: 4,096 x 4 | 20, 25, 35 | CMOS | 24 | P, SO | Now |
| 16K | VT20C78 | SRAM with Chip Enable, Auto Power Down: 4,096 x 4 | 20, 25, 35 | CMOS | 22<br>24 | P<br>SO | Now<br>Now |
| 16K | VT20C79 | SRAM with Fast Chip Select: 4,096 x 4 | 20, 25, 35 | CMOS | 22<br>24 | P<br>SO | Now<br>Now |
| 64K | VT20C98 | SRAM with Chip Enable, Auto Power Down: 8,192 x 8 | 25, 30, 35 | CMOS | 28 | P | Q288 |
| 64K | VT20C99 | SRAM with Fast Chip Select: 8,192 x 8 | 25, 30, 35 | CMOS | 28 | P | Q288 |



**Package Codes:** P = Plastic DIP; Q = PLCC; SO = Small Outline (Both Gull-Wing and J-Lead)


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## APPLICATION-SPECIFIC MEMORIES (ASMs)

| Size | Device | Description | Access Times (ns) | Technology | Pins | Packages | Samples |
|---|---|---|---|---|---|---|---|
| 4K | VT7150 | Cache Tag RAM: 512 x 9 | 20, 25, 35 | CMOS | 24 | P, SO | Q487 |
| 8K | VT2130 | Dual-Port RAM: 1,024 x 8 | 120, 150, 200 | NMOS | 48 | P | Now |
| 8K | VT2131 | Dual-Port RAM: 1,024 x 8 | 120, 150, 200 | NMOS | 48 | P | Now |
| 16K | VT16AM8 | Dual-Port RAM: 2,048 x 8/1,024 x 16 | 60, 70 | CMOS | 68 | Q | Q288 |
| 16K | VT16DP8 | Dual-Port RAM: 2,048 x 8/1,024 x 16 | 60, 70 | CMOS | 68 | Q | Now |
| 16K | VT7132 | Dual-Port RAM (Master): 2,048 x 8 | 55, 70, 90 | CMOS | 48<br>52 | P<br>Q | Q188<br>Q188 |
| 16K | VT7132A | Dual-Port RAM (Master): 2,048 x 8 | 30, 35, 45 | CMOS | 48<br>52 | P<br>Q | Q188<br>Q188 |
| 16K | VT7142 | Dual-Port RAM (Slave): 2,048 x 8 | 55, 70, 90 | CMOS | 48<br>52 | P<br>Q | Q188<br>Q188 |
| 16K | VT7142A | Dual-Port RAM (Slave): 2,048 x 8 | 30, 35, 45 | CMOS | 48<br>52 | P<br>Q | Q188<br>Q188 |
| 18K | VT2KF9 | FIFO: 2,064 x 9 | 50, 65, 80 | CMOS | 28<br>32 | P<br>Q | Q388<br>Q388 |
| 18K | VT2KF91 | FIFO: 2,064 x 9 | 50, 65, 80 | CMOS | 32 | Q | Q288 |

## ROMs

| Size | Device | Description | Access Times (ns) | Technology | Pins | Packages | Samples |
|---|---|---|---|---|---|---|---|
| 512K | VT23512 | ROM: 65,536 x 8 | 150, 200, 250 | NMOS | 28 | P | Now |
| 1M | VT231024 | ROM: 131,070 x 8 | 150, 200, 250 | NMOS | 28 | P | Now |
| 1M | VT231025 | ROM: 131,070 x 8 | 150, 200, 250 | NMOS | 32 | P | Now |





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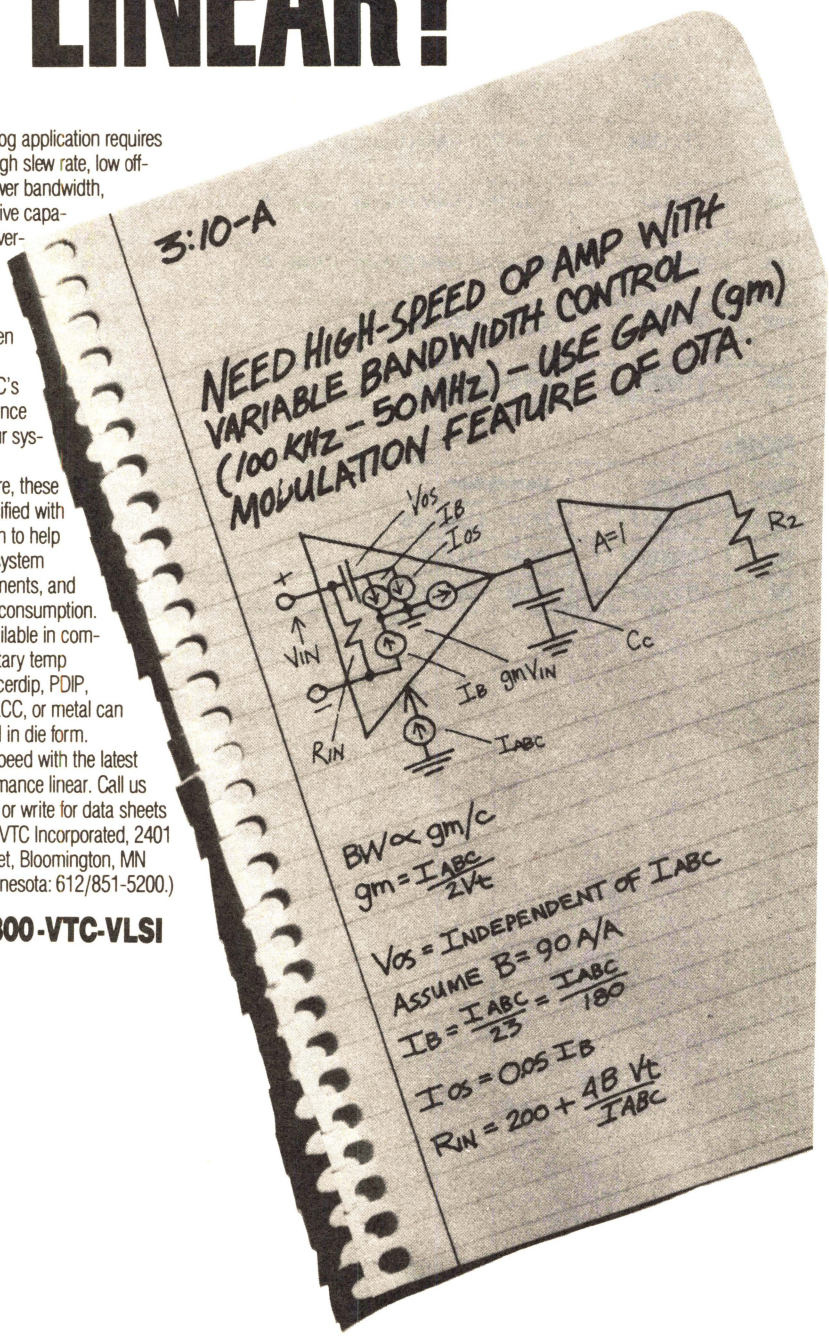


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| 240 | 540 | 245 | 861 | 374 | 823 | 373 | 843 |
| 241 | 541 | 620 | 862 | 534 | 824 | 533 | 844 |
| 244 | 827 | 623 | 863 | 564 | 825 | 563 | 845 |
| 465 | 828 | 640 | 864 | 574 | 826 | 573 | 846 |
| 466 | | 643 | | 575 | 874 | 580 | 880 |
| 467 | | 645 | | 576 | 876 | 841 | |
| 468 | | | | 577 | 878 | 842 | |
| | | | | 821 | 879 | | |
| | | | | 822 | | | |

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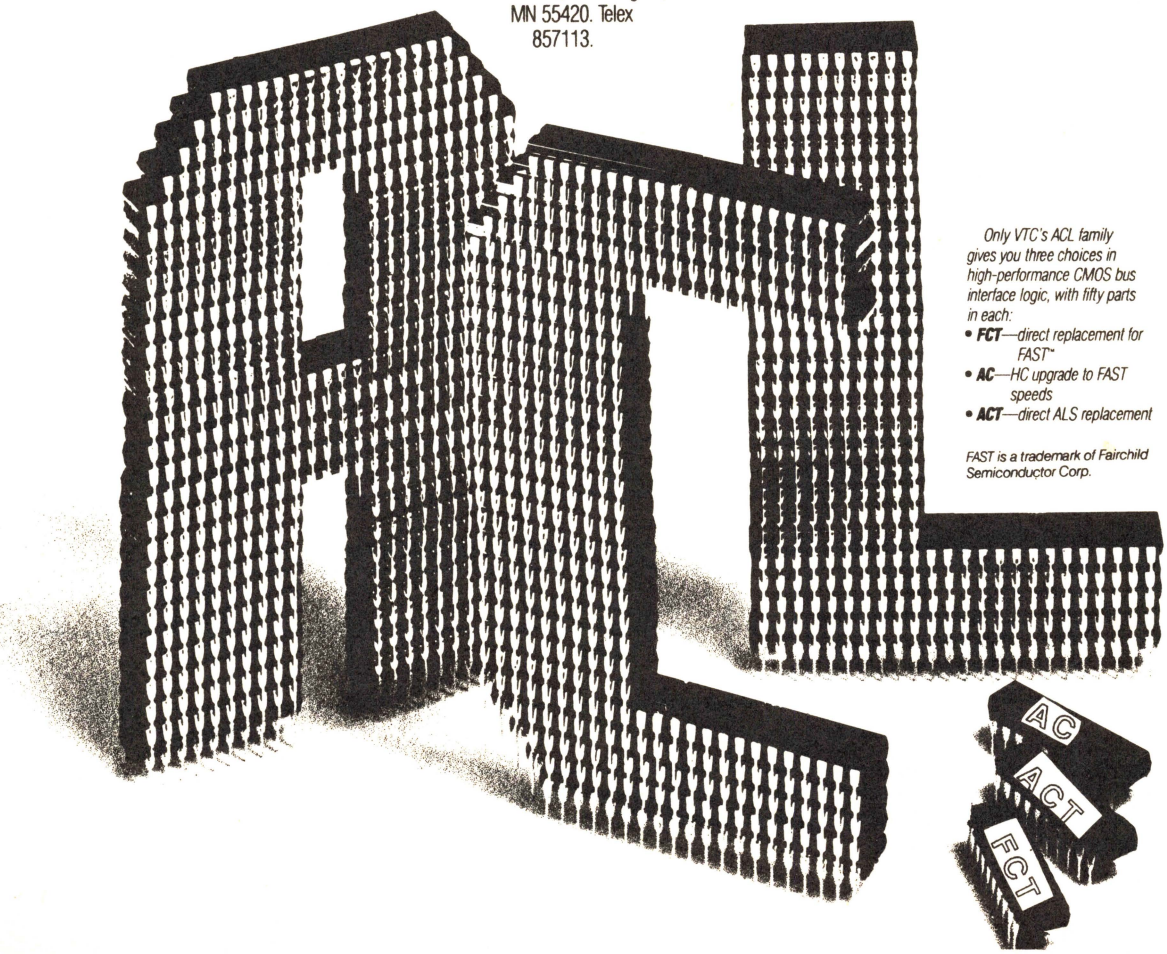


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**VTC's ACT FAMILY CROSS REFERENCE — EXAMPLE VTC PART NUMBER V74ACT240**

| FAMILY CROSSED TO | VTC ADVANTAGE | VENDOR | PART NUMBER EG. |
|---|---|---|---|
| ACT | Equal Performance | Fairchild<br>GE/RCA | 74ACT240<br>CD74ACT240 |
| AHCT | Meet or Exceed Performance Upgrade by 10% | IDT<br>Samsung<br>Zytrex | IDT74AHCT240<br>KS74AHCT240<br>ZX74AHCT240 |
| ALS | Equal Performance<br>Dramatic Power Savings | †Texas Instruments<br>†National<br>†Mitsubishi | SN74ALS240A<br>DM74ALS240<br>M74ALS240A |
| HCT | *System upgrade by 150% | Texas Instruments<br>GE/RCA<br>Hitachi<br>Motorola<br>National<br>Signetics | SN74HCT240<br>CD74HCT240<br>HD74HCT240<br>MC74HCT240<br>MM74HCT240<br>74HCT240 |

**VTC's AC FAMILY CROSS REFERENCE — EXAMPLE VTC PART NUMBER V74AC240**

| FAMILY CROSSED TO | VTC ADVANTAGE | VENDOR | PART NUMBER EG. |
|---|---|---|---|
| AC | Equal Performance | Fairchild<br>GE/RCA | 74AC240<br>CD74AC240 |
| HC | *System upgrade by 200% | Texas Instruments<br>GE/RCA<br>Hitachi<br>Motorola<br>National<br>Signetics<br>Fairchild | SN74HC240<br>CD74HC240<br>HD74HC240<br>MC74HC240<br>MM74HC240<br>74HC240<br>74HC240 |

**VTC's FCT FAMILY CROSS REFERENCE — EXAMPLE VTC PART NUMBER V74FCT240**

| FAMILY CROSSED TO | VTC ADVANTAGE | VENDOR | PART NUMBER EG. |
|---|---|---|---|
| FAST™ | Equal Performance<br>Dramatic Power Savings | †Texas Instruments<br>†Fairchild<br>†Motorola<br>†Signetics | SN74F240<br>74F240<br>MC74F240<br>74F240 |
| FCT | Equal Performance | IDT | IDT74FCT240 |

**VTC's FCT FAMILY CROSS REFERENCE — EXAMPLE VTC PART NUMBER V74FCT824A**

| FAMILY CROSSED TO | VTC ADVANTAGE | VENDOR | PART NUMBER EG. |
|---|---|---|---|
| 29XX | Equal Performance<br>Dramatic Power Savings | †AMD | A29824 |
| 39C | Equal Performance | IDT | IDT39C824 |

*†These are bipolar components which can be replaced by functionally and performance equivalent CMOS.*
**System upgrade refers to the clock rate attainable by substituting ACL parts. For instance a 6 MHz HC based system could be upgraded to a 18 MHz AC system.*

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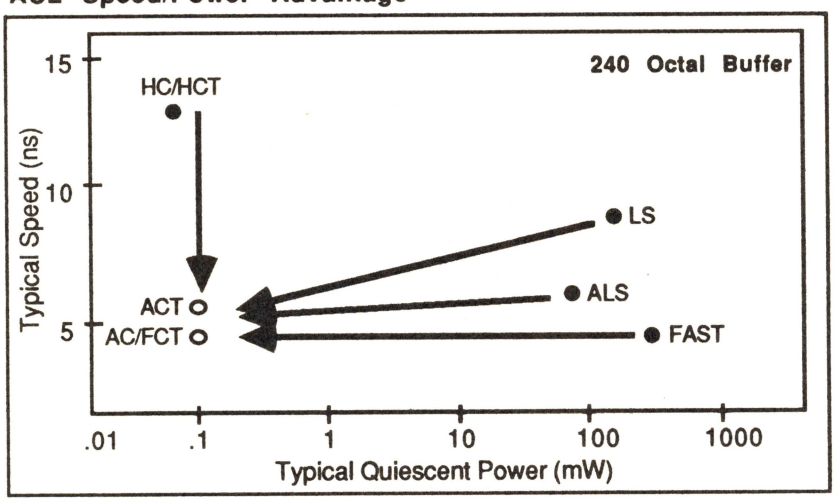
VTC's advanced CMOS logic families offer state-of-the-art interfaces for the latest generations of microprocessor, memory, standard cell, and gate array systems.

All of the ACL products are fabricated by VTC using an advanced 1.2-micron, double-level metal CMOS 1 process and are packaged in plastic and ceramic dual in-line packages, small outline and leaded chip carrier packages with JEDEC standard pinouts.

***High-Performance Interface***

ACL from VTC means high-performance and high-quality bus interface logic. VTC's ACL products with their patented output structure offer the high drive (48mA to 64mA) required by VMEbus, Multibus and many other high-performance systems along with the popular speeds of FAST™ and ALS. Our ACL products are also latch-up free to 400mA, have ESD protection greater than 2000V and are fully characterized and specified. These features, along with low CMOS power, make VTC's ACL products ideal for systems requiring high-performance bus interface logic.

**ACL Speed/Power Advantage**




***FCT***
- CMOS replacement for FAST™
- Upgrade for systems using ALS, LS and HCT
- High Drive:
  $I_{OL}/I_{OH}$ = 64/15mA;
  Line drivers and transceivers
  $I_{OL}/I_{OH}$ = 48/15mA;
  Latches and flip-flops
- Speed equivalent to FAST, typical 4 to 5ns
- Low CMOS power, 50µW typical
- TTL logic levels
- Second sourced by IDT

***ACT***
- CMOS replacement for ALS
- Upgrade for systems using LS and HCT
- High drive: $I_{OL}/I_{OH}$ = 48/24mA
- Speed equivalent to ALS, typical 5ns
- Low CMOS power, 50µW typical
- TTL logic levels

***AC***
- CMOS upgrade for HC
- CMOS logic levels
- High drive: $I_{OL}/I_{OH}$ = 24/24mA
- Speed equivalent to FAST, typical 4 to 5ns
- Low CMOS power, 50µW typical

| *54/74FCT* | *54/74ACT* | *54/74AC* | *Description* |
|---|---|---|---|
| 54/74FCT240 | 54/74ACT240 | 54/74AC240 | Octal Buffers and Line Drivers |
| 54/74FCT241 | 54/74ACT241 | 54/74AC241 | Octal Buffers and Line Drivers |
| 54/74FCT244 | 54/74ACT244 | 54/74AC244 | Octal Buffers and Line Drivers |
| 54/74FCT245 | 54/74ACT245 | 54/74AC245 | Octal Bus Transceivers |
| 54/74FCT373 | 54/74ACT373 | 54/74AC373 | Octal D-Type Transparent Latches |
| 54/74FCT374 | 54/74ACT374 | 54/74AC374 | Octal D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT465 | 54/74AC465 | Octal Buffers and Line Drivers |
| | 54/74ACT466 | 54/74AC466 | Octal Buffers and Line Drivers |
| | 54/74ACT467 | 54/74AC467 | Octal Buffers and Line Drivers |
| | 54/74ACT468 | 54/74AC468 | Octal Buffers and Line Drivers |
| 54/74FCT533 | 54/74ACT533 | 54/74AC533 | Octal D-Type Transparent Latches |
| 54/74FCT534 | 54/74ACT534 | 54/74AC534 | Octal D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT540 | 54/74AC540 | Octal Buffers and Line Drivers |
| | 54/74ACT541 | 54/74AC541 | Octal Buffers and Line Drivers |
| | 54/74ACT563 | 54/74AC563 | Octal D-Type Transparent Latches |
| | 54/74ACT564 | 54/74AC564 | Octal D-Type Edge-Triggered Flip-Flops |
| 54/74FCT573 | 54/74ACT573 | 54/74AC573 | Octal D-Type Transparent Latches |
| 54/74FCT574 | 54/74ACT574 | 54/74AC574 | Octal D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT575 | 54/74AC575 | Octal D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT576 | 54/74AC576 | Octal D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT577 | 54/74AC577 | Octal D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT580 | 54/74AC580 | Octal D-Type Transparent Latches |
| | 54/74ACT620 | 54/74AC620 | Octal Bus Transceivers |
| | 54/74ACT623 | 54/74AC623 | Octal Bus Transceivers |
| 54/74FCT640 | 54/74ACT640 | 54/74AC640 | Octal Bus Transceivers |
| | 54/74ACT643 | 54/74AC643 | Octal Bus Transceivers |
| 54/74FCT645 | 54/74ACT645 | 54/74AC645 | Octal Bus Transceivers |
| 54/74FCT821A | 54/74ACT821 | 54/74AC821 | 10-Bit D-Type Edge-Triggered Flip-Flops |
| 54/74FCT822A | 54/74ACT822 | 54/74AC822 | 10-Bit D-Type Edge-Triggered Flip-Flops |
| 54/74FCT823A | 54/74ACT823 | 54/74AC823 | 9-Bit D-Type Edge-Triggered Flip-Flops |
| 54/74FCT824A | 54/74ACT824 | 54/74AC824 | 9-Bit D-Type Edge-Triggered Flip-Flops |
| 54/74FCT825A | 54/74ACT825 | 54/74AC825 | Octal D-Type Edge-Triggered Flip-Flops |
| 54/74FCT826A | 54/74ACT826 | 54/74AC826 | Octal D-Type Edge-Triggered Flip-Flops |
| 54/74FCT827A | 54/74ACT827 | 54/74AC827 | 10-Bit Buffers and Line Drivers |
| 54/74FCT828A | 54/74ACT828 | 54/74AC828 | 10-Bit Buffers and Line Drivers |
| 54/74FCT841A | 54/74ACT841 | 54/74AC841 | 10-Bit D-Type Transparent Latches |
| 54/74FCT842A | 54/74ACT842 | 54/74AC842 | 10-Bit D-type Transparent Latches |
| 54/74FCT843A | 54/74ACT843 | 54/74AC843 | 9-Bit D-type Transparent Latches |
| 54/74FCT844A | 54/74ACT844 | 54/74AC844 | 9-Bit D-type Transparent Latches |
| 54/74FCT845A | 54/74ACT845 | 54/74AC845 | Octal D-type Transparent Latches |
| 54/74FCT846A | 54/74ACT846 | 54/74AC846 | Octal D-type Transparent Latches |
| 54/74FCT861A | 54/74ACT861 | 54/74AC861 | 10-Bit Bus Transceivers |
| 54/74FCT862A | 54/74ACT862 | 54/74AC862 | 10-Bit Bus Transceivers |
| 54/74FCT863A | 54/74ACT863 | 54/74AC863 | 9-Bit Bus Transceivers |
| 54/74FCT864A | 54/74ACT864 | 54/74AC864 | 9-Bit Bus Transceivers |
| | 54/74ACT874 | 54/74AC874 | Dual 4-Bit D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT876 | 54/74AC876 | Dual 4-Bit D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT878 | 54/74AC878 | Dual 4-Bit D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT879 | 54/74AC879 | Dual 4-Bit D-Type Edge-Triggered Flip-Flops |
| | 54/74ACT880 | 54/74AC880 | Dual 4-Bit D-Type Edge-Triggered Flip-Flops |

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# Linear Signal Processing

**VTC Incorporated**
*Performance, Pure & Simple.™*

The linear signal processing (LSP) product line is part of the system solution for such applications as scientific and medical instrumentation, data acquisition, process control and general signal processing on either side of the A/D and D/A conversion blocks.

VTC's unique processes couple high speed with close device matching along with laser trimming capability. LSP products include operational amplifiers, buffers, comparators, transconductance amplifiers, sample-hold and D to A and A to D converters.

As in all products offered by VTC, the emphasis is on performance and reliability. The devices are designed to fit applications where high performance, high slew rate, low offset, bandwidth and high output current capability is required.

**Operational Amplifiers (All Parameters @ 25°C, V supply = ±5V)**

| DEVICE | DESCRIPTION | PACKAGE* | SLEW RATE | GAIN BANDWIDTH PRODUCT | OFFSET | | OUTPUT CURRENT | BIAS CURRENT | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Voltage | Current | | | |
| VA701J | Op Amp, Precision | D,P,PO,T,DL | 8V/µs | 20MHz@$A_{CL}$ = 1 | 500µV | 100nA | 50mA | 80nA | Commercial |
| VA701K | Op Amp, Precision | D,P,PO,T,DL | 8V/µs | 20MHz@$A_{CL}$ = 1 | 100µV | 50nA | 50mA | 40nA | Commercial |
| VA701L | Op Amp, Precision | D,P,PO,T,DL | 8V/µs | 20MHz@$A_{CL}$ = 1 | 25µV | 50nA | 50mA | 40nA | Commercial |
| VA701S | Op Amp, Precision | D,T,DL | 8V/µs | 20MHz@$A_{CL}$ = 1 | 25µV | 50nA | 50mA | 40nA | Military |
| VA705J | Op Amp, Precision, High-Speed | D,P,T,PO | 30V/µs | 25MHz@$A_{CL}$ = 1 | 10mV | 100nA | 40mA | 1100nA | Commercial |
| VA705K | Op Amp, Precision, High-Speed | D,P,T,PO | 30V/µs | 25MHz@$A_{CL}$ = 1 | 5mV | 50nA | 50mA | 900nA | Commercial |
| VA705L | Op Amp, Precision, High-Speed | D,P,T,PO | 30V/µs | 25MHz@$A_{CL}$ = 1 | 2mV | 25nA | 50mA | 900nA | Commercial |
| VA705S | Op Amp, Precision, High-Speed | D,T,X | 30V/µs | 25MHz@$A_{CL}$ = 1 | 5mV | 25nA | 50mA | 1100nA | Military |
| VA705T | Op Amp, Precision, High-Speed | D,T | 30V/µs | 25MHz@$A_{CL}$ = 1 | 2mV | 25nA | 50mA | 900nA | Military |
| VA706J | Op Amp, Fast Settling, High-Speed | D,P,T,PO | 38V/µs | 25MHz@$A_{CL}$ = 1 | 20mV | 120nA | 40mA | 1100nA | Commercial |
| VA706K | Op Amp, Fast Settling, High-Speed | D,P,T,PO | 38V/µs | 25MHz@$A_{CL}$ = 1 | 10mV | 120nA | 50mA | 1100nA | Commercial |
| VA706S | Op Amp, Fast Settling, High-Speed | D,T,X | 38V/µs | 25MHz@$A_{CL}$ = 1 | 10mV | 120nA | 50mA | 1100nA | Military |
| VA707J | Op Amp, Fast Settling, High-Speed | D,P,T,PO | 80V/µs | 300MHz@$A_{CL}$ = 12 | 12mV | 120nA | 40mA | 1100nA | Commercial |
| VA707K | Op Amp, Fast Settling, High-Speed | D,P,T,PO | 80V/µs | 300MHz@$A_{CL}$ = 12 | 6mV | 120nA | 50mA | 1100nA | Commercial |
| VA707S | Op Amp, Fast Settling, High-Speed | D,T,X | 80V/µs | 300MHz@$A_{CL}$ = 12 | 6mV | 120nA | 50mA | 1100nA | Military |
| VA708J | Op Amp, Fast Settling, High-Speed | D,P,T,PO | 60V/µs | 100MHz@$A_{CL}$ = 3 | 12mV | 120nA | 40mA | 1100nA | Commercial |
| VA708K | Op Amp, Fast Settling, High-Speed | D,P,T,PO | 60V/µs | 100MHz@$A_{CL}$ = 3 | 6mV | 120nA | 50mA | 1100nA | Commercial |
| VA708S | Op Amp, Fast Settling, High-Speed | D,T,X | 60V/µs | 100MHz@$A_{CL}$ = 3 | 6mV | 120nA | 50mA | 1100nA | Military |
| VA711J | Op Amp, Precision | D,P,PO,T,DL | 40V/µs | 90MHz @ $A_{CL}$ = 5 | 500µV | 100nA | 50mA | 80nA | Commercial |
| VA711K | Op Amp, Precision | D,P,PO,T,DL | 40V/µs | 90MHz @ $A_{CL}$ = 5 | 100µV | 40nA | 50mA | 40nA | Commercial |
| VA711L | Op Amp, Precision | D,P,PO,T,DL | 40V/µs | 90MHz @$A_{CL}$ = 5 | 25µV | 40nA | 50mA | 40nA | Commercial |
| VA711S | Op Amp, Precision | D,T,DL | 40V/µs | 90MHz @ $A_{CL}$ = 5 | 25µV | 40nA | 50mA | 40nA | Military |
| VA721J | Precision Op Amp | D,P,PO,T,DL | 150V/µs | 500MHz @ $A_{CL}$ = 30 | 500µV | 100nA | 50mA | 80nA | Commercial |
| VA721K | Precision Op Amp | D,P,PO,T,DL | 150V/µs | 500MHz @ $A_{CL}$ = 30 | 100µV | 40nA | 50mA | 40nA | Commercial |
| VA721L | Precision Op Amp | D,P,PO,T,DL | 150V/µs | 500MHz @ $A_{CL}$ = 30 | 25µV | 40nA | 50mA | 40nA | Commercial |
| VA721S | Precision Op Amp | D,T,DL | 150V/µs | 500MHz @ $A_{CL}$ = 30 | 100µV | 40nA | 50mA | 40nA | Military |
| VA4701J | Quad Op Amp, Precision | D,P,PO,T,DL | 8V/µs | 20MHz @ $A_{CL}$ = 1 | 500µV | 100nA | 50mA | 80nA | Commercial |
| VA4701S | Quad Op Amp, Precision | D,T,DL | 8V/µs | 20MHz @ $A_{CL}$ = 1 | 500µV | 50nA | 50mA | 40nA | Military |
| VA2705J | Dual Op Amp | D,P,T | 30V/µs | 40MHz@$A_{CL}$ = 1 | 12mV | 50nA | 40mA | 1100nA | Commercial |
| VA2705K | Dual Op Amp | D,P,T | 30V/µs | 40MHz@$A_{CL}$ = 1 | 6mV | 50nA | 50mA | 900nA | Commercial |
| VA2705S | Dual Op Amp | D,T | 30V/µs | 40MHz@$A_{CL}$ = 1 | 6mV | 100nA | 50mA | 900nA | Military |
| VA2715J | Dual Op Amp w/Nulling | D,P | 30V/µs | 40MHz@$A_{CL}$ = 1 | 12mV | 50nA | 40mA | 1100nA | Commercial |
| VA2715K | Dual Op Amp w/Nulling | D,P | 30V/µs | 40MHz@$A_{CL}$ = 1 | 6mV | 50nA | 50mA | 900nA | Commercial |
| VA2715S | Dual Op Amp w/Nulling | D | 30V/µs | 40MHz@$A_{CL}$ = 1 | 6mV | 120nA | 50mA | 900nA | Military |
| VA2706J | Dual Op Amp | D,P,T | 38V/µs | 40MHz@$A_{CL}$ = 1 | 20mV | 120nA | 40mA | 1100nA | Commercial |
| VA2706S | Dual Op Amp | D,P | 38V/µs | 40MHz@$A_{CL}$ = 1 | 12mV | 120nA | 50mA | 1100nA | Military |
| VA2716J | Dual Op Amp w/Nulling | D,P | 38V/µs | 40MHz@$A_{CL}$ = 1 | 20mV | 120nA | 40mA | 1100nA | Commercial |
| VA2716S | Dual Op Amp w/Nulling | D | 38V/µs | 40MHz@$A_{CL}$ = 1 | 12mV | 120nA | 50mA | 1100nA | Military |
| VA2707J | Dual Op Amp | D,P,T | 80V/µs | 400MHz@$A_{CL}$ = 12 | 12mV | 120nA | 40mA | 1100nA | Commercial |
| VA2707K | Dual Op Amp | D,P,T | 80V/µs | 400MHz@$A_{CL}$ = 12 | 6mV | 120nA | 50mA | 1100nA | Commercial |
| VA2707S | Dual Op Amp | D,T | 80V/µs | 400MHz@$A_{CL}$ = 12 | 6mV | 120nA | 50mA | 1100nA | Military |
| VA4711J | Quad Op Amp | D,P,PO,T,DL | 40V/µs | 90MHz@$A_{CL}$ = 5 | 500µV | 100nA | 50mA | 80nA | Commercial |
| VA4711S | Quad Op Amp | D,T,DL | 40V/µs | 90MHz@$A_{CL}$ = 5 | 500µV | 50nA | 50mA | 40nA | Military |
| VA2717J | Dual Op Amp w/Nulling | D,P | 80V/µs | 300MHz@$A_{CL}$ = 12 | 12mv | 120nA | 40mA | 1100nA | Commercial |
| VA2717K | Dual Op Amp w/Nulling | D,P | 80V/µs | 300MHz@$A_{CL}$ = 12 | 6mV | 120nA | 50mA | 1100nA | Commercial |
| VA2717S | Dual Op Amp w/Nulling | D | 80V/µs | 300MHz@$A_{CL}$ = 12 | 6mV | 120nA | 50mA | 1100nA | Mlitary |
| VA2708J | Dual Op Amp | D,P,T | 60V/µs | 100MHz@$A_{CL}$ = 3 | 12mV | 120nA | 40mA | 1100nA | Commercial |
| VA2708K | Dual Op Amp | D,P,T | 60V/µs | 100MHz@$A_{CL}$ = 3 | 6mV | 120nA | 50mA | 1100nA | Commercial |
| VA2708S | Dual Op Amp | D,T | 60V/µs | 100MHz@$A_{CL}$ = 3 | 6mV | 120nA | 50mA | 1100nA | Military |
| VA2718J | Dual Op Amp w/Nulling | D,P | 60V/µs | 100MHz@$A_{CL}$ = 3 | 12mV | 120nA | 40mA | 1100nA | Commercial |
| VA2718K | Dual Op Amp w/Nulling | D,P | 60V/µs | 100MHz@$A_{CL}$ = 3 | 6mV | 120nA | 50mA | 1100nA | Commercial |
| VA2718S | Dual Op Amp w/Nulling | D | 60V/µs | 100MHz@$A_{CL}$ = 3 | 6mV | 120nA | 40mA | 1100nA | Military |
| VA4705J | Quad Op Amp | D,P | 30V/µs | 40MHz@$A_{CL}$ = 1 | 12mV | 100nA | 50mA | 1100nA | Commercial |
| VA4705K | Quad Op Amp | D,P | 30V/µs | 40MHz@$A_{CL}$ = 1 | 6mV | 50nA | 50mA | 900nA | Commercial |
| VA4705S | Quad Op Amp | D | 30V/µs | 40MHz@$A_{CL}$ = 1 | 6mV | 50nA | 50mA | 900nA | Military |
| VA4706J | Quad Op Amp | D,P | 38V/µs | 40MHz@$A_{CL}$ = 1 | 20mV | 120nA | 50mA | 1100nA | Commercial |
| VA4706S | Quad Op Amp | D | 38V/µs | 40MHz@$A_{CL}$ = 1 | 12mV | 120nA | 50mA | 1100nA | Military |
| VA4707J | Quad Op Amp | D,P | 80V/µs | 300MHz@$A_{CL}$ = 12 | 12mV | 120nA | 40mA | 1100nA | Commercial |
| VA4707K | Quad Op Amp | D,P | 80V/µs | 300MHz@$A_{CL}$ = 12 | 6mV | 120nA | 50mA | 1100nA | Commercial |
| VA4707S | Quad Op Amp | D | 80V/µs | 300MHz@$A_{CL}$ = 12 | 6mV | 120nA | 50mA | 1100nA | Military |
| VA4708J | Quad Op Amp | D,P | 60V/µs | 100MHz@$A_{CL}$ = 3 | 12mV | 120nA | 40mA | 1100nA | Commercial |
| VA4708K | Quad Op Amp | D,P | 60V/µs | 100MHz@$A_{CL}$ = 3 | 6mV | 120nA | 50mA | 1100nA | Commercial |
| VA4708S | Quad Op Amp | D | 60V/µs | 100MHz@$A_{CL}$ = 3 | 6mV | 120nA | 40mA | 1100nA | Military |
| VA4721J | Quad Precision Op Amp | D,P,PO,DL | 150V/µs | 500MHz@$A_{CL}$ = 30 | 500µV | 100nA | 50mA | 80nA | Commercial |
| VA4721S | Quad Precision Op Amp | D,DL | 150V/µs | 500MHz@$A_{CL}$ = 30 | 500µV | 100nA | 50mA | 80nA | Military |
| VA4741J | Quad Op Ar..p | D,P,PO | 2.7V/µs | 5MHz@$A_{CL}$ = 1 | 5mV | 200nA | 13mA | 400nA | Commercial |
| VA4741S | Quad Op Amp | D | 2.7V/µs | 5MHz@$A_{CL}$ = 1 | 5mV | 200nA | 13mA | 400nA | Military |
| VA4742J | Quad Op Amp | D,P,PO | 2.7V/µs | 5MHz@$A_{CL}$ = 1 | 5mV | 200nA | 13mA | 400nA | Commercial |
| VA4742S | Quad Op Amp | D | 2.7V/µs | 5MHz@$A_{CL}$ = 1 | 5mV | 200nA | 13mA | 400nA | Military |

## Operational Transconductance Amplifiers (OTA)

| DEVICE | DESCRIPTION | PACKAGE* | SLEW RATE | BANDWIDTH | OFFSET Voltage | OFFSET Current | OUTPUT CURRENT | BIAS CURRENT | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|
| VA703J | OTA | D,P,PO,T | 50V/µs | 75MHz | 5mV | 0.6µA | — | 5µA | Commercial |
| VA703S | OTA | D,T,X | 50V/µs | 75MHz | 3mV | 0.6µA | — | 5µA | Military |
| VA713J | OTA w/Buffer | D,P,PO,T | 50V/µs | 75MHz | 5mV | 0.6µA | 20mA | 5µA | Commercial |
| VA713S | OTA w/Buffer | D,T,X | 50V/µs | 75MHz | 3mV | 0.6µA | 20mA | 5µA | Military |
| VA2703J | Dual OTA | D,P,PO | 50V/µs | 75MHz | 5mV | 0.6µA | — | 5µA | Commercial |
| VA2703S | Dual OTA | D | 50V/µs | 75MHz | 3mV | 0.6µA | — | 5µA | Military |
| VA2713J | Dual OTA w/Buffer | D,P,PO | 50V/µs | 75MHz | 5mV | 0.6µA | 20mA | 5µA | Commercial |
| VA2713S | Dual OTA w/Buffer | D | 50V/µs | 75MHz | 3mV | 0.6µA | 20mA | 5µA | Military |

## Linear Amplifiers, Special Purpose

| DEVICE | DESCRIPTION | PACKAGE* | COMMENTS |
|---|---|---|---|
| VA702J | Op Amp, Wideband, w/AGC | D,P,PO,T,DL | 450MHz Bandwidth |
| VA712S | Op Amp, Wideband, w/AGC | D,T,DL,X | 450MHz Bandwidth |
| VA730J | Amplifier, Sample and Hold | D,DL | 50MHz Sampling Frequency |
| VA730S | Amplifier, Sample and Hold | D,DL,X | 50MHz Sampling Frequency |
| VA7505J | Amplifier, Low Voltage | TB,PO,X | 1.0-1.6V Operating Supply Voltage |
| VA7505K | Amplifier, Low Voltage | TB,PO,X | 1.0-1.6V Operating Supply Voltage |
| VA7505L | Amplifier, Low Volatge | TB,PO,X | 1.0-1.6V Operating Supply Voltage |

## Data Converters

| DEVICE | DESCRIPTION | PACKAGE* | COMMENTS |
|---|---|---|---|
| VC008J | 8-Bit Flash A/D | D,DL | 8-Bit A/D, 250MHz, Commercial |
| VC008S | 8-Bit Flash A/D | D,DL,X | 8-Bit A/D, 250MHz, Military |
| VC108J | 8-Bit Video DAC | D,DL,PL,P | 8-Bit DAC, 200MHz, Commercial |
| VC108K | 8-Bit Video DAC | D,DL,PL,P | 8-Bit DAC, 300MHz, Commercial |
| VC108S | 8-Bit Video DAC | D,DL,X | 8-Bit DAC, 250MHz Military, 300MHz Commercial |
| VC401J | V/F Converter | D,P,PO | 0-20MHz Frequency Range, Commercial |
| VC401S | V/F Converter | D,X | 0-20MHz Frequency Range, Military |
| VC512J | 12-Bit DAC | D,P,PO,PL,DL | 12-Bit DAC, 125ns Settling Time, Commercial |
| VC512S | 12-Bit DAC | D,DL,X | 12-Bit DAC, 125ns Settling Time, Military |
| VC594J | 12-Bit A/D | D,P,PO,PL,DL | 12-Bit A/D, 5µs Conversion Rate, Commercial |
| VC594K | 12-Bit A/D | D,P,PO,PL,DL | 12-Bit A/D, 2µs Conversion Rate, Commercial |
| VC594S | 12-Bit A/D | D,DL,X | 12-Bit A/D, 2µs Conversion Rate, Military |

## Comparators

| DEVICE | DESCRIPTION | PACKAGE* | OFFSET Voltage | OFFSET Current | PROP DELAY | ENABLE PW | ENABLE Set-up/Hold | COMMENTS |
|---|---|---|---|---|---|---|---|---|
| VC7690J | Comparator,Very Fast | D,P,PO,T | 5mV | 5µA | 1.9ns | — | — | Commercial |
| VC7690S | Comparator, Very Fast | D,T,X | 5mV | 5µA | 2.0ns | — | — | Military |
| VC7695J | Comparator, Ultra Fast | D,P,PO,T,DL | 5mV | 5µA | 1.9ns | 2.0ns | 1.0ns | Commercial |
| VC7695S | Comparator, Ultra Fast | D,T,DL,X | 5mV | 5µA | 2.0ns | 2.0ns | 1.0ns | Military |
| VC7696J | TTL Comparator | D,P,PO,T,DL | 5mV | 5µA | 6.0ns | 2.0ns | 2.0ns | Commercial |
| VC7696S | TTL Comparator | D,T,TL,X | 5mV | 5µA | 6.5ns | 2.0ns | 2.0ns | Military |
| VC7697J | Dual Comparator, Ultra Fast | D,P,PO,DL | 5mV | 5µA | 2.5ns | 2.0ns | 1.0ns | Commercial |
| VC7697S | Dual Comparator, Ultra Fast | D,DL | 5mV | 5µA | 2.8ns | 2.0ns | 1.0ns | Military |
| VC7698J | Dual TTL Comparator | D,P,PO,DL | 5mV | 5µA | 8.0ns | 2.0ns | 2.0ns | Commercial |
| VC7698S | Dual TTL Comparator | D,DL | 5mV | 5µA | 8.5ns | 2.0ns | 2.0ns | Military |

## Video Amplifiers

| DEVICE | DESCRIPTION | PACKAGE* | GAIN G1 | GAIN G2 | GAIN G3 | BANDWIDTH G1 | BANDWIDTH G2 | BANDWIDTH G3 | INPUT NOISE | PROP DELAY G1 | PROP DELAY G2 | PROP DELAY G3 | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VA592J | Video Ampilifer | D,P,PO,T | 400 | 100 | — | 80MHz | 100MHz | — | 4µVrms | 7.5ns | 6.0ns | — | Commercial |
| VA592S | Video Amplifier | D,X,T | 400 | 100 | — | 80MHz | 100MHz | — | 4µVrms | 7.5ns | 6.0ns | — | Military |
| VA733J | Video Amplifier | D,P,PO,T | 400 | 100 | 10 | 95MHz | 110MHz | 140MHz | 4µVrms | 7.5ns | 6.0ns | 3.6ns | Commercial |
| VA733S | Video Amplifier | D,X,T | 400 | 100 | 10 | 95MHz | 110MHz | 140MHz | 4µVrms | 7.5ns | 6.0ns | 3.6ns | Military |

## Buffer Amplifiers

| DEVICE | DESCRIPTION | PACKAGE* | SLEW RATE | BANDWIDTH | OUTPUT OFFSET VOLTAGE | OUTPUT CURRENT | COMMENTS |
|---|---|---|---|---|---|---|---|
| VA003J | Unity Gain Buffer | D,P,PO,T | 600V/µs | 200MHz | 15mV | ±100mA | Commercial |
| VA003S | Unity Gain Buffer | D,X,T | 600V/µs | 200MHz | 10mV | ±100mA | Military |
| VA033J | Unity Gain Buffer | D,P,PO,T | 1500V/µs | 300MHz | 15mV | ±100mA | Commercial |
| VA033S | Unity Gain Buffer | D,X,T | 1500V/µs | 300MHz | 10mV | ±100mA | Military |

## Line Drivers

| DEVICE | DESCRIPTION | PACKAGE* | COMMENTS |
|---|---|---|---|
| VS610S | NTDS Driver/Receiver | D,DL,X | MIL-STD-1397 TYPE B,C NTDS Driver/Receiver |





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# Standard Circuits for Mass Storage Products

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## DISK DRIVE READ/WRITE PREAMPLIFIERS

| DEVICE | DAMPING RESISTOR OPTION | CHANNELS | POWER SUPPLY | INPUT NOISE | VOLTAGE GAIN (TYP) | PIN | PACKAGE |
|---|---|---|---|---|---|---|---|
| **Ferrite Heads** | | | | | | | |
| VM104 | | 4 | +6V,-4V | 1.6nV/√Hz | 35 | 24 | P, PO, F |
| VM115 | | 5 | +5V,-5V | 2.5nV/√Hz | 40 | 24 | P, PO, F |
| VM117 | | 2,4,6 | +5V,+12V | 1.6nV/√Hz | 100 | 18,22,24,28 | P,D,F,PO |
| VM117R | X | 2,4,6 | +5V,+12V | 1.6nV/√Hz | 100 | 18,22,24,28 | P,D,F,PO |
| VM217 | | 6,8 | +5V,+12V | 1.6nV/√Hz | 100 | 28,40,44 | P,PL,TB |
| VM217R | X | 6,8 | +5V,+12V | 1.6nV/√Hz | 100 | 28,40,44 | P,PL,TB |
| **Center-Tapped Thin-Film Heads** | | | | | | | |
| VM118 | | 2,4,6 | +5V,+12V | 1.6nV/√Hz | 100 | 18,22,24,28 | P,PO |
| VM118R | X | 2,4,6 | +5V,+12V | 1.6nV/√Hz | 100 | 18,22,24,28 | P,PO |
| VM218 | | 6,8 | +5V,+12V | 1.6nV/√Hz | 100 | 28,40,44 | P,PL,TB |
| VM217R | X | 6,8 | +5V,+12V | 1.6nV/√Hz | 100 | 28,40,44 | P,PL,TB |
| **Thin-Film Heads** | | | | | | | |
| VM114 | | 4 | +5V,-5V | 1.1nV/√Hz | 100 | 24 | F |
| VM214 | | 4 | +5V,-5V | 1.1nV/√Hz | 125 | 24 | F |
| VM314 | | 4 | +5V,-5V | .6nV/√Hz | 100 | 24 | F |
| VM321 | | 6,8 | +5V,-5V | .6nV/√Hz | 100 | 28,40,44 | P,PL,TB |
| VM321R | X | 6,8 | +5V,-5V | .6nV/√Hz | 100 | 28,40,44 | P,PL,TB |
| **Vertical Heads** | | | | | | | |
| VM322 | X | 6,8 | +5V,+12V | .6nV/√Hz | 100 | 28,40,44 | P,PL,TB |

## DISK DRIVE SERVO PREAMPLIFIERS

| DEVICE | DESCRIPTION | POWER SUPPLY | CHARACTERISTICS | PACKAGE |
|---|---|---|---|---|
| VM101 | Servo Preamp, Ferrite Head | -8.3V, or +10V | ei = 6nV/√Hz | D, PO |
| VM201 | Servo Preamp, Ferrite Head, Low Noise | -8.3V, or +10V | ei = 1nV/√Hz | D, PO |
| VM216 | Servo Preamp, Thin-film Head | -8.3V, or +12V | ei = 1nV/√Hz | D, PO, F |

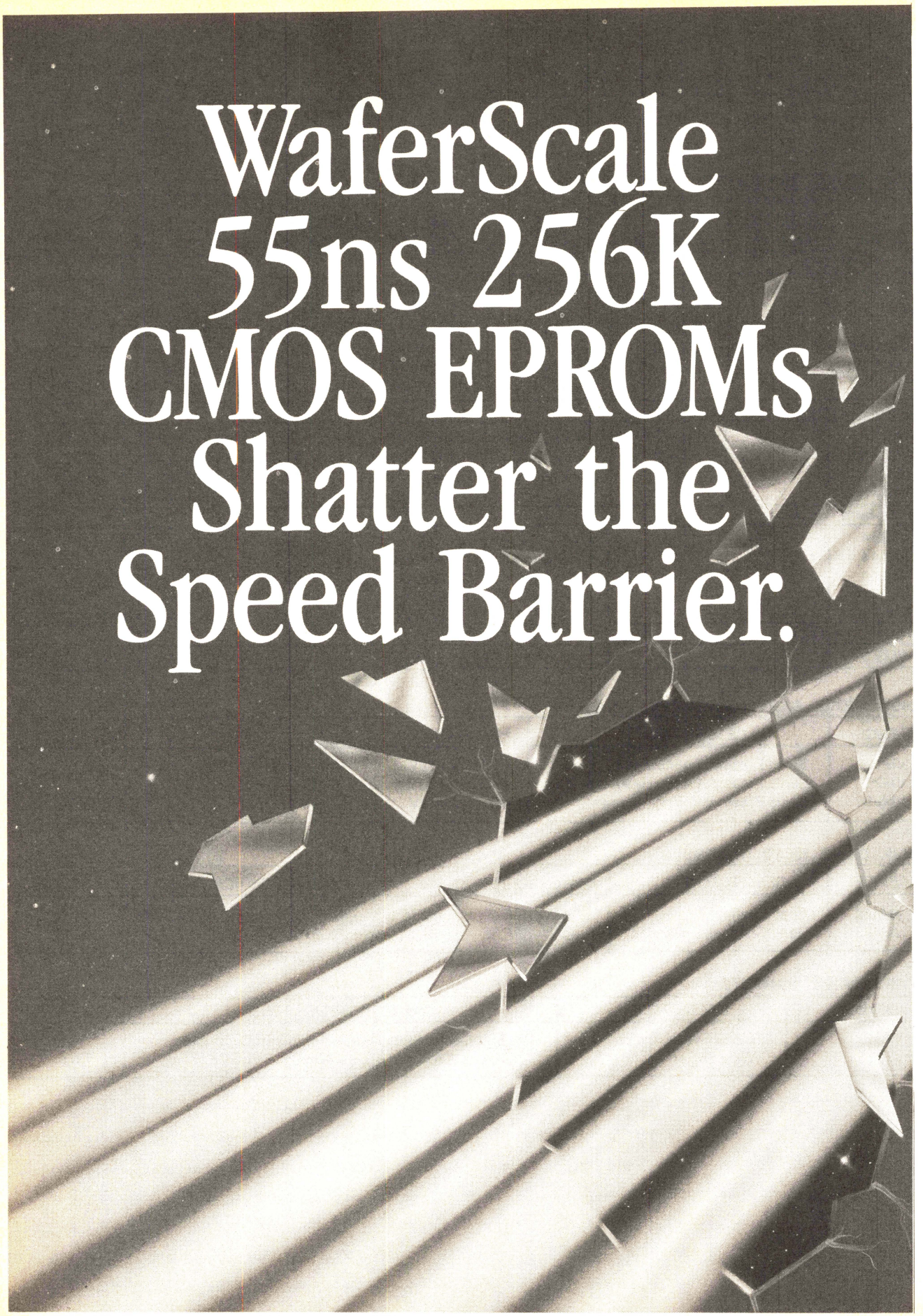
## DISK DRIVE READ CHANNELS

| DEVICE | DESCRIPTION | POWER SUPPLY | CHARACTERISTICS | PACKAGE |
|---|---|---|---|---|
| VM442 | Read Channel | +5V,+12V | MFM, BW = 12MHz, TTL to ECL Write Switch | P, PL |
| VM443 | Read Channel, Enhanced | +5V,+12V | RLL Compatible, BW = 30MHz | P,PL |

## TAPE DRIVE CIRCUITS

| DEVICE | DESCRIPTION | CHARACTERISTICS | PACKAGE |
|---|---|---|---|
| VT210 | Clock Synchronizer | Max Center Frequency = 2MHz, TTL Compatible | D |
| VT211 | Write Driver | $I_{WC}$ = 70mA ph, $I_{BIAS}$ = 40mA | D |

VTC Incorporated





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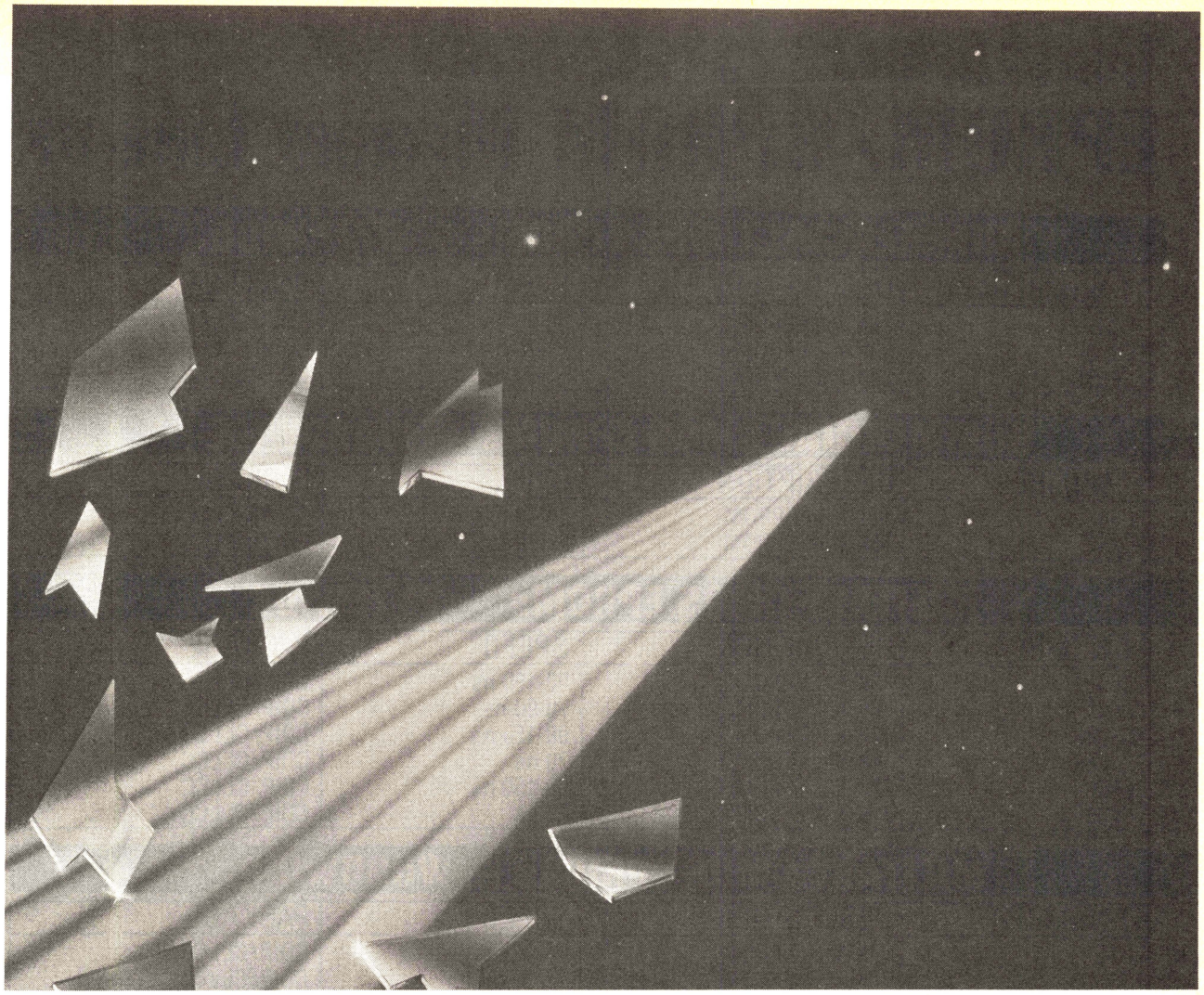

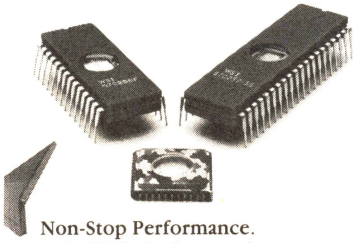

**Non-Stop Performance.**
Only WaferScale can take your high-performance MPU, microcontroller, or DSP processor past the conventional speed limitations of standard EPROMs. With a line-up of high-density CMOS EPROMs that make wait-states a thing of the past.

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**32K x 8 in 55 ns.**
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**16K x 16 in 55 ns.**
Designed for 16-bit, word-wide DSP and microprocessor applications, WSI's 16K x 16 CMOS EPROM (WS57C257) packs high performance and low power into less board space.

**32K x 8 goes Mil-Spec in 90 ns.**
WSI's very-low-power military 32K x 8 CMOS EPROM (WS27C256F) provides 90 ns access time over the full military temperature range, and fast standard CMOS EPROM programming.

In fact, WSI offers the broadest, fastest family of high-performance military CMOS EPROMS available. Every WSI CMOS EPROM can be specified for enlistment in military applications from advanced warning systems to secure digital communications. And WSI mil-spec devices are available in DIP or space-saving CLLCC packages.

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Whether you're piloting commercial or mil-spec, WSI can take your design through the performance barrier with the fastest fleet of high-performance CMOS EPROMs around. To find out more, call today: **800/331-1030, extension 234.**
In California, call:
**800/323-3939, extension 234.**

**Selected WSI High-Performance EPROMs/RPROMs™**

| Part No. | Commercial Speed | Military Speed | Type |
|---|---|---|---|
| WS57C256F | 55 ns | 70 ns | 32K x 8 CMOS EPROM |
| WS57C257 | 55 ns | 70 ns | 16K x 16 CMOS EPROM |
| WS27C256F | 90 ns | 90 ns | 32K x 8 CMOS EPROM |
| WS57C65 | 55 ns | 70 ns | 4K x 16 CMOS EPROM |
| WS57C64F | 55 ns | 70 ns | 8K x 8 CMOS EPROM |
| WS57C49 | 55 ns | 70 ns | 8K x 8 CMOS RPROM |
| WS57C49B | 35 ns | 45 ns | 8K x 8 CMOS RPROM |
| WS57C43 | 55 ns | 70 ns | 4K x 8 CMOS RPROM |
| WS57C191/291 | 45 ns | 50 ns | 2K x 8 CMOS RPROM |

WaferScale INTEGRATION, INC.

47280 Kato Road
Fremont, California 94538
(415) 656-5400

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# WAFERSCALE INTEGRATION
# EPROM/RPROM MEMORY LINE-UP

## COMMERCIAL CMOS EPROMs — BYTEWIDE

| PART NUMBER | DESCRIPTION | SPEED | PACKAGE |
|---|---|---|---|
| WS57C64F | 8K X 8 EPROM | 55-70 ns | CDIP/CLLCC |
| WS57C128F | 16K X 8 EPROM | 55-70 ns | CDIP/CLLCC |
| WS57C256F | 32K X 8 EPROM | 55-70 ns | CDIP/CLLCC |

## COMMERCIAL CMOS EPROMs — WORDWIDE

| PART NUMBER | DESCRIPTION | SPEED | PACKAGE |
|---|---|---|---|
| WS57C65 | 4K X 16 EPROM | 55-70 ns | CDIP/CLLCC |
| WS57C257 | 16K X 16 EPROM | 55-70 ns | CDIP/CLLCC |

## MILITARY CMOS EPROMs — BYTEWIDE

| PART NUMBER | DESCRIPTION | SPEED | PACKAGE |
|---|---|---|---|
| WS27C64F | 8K X 8 EPROM | 90-150 ns | CDIP/CLLCC |
| WS57C64F | 8K X 8 EPROM | 70-90 ns | CDIP/CLLCC |
| WS27C128F | 16K X 8 EPROM | 90-150 ns | CDIP/CLLCC |
| WS57C128F | 16K X 8 EPROM | 70 ns | CDIP/CLLCC |
| WS27C256F | 32K X 8 EPROM | 90-150 ns | CDIP/CLLCC |
| WS57C256F | 32K X 8 EPROM | 70 ns | CDIP/CLLCC |

## MILITARY CMOS EPROMs — WORDWIDE

| PART NUMBER | DESCRIPTION | SPEED | PACKAGE |
|---|---|---|---|
| WS57C65 | 4K X 16 EPROM | 70-90 ns | CDIP/CLLCC |
| WS57C257 | 16K X 16 EPROM | 70-90 ns | CDIP/CLLCC |

## COMMERCIAL CMOS RPROMs

| PART NUMBER | DESCRIPTION | SPEED | PACKAGE |
|---|---|---|---|
| WS57C191 | 2K X 8 RPROM | 45-55 ns | CDIP/CLLCC |
| WS57C291 | 2K X 8 RPROM | 45-55 ns | CDIP/CLLCC |
| WS57C43 | 4K X 8 RPROM | 55-70 ns | CDIP/SBRZD/CLLCC |
| WS57C43B | 4K X 8 RPROM | 35-45 ns | CDIP/CLLCC |
| WS57C49 | 8K X 8 RPROM | 55-70 ns | CDIP/CLLCC |
| WS57C49B | 8K X 8 RPROM | 35-45 ns | CDIP/CLLCC |
| WS57C51 | 16K X 8 RPROM | 70-90 ns | CDIP/CLLCC |
| WS57C51B | 16K X 8 RPROM | 40-55 ns | CDIP/CLLCC |

## MILITARY CMOS RPROMs

| PART NUMBER | DESCRIPTION | SPEED | PACKAGE |
|---|---|---|---|
| WS57C191 | 2K X 8 RPROM | 50-55 ns | CDIP/CLLCC |
| WS57C291 | 2K X 8 RPROM | 50-55 ns | CDIP/CLLCC |
| WS57C43 | 4K X 8 RPROM | 70 ns | CDIP/CLLCC |
| WS57C43B | 4K X 8 RPROM | 45-55 ns | CDIP/CLLCC |
| WS57C49 | 8K X 8 RPROM | 70-90 ns | CDIP/CLLCC |
| WS57C49B | 8K X 8 RPROM | 45-55 ns | CDIP/CLLCC |
| WS57C51 | 16K X 8 RPROM | 70-90 ns | CDIP/CLLCC |
| WS57C51B | 16K X 8 RPROM | 45-55 ns | CDIP/CLLCC |





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# HIGH SPEED BIT-SLICE LINE-UP

| PART NUMBER | SPEED | PRODUCT TYPE |
|---|---|---|
| WS5901 | 43 MHz | 4 Bit CMOS Bit Slice Processor |
| WS59016 | 32 MHz | 16 Bit CMOS Bit Slice Processor |
| WS59032 | 25 MHz | 32 Bit CMOS Bit Slice Processor |
| WS5910A/B | 30 MHz | Microprogram Controller |
| WS59520/21 | 45 MHz | Variable Pipeline |
| WS59510 | 30 ns | 16 x 16 Multiplier/Accumulator |
| WS59820 | 50 MHz | Bi-Directional Bus Interface Register |

# CROSS REFERENCE

## AMD

| AMD | WSI |
|---|---|
| AM27S191 | WS57C191 |
| AM27PS191 | WS57C191 |
| AM27S291 | WS57C291 |
| AM27PS191 | WS57C291 |
| AM27S43 | WS57C43 |
| AM27PS43 | WS57C43 |
| AM27S49 | WS57C49 |
| AM2901 | WS5901 |
| AM2910A | WS5910A |
| AM29520 | WS59520 |
| AM29521 | WS59521 |
| AM29C101 | WS59016* |
| AM29510 | WS59510 |

## ATMEL

| ATMEL | WSI |
|---|---|
| 27HC64 | WS57C64F |
| 27HC641 | WS57C49 |

## CYPRESS

| CYPRESS | WSI |
|---|---|
| CY7C291 | WS57C191 |
| CY7C292 | WS57C291 |
| CY7C264 | WS57C49 |
| CY7C901 | WS5901 |
| CY7C910 | WS5910A |
| CY7C9101 | WS59016* |
| CY7C510 | WS59610 |

*Functional Equivalent

## FAIRCHILD

| FSC | WSI |
|---|---|
| 93Z511 | WS57C191 |
| 93Z565 | WS57C49 |
| 29F01 | WS5901 |
| 29F10 | WS5910A |

## FUJITSU

| FUJITSU | WSI |
|---|---|
| MB7138 | WS57C191 |
| MB7138-SK | WS57C291 |
| MB7142 | WS57C43 |
| MB7144 | WS57C49 |

## G.I.

| G.I. | WSI |
|---|---|
| 27HC64 | WS57C64F |
| 27HC641 | WS57C49 |

## HARRIS

| HARRIS | WSI |
|---|---|
| HM-76161 | WS57C191 |
| HM-76321 | WS57C43 |
| HM-76641 | WS57C49 |

## IDT

| IDT | WSI |
|---|---|
| IDT39C01 | WS5901 |
| IDT39C10 | WS5910A |
| IDT49C401 | WS59016* |
| IDT7210 | WS59510 |

## LDI

| LDI | WSI |
|---|---|
| L29C520 | WS59520 |
| L29C521 | WS59521 |

## MMI

| MMI | WSI |
|---|---|
| 63S1681 | WS57C191 |
| 63S3281 | WS57C43 |

## NATIONAL

| NATIONAL | WSI |
|---|---|
| DM87S191 | WS57C191 |
| DM87S291 | WS57C291 |
| DM87S321 | WS57C43 |

## SIGNETICS

| SIGNETICS | WSI |
|---|---|
| N82S191 | WS57C191 |
| N82S191__-3 | WS57C291 |
| N82S321 | WS57C43 |
| N82HS321 | WS57C43 |
| N82HS641 | WS57C49 |

## T.I.

| T.I. | WSI |
|---|---|
| TBP38S166__W | WS57C191 |
| TBP38L166__W | WS57C191 |
| TBP38SA166__W | WS57C191 |
| TBP38S166__T | WS57C291 |
| TBP38L166__T | WS57C291 |
| TBP38SA166__T | WS57C291 |

# MILITARY ONLY

## AMD

| AMD | WSI |
|---|---|
| AM2764 | WS27C64F |
| AM27128 | WS27C128F |
| AM27256 | WS27C256F |

## INTEL

| INTEL | WSI |
|---|---|
| M2764 | WS27C64F |
| M27128 | WS27C128F |
| M27256 | WS27C256F |
| M27C64 | WS27C64F |
| M27C128 | WS27C128F |
| M27C256 | WS27C256C |

Waferscale Integration


Waferscale INTEGRATION, INC.

47280 Kato Road
Fremont, California 94538-7333
800-TEAM-WSI
415-656-5400
Telex: 289255
Facsimile 415-657-8495

# WD20C03A
# Data Encryption Device

## FEATURES

- CERTIFIED BY NATIONAL BUREAU OF STANDARDS
- TRANSFER RATE:
  UP TO 3.22 MBS WITH 5 MHZ CLOCK
  UP TO 5.10 MBS WITH 8 MHZ CLOCK
  UP TO 8.10 MBS WITH 10 MHZ CLOCK
- ENCRYPTS/DECRYPTS 64-BIT DATA WORDS USING 56-BIT KEY WORD
- ECB – ELECTRONIC CODE BOOK
  CBC – CIPHER BLOCK CHAINING
- SINGLE PORT 28-PIN PACKAGE
- COMMAND BIT PROGRAMMING VIA DAL BUS OR INPUT PINS
- PARITY CHECK ON KEY WORD LOADING
- STANDARD 8-BIT MICROPROCESSOR INTERFACE
- KEY STORED ON CHIP IS NOT EXTERNALLY ACCESSIBLE
- BATTERY BACK-UP MODE OF INTERNAL REGISTERS

## APPLICATIONS

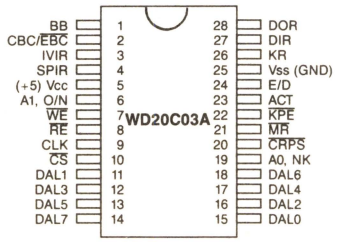
- SECURE BROKERAGE TRANSACTIONS
- ELECTRONIC FUNDS TRANSFERS
- SECURE BANKING/BUSINESS ACCOUNTING
- MAINFRAME COMMUNICATIONS
- REMOTE AND HOST COMPUTER COMMUNICATIONS

## DESCRIPTION

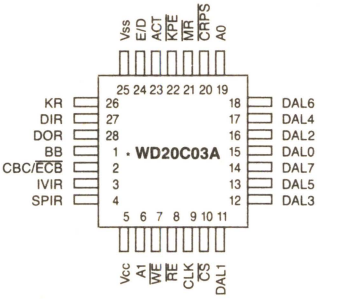
The Western Digital WD20C03A Data Encryption/Decryption device is designed to encrypt and decrypt 64-Bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard (#46). This device encrypts a 64-Bit clear text word using a 56-Bit, user-specified key to produce a 64-Bit cipher text word. When reversed, the cipher text word is decrypted to produce the original clear text word.

The WD20C03A is fabricated using silicon gate, CMOS technology. All inputs and outputs are TTL compatible in all devices.

NOTE: This device cannot be shipped outside of the United States of America without authorization from the State Department and the Department of Defense.




**WD20C03A**
**PIN DESIGNATION (DIP)**




**WD20C03A**
**PIN DESIGNATION (QUAD)**

Western Digital

Product specifications subject to change without notice.

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Western Digital
2445 McCabe Way
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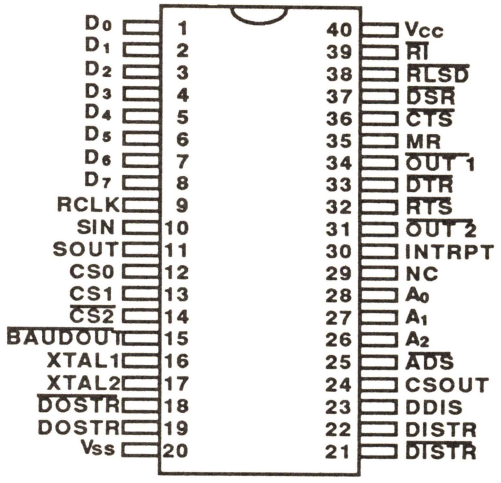
# WESTERN DIGITAL
CORPORATION

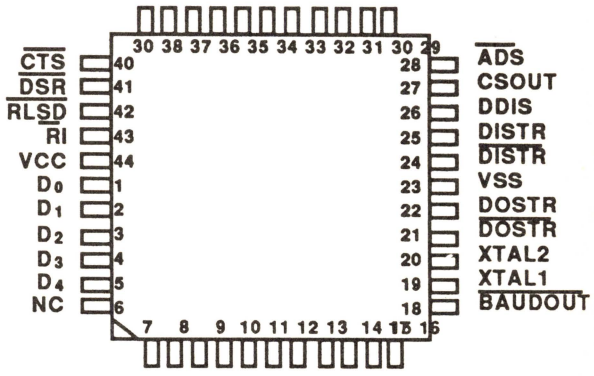
# WD8250/82C50/16C450 ASYNCHRONOUS COMMUNICATIONS ELEMENT (ACE)

## FEATURES

- Designed to be easily interfaced to most microprocessors (Z-80, 8088, 68000, etc.)
- Generating and stripping of Serial Async Control Bits (start, stop, parity)
- Full double buffering allows imprecise synchronization
- Independently controlled Transmit, Receive, Line Status, and data set Interrupts
- Programmable Baud Rate Generator allows division of any input Clock by 1 to ($2^{16}$-1) and generates the internal 16X Clock.
- Independent Receiver Clock input
- Modem interface capabilities
- Fully programmable Serial-Interface characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Rate Generation (DC to 56K Baud)**
- False Start Bit detector
- Complete status reporting capabilities
- Three-State TTL drive capabilities for bi-directional Data and Control bus
- Line break Generation and Detection
- Internal Diagnostic capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, and Framing Error Simulation
- Full prioritized interrupt system controls
- Single +5 Volt Power Supply
- Low CMOS Power Dissipation




PIN DESIGNATION (DIP)




PIN DESIGNATION (Quad) *

## DESCRIPTION

The WD8250/82C50/16C450 is a programmable Asynchonous Communication Element (ACE) in a 40-pin DIP or 44-pin Quad package. The device is fabricated in NMOS (WD8250) and CMOS (WD82C50 & WD16C450) silicon gate technology.

The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side and to convert serial data to a parallel format on the receive side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The recommended data rate is 56K baud.*

Internal register enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable Baud Rate Generator that is capable of dividing an internal XTAL or TTL signal clock by a division of up to $2^{16}$-1.

The ACE is designated to work in either a polling or interrupt driven system, which is programmable by users' software controlling an internal register.

* Contact WD Sales Office for other Pin Outs.

** Contact WD Sales Office for exceeding this recommended maximum baud rate.

Western Digital

# WD1935A Synchronous Data Link Controller

## FEATURES

- OFFERS COMPATIBILITY WITH MANY CURRENT COMMUNICATIONS STANDARDS, SUCH AS HDLC, SDLC, ADCCP, CCITT X.25 AND ISDN
- INCLUDES SDLC LOOP DATA LINK CAPABILITY
- PROVIDES DATA TRANSMISSION SPEEDS TO 4.0 MBPS
- ALLOWS ERROR CHECKING FOR CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS
- CONTAINS EXTENDABLE ADDRESS/CONTROL FIELD
- PERFORMS AUTOMATIC ZERO INSERTION AND DELETION
- USES SINGLE +5 VOLT POWER SOURCE
- 40 PIN DUAL-IN-LINE OR LEADED CHIP CARRIER FOR SMT
- PROVIDES ENHANCED DMA CAPABILITY/EOB OPTION
- ALLOWS VARIABLE CHARACTER LENGTH AND RESIDUAL CHARACTER CAPABILITY
- OFFERS PROGRAMMABLE MODEM CONTROL INTERRUPTS AND NRZI ENCODE/DECODE

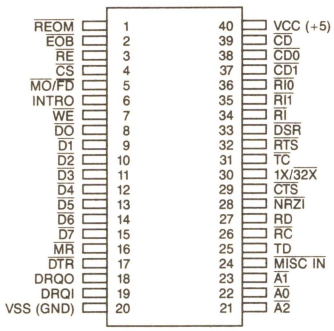
## DESCRIPTION

The WD1935A is a programmable Synchronous Data Link Controller that facilitates the easy design of interfaces between a parallel digital system and a serial data communication channel and vice versa. This controller is capable of full and half duplex operation and is particularly suited to high speed applications.

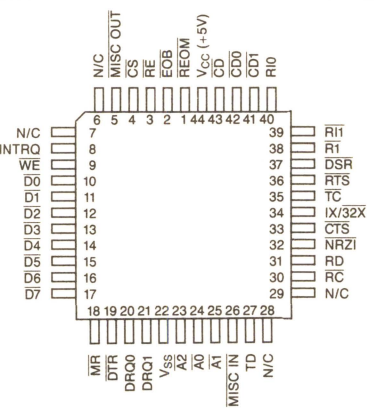
The 1935A is an NMOS/LSI device designed for bit-oriented SDLC, HDLC and other bit synchronous protocols. It is designed to be particularly efficient when used in DMA applications.

Applications include: computer to terminal communications, computer to modem interfacing, front end communications, message and packet switching, protocol converters, and communication test equipment.

The WD1935A is compatible with most eight bit microcomputers and can be connected directly to a microcomputer bus.




**WD1935A**
**PIN DESIGNATION (DIP)**




**WD1935A**
**PIN DESIGNATION (QUAD)**

Product specifications subject to change without notice.

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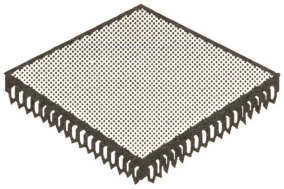
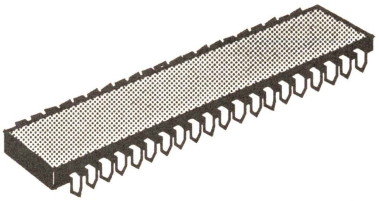
# StarLAN HUB CONTROLLERS

**WD83C503**



**StarLAN Mini-Hub Controller**

**WD83C510A**

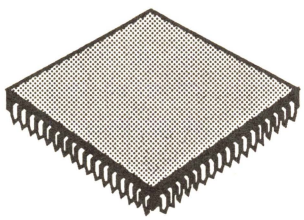


**StarLAN Hub Controller**

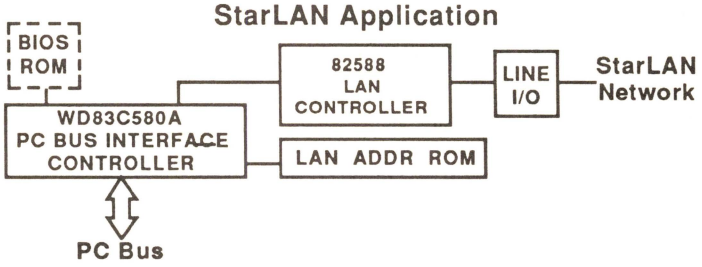
## FEATURES

| | WD83C503 | WD83C510A |
|---|---|---|
| • IEEE 802.3 1BASE5 StarLAN Compatible | X | X |
| • 1 MBPS Manchester Signal Regeneration | X | X |
| • Supports Hub Inputs | 3 | 10 |
| • Adds Hub Functions to StarLAN Station Adapters | X | |
| • Economical Repeater For StarLAN Network Extension | X | |
| • Cascadable For Larger Hubs Up To 40 Ports | | X |
| • Allows 10 Hub Levels | X | X |
| • Automatic Detection Of Upper-Level Hub Presence | X | X |
| • Collision Detection And Signalling | X | X |
| • Ancillary Collision Detection Circuitry Input | X | X |
| • Carrier Sense Function | X | X |
| • Jabber Detection And Inhibit | X | X |
| • Built-In Network Diagnostic Functions | X | X |
| • Packaging | 44-Pin PLCC | 40-Pin DIP<br>44-Pin PLCC |
| • 5-Volt CMOS Technology | X | X |

**WD83C580A**



**StarLAN Application**




## FEATURES

- Handles PC Interrupt, DMA Functions And Data Bus Control For StarLAN Adapters
- Handles 82588 LAN Controller Interrupt, DMA, Chip Select And Reset
- Handles 82586 LAN Controller Interrupt, Channel Attention and Reset
- Supports BIOS ROM And LAN Address ROM
- Software-Controlled Wait State Insertion For PC Data Bus
- Handles Jumpers For I/O Base Address And DMA Configuration
- Internal Control And Status Register
- Integrates Typical SSI/MSI PC Bus Interface Logic
- 5-Volt CMOS Technology In 68-Pin PLCC

CM100/jlb

Western Digital

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## WD25C17 Enhanced Synchronous Data Link Controller

### FEATURES:

- HDLC, SDLC, ADCCP, CCITT X.25, ISDN LAPD and SS7 capability
- Advanced CMOS technology
- SDLC loop mode capability
- Full/half duplex operation
- Up to 4.0 Mbps serial data rate
- Supports up to 8 logical channels for LAPD operation
- Programmable station address filtering
- Two receiver DMA channels and one transmitter DMA channel
- 8/16 bit DMA data bus to the memory buffer
- Two internal timers (T1 and T2)
- Programmable NRZI Encode/Decode option
- Digital Phase Locked Loop
- Full set of modem control signals
- Optional PCM Highway Interface supports from 32 to 128 time slots
- Programmable 16 Kbps rate adaption when used in PCM Interface Mode
- Up to 8K buffer length
- FLAG, ABORT and IDLE generation and detection
- Automatic FCS generation and checking
- Automatic Zero insertion and deletion
- Error detection on FCS error, transmitter underrun, receiver overrun, frame aborted and invalid frame (non-byte data and buffer length error)
- Generic CPU Host Interface
- Maintenance mode for self-testing
- TTL compatible I/O
- 68-pin package

### APPLICATIONS:

- PBX and Central Offices switches
- Computer communications
- Terminal communications (POS, Teletex, Videotex, G IV FAX, etc.)
- Computer to modem interfacing
- Line controllers
- Front end communications
- Network processors
- Telecommunication switching networks
- Packet switching
- Data concentrators/Multiplexers
- Multidrop line systems
- Protocol converters/gateways

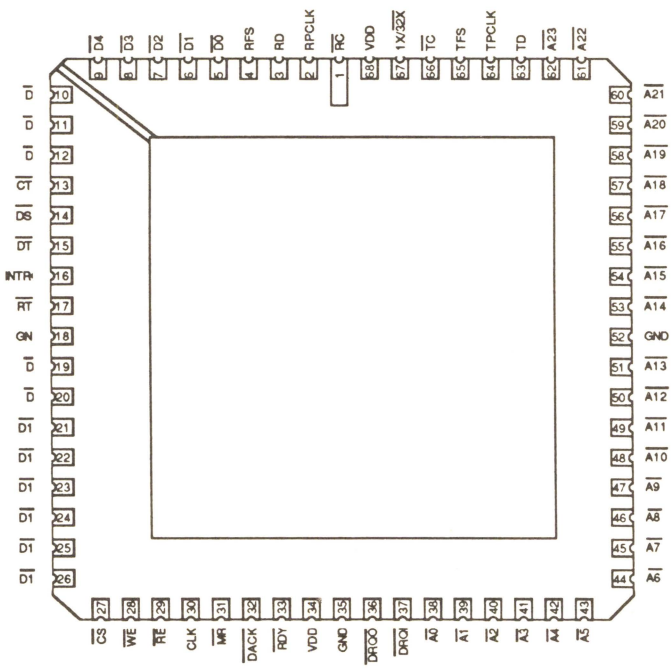


FIGURE 1: WD25C17 PIN DESIGNATION

CM116/7LB

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# WD2512/2511A
# X.25 Link Level Controllers

## FEATURES

### Managing the Communication Link

- HANDLES THE ENTIRE LINK LEVEL PROTOCOL OF CCITT X.25
- PROGRAMMABLE TIME OUT AND RETRANSMISSION PARAMETERS
- AUTOMATIC ERROR DETECTION AND DATA RETRANSMISSION
- AUTOMATIC FLOW CONTROL
- AUTOMATIC HANDLING OF ALL ADDRESS AND CONTROL FIELDS
- THE 2512 IS COMPATIBLE WITH THE 2511A
- BUILT-IN LOOPBACK TESTING
- CAN OPERATE AS A LAPB HALF-DUPLEX STATION

### VLSI Design Provides Top Performance

- THE 2512 HAS TRANSMISSION SPEEDS AVAILABLE TO 2.048 MP/S
- THE 2511A HAS TRANSMISSION SPEEDS TO 1.1 MBPS
- BUILT-IN DUAL CHANNEL DMA
- ON CHIP BUFFER MANAGEMENT
- AVAILABLE IN 48-PIN DIP AND 68-PIN PLCC

### WD2512 Extras

- SINGLE +5V SUPPLY
- LOWER POWER CONSUMPTION
- ENHANCED TO MEET THE DCNA GROUP IV FACSIMILE STANDARD FOR THE JAPANESE INS NETWORK

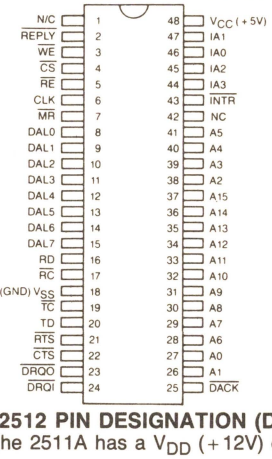
## DESCRIPTION

The 2512 link level controller provides a low cost solution for managing data communication links for CCITT X.25, Group IV FAX, and teletex equipment. This controller was especially designed for packet switching networks. The design was based on a proven and certified implementation, the 2511A, the first complete implementation of the CCITT Recommendation X.25 LAPB protocol in a chip.

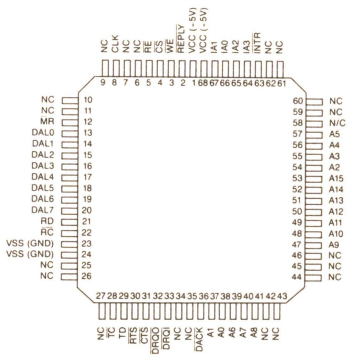
The 2512 is a NMOS LSI device which provides a unique solution for point-to-point communications.

It offloads the host by implementing the full link-layer protocol of the international standard recommendation X.25. This bit oriented, serial link controller automatically handles the transmission and reception of packets of data on two internal DMA channels, acknowledges the receipts of error free packets, and requests that lost or erroneous packets be retransmitted.

The host is interrupted after receiving an error free packet, after receiving acknowledgement of a transmitted packet, and after detecting certain error or abnormal conditions on the link.




**WD2512 PIN DESIGNATION (DIP)**
(Pin 42 on the 2511A has a $V_{DD}$ (+12V) connection)




**WD2512 PIN DESIGNATION (QUAD)**
(for 2511A pin-out, contact WD)

Product specifications subject to change without notice.

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# Reference Guide to Xicor Nonvolatile Memories

**NOVRAMs***

| Part Number | Organization | Access Time | Power | | Store Cycles | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Active | Standby | | | | P | J | D | E | G | C | | |
| X2201A | 1024 x 1 | 300 ns | 60 mA | N/A | 10,000 | 18 | † | | | • | | | | 1-1 | 9-1 |
| X2210 | 64 x 4 | 300 ns | 50 mA | N/A | 10,000 | 18 | † | • | | • | | | | 1-9 | 9-1 |
| X2210/5 | 64 x 4 | 300 ns | 50 mA | N/A | 10,000 | 18 | † | • | | • | | | | 1-9 | 9-1 |
| X2210/10 | 64 x 4 | 300 ns | 50 mA | N/A | 10,000 | 18 | † | • | | • | | | | 1-9 | 9-1 |
| X2210I | 64 x 4 | 300 ns | 55 mA | N/A | 10,000 | 18 | I | • | | • | | | | 1-9 | 9-1 |
| X2210I/5 | 64 x 4 | 300 ns | 55 mA | N/A | 10,000 | 18 | I | • | | • | | | | 1-9 | 9-1 |
| X2210I/10 | 64 x 4 | 300 ns | 55 mA | N/A | 10,000 | 18 | I | • | | • | | | | 1-9 | 9-1 |
| X2210M | 64 x 4 | 300 ns | 55 mA | N/A | 10,000 | 18 | M | | | • | | | | 1-17 | 9-1 |
| X2210M/5 | 64 x 4 | 300 ns | 55 mA | N/A | 10,000 | 18 | M | | | • | | | | 1-17 | 9-1 |
| X2210M/10 | 64 x 4 | 300 ns | 55 mA | N/A | 10,000 | 18 | M | | | • | | | | 1-17 | 9-1 |
| X2212 | 256 x 4 | 300 ns | 60 mA | N/A | 10,000 | 18 | † | • | | • | | | | 1-25 | 9-2 |
| X2212/5 | 256 x 4 | 300 ns | 60 mA | N/A | 10,000 | 18 | † | • | | • | | | | 1-25 | 9-1 |
| X2212/10 | 256 x 4 | 300 ns | 60 mA | N/A | 10,000 | 18 | † | • | | • | | | | 1-25 | 9-1 |
| X2212I | 256 x 4 | 300 ns | 70 mA | N/A | 10,000 | 18 | I | • | | • | | | | 1-25 | 9-2 |
| X2212I/5 | 256 x 4 | 300 ns | 70 mA | N/A | 10,000 | 18 | I | • | | • | | | | 1-25 | 9-2 |
| X2212I/10 | 256 x 4 | 300 ns | 70 mA | N/A | 10,000 | 18 | I | • | | • | | | | 1-25 | 9-2 |
| X2212M | 256 x 4 | 300 ns | 70 mA | N/A | 10,000 | 18 | M | | | • | | | | 1-33 | 9-2 |
| X2212M/5 | 256 x 4 | 300 ns | 70 mA | N/A | 10,000 | 18 | M | | | • | | | | 1-33 | 9-2 |
| X2212M/10 | 256 x 4 | 300 ns | 70 mA | N/A | 10,000 | 18 | M | | | • | | | | 1-33 | 9-2 |

N/A = Not Applicable

**Key:**
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

P = Plastic DIP
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
D = Cerdip
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
C = Side Braze

*NOVRAM is Xicor's nonvolatile static RAM device.




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# Reference Guide to Xicor Nonvolatile Memories

**NOVRAMs (Byte-Wide)**

| Part Number | Organization | Access Time | Power | | Store Cycles | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Active | Standby | | | | P | J | D | E | G | C | | |
| X2001-20 | 128 x 8 | 200 ns | 80 mA | 50 mA | 100,000 | 24 | † | • | | • | | | | 1-41 | 9-3 |
| X2001-25 | 128 x 8 | 250 ns | 80 mA | 50 mA | 100,000 | 24 | † | • | | • | | | | 1-41 | 9-3 |
| X2001 | 128 x 8 | 300 ns | 80 mA | 50 mA | 100,000 | 24 | † | • | | • | | | | 1-41 | 9-3 |
| X2001I-20 | 128 x 8 | 200 ns | 100 mA | 65 mA | 100,000 | 24 | I | • | | • | | | | 1-41 | 9-3 |
| X2001I-25 | 128 x 8 | 250 ns | 100 mA | 65 mA | 100,000 | 24 | I | • | | • | | | | 1-41 | 9-3 |
| X2001I | 128 x 8 | 300 ns | 100 mA | 65 mA | 100,000 | 24 | I | • | | • | | | | 1-41 | 9-3 |
| X2004-20 | 512 x 8 | 200 ns | 100 mA | 55 mA | 100,000 | 28 | † | | • | • | • | | | 1-51 | 9-3 |
| X2004-25 | 512 x 8 | 250 ns | 100 mA | 55 mA | 100,000 | 28 | † | | • | • | • | | | 1-51 | 9-3 |
| X2004 | 512 x 8 | 300 ns | 100 mA | 55 mA | 100,000 | 28 | † | | • | • | • | | | 1-51 | 9-3 |
| X2004I-20 | 512 x 8 | 200 ns | 120 mA | 90 mA | 100,000 | 28 | I | | • | • | • | | | 1-51 | 9-3 |
| X2004I-25 | 512 x 8 | 250 ns | 120 mA | 90 mA | 100,000 | 28 | I | | • | • | • | | | 1-51 | 9-3 |
| X2004I | 512 x 8 | 300 ns | 120 mA | 90 mA | 100,000 | 28 | I | | • | • | • | | | 1-51 | 9-3 |
| X2004M-20 | 512 x 8 | 200 ns | 120 mA | 90 mA | 100,000 | 28 | M | | | • | • | | | 1-61 | 9-3 |
| X2004M-25 | 512 x 8 | 250 ns | 120 mA | 90 mA | 100,000 | 28 | M | | | • | • | | | 1-61 | 9-3 |
| X2004M | 512 x 8 | 300 ns | 120 mA | 90 mA | 100,000 | 28 | M | | | • | • | | | 1-61 | 9-3 |

**Key:**

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

P = Plastic DIP
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
D = Cerdip
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
C = Side Braze

# Reference Guide to Xicor Nonvolatile Memories

## SERIAL NOVRAMs

| Part Number | Organization | CLK Frequency | Power | | | Store Cycles | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Active | Standby | Sleep | | | | P | J | D | E | G | C | | |
| X2444 | 16 x 16 | 1 MHz | 15 mA | 10 mA | 7 mA | 100,000 | 8 | † | • | | | | | | 2-1 | 9-5 |
| X2444I | 16 x 16 | 1 MHz | 25 mA | 15 mA | 10 mA | 100,000 | 8 | I | • | | | | | | 2-1 | 9-5 |
| X2444M | 16 x 16 | 1 MHz | 25 mA | 15 mA | 10 mA | 100,000 | 8 | M | • | | | | | | 2-11 | 9-5 |

## SERIAL E²PROMs

| Part Number | Organization | Page Size (# Bytes) | CLK Frequency | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X2402 | 256 x 8 | 8 | 100 KHz | 30 mA | 25 mA | 8 | † | • | | | | | | 2-21 | 9-5 |
| X2402I | 256 x 8 | 8 | 100 KHz | 35 mA | 30 mA | 8 | I | • | | | | | | 2-21 | 9-5 |
| X2404 | 512 x 8 | 8 | 100 KHz | 30 mA | 25 mA | 8 | † | • | | • | | | | 2-31 | 9-5 |
| X2404I | 512 x 8 | 8 | 100 KHz | 35 mA | 30 mA | 8 | I | • | | • | | | | 2-31 | 9-5 |
| X2404M | 512 x 8 | 8 | 100 KHz | 35 mA | 30 mA | 8 | M | • | | • | | | | 2-41 | 9-5 |
| X24C04 | 512 x 8 | 16 | 100 KHz | 2 mA | 60 μA | 8 | † | • | | | | | | 2-51 | 9-5 |
| X24C04I | 512 x 8 | 16 | 100 KHz | 2 mA | 60 μA | 8 | I | • | | | | | | 2-51 | 9-5 |
| X24C16 | 2048 x 8 | 16 | 100 KHz | 3 mA | 75 μA | 8 | † | • | | • | | | | 2-61 | 9-5 |
| X24C16I | 2048 x 8 | 16 | 100 KHz | 3 mA | 75 μA | 8 | I | • | | • | | | | 2-61 | 9-5 |
| X24C16M | 2048 x 8 | 16 | 100 KHz | 3 mA | 75 μA | 8 | M | • | | • | | | | 2-71 | 9-5 |

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J = 32-Lead J-Hook Plastic Leaded Chip Carrier
D = Cerdip
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
C = Side Braze




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## 4K E²PROMs

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X2804A-25 | 512 x 8 | N/A | 250 ns | 80 mA | 50 mA | 24 | † | • | | • | | | | 3-1 | 9-6 |
| X2804A | 512 x 8 | N/A | 300 ns | 80 mA | 50 mA | 24 | † | • | | • | | | | 3-1 | 9-6 |
| X2804A-35 | 512 x 8 | N/A | 350 ns | 80 mA | 50 mA | 24 | † | • | | • | | | | 3-1 | 9-6 |
| X2804A-45 | 512 x 8 | N/A | 450 ns | 80 mA | 50 mA | 24 | † | • | | • | | | | 3-1 | 9-6 |
| X2804AI-25 | 512 x 8 | N/A | 250 ns | 100 mA | 60 mA | 24 | I | • | | • | | | | 3-1 | 9-6 |
| X2804AI | 512 x 8 | N/A | 300 ns | 100 mA | 60 mA | 24 | I | • | | • | | | | 3-1 | 9-6 |
| X2804AI-35 | 512 x 8 | N/A | 350 ns | 100 mA | 60 mA | 24 | I | • | | • | | | | 3-1 | 9-6 |
| X2804AI-45 | 512 x 8 | N/A | 450 ns | 100 mA | 60 mA | 24 | I | • | | • | | | | 3-1 | 9-6 |
| X2804AM | 512 x 8 | N/A | 300 ns | 100 mA | 60 mA | 24 | M | • | | • | | | | 3-9 | 9-6 |
| X2804AM-35 | 512 x 8 | N/A | 350 ns | 100 mA | 60 mA | 24 | M | • | | • | | | | 3-9 | 9-6 |
| X2804AM-45 | 512 x 8 | N/A | 450 ns | 100 mA | 60 mA | 24 | M | • | | • | | | | 3-9 | 9-6 |

N/A = Not Applicable

**Key:**
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
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D = Cerdip
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G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
C = Side Braze



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### 16K E²PROMs

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X2816A-25 | 2048 x 8 | N/A | 250 ns | 110 mA | 50 mA | 24 | † | • | | • | • | | | 3-19 | 9-7 |
| X2816A | 2048 x 8 | N/A | 300 ns | 110 mA | 50 mA | 24 | † | • | | • | • | | | 3-19 | 9-7 |
| X2816A-35 | 2048 x 8 | N/A | 350 ns | 110 mA | 50 mA | 24 | † | • | | • | • | | | 3-19 | 9-7 |
| X2816A-45 | 2048 x 8 | N/A | 450 ns | 110 mA | 50 mA | 24 | † | • | | • | • | | | 3-19 | 9-7 |
| X2816AI-25 | 2048 x 8 | N/A | 250 ns | 140 mA | 60 mA | 24 | I | • | | • | • | | | 3-19 | 9-7 |
| X2816AI | 2048 x 8 | N/A | 300 ns | 140 mA | 60 mA | 24 | I | • | | • | • | | | 3-19 | 9-7 |
| X2816AI-35 | 2048 x 8 | N/A | 350 ns | 140 mA | 60 mA | 24 | I | • | | • | • | | | 3-19 | 9-7 |
| X2816AI-45 | 2048 x 8 | N/A | 450 ns | 140 mA | 60 mA | 24 | I | • | | • | • | | | 3-19 | 9-7 |
| X2816AM | 2048 x 8 | N/A | 300 ns | 140 mA | 60 mA | 24 | M | • | | • | • | | | 3-27 | 9-7 |
| X2816AM-35 | 2048 x 8 | N/A | 350 ns | 140 mA | 60 mA | 24 | M | • | | • | • | | | 3-27 | 9-7 |
| X2816AM-45 | 2048 x 8 | N/A | 450 ns | 140 mA | 60 mA | 24 | M | • | | • | • | | | 3-27 | 9-7 |

### 16K E²PROMs (Continued)

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X2816B-25 | 2048 x 8 | 16 | 250 ns | 120 mA | 60 mA | 24 | † | • | • | • | • | | | 3-35 | 9-9 |
| X2816B | 2048 x 8 | 16 | 300 ns | 120 mA | 60 mA | 24 | † | • | • | • | • | | | 3-35 | 9-9 |
| X2816BI-25 | 2048 x 8 | 16 | 250 ns | 120 mA | 60 mA | 24 | † | • | • | • | • | | | 3-35 | 9-9 |
| X2816BI | 2048 x 8 | 16 | 300 ns | 140 mA | 70 mA | 24 | I | • | • | • | • | | | 3-35 | 9-9 |
| X2816BM-25 | 2048 x 8 | 16 | 250 ns | 140 mA | 70 mA | 24 | M | | | • | • | | | 3-45 | 9-9 |
| X2816BM | 2048 x 8 | 16 | 300 ns | 140 mA | 70 mA | 24 | M | | | • | • | | | 3-45 | 9-9 |

N/A = Not Applicable

**Key:**
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I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

P = Plastic DIP
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
D = Cerdip
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
C = Side Braze




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## 64K E²PROMs

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X2864A-25 | 8192 x 8 | 16 | 250 ns | 140 mA | 60 mA | 28 | † | ● | ● | ● | ● | | | 3-57 | 9-10 |
| X2864A | 8192 x 8 | 16 | 300 ns | 140 mA | 60 mA | 28 | † | ● | ● | ● | ● | | | 3-57 | 9-10 |
| X2864A-35 | 8192 x 8 | 16 | 350 ns | 140 mA | 60 mA | 28 | † | ● | ● | ● | ● | | | 3-57 | 9-10 |
| X2864A-45 | 8192 x 8 | 16 | 450 ns | 140 mA | 60 mA | 28 | † | ● | ● | ● | ● | | | 3-57 | 9-10 |
| X2864AI-25 | 8192 x 8 | 16 | 250 ns | 140 mA | 70 mA | 28 | I | ● | ● | ● | ● | | | 3-57 | 9-10 |
| X2864AI | 8192 x 8 | 16 | 300 ns | 140 mA | 70 mA | 28 | I | ● | ● | ● | ● | | | 3-57 | 9-10 |
| X2864AI-35 | 8192 x 8 | 16 | 350 ns | 140 mA | 70 mA | 28 | I | ● | ● | ● | ● | | | 3-57 | 9-10 |
| X2864AI-45 | 8192 x 8 | 16 | 450 ns | 140 mA | 70 mA | 28 | I | ● | ● | ● | ● | | | 3-57 | 9-10 |
| X2864AM-25 | 8192 x 8 | 16 | 250 ns | 140 mA | 70 mA | 28 | M | ● | ● | ● | ● | ● | | 3-67 | 9-10 |
| X2864AM | 8192 x 8 | 16 | 300 ns | 140 mA | 70 mA | 28 | M | | | ● | ● | ● | | 3-67 | 9-10 |
| X2864AM-35 | 8192 x 8 | 16 | 350 ns | 140 mA | 70 mA | 28 | M | | | ● | ● | ● | | 3-67 | 9-10 |
| X2864AM-45 | 8192 x 8 | 16 | 450 ns | 140 mA | 70 mA | 28 | M | | | ● | ● | ● | | 3-67 | 9-10 |
| X2864AT-35 | 8192 x 8 | 16 | 350 ns | 110 mA | 60 mA | 28 | T | | | ● | ● | | | 3-79 | 9-12 |
| X2864AT-45 | 8192 x 8 | 16 | 450 ns | 110 mA | 60 mA | 28 | T | | | ● | ● | | | 3-79 | 9-12 |

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J = 32-Lead J-Hook Plastic Leaded Chip Carrier
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**64K E²PROMs** (Continued)

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X2864B-120 | 8192 x 8 | 32 | 120 ns | 150 mA | 80 mA | 28 | † | ● | ● | ● | ● | | | 3-89 | 9-12 |
| X2864B-150 | 8192 x 8 | 32 | 150 ns | 150 mA | 80 mA | 28 | † | ● | ● | ● | ● | | | 3-89 | 9-12 |
| X2864B-180 | 8192 x 8 | 32 | 180 ns | 150 mA | 80 mA | 28 | † | ● | ● | ● | ● | | | 3-89 | 9-12 |
| X2864BI-120 | 8192 x 8 | 32 | 120 ns | 150 mA | 80 mA | 28 | I | ● | ● | ● | ● | | | 3-89 | 9-12 |
| X2864BI-150 | 8192 x 8 | 32 | 150 ns | 150 mA | 80 mA | 28 | I | ● | ● | ● | ● | | | 3-89 | 9-12 |
| X2864BI-180 | 8192 x 8 | 32 | 180 ns | 150 mA | 80 mA | 28 | I | ● | ● | ● | ● | | | 3-89 | 9-12 |
| X2864BM-120 | 8192 x 8 | 32 | 120 ns | 150 mA | 80 mA | 28 | M | | | ● | ● | | | 3-97 | 9-13 |
| X2864BM-150 | 8192 x 8 | 32 | 150 ns | 150 mA | 80 mA | 28 | M | | | ● | ● | | | 3-97 | 9-13 |
| X2864BM-180 | 8192 x 8 | 32 | 180 ns | 150 mA | 80 mA | 28 | M | | | ● | ● | | | 3-97 | 9-13 |

**64K E²PROMs** (Continued)

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X2864H-70 | 8192 x 8 | 32 | 70 ns | 150 mA | 80 mA | 28 | † | ● | ● | ● | ● | | | 3-105 | 9-14 |
| X2864H-90 | 8192 x 8 | 32 | 90 ns | 150 mA | 80 mA | 28 | † | ● | ● | ● | ● | | | 3-105 | 9-14 |
| X2864HI-90 | 8192 x 8 | 32 | 90 ns | 150 mA | 80 mA | 28 | I | ● | ● | ● | ● | | | 3-105 | 9-14 |
| X2864HM-90 | 8192 x 8 | 32 | 90 ns | 150 mA | 80 mA | 28 | M | | | ● | ● | | | 3-113 | 9-14 |

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## 256K E²PROMs

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X28256-25 | 32768 x 8 | 64 | 250 ns | 120 mA | 60 mA | 28 | † | ● | ● | ● | ● | | | 3-121 | 9-15 |
| X28256 | 32768 x 8 | 64 | 300 ns | 120 mA | 60 mA | 28 | † | ● | ● | ● | ● | | | 3-121 | 9-15 |
| X28256-35 | 32768 x 8 | 64 | 350 ns | 120 mA | 60 mA | 28 | † | ● | ● | ● | ● | | | 3-121 | 9-15 |
| X28256I-25 | 32768 x 8 | 64 | 250 ns | 120 mA | 60 mA | 28 | I | ● | ● | ● | ● | | | 3-121 | 9-15 |
| X28256I | 32768 x 8 | 64 | 300 ns | 120 mA | 60 mA | 28 | I | ● | ● | ● | ● | | | 3-121 | 9-15 |
| X28256I-35 | 32768 x 8 | 64 | 350 ns | 120 mA | 60 mA | 28 | I | ● | ● | ● | ● | | | 3-121 | 9-15 |
| X28256M-25 | 32768 x 8 | 64 | 250 ns | 120 mA | 60 mA | 28 | M | | | ● | ● | | | 3-135 | 9-15 |
| X28256M | 32768 x 8 | 64 | 300 ns | 120 mA | 60 mA | 28 | M | | | ● | ● | | | 3-135 | 9-15 |
| X28256M-35 | 32768 x 8 | 64 | 350 ns | 120 mA | 60 mA | 28 | M | | | ● | ● | | | 3-135 | 9-15 |

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G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
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**256K E²PROMs** (Continued)

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X28C256-25 | 32768 x 8 | 64 | 250 ns | 60 mA | 200 µA | 28 | † | • | • | • | • | | | 3-149 | 9-16 |
| X28C256 | 32768 x 8 | 64 | 300 ns | 60 mA | 200 µA | 28 | † | • | • | • | • | | | 3-149 | 9-16 |
| X28C256-35 | 32768 x 8 | 64 | 350 ns | 60 mA | 200 µA | 28 | † | • | • | • | • | | | 3-149 | 9-16 |
| X28C256I-25 | 32768 x 8 | 64 | 250 ns | 60 mA | 200 µA | 28 | I | • | • | • | • | | | 3-149 | 9-16 |
| X28C256I | 32768 x 8 | 64 | 300 ns | 60 mA | 200 µA | 28 | I | • | • | • | • | | | 3-149 | 9-16 |
| X28C256I-35 | 32768 x 8 | 64 | 350 ns | 60 mA | 200 µA | 28 | I | • | • | • | • | | | 3-149 | 9-16 |
| X28C256M-25 | 32768 x 8 | 64 | 250 ns | 60 mA | 200 µA | 28 | M | | | • | • | | | 3-163 | 9-17 |
| X28C256M | 32768 x 8 | 64 | 300 ns | 60 mA | 200 µA | 28 | M | | | • | • | | | 3-163 | 9-17 |
| X28C256M-35 | 32768 x 8 | 64 | 350 ns | 60 mA | 200 µA | 28 | M | | | • | • | | | 3-163 | 9-17 |

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# Reference Guide to Xicor Nonvolatile Memories

### 1M E²PROMs

| Part Number | Organization | Page Size (# Bytes) | Access Time | Power | | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Active | Standby | | | P | J | D | E | G | C | | |
| X28C010 | 131072 x 8 | 128 | 200 ns | 80 mA | 500 μA | 32 | †, I, M | | | • | | | • | 3-177 | N/A |

### E²POTENTIOMETERs

| Part Number | Minimal Resistance | Wiper Increments | Maximum Resistance | No. of Pins | Temp. Range(s) | Package | | | | | | Data Sheet Page No. | Order Info. Page No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | P | J | D | E | G | C | | |
| X9103 | 40Ω | 101Ω | 10 KΩ | 8 | †, I, M | • | | | | | | 4-1, 4-7 | 9-18 |
| X9503 | 40Ω | 505Ω | 50 KΩ | 8 | †, I, M | • | | | | | | | 9-18 |
| X9104 | 40Ω | 1010Ω | 100 KΩ | 8 | †, I, M | • | | | | | | | 9-18 |

N/A = Not Applicable

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M = Military = −55°C to +125°C
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C = Side Braze

# Nonvolatile Static RAM

## FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 300 ns Max.**
- **Nonvolatile Store Inhibit: $V_{CC}$ = 3V Typical**
- **100 Year Data Retention**
- **JEDEC Standard 18-Pin Package**

## DESCRIPTION

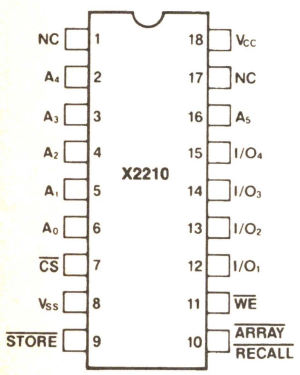
The Xicor X2210 is a 64 x 4 NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2210 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories. The X2210 features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 10,000 store cycles. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

## PIN CONFIGURATION

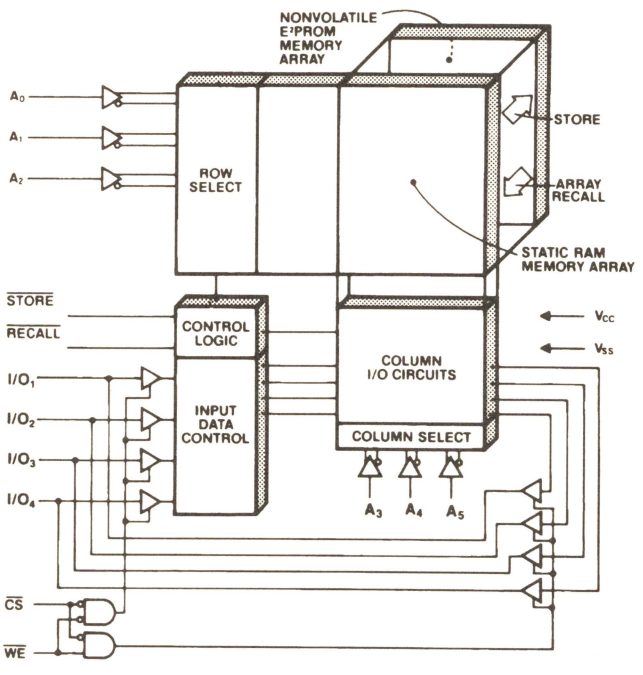



0045-1

## PIN NAMES

| | |
|---|---|
| $A_0$–$A_5$ | Address Inputs |
| $I/O_1$–$I/O_4$ | Data Inputs/Outputs |
| $\overline{WE}$ | Write Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{ARRAY\ RECALL}$ | Array Recall |
| $\overline{STORE}$ | Store |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

## FUNCTIONAL DIAGRAM




0045-2

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# 1K Commercial Industrial X2212 X2212I 256 x 4 Bit

## Nonvolatile Static RAM

### FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 300 ns Max.**
- **Nonvolatile Store Inhibit: $V_{CC}$ = 3V Typical**
- **100 Year Data Retention**
- **JEDEC Standard 18-Pin Package**

### DESCRIPTION

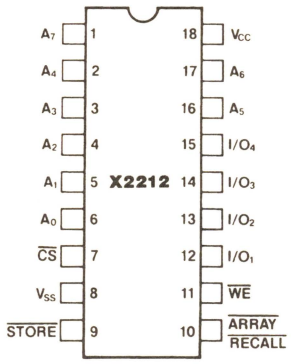
The Xicor X2212 is a 256 x 4 NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2212 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories. The X2212 features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 10,000 store cycles. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

### PIN CONFIGURATION

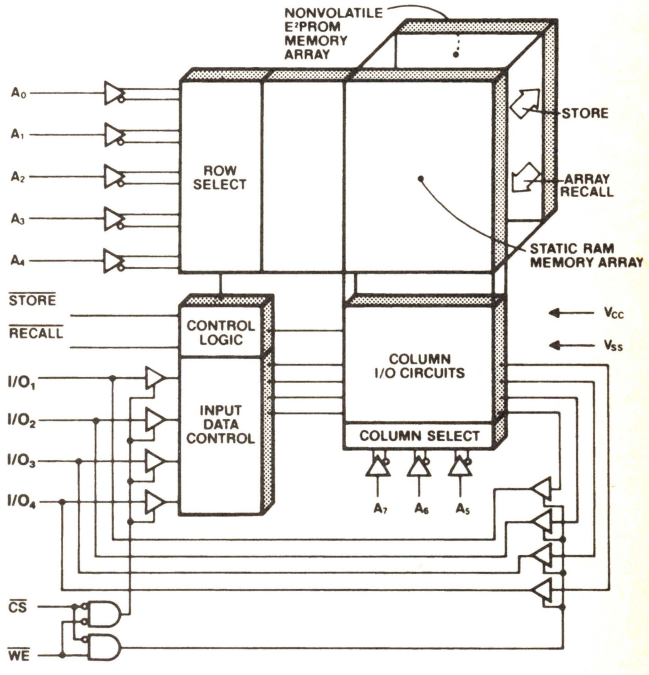



0058-1

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_7$ | Address Inputs |
| $I/O_1$–$I/O_4$ | Data Inputs/Outputs |
| $\overline{WE}$ | Write Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{ARRAY\ RECALL}$ | Array Recall |
| $\overline{STORE}$ | Store |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

### FUNCTIONAL DIAGRAM




0058-2

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# 1K Commercial Industrial X2001 X2001I 128 x 8 Bit

## Nonvolatile Static RAM

### FEATURES

- **Nonvolatile Data Integrity**
- **Automatic Store Timing**
- **Store and Array Recall Combined on One Line ($\overline{NE}$)**
- **Enhanced Store Protection**
- **Infinite E²PROM Array Recall, and RAM Read and Write Cycles**
- **Single 5V Supply**
- **100 Year Data Retention**
- **Fast Access Time: 200 ns Max.**
- **Automatic Recall on Power-Up**
- **JEDEC Approved Byte-Wide Pinout**

### DESCRIPTION

The Xicor X2001 is a byte-wide NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E²PROM). The X2001 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2001 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E²PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and E²PROM to RAM (recall). With $\overline{NE}$ LOW, these functions are performed in the same manner as RAM read and write operations. The store operation is completed in 10 ms or less and the recall operation is completed in 5 $\mu$s or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM, and a minimum 100,000 store operations to the E²PROM. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

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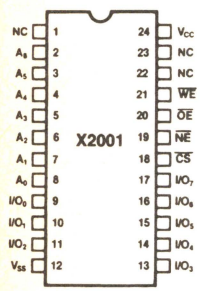
### PIN CONFIGURATION

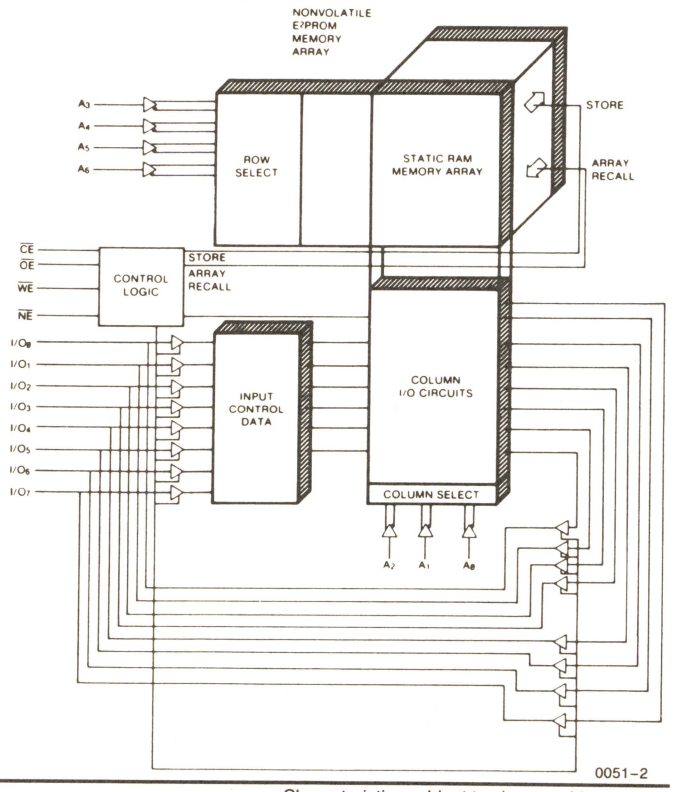



0051-1

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_6$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Inputs/Outputs |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{NE}$ | Nonvolatile Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

### FUNCTIONAL DIAGRAM




0051-2

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# Nonvolatile Static RAM

## FEATURES

- **Nonvolatile Data Integrity**
- **Automatic Store Timing**
- **Store and Array Recall Combined on One Line ($\overline{NE}$)**
- **Enhanced Store Protection**
- **Infinite E²PROM Array Recall, and RAM Read and Write Cycles**
- **Single 5V Supply**
- **100 Year Data Retention**
- **Fast Access Time: 200 ns Max.**
- **Automatic Recall on Power-Up**
- **JEDEC Approved Byte-Wide Pinout**

## DESCRIPTION

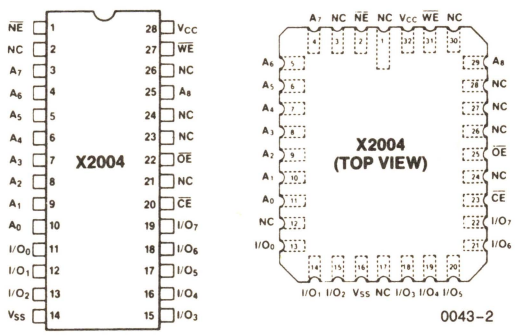
The Xicor X2004 is a byte-wide NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E²PROM). The X2004 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2004 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E²PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and E²PROM to RAM (recall). With $\overline{NE}$ LOW, these functions are performed in the same manner as RAM read and write operations. The store operation is completed in 10 ms or less and the recall operation is completed in 5 $\mu$s or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM, and a minimum 100,000 store operations to the E²PROM. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

## PIN CONFIGURATIONS



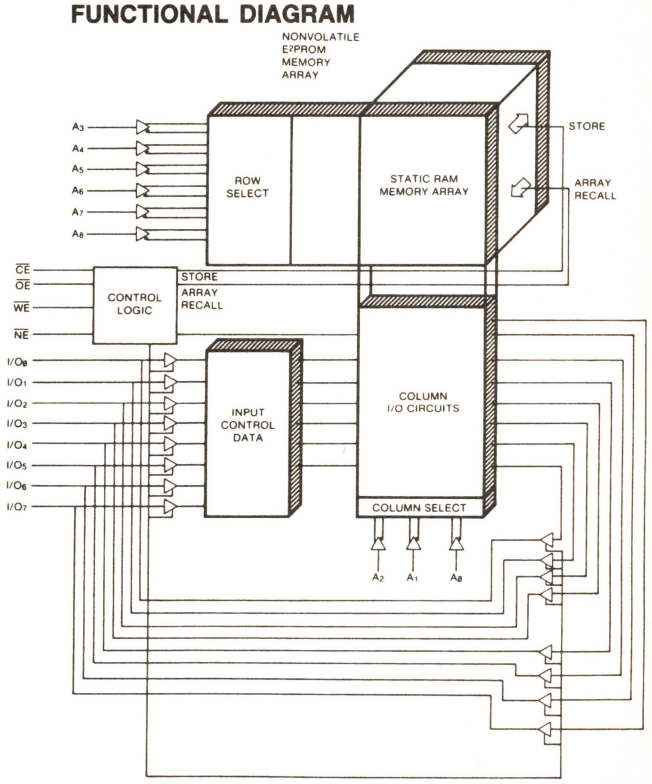

0043-1

0043-2

## PIN NAMES

| | |
|---|---|
| $A_0$–$A_8$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Inputs/Outputs |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{NE}$ | Nonvolatile Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

## FUNCTIONAL DIAGRAM




0043-3

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# Nonvolatile Static RAM

## FEATURES

- **Ideal for use with Single Chip Microcomputers**
  - **—Static Timing**
  - **—Minimum I/O Interface**
  - **—Serial Port Compatible (COPS™, 8051)**
  - **—Easily Interfaces to Microcontroller Ports**
  - **—Minimum Support Circuits**
- **Software and Hardware Control of Nonvolatile Functions**
  - **—Maximum Store Protection**
- **TTL Compatible**
- **16 x 16 Organization**
- **Low Power Dissipation**
  - **—Active Current: 15 mA Typical**
  - **—Store Current: 8 mA Typical**
  - **—Standby Current: 6 mA Typical**
  - **—Sleep Current: 5 mA Typical**
- **8 Pin Mini-DIP Package**

Xicor

## DESCRIPTION

The Xicor X2444 is a serial 256 bit NOVRAM* featuring a static RAM configured 16 x 16, overlaid bit for bit with a nonvolatile $E^2$PROM array. The X2444 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories.

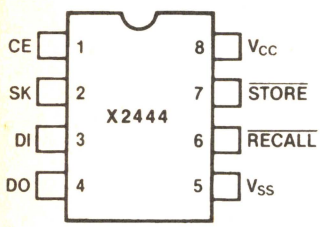
The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to $E^2$PROM) is completed in 10 ms or less and a recall operation ($E^2$PROM data to RAM) is completed in 2.5 $\mu$s or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from $E^2$PROM and a minimum 100,000 store operations. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

COPS™ is a trademark of National Semiconductor Corp.

## PIN CONFIGURATION

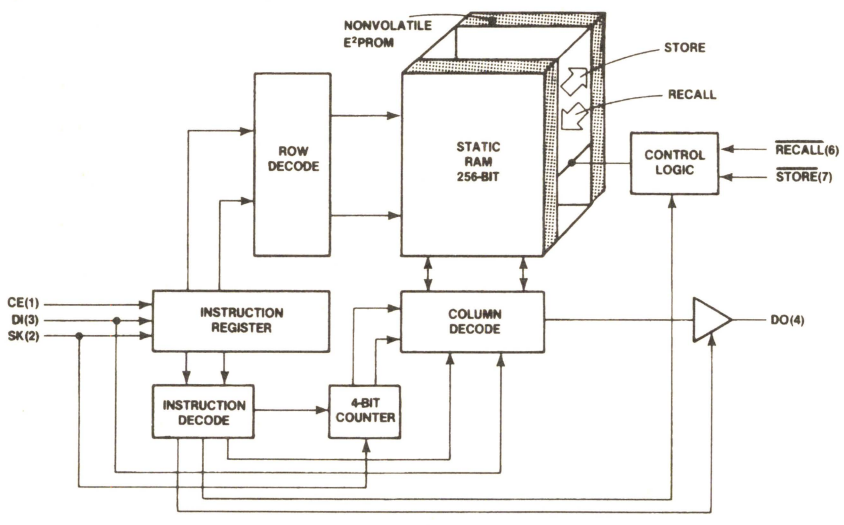



0042-1

## PIN NAMES

| | |
|---|---|
| CE | Chip Enable |
| SK | Serial Clock |
| DI | Serial Data In |
| DO | Serial Data Out |
| $\overline{\text{RECALL}}$ | Recall |
| $\overline{\text{STORE}}$ | Store |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |

## FUNCTIONAL DIAGRAM




0042-2

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PRELIMINARY INFORMATION

# 2K Commercial Industrial X2402 X2402I 256 x 8 Bit

## Electrically Erasable PROM

### TYPICAL FEATURES

- Internally Organized 256 x 8
- 2 Wire Serial Interface
- Provides Bidirectional Data Transfer Protocol
- Eight Byte Page Write Mode
  —Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  —Typical Write Cycle Time of 5 ms
- Data Retention Greater Than 100 Years
- 8 Pin Mini-DIP Package

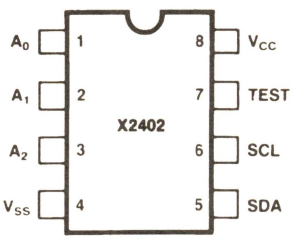
### DESCRIPTION

The X2402 is a 2048 bit serial E²PROM, internally organized as one 256 x 8 page. The X2402 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories.

The X2402 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Refer to RR504 for further endurance information. Data retention is specified to be greater than 100 years.

### PIN CONFIGURATION

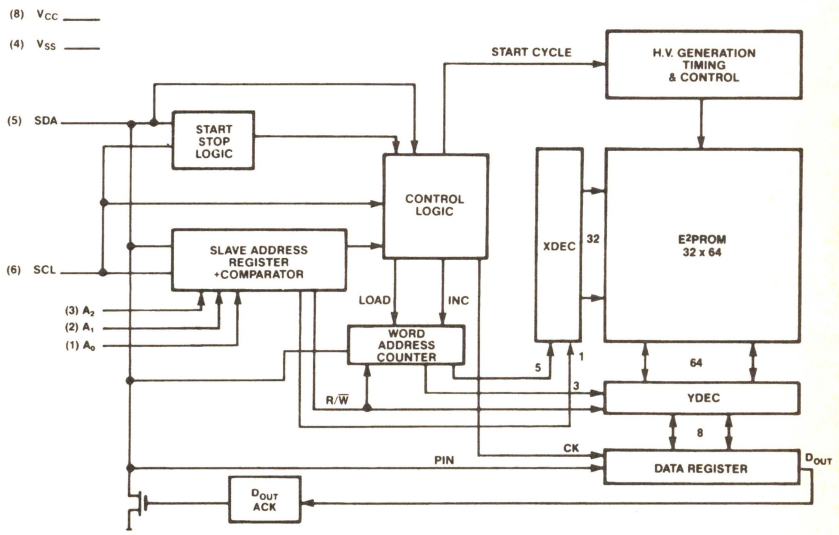



0035-1

### PIN NAMES

| | |
|---|---|
| 1 to 3 | $A_0$ to $A_2$ Address Inputs |
| 4 | $V_{SS}$ |
| 5 | SDA Serial Data |
| 6 | SCL Serial Clock |
| 7 | **Test Input → to $V_{SS}$** |
| 8 | $V_{CC}$ |

### FUNCTIONAL DIAGRAM




0035-2

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| 4K | Commercial<br>Industrial | X2404<br>X2404I | 512 x 8 Bit |
|---|---|---|---|

# Electrically Erasable PROM

## TYPICAL FEATURES

- **Internally Organized as Two Pages**
  **—Each 256 x 8**
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Eight Byte Page Write Mode**
  **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  **—Typical Write Cycle Time of 5 ms**
- **Data Retention Greater Than 100 Years**
- **8 Pin Mini-DIP Package**

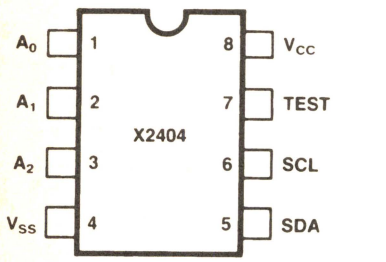
## DESCRIPTION

The X2404 is a 4096 bit serial $E^2$PROM, internally organized as two 256 x 8 pages. The X2404 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories.

The X2404 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor $E^2$PROMs are designed and tested for applications requiring extended endurance. Refer to RR504 for further endurance information. Data retention is specified to be greater than 100 years.

## PIN CONFIGURATION

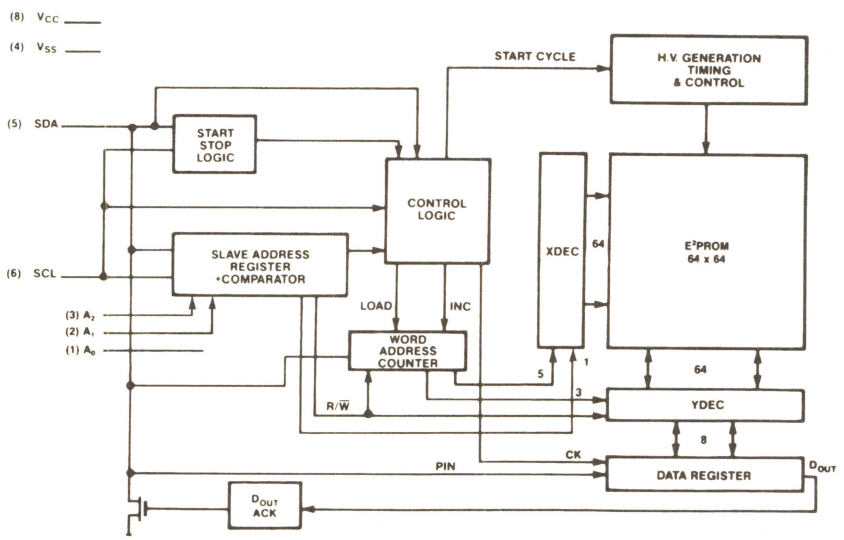



0041-1

## PIN NAMES

| | |
|---|---|
| 1 to 3 | $A_0$ to $A_2$ Address Inputs |
| 4 | $V_{SS}$ |
| 5 | SDA Serial Data |
| 6 | SCL Serial Clock |
| 7 | **Test Input → to $V_{SS}$** |
| 8 | $V_{CC}$ |

## FUNCTIONAL DIAGRAM




0041-2

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ADVANCED INFORMATION

# 4K Commercial Industrial X24C04 X24C04I 512 x 8 Bit

## Electrically Erasable PROM

### TYPICAL FEATURES

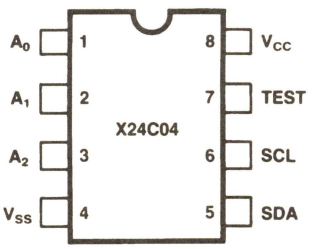
- Low Power CMOS
  - —2 mA Active Current Typical
  - —60 μA Standby Current Typical
- Internally Organized as Two Pages
  - —Each 256 x 8
- 2 Wire Serial Interface
- Provides Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - —Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5 ms
- Data Retention Greater Than 100 Years
- 8 Pin Mini-DIP Package

### DESCRIPTION

The X24C04 is a CMOS 4096 bit serial E²PROM, internally organized as two 256 x 8 pages. The X24C04 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

### PIN CONFIGURATION

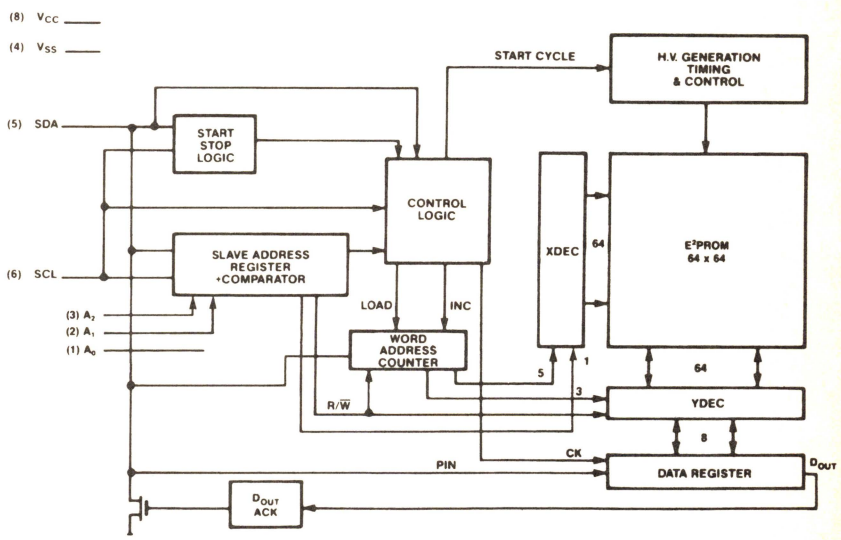



0046-1

### PIN NAMES

| | |
|---|---|
| 1 to 3 | $A_0$ to $A_2$ Address Inputs |
| 4 | $V_{SS}$ |
| 5 | SDA Serial Data |
| 6 | SCL Serial Clock |
| 7 | **Test Input → to $V_{SS}$** |
| 8 | $V_{CC}$ |

### FUNCTIONAL DIAGRAM




0046-2

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PRELIMINARY INFORMATION

# 16K Commercial Industrial X24C16 X24C16I 2048 x 8 Bit

## Electrically Erasable PROM

### TYPICAL FEATURES

- Low Power CMOS
  - —2 mA Active Current Typical
  - —60 μA Standby Current Typical
- Internally Organized as Eight Pages
  - —Each 256 x 8
- 2 Wire Serial Interface
- Provides Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - —Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5 ms
- Data Retention Greater Than 100 Years
- 8 Pin Mini-DIP Package

### DESCRIPTION

The X24C16 is a CMOS 16,384 bit serial E²PROM, internally organized as eight 256 x 8 pages. The X24C16 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

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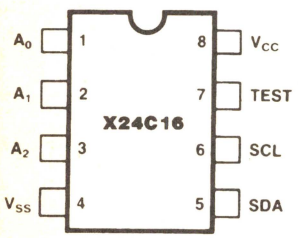
### PIN CONFIGURATION

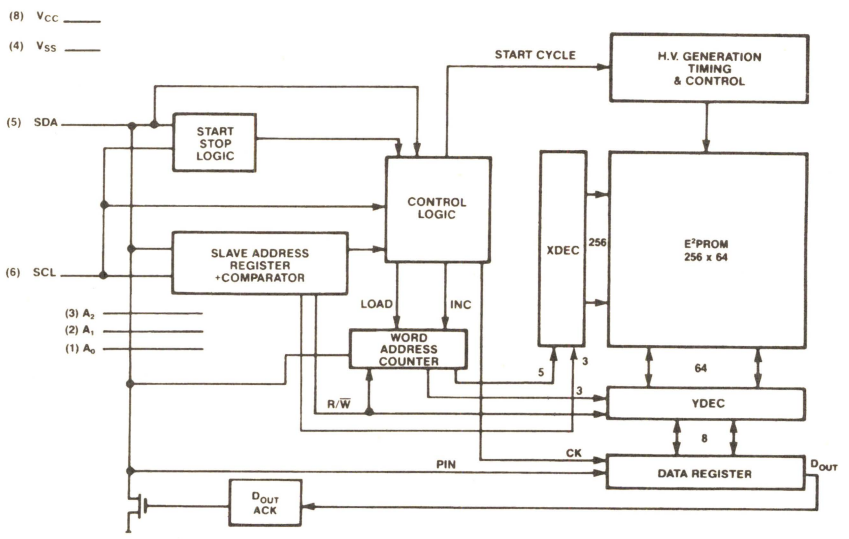



0038-1

### PIN NAMES

| | |
|---|---|
| 1 to 3 | $A_0$ to $A_2$ Address Inputs |
| 4 | $V_{SS}$ |
| 5 | SDA Serial Data |
| 6 | SCL Serial Clock |
| 7 | **Test Input → to $V_{SS}$** |
| 8 | $V_{CC}$ |

### FUNCTIONAL DIAGRAM




0038-2

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# 4K Commercial Industrial X2804A X2804AI 512 x 8 Bit

## Electrically Erasable PROM

### FEATURES

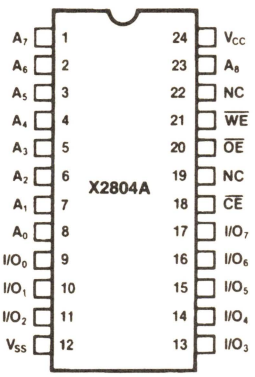
- **Simple Byte Write Operation**
  - **—No High Voltages Necessary**
  - **—Single TTL Level $\overline{WE}$ Signal Modifies Data**
  - **—Internally Latched Address and Data**
  - **—Self Timed Write**
  - **—Noise Protected $\overline{WE}$ Pin**
- **Reliable N-Channel Floating Gate MOS Technology**
- **Single 5V Supply**
- **Byte Write Time: 10 ms Max.**
- **Fast Access Time: 250 ns Max.**
- **Low Power Dissipation**
  - **—Active Current: 80 mA Max.**
  - **—Standby Current: 50 mA Max.**

### DESCRIPTION

The Xicor X2804A is a 512 x 8 $E^2$PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2804A is compatible with the JEDEC approved pinout for byte-wide memories.

Xicor $E^2$PROMs are designed and tested for applications requiring extended endurance. Refer to Device Operation for further endurance information. Data retention is specified to be greater than 100 years.

### PIN CONFIGURATION

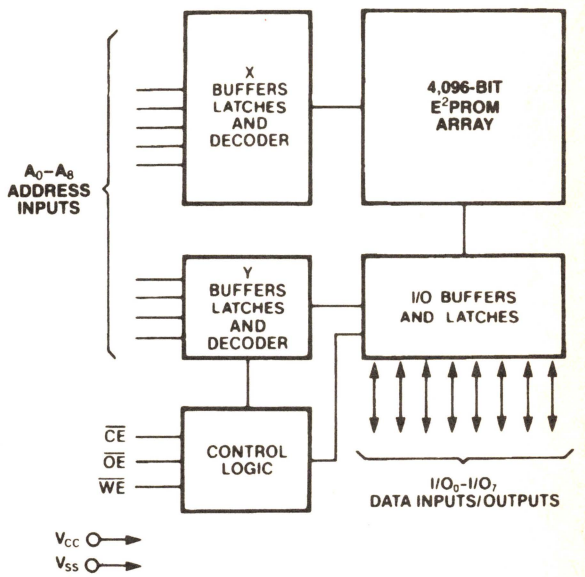



0044-1

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_8$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

### FUNCTIONAL DIAGRAM




0044-2

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Characteristics subject to change without notice

| 16K | Commercial<br>Industrial | X2816A<br>X2816AI | 2048 x 8 Bit |
|---|---|---|---|

# Electrically Erasable PROM

## FEATURES

- **Simple Byte Write Operation**
  - **—No High Voltages Necessary**
  - **—Single TTL Level $\overline{WE}$ Signal Modifies Data**
  - **—Internally Latched Address and Data**
  - **—Self Timed Write**
  - **—Noise Protected $\overline{WE}$ Pin**
- **Reliable N-Channel Floating Gate MOS Technology**
- **Single 5V Supply**
- **Byte Write Time: 10 ms Max.**
- **Fast Access Time: 250 ns Max.**
- **Low Power Dissipation**
  - **—Active Current: 110 mA Max.**
  - **—Standby Current: 50 mA Max.**
- **JEDEC Approved Byte-Wide Pinout**

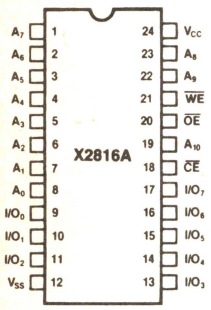
## DESCRIPTION

The Xicor X2816A is a 2K x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2816A features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, and EPROMs.

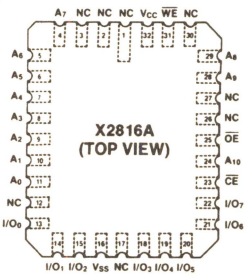
Xicor E²PROMs are designed and tested for applications requiring extended endurance. Refer to Device Operation for further endurance information. Data retention is specified to be greater than 100 years.

Xicor

## PIN CONFIGURATIONS

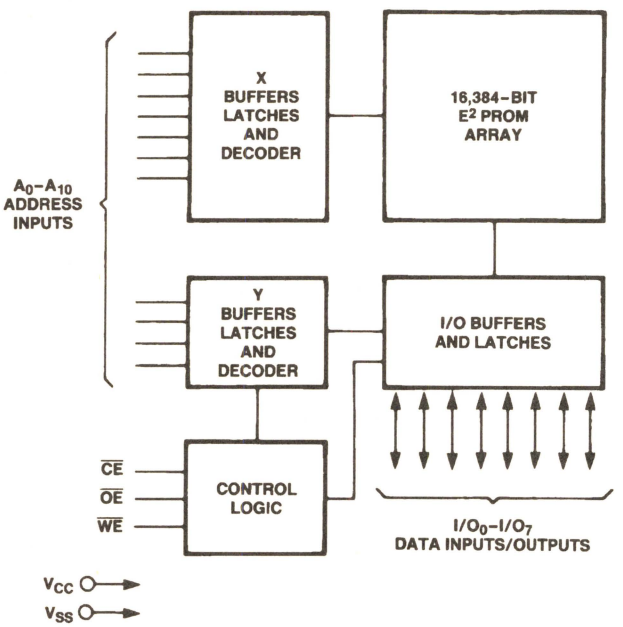



0054-1




0054-2

## FUNCTIONAL DIAGRAM




0054-3

## PIN NAMES

| | |
|---|---|
| $A_0$–$A_{10}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

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PRELIMINARY INFORMATION

# 16K Commercial Industrial X2816B X2816BI 2048 x 8 Bit

## Electrically Erasable PROM

### FEATURES

- 250 ns Access Time
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 640 ms Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{DATA}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{WE}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

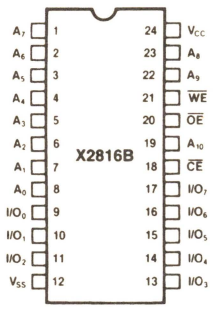
### DESCRIPTION

The Xicor X2816B is a 2K x 8 $E^2$PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2816B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

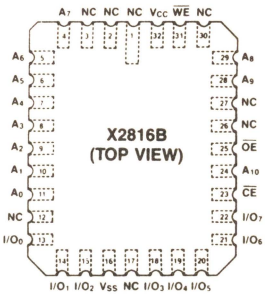
The X2816B supports a 16-byte page write operation, typically providing a 300 μs/byte write cycle, enabling the entire memory to be written in less than 640 ms. The X2816B also features $\overline{DATA}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor $E^2$PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

### PIN CONFIGURATIONS




0071-1

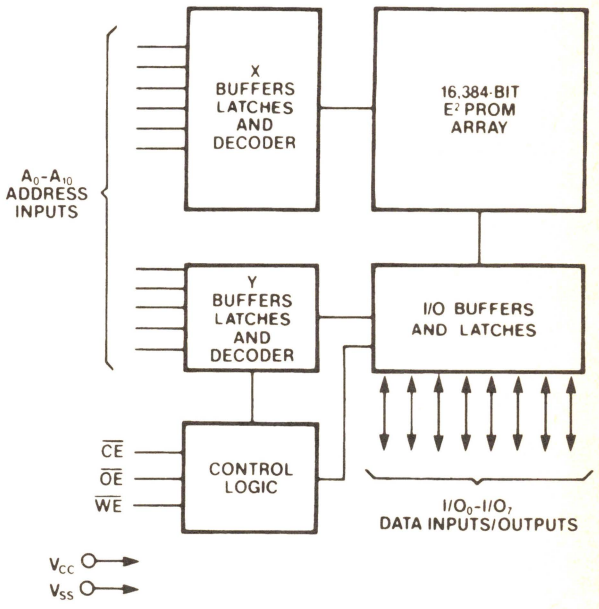



0071-2

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_{10}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

### FUNCTIONAL DIAGRAM




0071-3

Xicor

# 64K Commercial Industrial X2864A X2864AI 8192 x 8 Bit

## Electrically Erasable PROM

### FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.6 Sec. Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

### DESCRIPTION

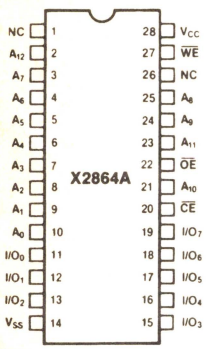
The Xicor X2864A is a 8K x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2864A features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864A supports a 16-byte page write operation, effectively providing a 300 μs/byte write and enabling the entire memory to be written in less than 2.6 seconds. The X2864A also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

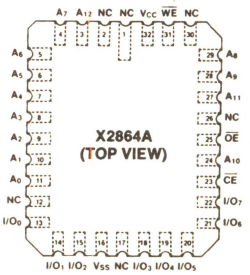
Xicor E²PROMs are designed and tested for applications requiring extended endurance. Refer to Device Operation for further endurance information. Data retention is specified to be greater than 100 years.

Xicor

### PIN CONFIGURATIONS

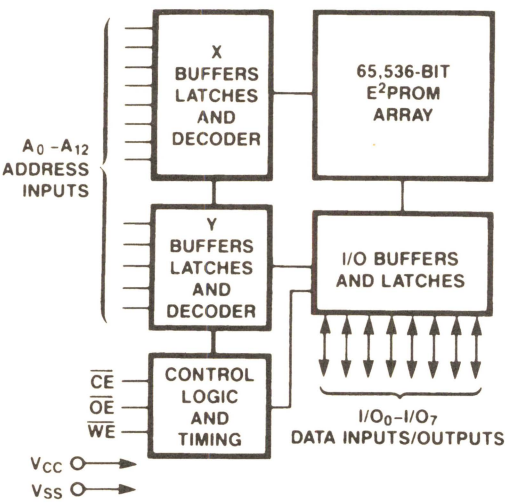



0070-1




0070-2

### FUNCTIONAL DIAGRAM




0070-3

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_{12}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

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PRELIMINARY INFORMATION

# 64K Commercial Industrial X2864B X2864BI 8192 x 8 Bit

## Electrically Erasable PROM

### TYPICAL FEATURES

- 120 ns Access Time
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - —32-Byte Page Write Operation
  - —Byte or Page Write Cycle: 3 ms Typical
  - —Complete Memory Rewrite: 750 ms Typical
  - —Effective Byte Write Cycle Time of 95 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

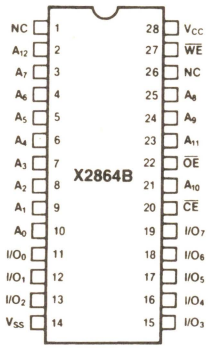
### DESCRIPTION

The Xicor X2864B is a 8K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

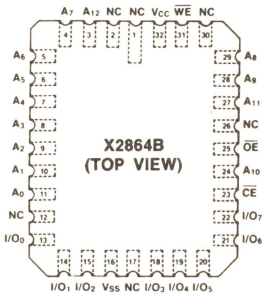
The X2864B supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864B also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

### PIN CONFIGURATIONS

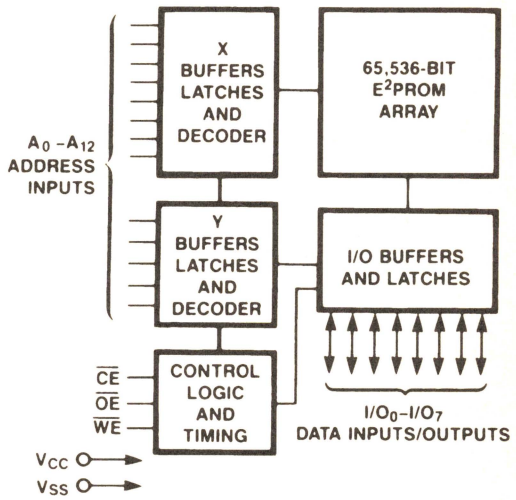



0031-1




0031-2

### FUNCTIONAL DIAGRAM




0031-3

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_{12}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

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# Electrically Erasable PROM

## FEATURES

- 350 ns Access Time
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 10 ms Typical
  - —Complete Memory Rewrite: 5.2 Sec. Typical
  - —Effective Byte Write Cycle Time of 600 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

## DESCRIPTION

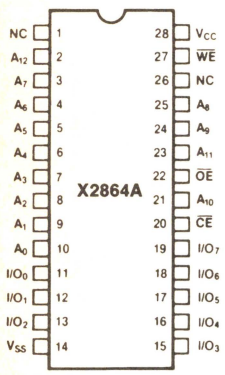
The Xicor X2864A is a 8K x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2864A features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864A supports a 16-byte page write operation, effectively providing a 600 μs/byte write and enabling the entire memory to be written in less than 5.2 seconds. The X2864A also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

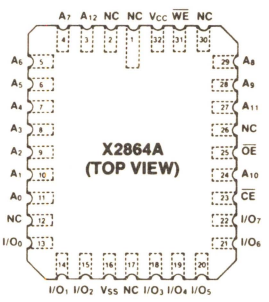
Xicor E²PROMs are designed and tested for applications requiring extended endurance. Refer to Device Operation for further endurance information. Data retention is specified to be greater than 100 years.

Xicor

## PIN CONFIGURATIONS




0066-1

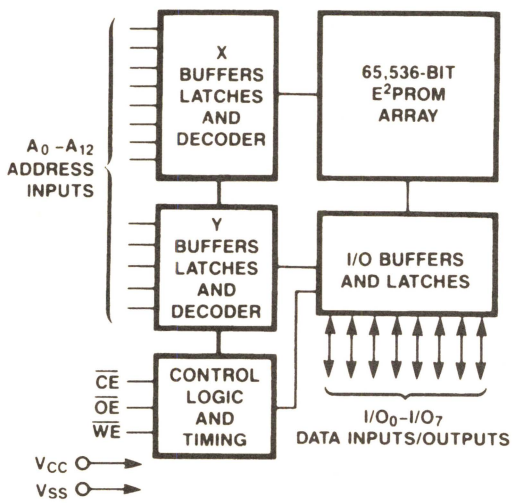



0066-2

## PIN NAMES

| | |
|---|---|
| $A_0$–$A_{12}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{\text{WE}}$ | Write Enable |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

## FUNCTIONAL DIAGRAM




0066-3

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PRELIMINARY INFORMATION

# 64K Commercial Industrial X2864H X2864HI 8192 x 8 Bit

## Electrically Erasable PROM

### TYPICAL FEATURES

- 70 ns Access Time
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - —32-Byte Page Write Operation
  - —Byte or Page Write Cycle: 3 ms Typical
  - —Complete Memory Rewrite: 750 ms Typical
  - —Effective Byte Write Cycle Time of 95 $\mu$s Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

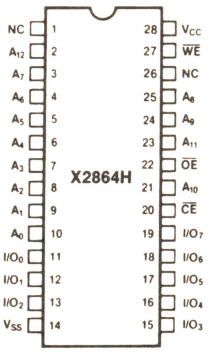
### DESCRIPTION

The Xicor X2864H is a high speed 8K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864H features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, and EPROMs.

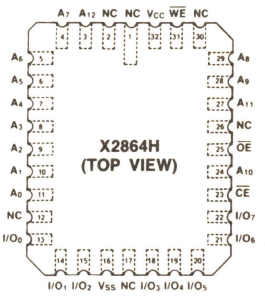
The X2864H supports a 32-byte page write operation, effectively providing a 95 $\mu$s/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864H also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

### PIN CONFIGURATIONS

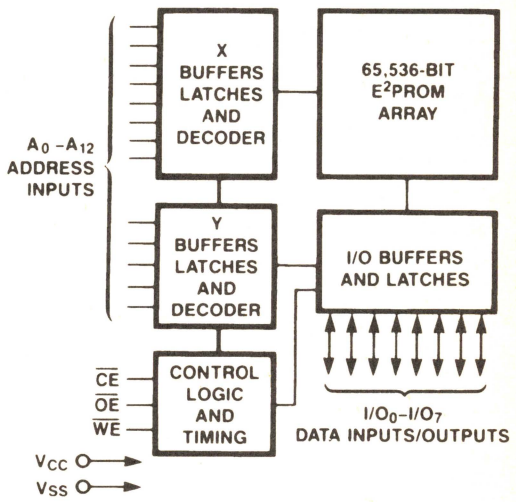



0034-1




0034-2

### FUNCTIONAL DIAGRAM




0034-3

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_{12}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

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PRELIMINARY INFORMATION

# 256K Commercial Industrial X28256 X28256I 32K x 8 Bit

## Electrically Erasable PROM

### FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- Upward Compatible with X2864A
- JEDEC Approved Byte-Wide Pinout

Xicor

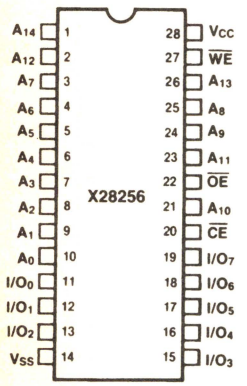
### DESCRIPTION

The Xicor X28256 is a 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories the X28256 is a 5V only device. The X28256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

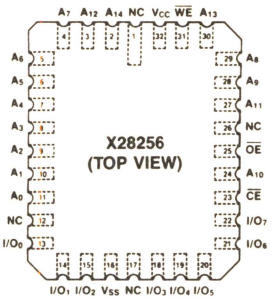
The X28256 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28256 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

### PIN CONFIGURATIONS

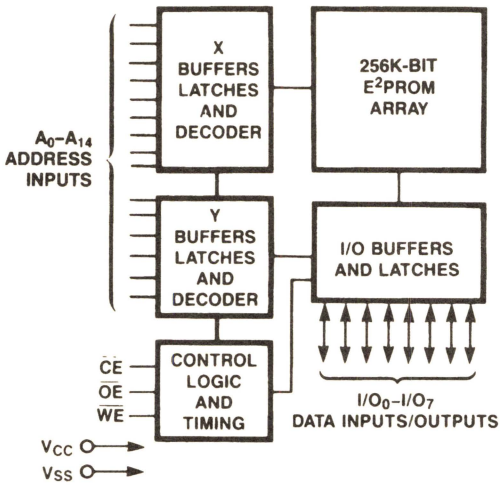



0029-1




0029-2

### FUNCTIONAL DIAGRAM




0029-3

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_{14}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

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PRELIMINARY INFORMATION

# 256K Commercial Industrial X28C256 X28C256I 32K x 8 Bit

## Electrically Erasable PROM

### FEATURES

- LOW Power CMOS
  - —60 mA Active Current Max.
  - —200 μA Standby Current Max.
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- Upward Compatible with X2864A
- JEDEC Approved Byte-Wide Pinout

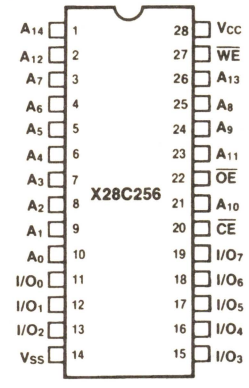
### DESCRIPTION

The Xicor X28C256 is a 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

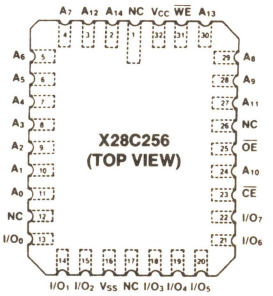
The X28C256 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

### PIN CONFIGURATIONS




0067-1

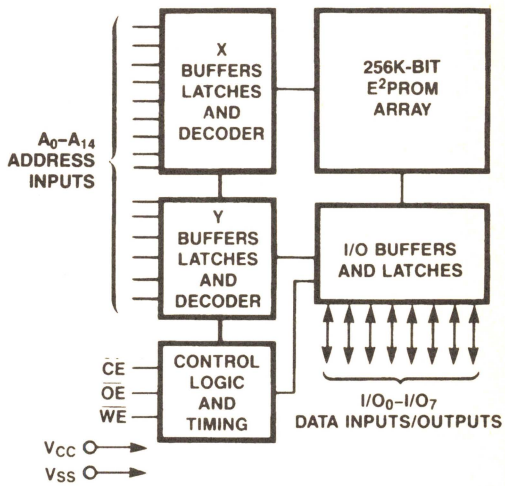



0067-2

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_{14}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

### FUNCTIONAL DIAGRAM




0067-3

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FACT SHEET

# 1M Commercial X28C010 128K x 8 Bit

## Electrically Erasable PROM

### FEATURES

- 200 ns Access Time
- LOW Power CMOS
  - —80 mA Active Current Typical
  - —500 μA Standby Current Typical
- Fast Write Cycle Times
  - —128-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 5 Sec. Typical
  - —Effective Byte Write Cycle Time: 39 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

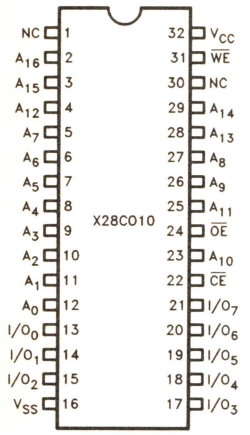
### DESCRIPTION

The Xicor X28C010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

The X28C010 supports a 128-byte page write operation, effectively providing a 39 μs/byte write cycle and enabling the entire memory to be typically written in less than 5 seconds. The X28C010 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C010 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

### PIN CONFIGURATION

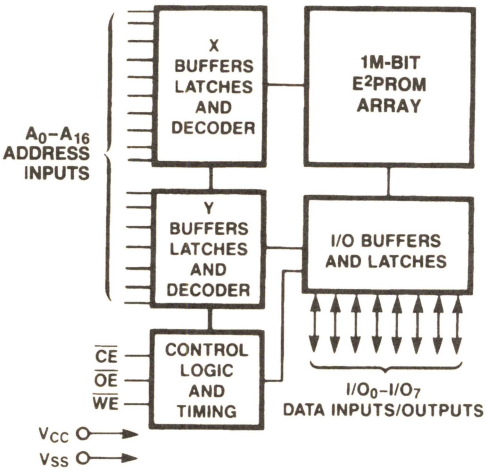



0084-1

### PIN NAMES

| | |
|---|---|
| $A_0$–$A_{16}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

### FUNCTIONAL DIAGRAM




0084-2

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PRELIMINARY INFORMATION

# Commercial X9MME
# Industrial X9MMEI

## E²POT™ Digitally Controlled Potentiometer

### FEATURES

- Solid State Reliability
- Single Chip MOS Implementation
- Three Wire TTL Control
- Operates From Standard 5V Supply
- Wide Analog Voltage Range ±5V Min.
- 99 Resistive Elements
  - —Temperature Compensated
  - —±20% End to End Resistance Range
- 100 Wiper Tap Points
  - —Wiper Position Digitally Controlled
  - —Wiper Position Stored in Nonvolatile Memory Then Automatically Recalled on Power-Up
- 100 Year Wiper Position Retention
- 8 Pin Mini-DIP Package

### DESCRIPTION

The Xicor X9MME is a solid state nonvolatile potentiometer, packaged in an 8 pin mini-DIP and is ideal for digitally controlled resistance trimming.

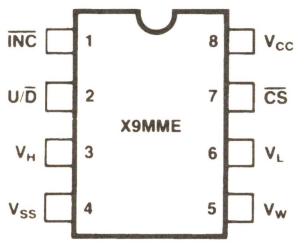
The X9MME is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element on the array is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and is recalled upon a subsequent power-up.

The resolution of the X9MME is equal to the maximum resistance value divided by 99. As an example; for the X9503 (50 KΩ) each tap point represents 505Ω.

Xicor E² products are designed and tested for applications requiring extended endurance. Refer to Xicor reliability reports for further endurance information.

E²POT™ is a trademark of Xicor, Inc.

### PIN CONFIGURATION

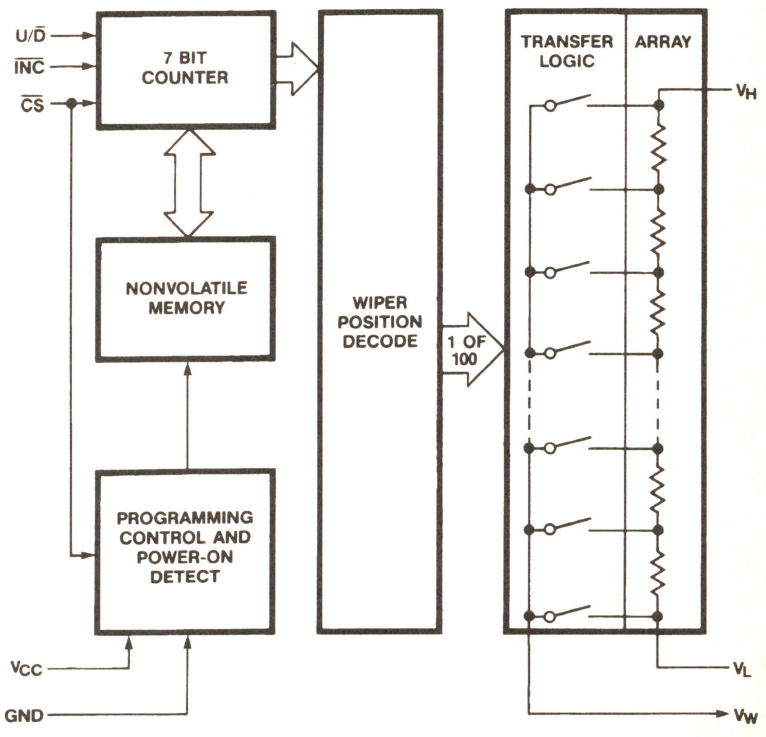



0039-1

### PIN NAMES

| | |
|---|---|
| $V_H$ | High Terminal of Pot |
| $V_W$ | Wiper Terminal of Pot |
| $V_L$ | Low Terminal of Pot |
| $V_{SS}$ | Ground |
| $V_{CC}$ | System Power |
| U/$\overline{D}$ | Up/Down Control |
| $\overline{INC}$ | Wiper Movement Control |
| $\overline{CS}$ | Chip Select for Wiper Movement/Storage |

### FUNCTIONAL DIAGRAM




0039-2

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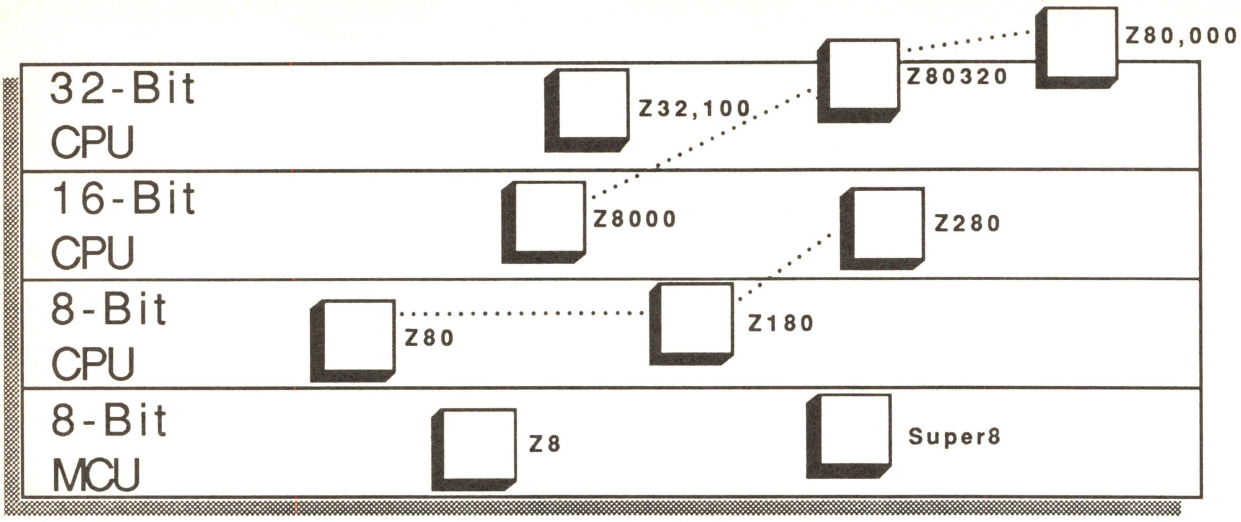
# Z I L O G




**Product Evolution**

Following on the success of the Z80 CPU, Zilog continues its record of excellence with the Z8 MCU 8-bit microcontroller, the Z8000 MPU 16-bit microprocessor, the Super8 enhanced high-performance 8-bit microcontroller, the Z80,000 32-bit microprocessor, and most recently, the Z280 MPU, an 8/16-bit microprocessor that is software compatible with the Z80 CPU.

A complete line of peripheral products complement the processor families. Included in the peripheral line are such industry-standards as the Z8030/8530 Serial Communications Controller, the Z8038 FIFO I/O Interface Unit (dual-port), and the Z8036/8536 CIO Counter/Timer and Parallel I/O Unit. Add to that a series of Zilog products obtained through various partnership agreements and Zilog is able to provide a stable of products unmatched in the industry. All of these fine products are supported via a network of sales offices around the world – ready to provide customers with the most complete offerings at attractive prices, and backed by Zilog's high quality and support.

## APPLICATIONS

Zilog offers products that meet customer needs in a wide variety of industries -- in military applications such as missile guidance, communications, avionics, and artillery; in office automation with microprocessors in typewriters, copiers and facsimile machines. And, both embedded and visible reprogrammable markets for Zilog products keep expanding, with applications in industrial controllers (robotics, process control), telecommunications (modems, switching networks), automotive (dashboard displays), and consumer electronics (VCRs, cable television) markets.

## ADVANCEMENTS IN TECHNOLOGY

Zilog technology continues to pace the industry. All products are moving to CMOS with the Z280 MPU and the Z85C30 SCC leading the way. In addition, Zilog is at the forefront of the industry in the design and manufacturing of a line of Superintegration products. Zilog's technology library includes megacells from the industry-standard Z80 CPU family, the Z8 microcontroller family and several industry standard peripherals. OTP (one-time programmable) technology was introduced this year. All are manufactured in Zilog's reliable n-Well 1.5 -2u CMOS technology.

## SUPPORT PRODUCTS

The efficient hardware and software design of a microprocessor-based application is accomplished through the use of advanced development tools. Zilog's partnerships with the industry leaders in the microprocessor development system business, ensure timely, optimal support for microprocessor and microcontrollers on a variety of host machines from IBM PC through DEC VAX.

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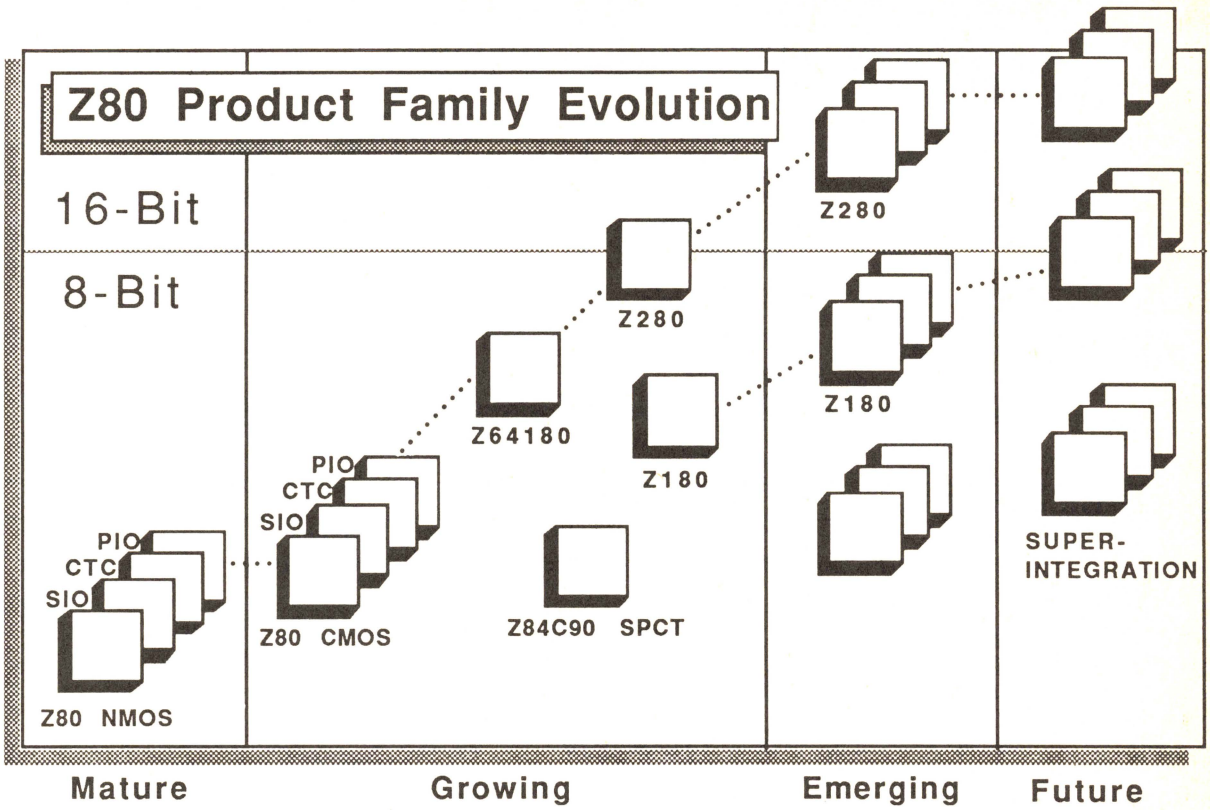


Zilog

| Z80 REFERENCE CHART | | COMMERCIAL | | | | | | MILITARY | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Product | Pin Count | QFP | Dip | PCC | Cerdip | Speed | Temp | Ceramic Dip | LCC | Speed | Desc | JAN |
| **NMOS** | | | | | | | | | | | | |
| Z8400 CPU | 40,44 | – | X | X | X | 4,6,8 | S | X | X | 2.5,4 | – | X |
| Z8410 DMA | 40,44 | – | X | X | X | 4 | S | – | – | – | – | – |
| Z8420 PIO | 40,44 | – | X | X | X | 4,6 | S | X | – | 2.5,4 | X | – |
| Z8430 CTC | 28,44 | – | X | X | X | 4,6 | S | X | – | 2.5,4 | X | – |
| Z8440/1/2/4 SIO | 40,44 | – | X | X | X | 4,6 | S | X | – | 2.5,4 | X | – |
| Z8470 DART | 40,44 | – | X | X | X | 4,6 | S | – | – | – | – | – |
| **CMOS** | | | | | | | | | | | | |
| Z84C00 CPU | 40,44 | X | X | X | X | 4,6,8 | S,E | X | – | 4,6 | – | – |
| Z84C10 DMA | 40,44 | X | X | X | X | 4,6 | S,E | – | – | – | – | – |
| Z84C20 PIO | 40,44 | X | X | X | X | 4,6,8 | S,E | X | – | 4,6 | – | – |
| Z84C30 CTC | 28,44 | X | X | X | X | 4,6,8 | S,E | X | – | 4,6 | – | – |
| Z84C40/1/2/4 SIO | 40,44 | X | X | X | X | 4,6,8 | S,E | X | – | 4,6 | – | – |
| Z80180 MPU | 64,68 | – | X | X | – | 6,8 | S,E | – | – | – | – | – |
| Z80280 MPU | 68 | – | – | X | – | 10 | S,E | – | – | – | – | – |
| Z84C80 GLU | 44,68 | X | – | X | – | 10 | S,E | – | – | – | – | – |
| Z84C90 SPCT | 80,84 | X | – | X | – | 8,10 | S,E | – | – | – | – | – |

S = 0°C to +70°C  E = -40°C to +100°C

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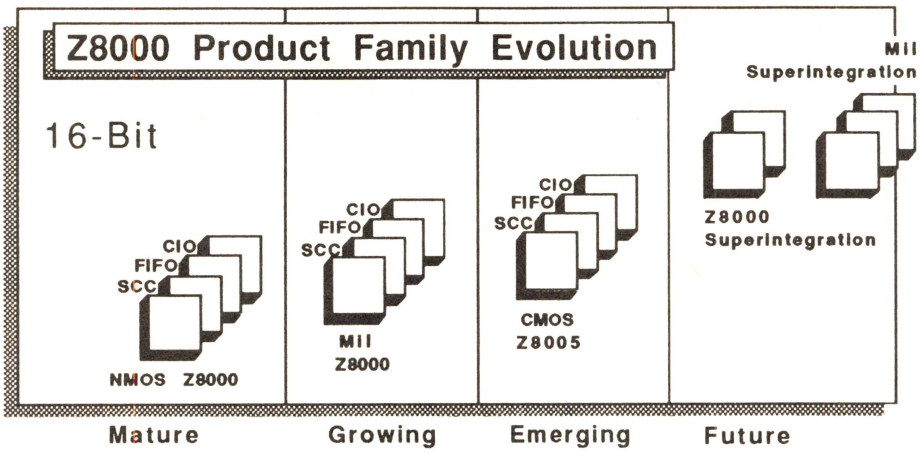
# Z I L O G




## Z8000 REFERENCE CHART

| | | COMMERCIAL | | | | | | MILITARY | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Product | Pin Count | QFP | Dip | PCC | Cerdip | Speed | Temp | Ceramic Dip | LCC | Speed | Desc | JAN |
| **NMOS** | | | | | | | | | | | | |
| Z8001 CPU | 48 | – | X | – | CERAM | 6,10 | S,E | X | X | 6,10 | – | – |
| Z8002 CPU | 40,44 | – | X | X | X | 6,10 | S,E | X | X | 4,6,10 | X | X |
| Z8005 CPU | 44 | – | – | X | – | 6,10 | S | – | X | 6,10 | – | – |
| **Z-BUS PERIPHERALS** | | | | | | | | | | | | |
| Z8016 Z-DTC | 48,68 | – | X | X | CERAM | 6 | S | – | – | – | – | – |
| Z8030 Z-SCC | 40,44 | X | X | X | X | 6,8 | S,E | X | X | 4,6,8 | X | – |
| Z8036 Z-CIO | 40,44 | – | X | X | X | 6 | S,E | X | X | 4,6 | X | – |
| Z8038 Z-FIO | 40,44 | – | X | X | X | 6 | S,E | X | X | 6 | – | – |
| Z8060 -FIFO | 28 | – | X | – | CERAM | 1 MB/S | S | – | – | – | – | – |
| Z8068 DCP | 40 | – | X | – | – | 4 | S | – | – | – | – | – |
| Z8581 CGC | 18 | – | X | – | CERAM | 10 | S,E | X | X | 6,10 | X | – |
| **UNIVERSAL PERIPHERALS** | | | | | | | | | | | | |
| Z8516 DTC | 48,68 | – | X | X | CERAM | 6 | S | – | – | – | – | – |
| Z8530 SCC | 40,44 | X | X | X | X | 6,8 | S | X | X | 4,6,8 | X | – |
| Z8536 CIO | 40,44 | – | X | X | X | 6 | S,E | X | X | 4,6 | X | – |
| Z8538 FIO | 40 | – | X | – | – | 6 | S | – | – | – | – | – |
| Z8560 FIFO | 28 | – | X | – | – | 1MB/S | S | – | – | – | – | – |
| Z8581 CGC | 18 | – | X | – | CERAM | 10 | S,E | X | X | 6,10 | X | – |
| Z9516 DTC | 48,68 | – | X | X | CERAM | 6 | S | – | – | – | – | – |
| Z9518 DCP | 40 | – | X | – | – | 3 | S | – | – | – | – | – |
| **CMOS** | | | | | | | | | | | | |
| Z80C30 Z-SCC | 40,44 | X | X | X | – | 8,10 | S,E | – | – | – | – | – |
| Z85C30 SCC | 40,44 | X | X | X | – | 8,10 | S,E | – | – | – | – | – |
| Z80C20 Z-GLU | 84 | – | – | X | – | 10,16 | S | – | – | – | – | – |
| Z5380 SCSI | 40,44 | – | X | X | – | 20 | S,E | – | – | – | – | – |

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## ZILOG PERIPHERAL FAMILIES

| | Z80 | Z8000 | Z8500 | Z32100 |
|---|---|---|---|---|
| Z8/SUPER8 | | X | X | |
| Z80 | X | | X | |
| Z8000 | | X | | X |
| Z32100 | | | X | X |
| OTHER CPUs | | X | X | X |

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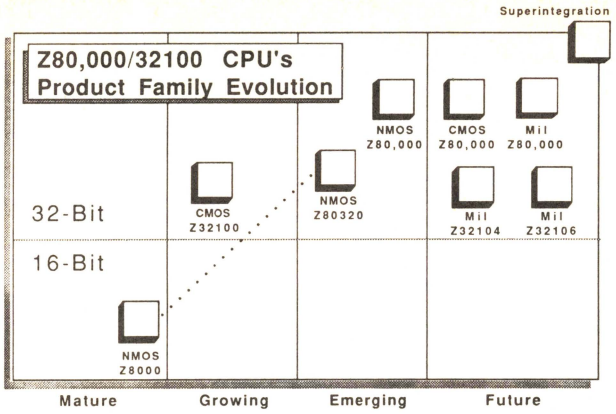
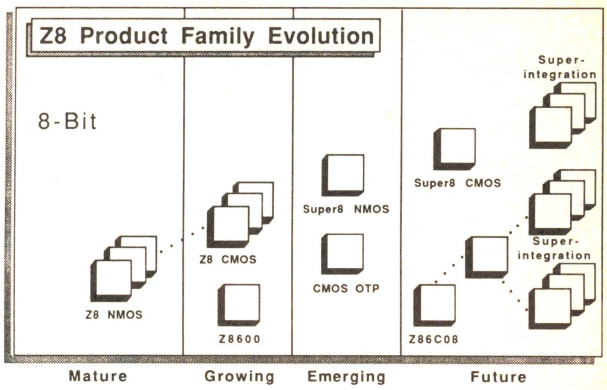
# Z I L O G




## ADVANCED PROCESSOR REFERENCE CHART

| Product | Pin Count | Package | Speed | Temp | Pkg | Spd | Desc | JAN |
|---|---|---|---|---|---|---|---|---|
| **NMOS** | | | | | | | | |
| Z80,000 CPU | 84 | PGA | 10 | S | – | – | – | – |
| Z80320 | 68 | PLCC | 8 | S | – | – | – | – |
| **CMOS** | | | | | | | | |
| Z32100 MPU | 125 | PGA | 10,14,18 | S | – | – | – | – |
| Z32101 MMU | 125 | PGA | 10,14,18 | S | – | – | – | – |
| Z32102 CLOCK | 16 | DOUBLE-WIDTH DIP | 10,14,18 | S | – | – | – | – |
| Z32103 DRAM | 125 | PGA | 10,14,18 | S | – | – | – | – |
| Z32104 DMA | 133 | PGA | 10,14,18 | S | – | – | – | – |
| Z32106 MAU | 125 | PGA | 10,14,18 | S | – | – | – | – |

S = 0°C to +70°C E = -40°C to +100°C

## Z8 REFERENCE CHART

| | | COMMERCIAL | | | | | | MILITARY | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Product | Pin Count | QFP | Dip | PCC | Cerdip | Speed | Temp | Ceramic Dip | LCC | Speed | Desc | JAN |
| **NMOS** | | | | | | | | | | | | |
| Z8601 MCU 2K ROM | 40,44 | – | X | X | X | 8 | S,E | – | – | – | – | – |
| Z8603 PROTOPAK | 40 | – | X | – | – | 8 | S,E | – | – | – | – | – |
| Z8611 MCU 4K ROM | 40,44 | – | X | X | X | 12 | S,E | – | – | – | – | – |
| Z8613 PROTOPAK | 40 | – | X | – | – | 12 | S,E | – | – | – | – | – |
| Z8681 ROMless MCU | 40,44 | – | X | X | X | 8,12,16 | S,E | X | – | 8,12 | – | – |
| Z8600 MCU | 28 | – | X | – | – | 8 | S,E | – | – | – | – | – |
| Z8800 SUPER8 ROMless MCU | 48,68 | – | X | X | – | 20 | S,E | – | – | – | – | – |
| Z8801 SUPER8 | 44 | – | – | X | – | 8,12 | S,E | – | – | – | – | – |
| Z8691 ROMless MCU | 40,44 | – | X | X | X | 12,16 | S,E | – | – | – | – | – |
| Z8671 MCU BASIC DEBUG | 40 | – | X | – | – | 8 | S,E | X | – | 8 | – | – |
| **CMOS** | | | | | | | | | | | | |
| Z86C08 MCU | 18 | X | X | – | – | 12,16 | S,E | – | – | – | – | – |
| Z86C10 MCU | 28 | X | X | – | – | 12,16 | S,E | – | – | – | – | – |
| Z86C20 MCU | 28 | X | X | – | – | 12,16 | S,E | – | – | – | – | – |
| Z86C21 MCU | 40,44 | X | X | X | – | 12,16 | S,E | – | – | 12 | – | – |
| Z86E21 MCU | 40,44 | X | X | X | – | 12,16 | S,E | – | – | – | – | – |

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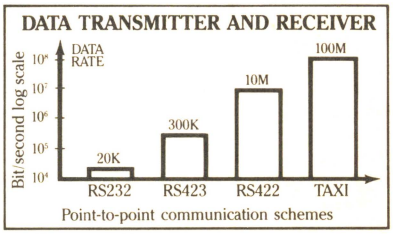


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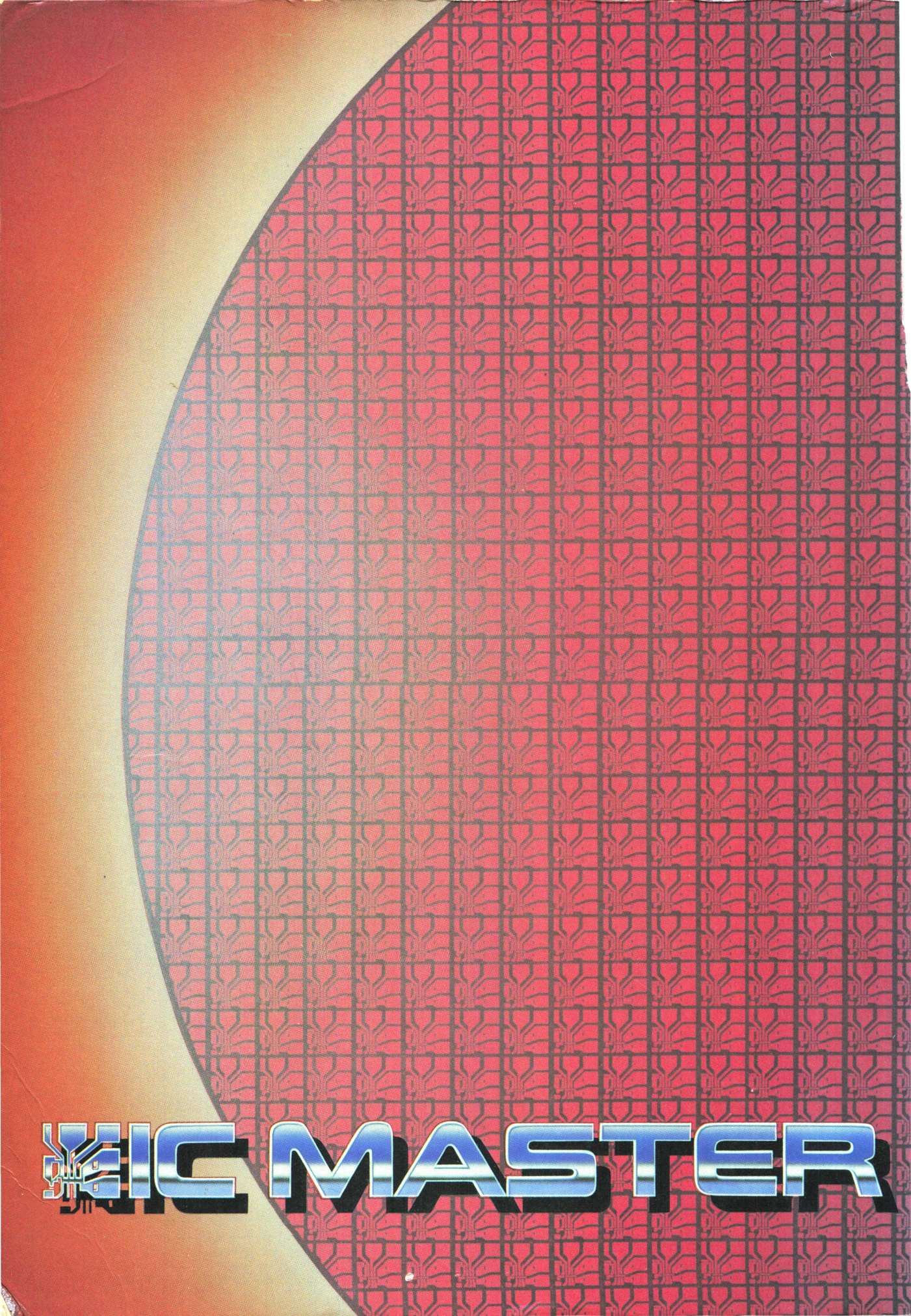
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